

# *Flying Probe Testing Overview*



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*DFT Seminar Series 2011*

*Experts In Limited Access Testing*



1. Types of Flying Probe systems
2. Application of Flying Probers
3. PCBA physical limits & requirements
4. Test Access
5. Test Program Methodology
6. Complementary technologies integration

## *Types of Flying Probers*

- A. First Generation FP – starting mid 1990s in N.A.
  - Single Sided with flying probes on the top side only
  - Four angled Flying Probes on top side
  - Manually placed (Fixed) Probes on bottom side
  
- B. Second Generation FP – starting mid 2000s in N.A.
  - Double Sided with angled flying probes on the top and bottom side
  - Four angled Flying Probes on top side
  - Two Flying Probes on bottom side
  
- C. Third Generation FP – two suppliers W.W.
  - Double Sided with flying probes on the top and bottom side
  - Four or more Flying Probes on top side
  - Four or more Flying Probes on bottom side
  - Incorporate complementary technologies such as Boundary Scan, Thermal...
  
- D. Other FP types
  - One and/or two Flying probes from one side for diagnosing defects
  - Backplane testing using connectors
  - Bareboard Flying Probers for testing bare PCBs without components

- New PCBAs for NPI, prototype and low volume testing
- Connector testing
- Backplane testing
- Field returns
- Reverse Engineering
- Battery
- Continuity (Link) testing
- Substrate testing
- Load Board testing
- Fault Injection
- Copper plating measurement
- Wafer testing

## *Flying Prober Selection Factors*

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1. PCBA Volume - FP best suited for low-volume/high-mix production environment
2. Test Access - FP best solution when electrical test is required and insufficient ICT test access (18mil+) is not available
3. Deployment Time - FP best solution when test window is limited to a few hours or a few days
4. Changing PCB Layout - best solution when the PCB layout can be revised such as prototype, NPI and short runs
5. Non Traditional Applications - testing of substrates, connectors, and other electrical cases

## *Low Volume/ High Mix Usage Model*

*Strategy: highest test coverage within delivery time constraint.*

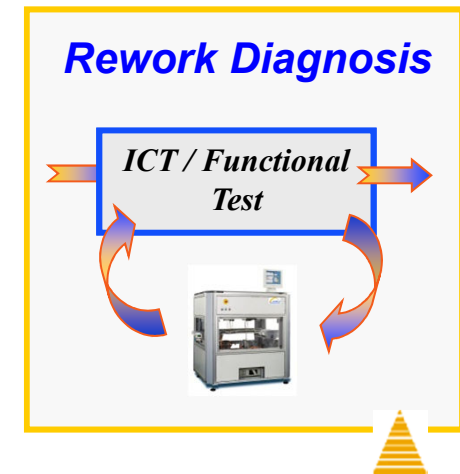
- *Includes NPI, Prototypes, first articles and evaluation boards.*
- *Other Test & Inspection Technologies: SPI, AOI and HVI*
- *Development time: 1 to 16 hours (offline)*
- *Debug time: 4 to 16 hours*
- *Segment: EMS & OEM*
- *Functional test at OEM*
- *Batch Testing*
- *Industries: Mil/Aero, Industrial, Server, Telecom ...*



# Repair/Rework Usage Model

*Strategy: highest test coverage.*

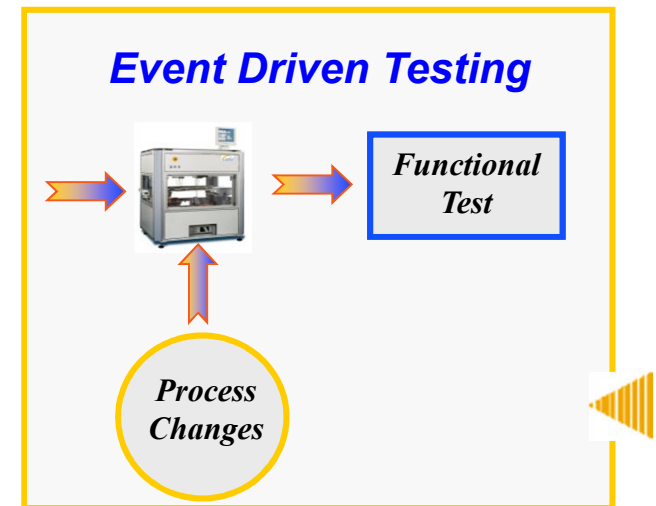
- *Low volumes*
- *Other Test & Inspection Technologies: SPI, AOI, AXI, ICT(programming) and HVI*
- *Development time: 1 to 16 hours (offline)*
- *Debug time: 4 to 40 hours*
- *Segment: OEM*
- *Functional test at OEM*
- *Batch Testing*
- *Industries: Mil/Aero, Industrial, Server, Telecom ...*



## Selective/Sample Usage Model

*Strategy: highest test coverage within line beat rate.  
Typically test first board 100% and then verify any  
line changes*

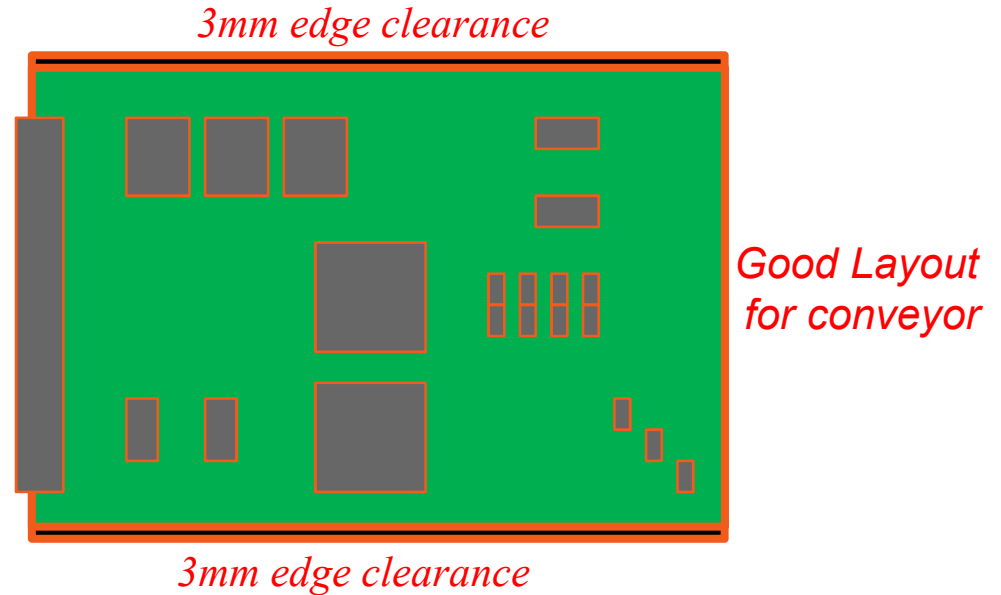
- *High volume such as automotive boards.*
- *Other Test & Inspection Technologies: SPI, AOI, AXI, ICT(programming) and HVI*
- *Development time: 1 to 16 hours (offline)*
- *Debug time: 4 to 32 hours*
- *Segment: OEM*
- *Functional test at OEM*
- *Inline Testing*





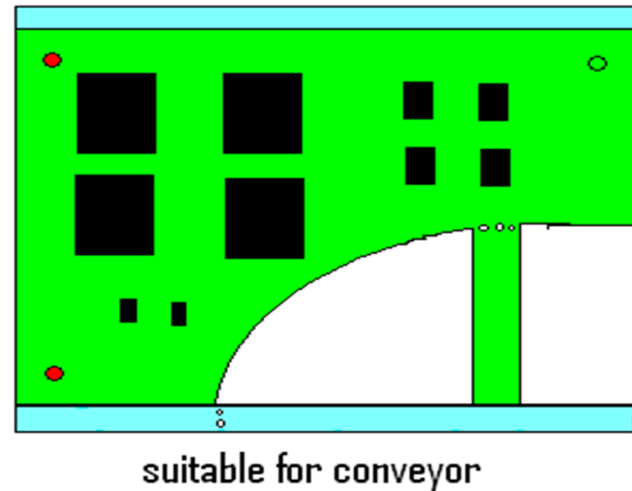
# PCBA Loading Issues - Conveyors

- Edge Clearance on two Parallel sides of the UUT are required – 3 mm
- Best along the longest edges of the UUT to prevent sag
- Predictable leading edge dimension required for board stopping position on systems with automatic conveyors



In the case with odd shaped boards two solutions exist:

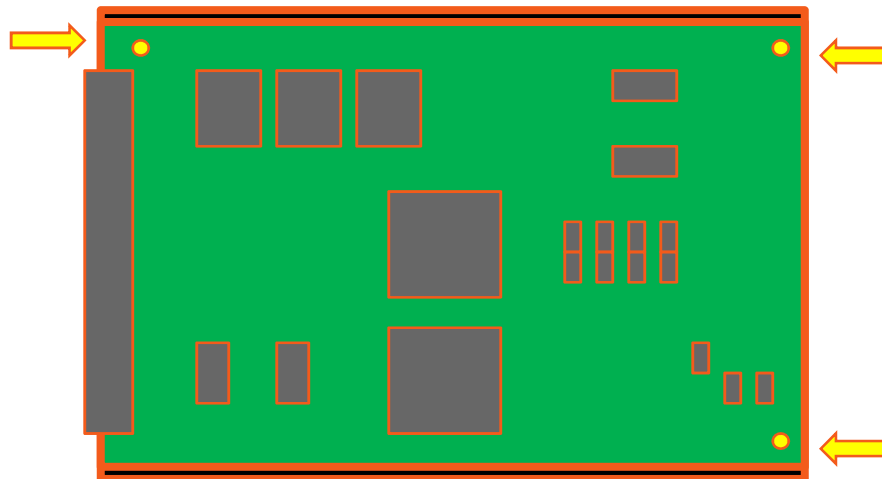
- Use break away rails that comply with the above
- Use a custom or universal carrier to move the UUT into the machine.



## PCBA Alignment and Fiducials

3 Board FID points are required on both **top** and **bottom** of the UUT

- Placed near the perimeter of the UUT
- Must be free from solder after production
- Must not be identical from top to bottom
- Must not be near similar graphics, etches, silk screens.
- Must be clear from the 3mm edge clearance
- Should be in the CAD as a part or easily identifiable entity.



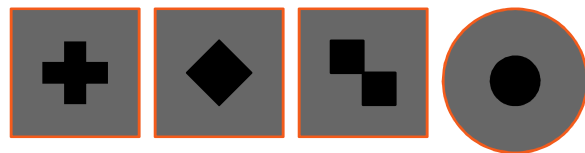
*3 Fiducial points place properly*

# PCBA Fiducial Qualities

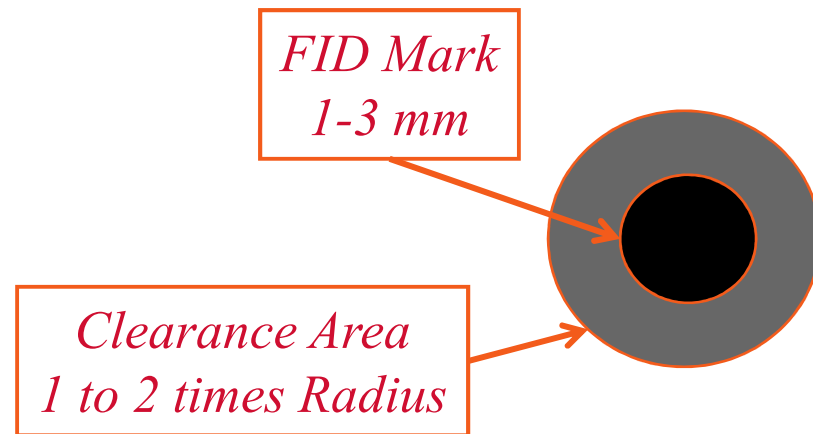
According to the IPC-SMEMA Council Fiducial Locating marks should have the following characteristics:

- Size: 1 mm to 3 mm in diameter (40 – 118 mils)
- Clearance Area around the FID: 1-2 times the radius of the size

Some samples are below, most commonly used is the circle in circular clearance area.



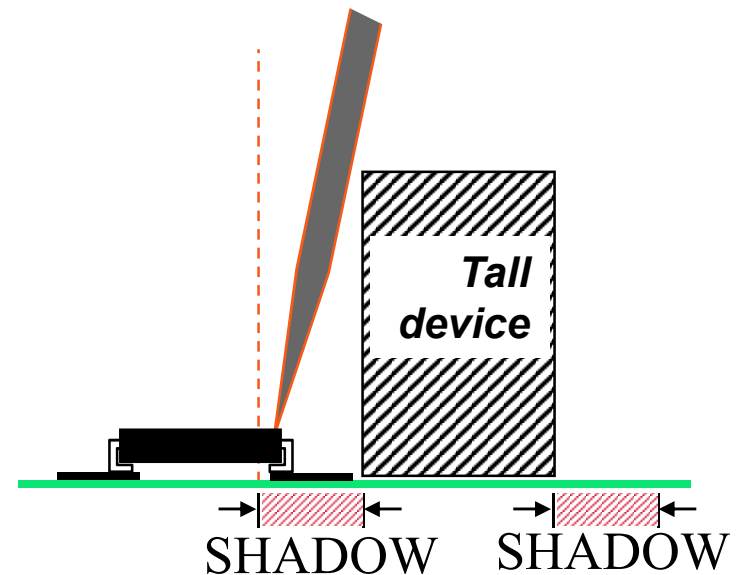
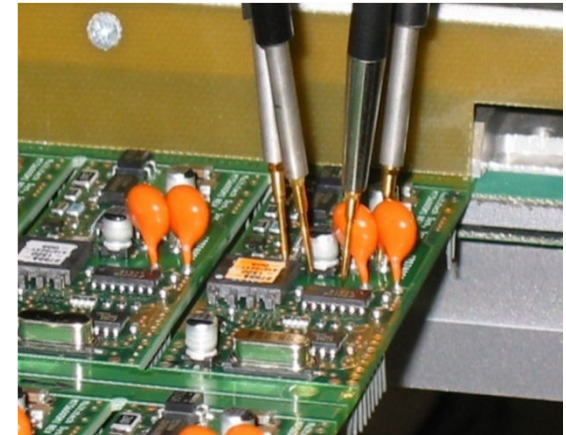
Sample FID Patterns



## *PCBA Physical Limits*

As robotic systems, flying probe machines need to move over parts to go from place to place. Given that they are to contact the board under test and they are not infinitely high from the surface of the UUT. Mechanical limits exist depending on the system you have, or plan to use:

- Fly over heights ranges up to 45mm
- Fly around heights ranges up to 85mm
- Different top and bottom height restrictions
- Test prior to tall part placement
- Weight up to 25 lb. (12Kg)
- Size up to 25" by 39"
- Component shadows



## *Test Access Requirements*

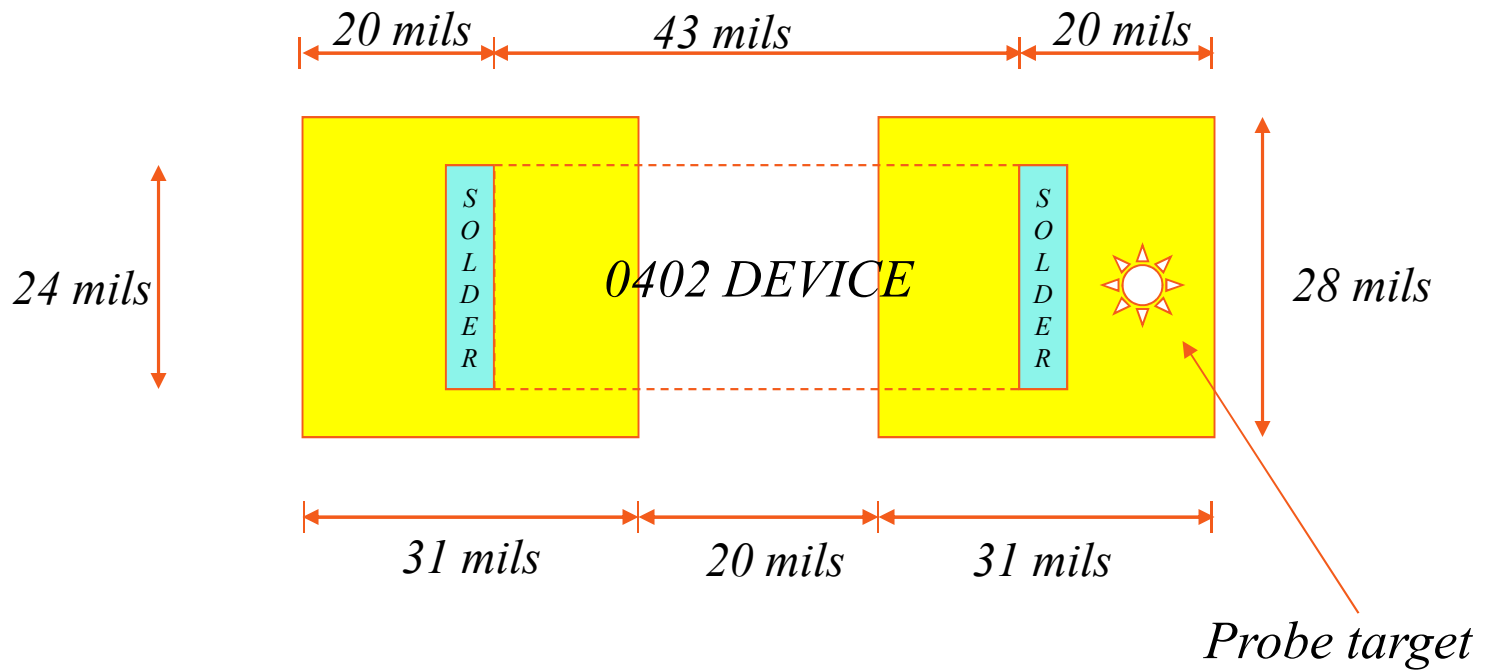
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Goal is physical flying probe access to every net on the board.

1. *Dedicated Test Points - specifically meant for test access*
2. *Through Hole Pins as Test Points*
3. *Via Holes as Test Points – standard or blind but not buried or masked*
4. *Surface Mount Pads as Test Points*
5. *Virtual Test Points*
6. *One access point per unconnected net??*

**DO NOT PROBE ON DEVICES LEADS DUE TO POTENTIAL DAMAGE**

# TYPICAL 0402 LAND PATTERN



*drawing not to scale*

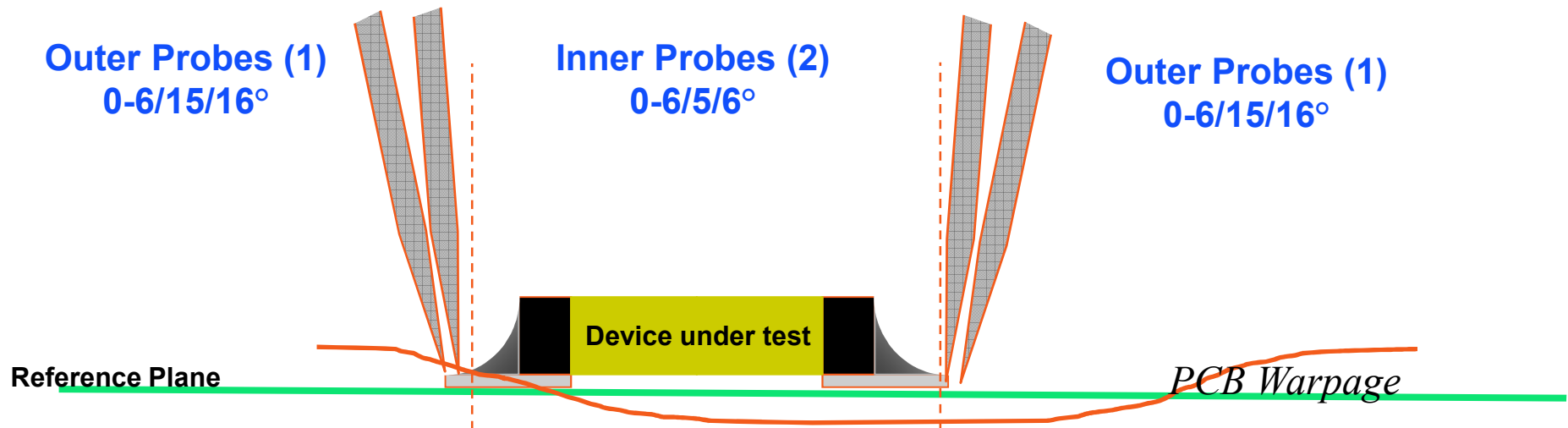
# Probing Error

Causes:

- PCB Production tolerances
- Fiducial recognition
- Steep probe angle
- Conveyors
- Mechanical calibration tolerances
- Different heads

Probe Angle	Tangent	Shadow
0	0.000	0.000
1	0.017	0.244
2	0.035	0.489
3	0.052	0.734
4	0.070	0.979
5	0.087	1.225
6	0.105	1.471
15	0.268	3.751
16	0.287	4.014

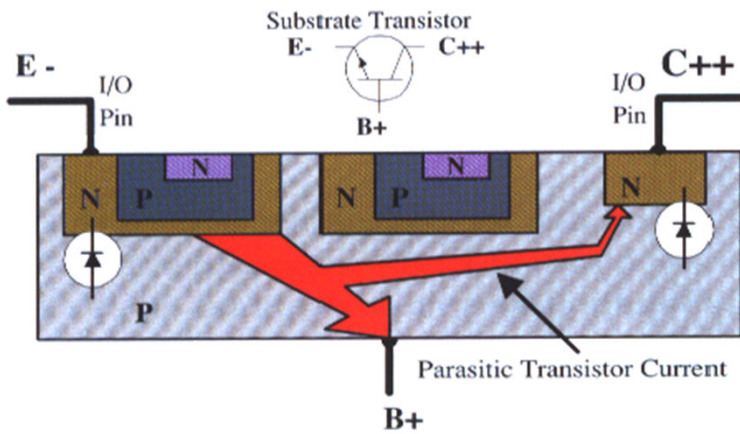
\*10 mil high device



# Opens Testing Technology

Defects	Diode	Sensor
Opens on ICs	Yes	Yes
Opens on BGAs	Yes	Yes
Opens on BGAs with a metal cap or heat sink	Yes	Yes
Opens on connectors	No	Yes
Opens on BGAs with grounded metal cap or grounded heat sink	Yes	No
Polarized caps	No	Yes
ICs on buses	Yes	Yes
IC w/o Chip Select pin	No	Yes

*Diode Method*

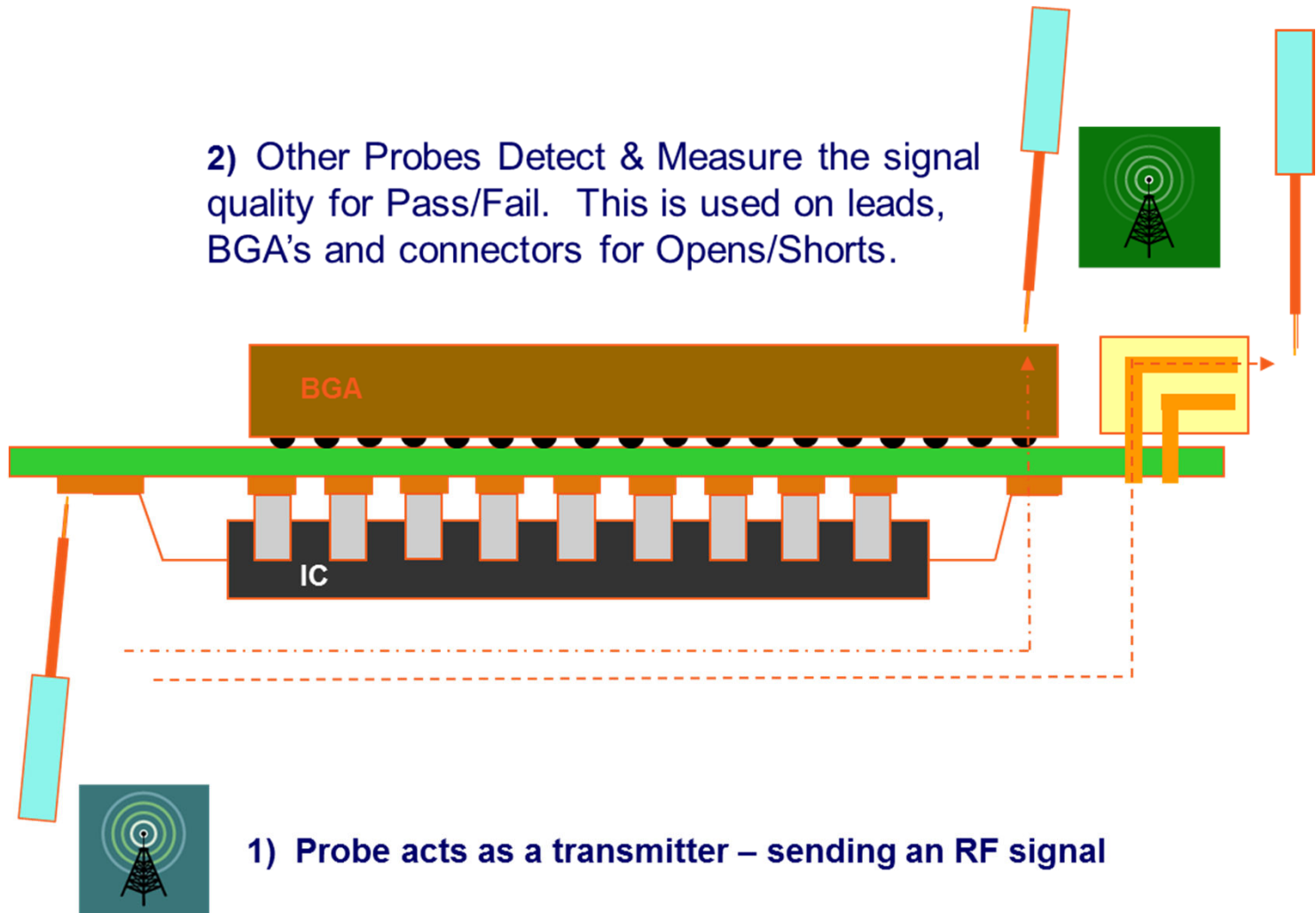




# Opens Testing – Sensors Method



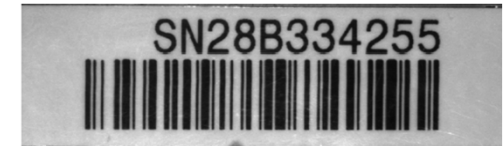
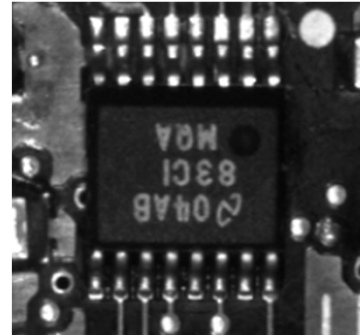
2) Other Probes Detect & Measure the signal quality for Pass/Fail. This is used on leads, BGA's and connectors for Opens/Shorts.



- 1 camera Top side



- 1 camera Bottom side



## OPTICAL CAPABILITIES

- Fiducials
- Reading 1D & 2D barcodes
- Component Presence
- Component Absence
- Component Skew
- Component Part Markings
- No Solder Inspection

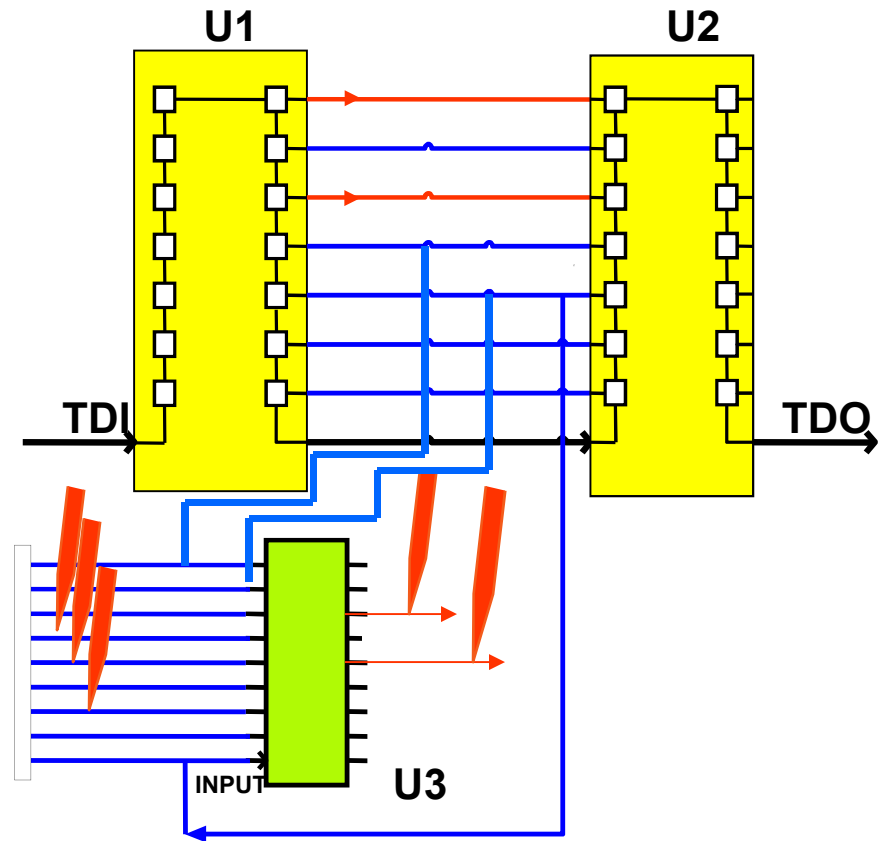
1. Shorts testing - not practical to test every net against every other net
  - Adjacent pins technique
  - Geographical distance as defined by the user
  - Selective nets such as power and/or ground to other nets
  - Net impedance learned from a golden PCBA
2. Passive Component electrical testing
  - BOM method – BOM value + device tolerance + system tolerance
  - AutoLearn method – learned golden board + user tolerance
3. Active Component electrical testing
4. Opens testing (Vectorless)
  - IC pins except for power and ground
  - Connector pins if accessible to sensor
5. Optical test
  - Presence, absence, skew and markings of device not electrically testable
6. Power On testing
7. Voltage, currents and other technologies

Different supplier may offer combinations of these options:

- Boundary Scan (Basic & Advanced)
- Laser mapping
- Microscopy
- Bed-Of-Nails
- Device Programming
- Thermal measurement
- External instrumentation integration

# *Incorporating Boundary Scan Test*

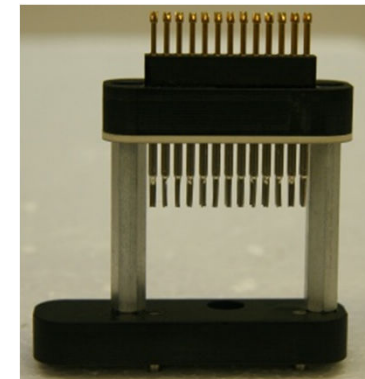
- PCBA Power can be provided via probes or external supply
- Boundary Scan controller applies vectors via DUTs' JTAG port
- Unused probes can monitor internal net for additional test coverage
- Redundant tests can be removed
- Automated test optimization and coverage report generation



## *Incorporating Flying Bed-of-Nails*



Mobile head that carries a Bed of Nails (BON) designed for a fixed pin pattern. BON carry power and/or fixed channels.



# *Boundary Scan vs Flying Prober vs ICT*

TEST TECHNIQUE	BS	PON FP-DS	ICT	NOTES
Shorts	Yellow	Green	Green	Non BS nets; FP slowest; ICT needs access
Opens	Yellow	Green	Green	
Passives	Yellow	Green	Green	
Bypass caps	Red	Green	Yellow	Vision option on FP
Low value RLC	Red	Green	Yellow	FP has dedicated hardware
Actives	Red	Green	Green	
Markings/Barcode	Red	Green	Red	FP has AOI
Switches	Red	Green	Yellow	Mechanical contact
Connectors	Red	Green	Yellow	
LED colors	Red	Yellow	Green	ICT fixture sensor
IC Opens	Red	Green	Green	Vectorless testing (TestJet, FrameScan...)
Frequency Test	Red	Green	Yellow	
Voltage Test	Yellow	Green	Green	
IC Internal Logic	Yellow	Red	Green	
Device Programming	Yellow	Yellow	Yellow	Using BS
Test Access	Yellow	Green	Red	BS port; FP 4-8mil; ICT 18-25mil
Test Fixture Costs	Green	Green	Red	ICT fixture \$5-\$50K
Development time	Green	Yellow	Red	ICT fixture
Test time	Green	Red	Yellow	

*What the future holds???*

- *Faster testing*
- *Smaller test targets*
- *Incorporating complementary technologies*
- *Industry specific solutions*
- *Growing usage*