Semiconductor Wafer Test Technology and Trends: Lessons for MEMS Test Engineers

Ira Feldman
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Outline

- Market Dynamics
- Testing Semiconductors vs. MEMS
- Cost of Test
  - Semiconductor Solutions
- MEMS Challenges
- MEMS @ Semiconductor Wafer Test Workshop
- Conclusion
NEW 2011 Yole MEMS Forecasts

In units

- 15.8 B units of MEMS devices in 2016 with a 24% CAGR over 2010-2016

"MEMS Roadmap: From Device to Function" Jean-Christophe Eloy, Semicon West 2011
DRAM

~ 17.4 B Units in 2011

http://www.dramexchange.com/Market/market_activity.aspx
1997 SIA Roadmap – Alarming!

- 1997: Predicted per xtor test cost to exceed fabrication cost
- 2001: DFT & Structural Test reduce equipment cost & complexity
  - Lower requirements on I/O data rate, #IO, etc

June 3-6, 2007
IEEE SW Test Workshop
Package Proliferation

25+ Years of Semiconductor Packaging

Leading edge CMOS node (approx): 0.25um 0.18um 0.13um 90nm 65nm 40nm 28nm


Sophistication & diversification increasing over time

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“Backend to the Front Line” William Chen, ASE Group, SWTW 2011
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Device Testing

Stimulus ➔ Device Under Test (DUT) ➔ Response ➔ Correct?
Traditional Wafer Probe Test Cell

Stimulus

Electrical

Response

DUT

Thermal

Verigy / Advantest
Stimulus & Response - Traditional

Electrical

Thermal

Device Under Test (DUT)

- Semiconductors
- Oscillators
- MEMS switches
- MEMS filters
- MEMS oscillators

Electrical
Stimulus & Response - Optical

Device Under Test (DUT)

- Image Sensors
- LEDs
- Micro- / Pico - projectors (DLP, etc.)
- Micro bolometers

Electrical

Thermal

Optical
Stimulus & Response – MEMS Sensors

- Device Under Test (DUT)
  - Accelerometers
  - Gyroscopes
  - Magnetic Compass
  - Microphones
  - Speakers
  - Pressure sensors
  - ...
Stimulus & Response – Life Science + ?

Mass include movement of material in / out of DUT such as fluids & gas.

- Valves
- Pumps
- Mixers
- Micro reactors
- Sensors
- Micro explosives
...

MEMS Testing & Reliability Conference 2011
Device Testing

Stimulus → Device Under Test (DUT) → Response → Correct?
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Cost of Test Drivers

- Increasing test frequency
- Tighter pad pitches
- Increasing transistor count
- Increasing probe count

Increased Cost
Semiconductor Cost - Test Solutions

- Test Reduction
- Increased Parallelism
- Test Partitioning
- Lower Cost
- Silicon Velocity
Conflicting & Counter Intuitive Solutions
Semiconductor Cost - Test Solutions

- Test Reduction
- Increased Parallelism
- Test Partitioning
- Lower Cost
- Silicon Velocity
- Test Escapes
- Run time complexity
+ Statistical based sampling
+ Test elimination
- Increased probe card cost
- Increased tester resources
+ Decreased handling time
+ Greater prober amortization
+ Reduced floor space
+ Increased Silicon Velocity
- Increased process steps
- Increased process complexity
+ Optimized high-cost ATE
Remo

Example of using old depreciated Memory Testers to Reduce Test Costs

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Manual Alignment

Electroglas 2001 ca. 1982-5

www.vortexcontrolsystems.com
Cantilever & Blade

Technoprobe

SV Probe
Vertical - Buckling Beam

Cobra “Buckling Beam” Card
Patented by IBM in June 1977
Mann: SWTW Tutorial 2004

SV Probe “Trio”

FormFactor: “MEMS for ProbeCard Applications”
Chong Chan Pin – Semicon Singapore 2010
Vertical - Buckling Beam

MicroProbe: Apollo Vertical

SV Probe: Trio

JEM: VC
MEMS - Vertical

Microfabrica  MicroProbe  FormFactor (T1)

MicroProbe (Vx-MP)
MEMS - Micro Cantilever

Microfabrica

FormFactor (T3)

MJC (U Probe)
http://www.mjc.co.jp/eng/ir/pdf/MJC070226-s.pdf

JEM
Vertical Probe Head

- Printed Circuit Board
- BGA (Solder Attach)
- Space Transformer
- Upper Guide Plate
- Spacer
- Lower Guide Plate
- MicroProbes Apollo
- Probes
FormFactor CMOS Imaging Solution
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MEMS chip structure

- SENSOR test pads
  - electrical testing
  - probe card needles contact area
- CAP wafer surface
  - NO-contact area for probe card needles

MEMS multi site test

- UNTOUCHABLE DIES
- Automatic touchdown repositioning → creating 2 double touched dies!

=> Safe needle contacting via 
untouchable die zones!
Film Bulk Acoustic Resonator

• New product development geared towards using FBARs in oscillators for timing solutions
• 1.5GHz resonant frequency
• 27,000 um² resonator area
• Quality factor over 1000, up to several thousand
• 1 year aging spec less than 25ppm

De-embedding Structure Layout

Start with Device Under Test (DUT), then reproduce pads replacing device with Open and Short at device plane

Open and Short structure repeated 80 times equally spaced on wafer

"Probe to Pad Placement Error Correction for Wafer Level S-Parameter Measurements"
Steven Ortiz
(Avago Technologies - USA)

• FBAR structure – resonator plus cap wafer. Vias through cap wafer to resonator.

• Due to very high frequency and tight specification tolerance, very sensitive to location of probes on pad. Implemented “calibration” structures to de-embed the measurements.
"Ghosting: Touchdown Reduction Using Alternate Site Sharing"
Doron Avidar and Yossi Dadi (Micron - Israel)
When using large multisite arrays that need > 3 touchdowns/wafer, “ghosting” may save several touchdowns. Examples showed 12 to 20% savings.
Summary

- Proven semiconductor cost reduction techniques
  - Not always intuitive
  - Require test engineering
  - Can be applied to MEMS

- MEMS wafer test challenge
  - Multi-site stimulus and response
  - Proper probe card architectures required
  - Solution integration support
Resources

- IEEE Semiconductor Wafer Test Workshop (SWTW)
  - [http://www.swtest.org](http://www.swtest.org)

- International SEMATECH Manufacturing Initiative (ISMI) Probe Card Cost Model
  - [http://ismi.sematech.org/modeling/probeCOO.htm](http://ismi.sematech.org/modeling/probeCOO.htm)

- SEMI E35-0307
  - Guide to Calculate Cost of Ownership (COO) Metrics for Semiconductor Manufacturing Equipment
Thank You!

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