

# MEPTEC 2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM

MEPTEC INITIATES COLLABORATION  
WITH HETEROGENEOUS INTEGRATION ROADMAP

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# MEPTEC 2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM

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*Wilmer R. Bottoms, Ph.D., Chairman, Third Millennium Test Solutions and Co-chair, Heterogeneous Integration Roadmap*

### SESSION 1 – DRIVERS FOR HETEROGENEOUS INTEGRATION

- **Grand Challenges and Timelines for Electronic-Photonic Integration**  
*Lionel C. Kimerling, Ph.D., Thomas Lord Professor of Materials Science and Engineering, Director of the Materials Processing Center at the Massachusetts Institute of Technology*
- **New Die-Mensions in Heterogeneous Integration**  
*Subramanian S. Iyer, Ph.D., Center for Heterogeneous Integration and Performance Scaling (CHIPS), Henry Samueli School of Engineering, Electrical Engineering Department, University of California at Los Angeles*
- **Technology Integration for Vital Sensing**  
*Igino Padovani, Business Development Manager for Vital Sensors, Robert Bosch LLC*

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- **Catching up with Evolution – How to make Robots See**  
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- **Practice and Prospects of Heterogeneous Integration at DARPA**  
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- **The Evolution of Multi-Chip Packaging: from MCMs to 2.5/3D to Photonics**  
*David McCann, Vice President of Packaging R&D and Operations, GLOBALFOUNDRIES*
- **SiP Modules – Application Driven Integration**  
*Eelco Bergman, Senior Director of Sales & Business Development, ASE Group*

### PANEL: PACKAGING SOLUTIONS TO MEET NEEDS OF THE HETEROGENEOUS INTEGRATION ROADMAP

*Moderator: Ivor Barber, Corporate Vice President of Packaging, AMD*

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## MEPTEC 2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM

MEPTEC initiates collaboration with *Heterogeneous Integration Roadmap*

### MORNING AGENDA

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7:30 am	<b>Registration Opens</b>
8:15 am – 8:30 am	<b>Welcome and Introduction</b>
8:30 am – 9:00 am	<b>MORNING KEYNOTE</b> <b>Heterogeneous Integration: Enabling the Future of the Electronic Industry</b> <i>Wilmer R. Bottoms, Ph.D., Chairman, Third Millennium Test Solutions and Co-chair, Heterogeneous Integration Roadmap (HIR)</i>
<b>SESSION 1</b>	<b>DRIVERS FOR HETEROGENEOUS INTEGRATION</b>
9:00 am – 9:30 am	<b>Grand Challenges and Timelines for Electronic-Photonic Integration</b> <i>Lionel C. Kimerling, Ph.D., Thomas Lord Professor of Materials Science and Engineering, Director of the Materials Processing Center at the Massachusetts Institute of Technology</i>
9:30 am – 10:00 am	<b>New Die-Mensions in Heterogeneous Integration</b> <i>Subramanian S. Iyer, Ph.D., Center for Heterogeneous Integration and Performance Scaling (CHIPS), Henry Samueli School of Engineering, Electrical Engineering Department, UC Los Angeles</i>
10:00 am – 10:30 am	<b>Technology Integration for Vital Sensing</b> <i>Igino Padovani, Business Development Manager for Vital Sensors, Robert Bosch LLC</i>
10:30 am – 11:00 am	<b>Morning Break and Exhibits</b>
<b>SESSION 2</b>	<b>CHALLENGES FOR HETEROGENEOUS INTEGRATION (PART 1)</b>
11:00 am – 11:30 am	<b>Catching up with Evolution – How to make Robots See</b> <i>Anders Grunnet-Jepsen, Ph.D., CTO and Director of Advanced Technology in Intel's Perceptual Computing Group</i>
11:30 am – 12:00 pm	<b>Practice and Prospects of Heterogeneous Integration at DARPA</b> <i>Daniel Green, Ph.D., Program Manager, DARPA</i>
12:00 pm – 12:30 pm	<b>The Memory of Future Cars</b> <i>Thomas M. Coughlin, President, Coughlin Associates</i>
12:30 pm – 1:30 pm	<b>Lunch and Exhibits</b>

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## MEPTEC 2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM

*MEPTEC initiates collaboration with **Heterogeneous Integration Roadmap***

### AFTERNOON AGENDA

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1:30 pm – 2:00 pm

#### **AFTERNOON KEYNOTE**

##### **Heterogeneous Integration Roadmap - A Status Report**

*William (Bill) Chen, Ph.D., ASE Fellow and Senior Technical Advisor, and  
Co-chair, Heterogeneous Integration Roadmap (HIR)*

#### **SESSION 3**

#### **CHALLENGES FOR HETEROGENEOUS INTEGRATION (PART 2)**

2:00 pm – 2:30 pm

##### **The Evolution of Multi-Chip Packaging: from MCMs to 2.5/3D to Photonics**

*David McCann, Vice President of Packaging R&D and Operations, GLOBALFOUNDRIES*

2:30 pm – 3:00 pm

##### **SiP Modules – Application Driven Integration**

*Elco Bergman, Senior Director of Sales & Business Development, ASE Group*

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3:00 pm – 3:30 pm

#### **Afternoon Break and Exhibits**

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#### **PANEL**

#### **PACKAGING SOLUTIONS TO MEET NEEDS OF THE HETEROGENEOUS INTEGRATION ROADMAP**

3:30 pm – 5:00 pm

**Moderator:** *Ivor Barber, Corporate Vice President of Packaging, AMD*

##### **Panelists:**

*Andrew B. Kahng, Ph.D., Professor of CSE and ECE at UC San Diego, Endowed Chair in High-Performance Computing*

*Li Li, Ph.D, Distinguished Engineer at Cisco Systems, Inc.*

*Dave McCann, Vice President of Packaging R&D and Operations, GLOBALFOUNDRIES*

*Gamal Refal-Ahmed, Ph.D, Distinguished Engineer of Thermal Packaging, Xilinx/Visiting Professor, SUNY and*

*Adjunct Professor University of Toronto*

*Brandon Wang, Group Director, Cadence Design Systems*

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5:00 pm – 6:30 pm

#### **Reception and Exhibits**

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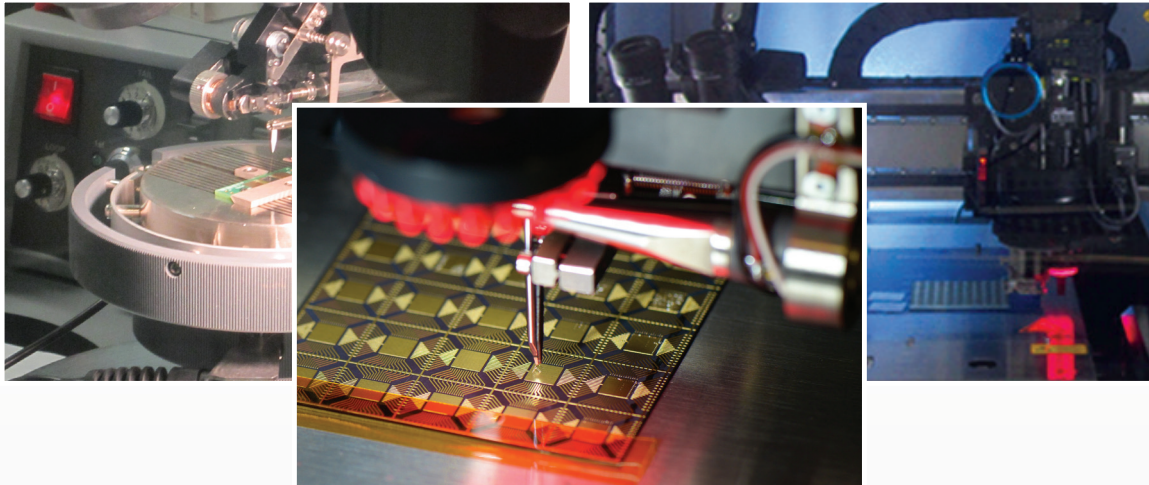
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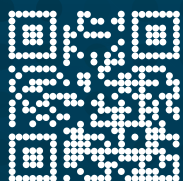
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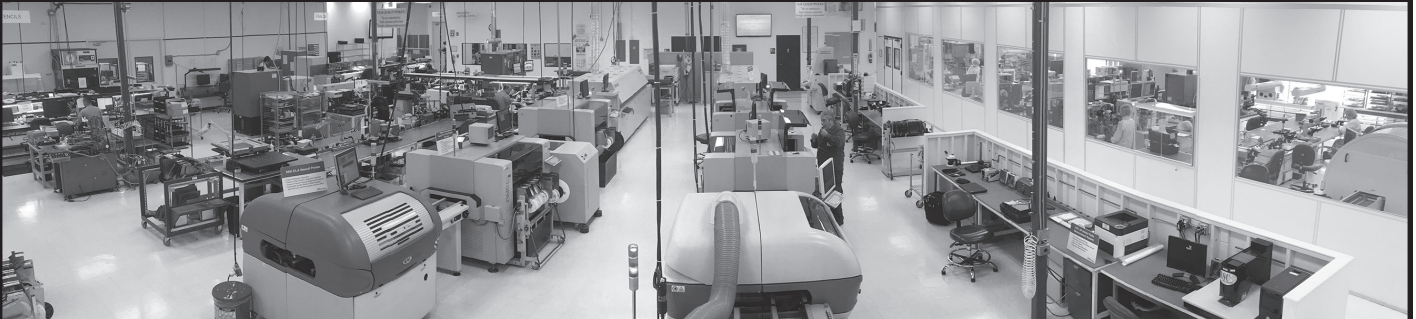
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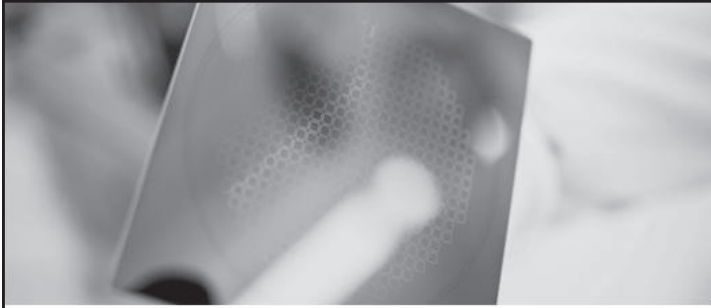
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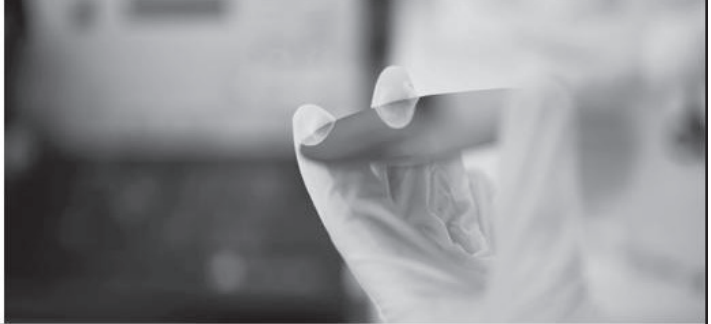
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### **ASM Pacific Technology**

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ASM Pacific Technology is the world's largest assembly and packaging equipment supplier for the semiconductor and LED industries. The company is engaged in the design, manufacture and marketing of machines, tools and materials used in the semiconductor and electronic assembly industry. The Company operates in three segments: back-end equipment segment, engaged in the development, production and sales of back-end equipment segment; surface mount technology equipment segment, which engages in the development, production and sales of

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### **ESD Alliance**

Phone: 408-287-3322

[www.esd-alliance.org](http://www.esd-alliance.org)

The Electronic System Design Alliance (ESD Alliance), an international association of companies providing goods and services throughout the semiconductor design ecosystem, is a forum to address technical, marketing, economic and legislative issues affecting the entire industry. It acts as the central voice to communicate and promote the value of the semiconductor design industry as a vital component of the global electronics industry.

### **Finetech**

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Phone: 607-779-7522

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## BIOGRAPHIES

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### SYMPOSIUM CO-CHAIRS

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**Ivor Barber** is Corporate Vice President for Packaging at AMD. An industry veteran, Ivor has over 35 years experience in package assembly, design and characterization including 23 years at LSI Corporation in Milpitas in various Engineering and Leadership positions in Packaging and 4 years as Senior Director of Package Process Technology Development at Xilinx. Ivor graduated from Napier University in Edinburgh, Scotland with a Bachelors degree in Technology and holds 13 US patents related to package design.

**Joel Camarda** is an industry consultant, concentrating on manufacturing operations management. He well known in the international packaging community via his work history of 30+ years in the USA and Asia. He has been active in IMAPS and is an advisor for MEPTEC. Joel has held several executive management positions: VP Operations at Sipex/Exar, President of K&S Flip Chip Technology, and Director of Worldwide Assembly and Packaging at Cypress Semiconductor. He started his career at National Semiconductor.

**Rich Rice** is Senior Vice President of Sales for ASE (U.S.) Inc., with responsibility for the North American region. Appointed in 2003, Mr. Rice oversees field sales and engineering support teams. Prior to joining ASE, Mr. Rice spent over ten years at Amkor Technology, where he held various management roles, including Vice President of Sales and Vice President of Business Development. Previously, Mr. Rice performed engineering roles at Nara Technologies and National Semiconductor Corporation. Mr. Rice holds a BS degree in Agricultural Engineering from the University of Illinois.

**Tom Salmon**, as Vice President of Collaborative Technology Platforms, works with SEMI's staff to ensure that members, standards users, and volunteers worldwide receive maximum value from their association with SEMI. Additionally, he manages a number of SEMI's business and technology programs, including device manufacturer outreach, and the Chemical and Gas Manufacturers, Advanced Packaging, and Secondary Equipment and Applications groups. Before joining SEMI, he held several management positions in manufacturing, logistics, customer relations, and sales.

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### KEYNOTE SPEAKERS

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**Dr. Wilmer R. Bottoms** received his Ph.D. in Physics from Tulane University in 1969 and is currently Chairman of Third Millennium Test Solutions. He has served as a faculty member at Princeton University, manager of Research and Development at Varian Associates, founding President of the Semiconductor Equipment Group of Varian Associates, General Partner of Patricof & Co. Ventures as well as Chairman and CEO of several companies both public and private. He has also served as a member of several government advisory groups. Dr. Bottoms currently serves as Co-chair of the Heterogeneous Integration Roadmap (HIR), Chairman of the Packaging and Component Substrates Technical Working Group for INEMI, Emeritus Member of the Board of Tulane University, Chairman of the Semiconductor Equipment and Materials International's SEMI Awards Committee, and Chairman of APMT.

**Dr. William (Bill) Chen** holds the position of ASE Fellow and Senior Technical Advisor at ASE Group. Prior to joining ASE, he was the Director at the Institute of Materials Research & Engineering in Singapore. Bill retired from IBM Corporation after a career spanning over thirty years in various R&D positions. He has held adjunct and visiting faculty positions at Cornell University, Hong Kong University of Science and Technology, and Binghamton University. Currently, he is the co-chair of the ITRS Assembly Packaging Technical Working Group. He also chairs SEMI's Advanced Packaging Committee, as well as serving

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as Co-chair of the Heterogeneous Integration Roadmap (HIR). In 2009, Bill received the InterPACK Excellence Award for his contributions, and in 2010, he was presented with the IEEE CPMT David Feldman Outstanding Contribution Award. He was a past President of the IEEE CPMT Society, and has been elected a Fellow of IEEE and a Fellow of ASME. Bill has served as a member of the Board of iNEMI since 2012. Bill received B. Sc. from London University, M.Sc. from Brown University and Ph.D. from Cornell University.

## PRESENTERS AND PANELISTS

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**Eelco Bergman** has 30+ years of semiconductor industry experience in roles spanning engineering, operations, sales and marketing disciplines. He is currently Sr. Director of Sales & Business Development with ASE Group where he is focused specifically on the enablement and growth of SiP opportunities with system OEMs. Before joining ASE, Eelco was the Director of Product Marketing for Advanced Interconnect with Global Foundries, prior to which he provided strategic sales, marketing and operational consulting services to a number of fabless technology companies. Eelco spent 14 years with Amkor Technology leading their business development and marketing activities and started his semiconductor career with Micron Technology during its formative years. Eelco has a BS degree in Aerospace Engineering from the University of Michigan (Go Blue!).

**Tom Coughlin**, President, Coughlin Associates is a widely respected digital storage analyst as well as business and technology consultant. He has over 35 years in the data storage industry with multiple engineering and management positions at high profile companies. Tom is active with SMPTE, SNIA, the IEEE (he is Director for IEEE Region 6 and active in the Consumer Electronics Society where he is chairman of the Future Directions Committee) and other professional organizations. Tom is the founder and organizer of the Annual Storage Visions Conference ([www.storagevisions.com](http://www.storagevisions.com)), a partner to the International Consumer Electronics Show, as well as the Creative Storage Conference ([www.creativestorage.org](http://www.creativestorage.org)). He is the general chairman of the annual Flash Memory Summit. He is a Senior member of the IEEE, Leader in the Gerson Lehrman Group Councils of Advisors and a member of the Consultants Network of Silicon Valley (CNSV).

**Dr. Daniel Green** joined DARPA as a program manager in March 2013. His interests include advanced materials, devices and technology integration for electronic systems. Prior to DARPA, Dr. Green was at the Office of Naval Research (ONR), where he managed both fundamental and applied research programs in the areas of electronic materials and devices focusing on advanced III-V semiconductors including wide bandgap materials, magnetic and magneto electric devices and oxide materials. From 2003 to 2009, Dr. Green served as a materials/device engineer and program manager at RF Micro Devices, Inc. where he developed Gallium Nitride (GaN) transistor technology for amplifier applications in both the commercial and defense markets. Dr. Green received his Bachelor of Science in Physics and Electrical Engineering from Yale University. He completed his Master of Science and Doctor of Philosophy work at the University of California, Santa Barbara studying GaN materials and device technology.

**Dr. Anders Grunnet-Jepsen** is currently the CTO and Director of the Advanced Technology Group in Intel's Perceptual Computing group. He has a Ph.D. from Oxford University in Nonlinear Optics, and M.Sc. in Electrical Engineering from the Technical University of Denmark. He has worked in NKT Research Center in Denmark, Thomson-CSF in Paris, University of California San Diego (UCSD), and Templex Technology. He is also co-founder and CTO for ThinkOptics, Inc.

**Dr. Subramanian S. Iyer (Subu)** is Distinguished Chancellor's Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department at the University of California at Los Angeles where he is director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). He obtained his B.Tech. from IIT-Bombay, and Ph.D. from UCLA and joined the IBM, where he was appointed IBM Fellow and was till 2015, Director of the Systems Scaling Technology Department. His key technical



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contributions have been the development of the world's first SiGe base HBT, Salicide, eFuses, eDRAM, 45nm technology used at IBM and IBM's development partners and 3-Dimensional Integration. He cofounded SiBond LLC to develop SOI substrates. He has published over 250 papers and holds over 70 patents. He has received several outstanding technical achievements and corporate awards at IBM. He is an IEEE Fellow and a Distinguished Lecturer of the IEEE EDS. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal in 2012.

**Dr. Andrew B. Kahng** is Professor of CSE and ECE at UC San Diego, where he holds the endowed chair in High-Performance Computing. He has served as visiting scientist at Cadence (1995-1997) and as founder/CTO at Blaze DFM (2004-2006). He is the coauthor of 3 books and over 400 journal and conference papers, holds 33 issued U.S. patents, and is a fellow of ACM and IEEE. He has served as general chair of DAC, ISQED, ISPD and other conferences. His research interests include IC physical design and performance analysis, the IC design-manufacturing interface, combinatorial algorithms and optimization, and the roadmapping of systems and technology.

**Dr. Lionel C. Kimerling** is the Thomas Lord Professor of Materials Science and Engineering at MIT and the founding Director of the MIT Microphotonics Center, where he conducts an active research program in the design and processing of semiconductor materials and devices. He has also served as Director of the MIT Materials Processing Center (1993-2008). Dr. Kimerling was Head of the Materials Physics Research Department at AT&T Bell Laboratories when he joined the faculty of MIT as Professor in 1990. He has authored more than 350 technical articles and holds more than 50 patents. He leads the MIT-Industry team of the Communication Technology Roadmap. He is one of two Principal Investigators for the Photonic Systems Manufacturing Consortium (PSMC) and is also Chair of the Monolithic Integration Technology Working Group (TWG). He is responsible for managing the development of the product emulator cost model and the three PSMC workshops to begin broader discussions on architectures and component needs among all roadmapping TWGs and Product Emulator Groups (PEGs) and industrial stakeholders.

**Dr. Li Li** is a Distinguished Engineer at Cisco Systems, Inc. where he leads an initiative on 3D IC integration and advanced packaging development. He has been with Cisco for about 10 years and has 18 years industry experience in IC packaging design, technology development and qualification. He was promoted to a Cisco Distinguished Engineer in 2008 for his outstanding contributions in advanced technology and supply chain development. Dr. Li began his career at IBM as an Advisory Engineer. He was part of the team who developed the industry first Flip Chip Plastic Ball Grid Array (FC-BGA) for fast SRAM applications. He led a cross-functional team to develop an optoelectronics package for Philips Electronics' Liquid Crystal on Silicon (LCOS) devices before joining Cisco System. He received his M.S. and Ph.D. degrees in Mechanical Science and Engineering from the University of Illinois at Urbana-Champaign.

**David McCann** has been at GLOBALFOUNDRIES for five years, where he is Vice President of Packaging R+D and Operations. He is responsible for groups in Dresden Germany, New York, California, and Singapore. He is based at the Fab 8 site, in Malta, New York. David's groups are responsible for Advanced Silicon Packaging development, qualification of GLOBALFOUNDRIES silicon application representative devices and packages, interconnect development, Post Fab strategy, GLOBALFOUNDRIES's internal bump and probe factories, and external OSAT supply chain development and execution. He also led the GLOBALFOUNDRIES/IBM post-fab process and business integration. David's background prior to GLOBALFOUNDRIES was in flip chip technology development and business management in the OSAT industry, and prior to that, flip chip assembly and product development in implantable medical electronics. David was a member of the ECTC Executive Committee for 10 years.

**Igino Padovani** is Business Development Manager for Vital Sensors at Robert Bosch LLC in Palo Alto, CA. He has a long history in MEMS and BioSensors product development and product definition. His mission at Bosch is to generate new business opportunities and to develop strategic partnerships in health and well-being areas. Prior to Bosch, he was Product definer for Maxim Integrated in San Jose, CA working on BioSensors for consumer and medical markets. At Maxim, Mr. Padovani was also founding member

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of the Sensing Solutions business unit and he was instrumental in building and marketing the MEMS product line from ground up. Before Maxim, Mr. Padovani worked in MEMS R&D at STMicroelectronics in Cornaredo, Italy where he developed the microphone product line in partnership with OMRON, JP. Mr. Padovani holds seventeen patents and patent applications and has Master degree in Electrical Engineering from Politecnico di Milano, Italy.

**Dr. Gamal Refai-Ahmed** is a Distinguished Engineer of thermal packaging at Xilinx, Visiting Professor at SUNY and Adjunct Professor University of Toronto. Prior to Xilinx, he was a Senior Engineer with GE Global Research Center, AMD Fellow. Dr. Refai-Ahmed obtained his B. Sc. and M. Sc. degrees from Alexandria University. He obtained the M. A. SC. and Ph. D. degrees in Mechanical Engineering from the University of Waterloo. Dr. Refai is an Associate Editor of Journal Components and Packaging, IEEE and Journal of Electronic Packaging, Transactions of the ASME. Gamal is the recipient of 2008 excellent thermal management award, 2010 best Associate Editor J Electronics Packaging, 2010 Calvin Lecture and 2013 K16- Clock award in recognition for his scientific contributions and leadership of promoting best electronics packaging engineering practice. In 2014, Gamal received the IEEE Canada R. H. Tanner Industry Leadership for sustained leadership in product development and industrial innovation.

**Brandon Wang** is a Group Director at Cadence Design Systems. Brandon Wang oversees the overall Cadence 3D-IC, and ULP (Ultra Low Power) solution marketing and product development activities, as well as enablement efforts on various advanced technologies with strategic partners. Prior to joining Cadence, Brandon spent more than 6 years at ARM, managing the Interface IP Group, and later the PHY product line. Before that, Brandon was with UBICOM, a network processor startup that is now part of Qualcomm. Brandon holds 6 US patents, and has published at a number of IEEE conferences and in journal papers. Brandon is a graduate in Electrical and Computer Engineering from New Jersey Institute of Technology, he also holds an MBA from the Wharton School at the University of Pennsylvania.

## **MORNING KEYNOTE**

# **Heterogeneous Integration: Enabling the Future of the Electronic Industry**

**Wilmer R. Bottoms, Ph.D.**

**Chairman, Third Millennium Test Solutions**

**Co-chair, Heterogeneous Integration Roadmap (HIR)**

The major factors driving the information technology and electronics industries as the end of Moore's Law approaches are changing. The challenges associated with the migration of data, logic and applications to the Cloud, the evolution from the Internet of Things to the Internet of Everything and the consumerization of data, data access and data analytics will be discussed. The crucial role of Heterogeneous Integration to maintain the pace of progress and the difficult challenges, potential roadblocks and potential solutions will be presented. Some specific examples of 3D complex system in package architecture, the incorporation of photonics as a key enabler and requirements for materials innovation will be presented to illustrate future directions in heterogeneous integration.

**SESSION 1**

**DRIVERS FOR  
HETEROGENEOUS INTEGRATION**

## Grand Challenges and Timelines for Electronic-Photonic Integration

Lionel C. Kimerling, Ph.D.  
Thomas Lord Professor of Materials Science and Engineering  
and the Director of the Materials Processing Center  
Massachusetts Institute of Technology

Transistor dimensional shrink enabled constant-cost performance scaling of integrated circuit chip performance at a rate of 100x/10yr. During the same period, interconnection proliferation among distributed resources has enabled computation system performance to scale at a rate of 1000x/10yr. Interconnection is new scaling paradigm for chips and subsystems, and bandwidth density is the new shrink metric. Photonic interconnects are dominant in telecommunication networks, and they have successfully penetrated both data center and HPC rack-to-rack interconnection. In general, the transition from electrical to photonic interconnection occurs at a single-channel bandwidth x distance product of 1-3 Tb/s\*cm (BxD = 1-3 Tb/s\*cm). In 2017 single-channel bandwidth (B) will cross 400Gb/s threshold for board-level distances of >10cm. Board-level optical interconnection will require high volume manufacturing solutions with minimal impact on system cost. Package-level, intra-module photonic interconnection for distances of >1cm are forecast for ~2020 and data rates of 1-3Tb/s. Photonic interconnect solutions can meet system requirements for power and bandwidth density, but they have not yet met the cost point for pervasive intra-system deployment. Silicon photonics is being universally adopted to establish a 'future proof' platform that can achieve 'learning curve' cost reduction with cumulative production. Highlights of the recently released Integrated Photonics System Roadmap (IPSR 2016) will provide the context for discussion of the silicon photonics hardware platform, its architectural evolution over the next two decades and its monolithic integration with electronics for the next scaling paradigm.

## New Die-Dimensions in Heterogeneous Integration

Subramanian S. Iyer, Ph.D.

Center for Heterogeneous Integration and Performance Scaling (CHIPS)  
Henry Samueli School of Engineering, Electrical Engineering Department  
University of California at Los Angeles.

Moore's law has so far relied on the aggressive scaling of CMOS silicon minimum features of over 1000X for over four decades, and recently, on the adoption of innovative features, such as Cu interconnects, low-*k* dielectrics for interconnects, strained channels, and high-*k* materials for gate dielectrics, resulting in a better power performance, cost per function, and density every generation. This has spawned a vibrant system-on-chip (SoC) approach, where progressively more function has been integrated on a single die. The integration of multiple dies on packages and boards has, however, scaled only modestly by a factor of three to five times. However, as SoC's have become more complex and bigger, the NRE and time to market have both ballooned out of control leading to ever increasing consolidation. In this presentation, we show that with the apparent slowing down of semiconductor scaling and the advent of the Internet of Things, there is a focus on heterogeneous integration and system-level scaling. Packaging is undergoing a transformation that focuses on overall system performance through integration rather than on packaging individual components. We propose ways in which this transformation can evolve to provide a significant value at the system level while providing a significantly lower barrier to entry compared with a chip-based SoC approach that is currently used. More importantly it will allow us to re-architect systems in a very significant way. This transformation is already under way with 3-D stacking of dies and will evolve to make heterogeneous integration the backbone of a new SoC methodology.

## Technology Integration for Vital Sensing

Igino Padovani  
Business Development Manager for Vital Sensors  
Robert Bosch LLC

This presentation will discuss a roadmap which delivers system solutions to serve the end-user needs in the health and wellness space – specifically a full system solution for wellness monitoring which provides continuous, motion-compensated heart rate measurement as well as cardiovascular fitness and stress/recovery metrics. On the environmental sensing side, a complete hardware and software solution for indoor air quality will also be discussed.

In order to deliver such solutions multiple technology building blocks have to be integrated while fulfilling severe space and power consumption requirements. This presentation will focus on the evolution of the sensing solutions driven by the Bosch's Vital Sensing applications. The underlying sensing technologies along with the trends in embedded processing and sensor algorithms will be also discussed.

**SESSION 2**

**CHALLENGES FOR  
HETEROGENEOUS INTEGRATION**

**PART 1**



## **Catching Up with Evolution – How to Make Robots See**

**Anders Grunnet-Jepsen, Ph.D.**  
**CTO and Director of the Advanced Technology Group**  
**in Intel's Perceptual Computing Group**

We present Intel's progress on RealSense™ depth cameras, focusing on the latest vision and compute technologies that enable autonomous machines to coexist harmoniously with humans. We showcase usages ranging from small cute robots to fast and nimble drones, and even how it may lead to better autonomous cars. Finally, we touch on how the same technology allows for amazing Augmented Reality and Virtual Reality experiences.

## **Practice and Prospects of Heterogeneous Integration at DARPA**

Daniel Green, Ph.D.  
Program Manager  
DARPA

Abstract not available at time of printing.

## **The Memory of Future Cars**

**Thomas M. Coughlin**  
**President**  
**Coughlin Associates**

Automobiles are becoming rolling applications platforms needing computing power, networking to other cars and the cloud as well as digital memory and storage. This talk will look at the requirements for memory as well as digital storage in automotive entertainment and navigations systems, including expectations for connected cars with driver assist features and autonomous driving. This evolution will include storage in the car, in local as well as remote networks. The evolution of memory and storage technology are key drivers for creating the deep learning capabilities required for the car of tomorrow.

## **AFTERNOON KEYNOTE**

# **Heterogeneous Integration Roadmap: A Status Report**

**William (Bill) Chen, Ph.D.**  
**ASE Fellow and Senior Technical Advisor**  
**Co-chair, Heterogeneous Integration Roadmap (HIR)**

The history of the International Technology Roadmap for Semiconductors (ITRS) including the structure representing the global semiconductor industries will be presented. The various ITRS technical working groups spanning the total technology ecosystem will be discussed. When the end of the ITRS was announced a new Roadmap was established by two IEEE Technical Societies and SEMI focused on Heterogeneous Integration to serve the profession and electronics industry. This Heterogeneous Integration Roadmap (HIR) addresses 19 different technical areas, each with its own Technical Working Group. The specific technical areas in the Heterogeneous Integration Roadmap, as well as other complementary roadmaps and organization working in collaboration with the HIR will be discussed. The working schedules for global collaboration to complete the roadmap by end of 1st quarter 2017 will be presented.

**SESSION 3**

**CHALLENGES FOR  
HETEROGENEOUS INTEGRATION**

**PART 2**

## **The Evolution of Multi-Chip Packaging: From MCMs to 2.5/3D to Photonics**

**David McCann**  
Vice President of Packaging R&D and Operations  
GLOBALFOUNDRIES

We saw successful implementation of products using multi-chip packaging in the 80's and 90's but the expected rate of adoption sputtered. What happened and why? Today we are seeing multi-chip packaging technologies return in abundance. The market drivers of multi-chip packaging will be described and how they differ by market. In addition, multi-chip technologies and the requirements for successful adoption will be presented. We will also take a look at what the future will deliver.

## **SiP Modules – Application Driven Integration**

Eelco Bergman  
Senior Director of Sales & Business Development  
ASE Group

Abstract not available at time of printing.

**PANEL DISCUSSION:**

**Packaging Solutions to Meet Needs  
of the Heterogeneous Integration Roadmap**

**Moderator:**

**Ivor Barber**

**Corporate Vice President of Packaging  
AMD**

**Panelists:**

**Andrew B. Kahng, Ph.D.**

**Professor of CSE and ECE at UC San Diego  
Endowed Chair in High-Performance Computing**

**Li Li, Ph.D.**

**Distinguished Engineer  
Cisco Systems, Inc.**

**Dave McCann**

**Vice President of Packaging R&D and Operations  
GLOBALFOUNDRIES**

**Gamal Refal-Ahmed, Ph.D.**

**Distinguished Engineer of Thermal Packaging  
Xilinx**

**Visiting Professor, SUNY and Adjunct Professor University of Toronto**

**Brandon Wang**

**Group Director  
Cadence Design Systems**



## **About MEPTEC**

MEPTEC is a trade association of semiconductor companies and professionals involved in the manufacturing, packaging, assembling and testing of integrated circuits. Since its inception over 30 years ago, MEPTEC has provided a forum for the semiconductor industry to learn and exchange ideas through our monthly luncheons, conferences, and our quarterly publication, the MEPTEC Report. With the support of an Advisory Board consisting of individuals from all segments of the industry, MEPTEC has, over the years, kept current not just with semiconductor industry developments, but has expanded its scope to cover relevant industry segments such as MEMS and medical electronics. For more information about MEPTEC events and membership please visit [www.meptec.org](http://www.meptec.org).



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