Reliability Testing of Medical Electronic Circuits using IST

Bill Birch
President PWB Interconnect Solutions

What is IST

- *IST = Interconnect Stress Testing*
- *Determines Overall Reliability of PCB's*
- *Powerful and Flexible Reliability Tool*
- *Objective Test Results*
- *Reproducible Test Results*
- *Automated - Set It and For Get It*
- *Complies to IPC TM 650 2.6.26*
- *Industry Wide Acceptance*

How Does IST Work?

- *Uses an IST Coupon that is the Same Configuration as the Board*
- *Thermal Cycles by Electrically Heating the Test Coupon*
- *Continuously Measures Resistance of Circuits During Heating*
- *10% Increase in Resistance is a Failure*
- *Heating Stops within Seconds of a Failure*
- *This Allows for Failure Location of the Most Damaged Via Using a Thermal Camera*

Material Testing

- *With the Advent of RoHS – Material Damage*
- *IST coupon are design with Capacitance Circuits*
- *Measure the Capacitance of a the Coupon*
- *Capacitance is Measured Before, After Precon and End of Test*
- *Greater than a -4% Change in Capacitance is Material Damage*
- *IST Tests the Circuits (copper) and the Material (dielectric)*

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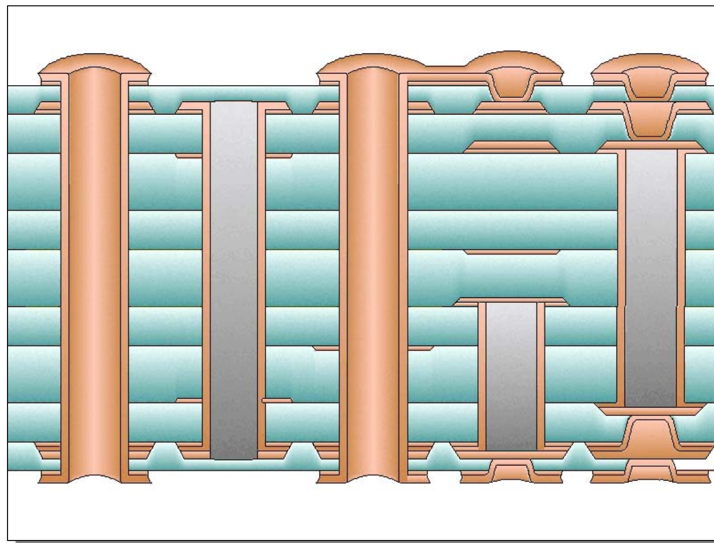
Z Axis Expansion



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Case Study – Three Fabricators

- *This was for a Major Medical OEM*
- *The device is an internal ECG and Defibrillator*
- *This is a sequential laminated eight layer design*
- *Interconnections - microvias and buried vias.*
- *The PWB is made of polyimide*
- *The IST coupon design used is a SL08022*
- *This coupon is tested at 210°C*
- *The test is for 500 cycles*
- *A 10% increase in resistance is a failure*
- *Delamination is a failure*

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Case Study – Design SL08022

- *The coupon is an SL08022 – four circuits*
- *The power circuit P is a buried via on layer 4/5*
- *The sense circuit S1 is microvias on layers 1/2 and 7/8*
- *The sense circuit S2 is microvias on layers 2/3 and 6/7*
- *The sense circuit S3 is microvias on layers 3/4 and 5/5*
- *This coupon is tested at 210°C*
- *This coupon does not have capacitance circuits*

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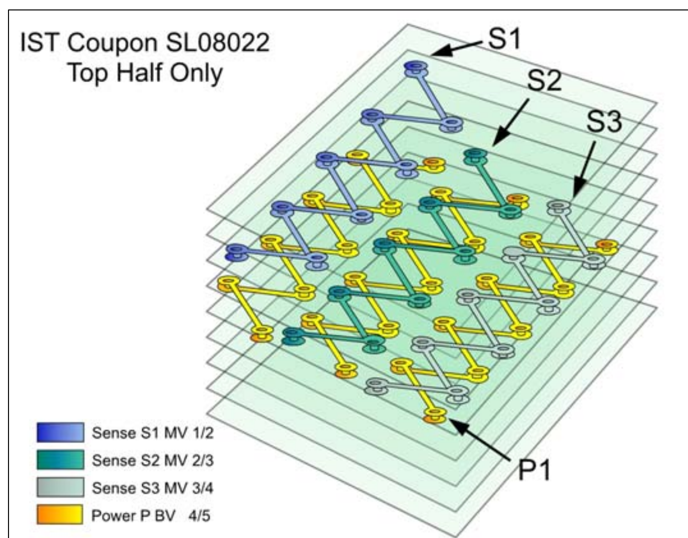
Case Study – Design SL08022



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Case Study – Three Fabricators

- *Fabricator One had no failures and no delamination after testing 80 coupons*
- *Fabricator Two had one power circuit failure and 6 coupons with delamination after testing 10 coupons*
- *Fabricator Three had 18 power circuit failures out of 18 coupons*

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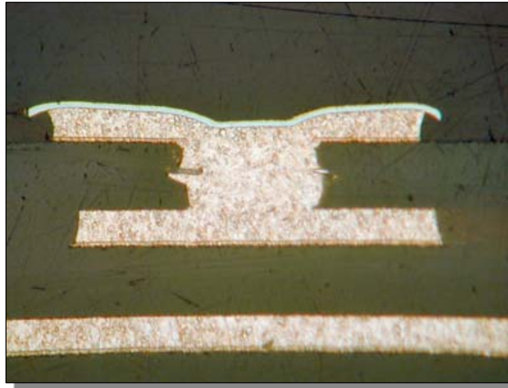
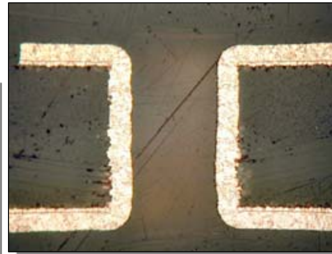
Case Study – Fabricator 1

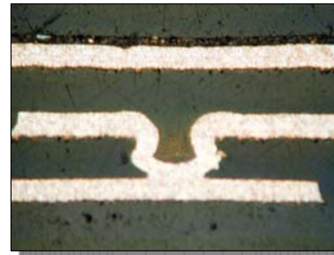
- *The first fabricator has no failures after testing 500 cycles at 210°C, on 80 coupons*
- *There was no delamination*

IST Cycles to Failure - Tested 500 cycles at 210°C -									
Coupon	**P**	**P%**	**S1**	**S1%**	**S2**	**S2%**	**S3**	**S3%**	**Result**
S1_06	500	-2.6	500	-2.6	500	-2.6			Accept
S10_04			500	-0.5	500	-0.4	500	-0.5	Accept
S10_06	500	-0.3			500	-0.3	500	-0.4	Accept
S10_07			500	0.3	500	0.4	500	0.4	Accept
S11_05	500	-0.1	500	-0.1			500	-0.2	Accept
S15_04	500	0.1			500	0.1	500	0.1	Accept
S15_05	500	-1.4	500	-1.5	500	-1.6			Accept
S15_06	500	-1	500	-1.1			500	-1.2	Accept
S15_12	500	-0.8			500	-1	500	-1	Accept
S16_05	500	-1.2	500	-1.1	500	-1.2			Accept
S8_06	500	-0.7	500	-0.5			500	-0.7	Accept
S8_12			500	-0.6	500	-0.7	500	-0.8	Accept
S9_05	500	-0.6	500	-0.7	500	-0.6			Accept
S9_06			500	-1.4	500	-1.4	500	-1.4	Accept
S9_12	500	-1.4			500	-1.4	500	-1.3	Accept
R2_02			500	1.2	500	1.3	500	1.4	Accept
R4_04	500	0.7	500	0.6			500	0.8	Accept
R6_04	500	1.3			500	1.3	500	1.4	Accept
S11_06			500	-1.4	500	-1.4	500	-1.2	Accept
S11_07	500	-2	500	-1.9			500	-1.8	Accept
S11_12	500	-0.5			500	-0.5	500	-0.4	Accept
R6_08	500	0.8	500	0.8	500	0.8			Accept
R6_02	500	0.6	500	0.6			500	0.6	Accept
R7_04			500	1.5	500	1.5	500	1.5	Accept
R14_02	500	0.3	500	0.2	500	0.3			Accept
R4_07			500	1.7	500	1.9	500	1.9	Accept
R13_07	500	1.3			500	1.4	500	1.3	Accept
Q5_05			500	0.8	500	0.8	500	0.9	Accept
Q2_10	500	2.3	500	2.2			500	2.3	Accept
Q1_03	500	2.1			500	2	500	2.2	Accept
Mean	**500**	**0**	**500**	**0**	**500**	**0**	**500**	**0**	
Std Dev	0.0	1.3	0.0	1.3	0.0	1.3	0.0	1.2	
Min	500	-2.6	500	-2.6	500	-2.6	500	-1.8	
Max	500	2.3	500	2.2	500	2	500	2.3	
Range	0	4.9	0	4.8	0	4.6	0	4.1	
Coef Var	**0.0%**		**0.0%**		**0.0%**		**0.0%**		

Case Study – Fabricator 1







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Case Study – Fabricator 2

- *The second fabricator had one failure out of 10 coupons*
- *There was delamination in 6 coupons*

IST Cycles to Faiure - 210°C -										
COUPON	**P1**	**% P**	**S1**	**% S1**	**S2**	**% S2**	**S3**	**% S3**	**Delam**	**Results**
1	500	0.3	500	-0.1	500	0.1			Yes	Accept
2	500	-0.3	500	-0.7			500	-0.4	Yes	Accept
3	500	3.6			500	4	500	3.3	Yes	Accept
4	500	-1.3	500	-1.3	500	-1.2			No	Accept
5	500	-2.8	500	-2.7			500	-2.6	No	Accept
6			500	1	500	1.1	500	1	No	Accept
7	500	1.5	500	1.3	500	2.5			Yes	Accept
8			500	2.4	500	3.8	500	2.5	Yes	Accept
9	500	0.9			500	1.3	500	0.6	yes	Accept
10			250	0	249	0.7	250	10	No	S3
Mean	**500**	**0**	**469**	**0**	**469**	**2**	**464**	**2**		
StDev	0	2	88	2	89	2	94	4		
Min	500	-3	250	-3	249	-1	250	-3		
Max	500	4	500	2	500	4	500	10		
Range	0	6	250	5	251	5	250	13		
Coef Var	**0%**		**19%**		**19%**		**20%**			

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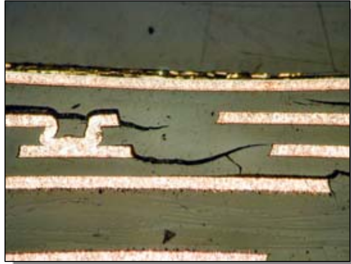
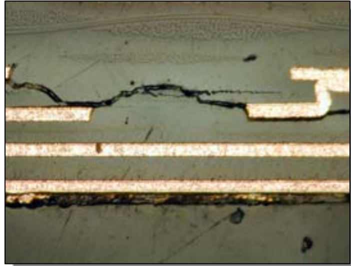
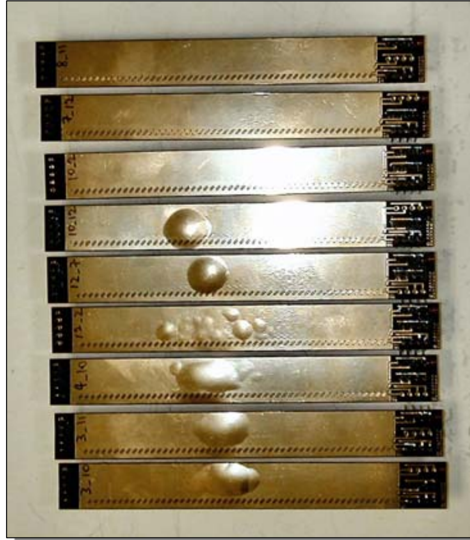
Case Study – Fabricator 2







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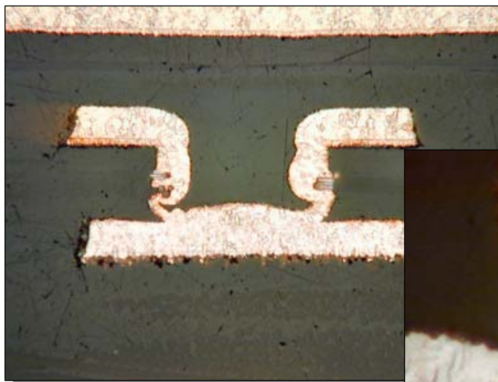
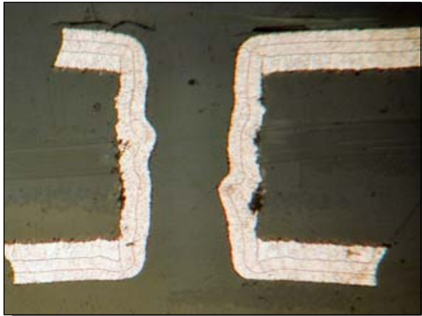
Case Study – Fabricator 2



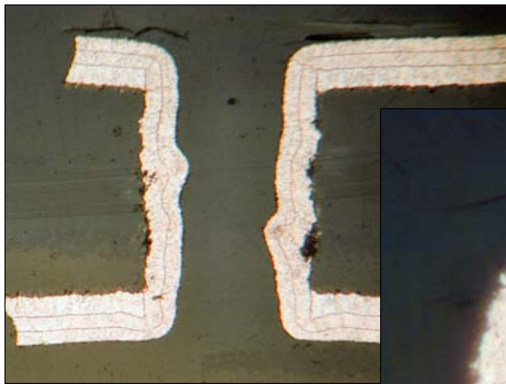
Case Study – Fabricator 3

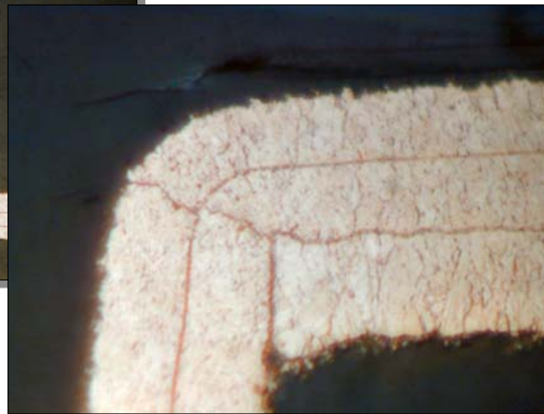
- *The third fabricator had 18 power circuit failures out of 18 coupons – mean cycles to failure 112*
- *There was no delamination*



Coupon	Power P1	% P1	Sense S1	%S1	Sense 2	% S2	Sense 3	% S3	Failure
E3	100	10	100	1	100	1			Post
E4	103	10	103	1.1			103	1.1	Post
E5	103	10			103	0.7	103	0.7	Post
E6	112	10	112	1.5	112	1.5			Post
E7	149	10	149	0.2			149	0.2	Post
E8	183	10			183	2.7	183	2.7	Post
E9	119	10	119	1.3	119	1.3			Post
E10	149	10	149	1.2			149	1.1	Post
E11	126	10			126	0.9	126	1	Post
E12	114	10	114	1.5	114	1.5			Post
E13	71	10	71	0			71	0	Post
E14	143	10			143	1.2	143	1.2	Post
E15	273	10	273	5.2	273	2.4			Post
E16	24	10	24	1			24	1	Post
E17	213	10			213	2.8	213	2.8	Post
E18	0	10	0	1	0	0			Prec
E19	0	10	0	1			0	0	Prec
E20	42	10			42	-1.5	42	-1.5	Post
Mean	112	10	101	1	127	1	109	1	
StDev	70.6	0.0	75.1	1.3	72.1	1.2	64.7	1.2	
Min	0	10	0	0	0	-1.5	0	-1.5	
Max	273	10	273	5.2	273	2.8	213	2.8	
Range	273	0	273	5.2	273	4.3	213	4.3	
Coef Variation	62.8%		74.2%		56.6%		59.4%		

Case Study – Fabricator Three





Case Study – Three Fabricators

- *Fabricator One was approved after qualification*
- *Fabricator Two changed the material and process and qualified on subsequent tries*
- *Fabricator Three after a few more tries withdrew from consideration*
- *The fabricators are now monitored using two IST coupons per lot*
- *The OEM has never had a circuit board failure*

Failure Location

- *Testing Stops at 10% Increase in Resistance*
- *The Failed Circuit is not Open*
- *The Failed Circuit can be Heated with a Small Amount of Current*
- *While Being Heated the Failed Circuit is Observed with a Thermal Camera*
- *The Most Damaged Circuits Shows as a Hot Spot*
- *Thermo-graphic Camera allows the Identification of the Most Damaged Interconnection*

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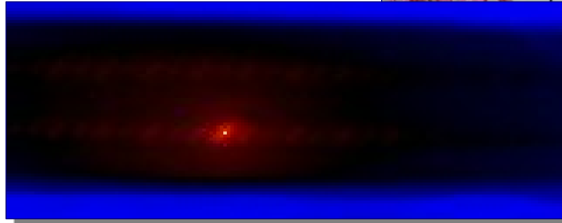
Failure Location



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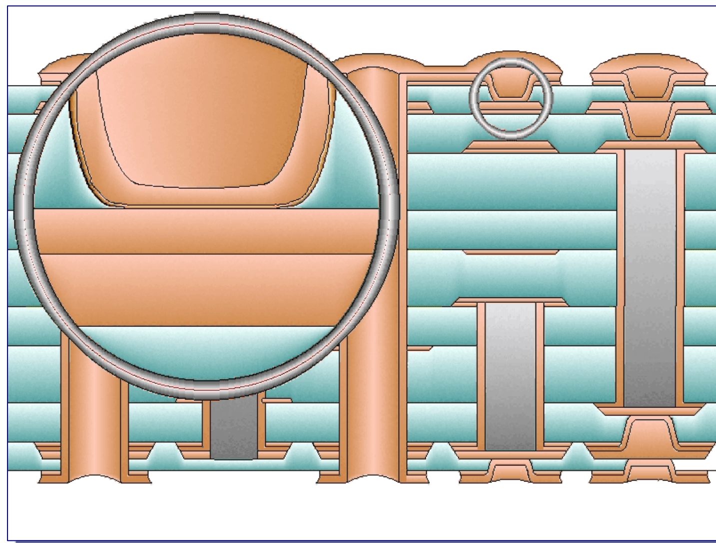
Microvia Separation



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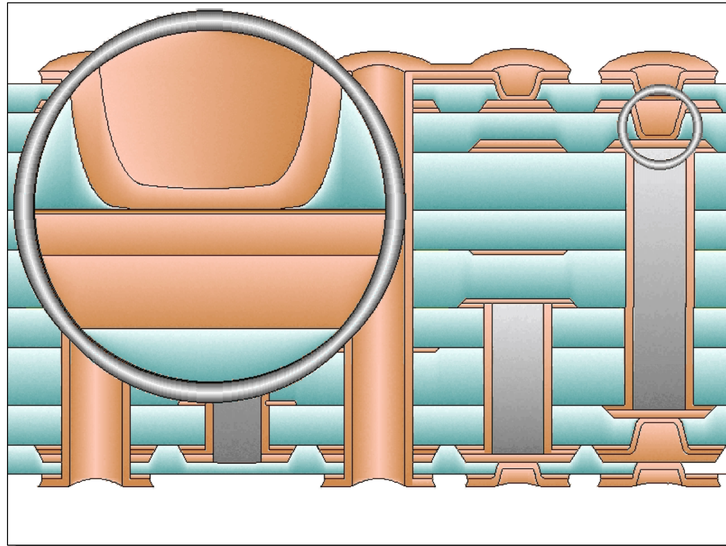
Microvia Barrel Crack



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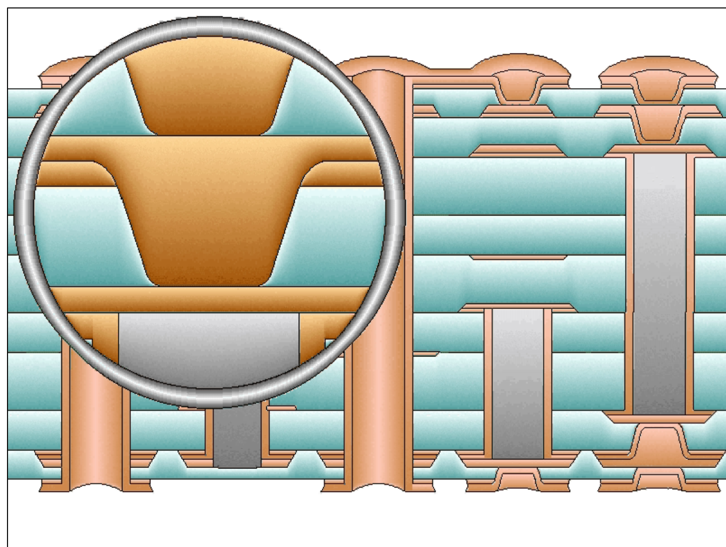
Microvia Corner Crack



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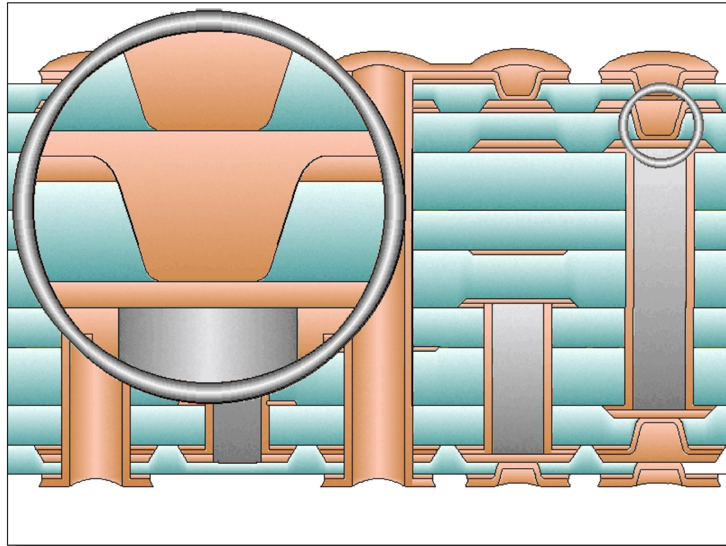
Microvia Pull Out



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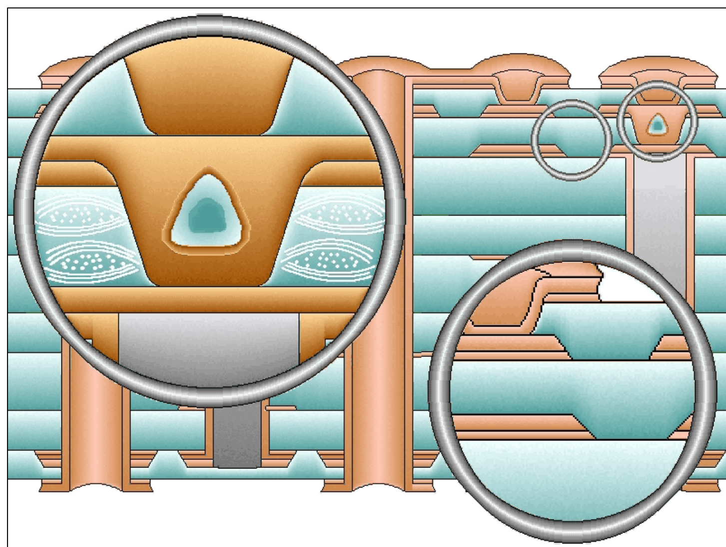
Microvia Void



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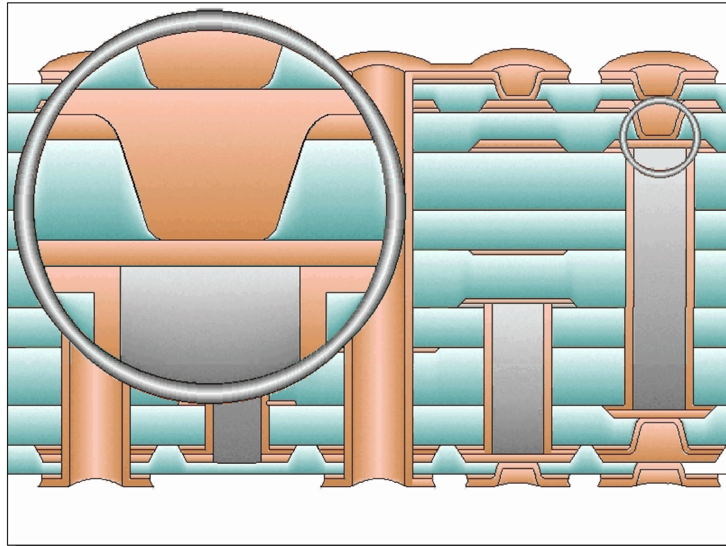
Microvia/Buried Via Lifted Cap



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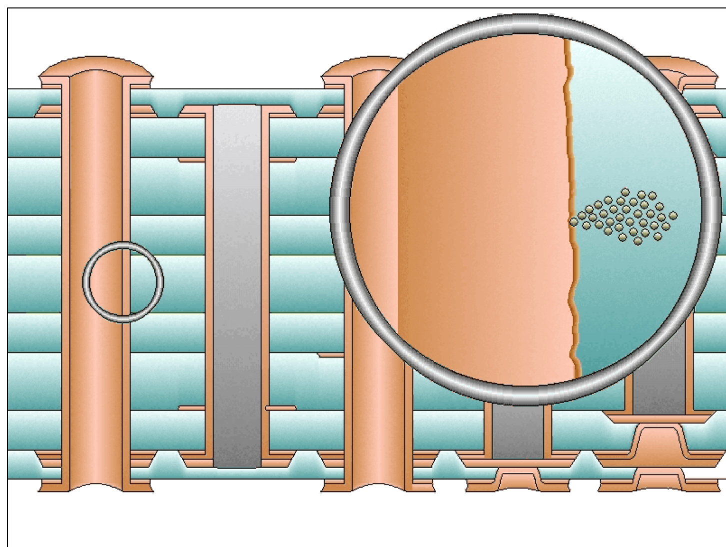
Barrel Crack – Metal Fatigue



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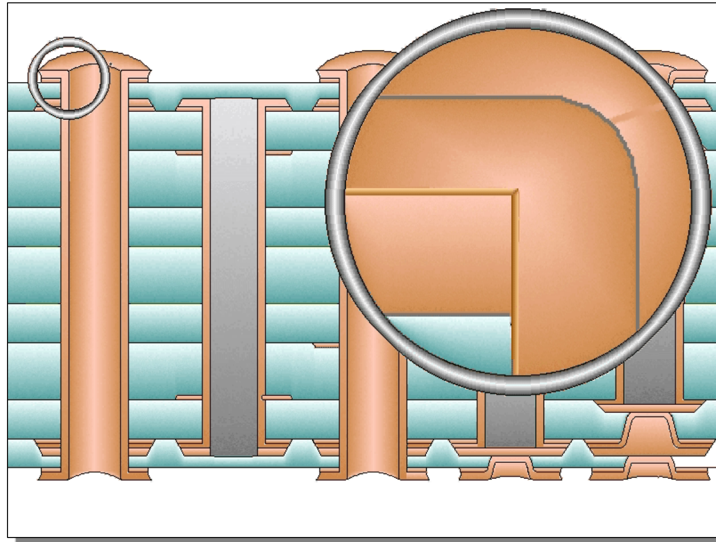
Knee Crack



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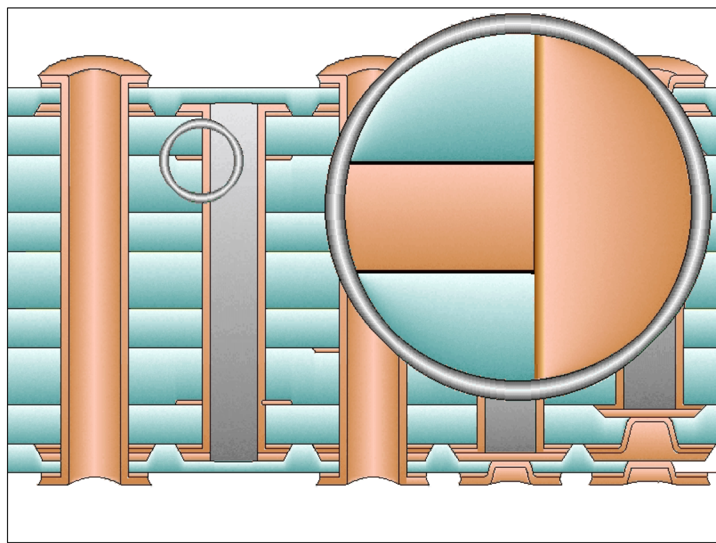
Interconnect Separation



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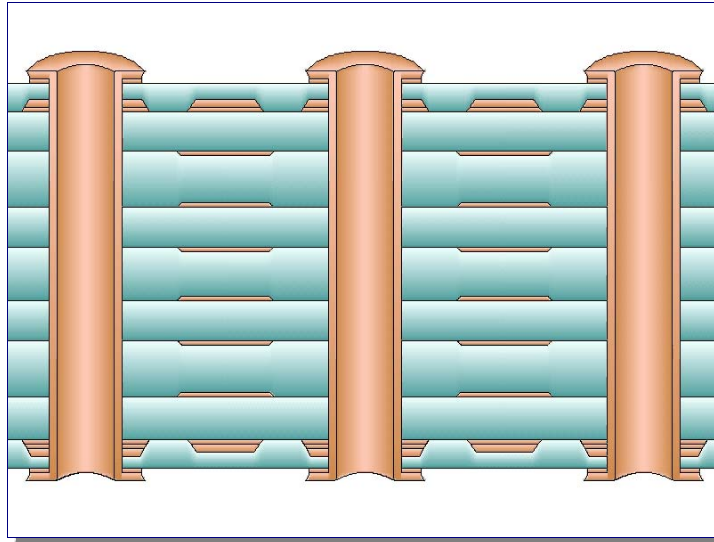
Delamination



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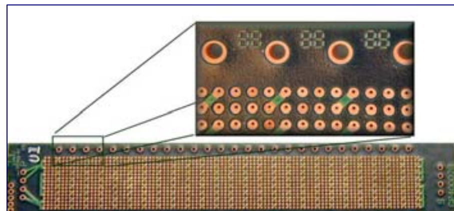
Capacitance Measurement

- *IST Coupon Design Critical to Measurement Sensitivity*
- *Validation of Product Construction / Material Dk*
- *Measurements Taken Before & After IST Thermal Cycles*
- *Changes in Capacitance Signify Delamination*
- *Capability Confirmed, Test Protocol Established/Available*



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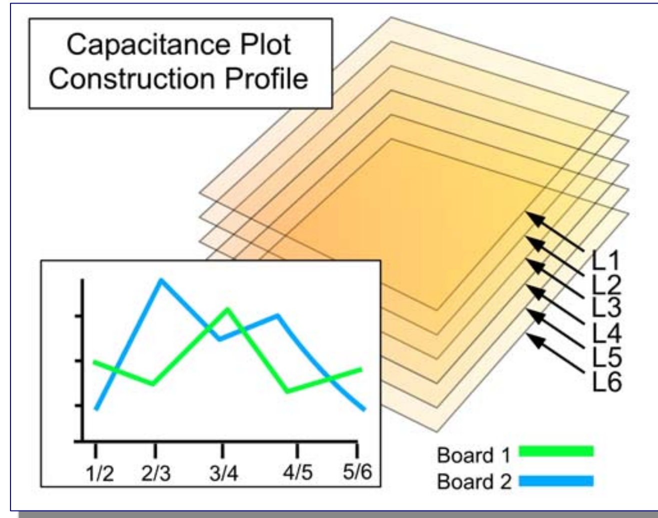
Construction Profile



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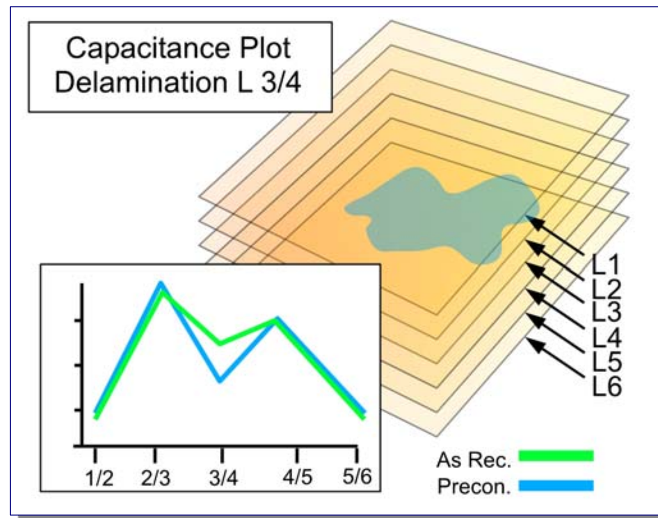
Material Damage



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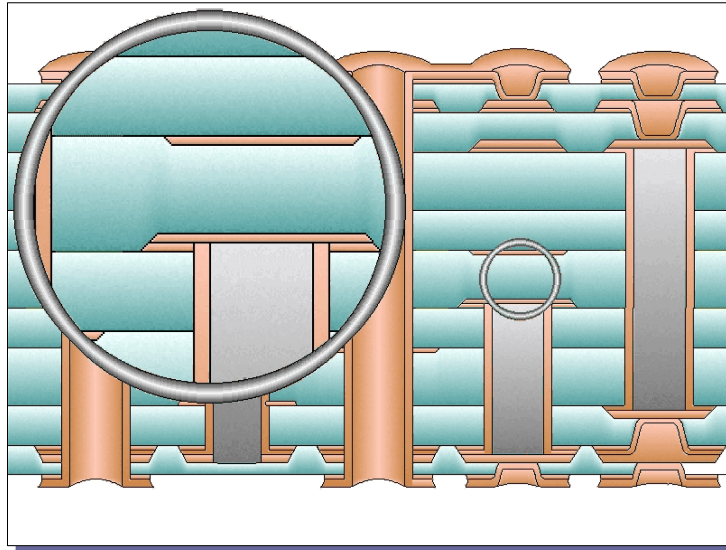
Adhesive Delamination



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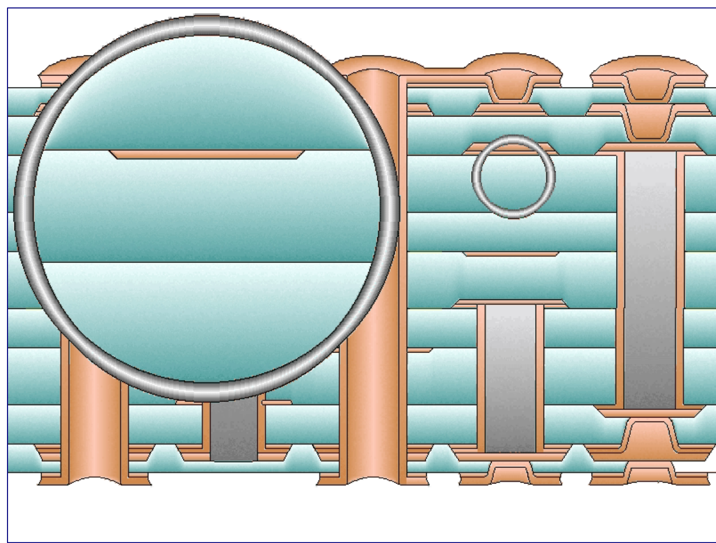
Cohesive Failure



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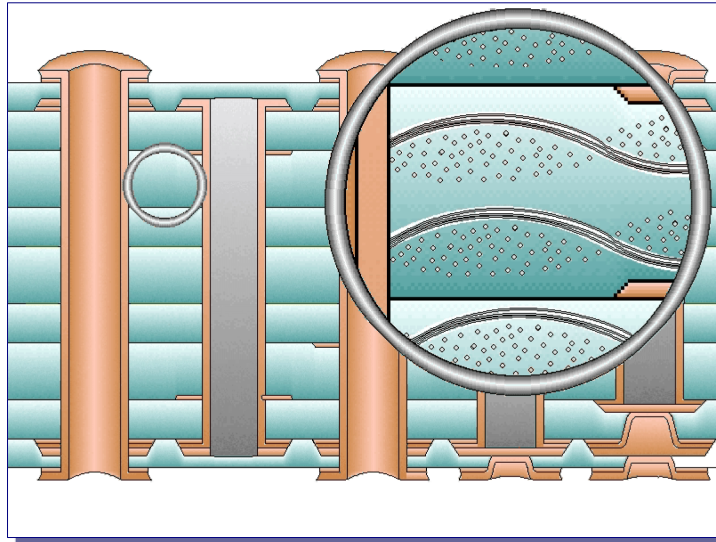
Crazing



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Reliability Testing of Medical Electronic Circuits using IST

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Additional Information

- *The following slides are offered here for additional information about the IST process*

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IST Process

- *Select or Have Design the Correct Test Vehicle (Coupon)*
- *Fabricate a Coupon with Appropriate Attributes*
- *Prescreen Resistance & Capacitance and Select a Test Sample*
- *Precondition – Simulate Assembly and Rework*
- *Capacitance after Preconditioning for Material Damage*
- *Test Coupons by Thermal Cycling to Failure*

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IST Process

- *Plot Damage Accumulation*
- *Capacitance at End of Test to Determine Material Damage*
- *Determine the Circuit Failure Location (Thermal Camera)*
- *Cross Section Perform Failure Analysis for the Root Cause*
- *Determine Observed and Latent Failure Modes*
- *Evaluate Data and Draw Conclusions*

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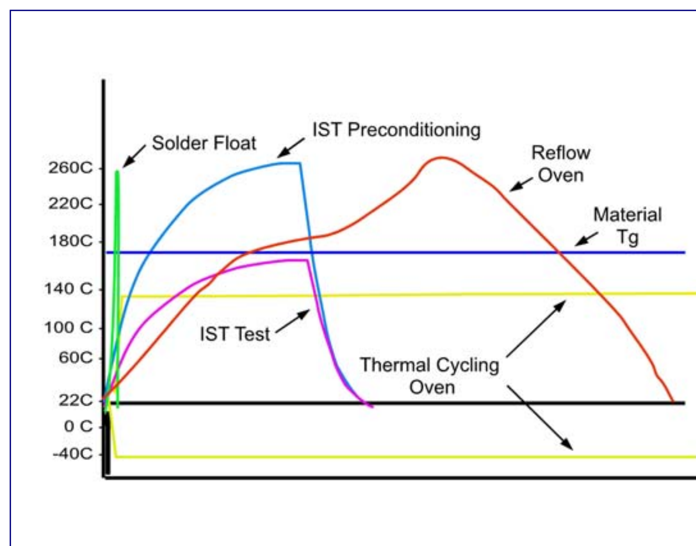
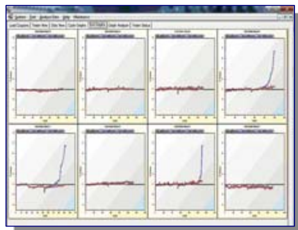
Thermal Profiles

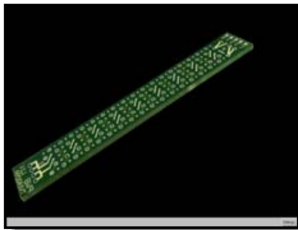
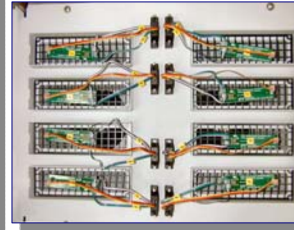


IST Hardware and Software

- *Hardware - IST Testing Machine*
  - *Eight Individually Controlled Test Heads*
  - *Automated – Preconditioning and Testing*
  - *Requires Clean, Controlled Environment*
- *Software*
  - *Automated Control of Heating and Cooling*
  - *Continuous Measurements of Environment and Product*
  - *Automated Report Generation*
  - *Automatic Safety Controls (Watch Dog, Emergency Shutoff)*

IST Equipment



IST Testing

- *Automated Testing Protocol*
- *Operator Independent*
- *Coupons Have Two or More Circuits*
  - *"Power, Sense 1, Sense 2, Sense 3"*
- *Ohmic Heating of Coupon - Tight Control*
- *Coupons are Heated for 3 Minutes +/- 3 Seconds*
- *Coupons Preconditioned to*
  - *Simulate Assembly (3X) and Rework (6X)*
  - *Tin/Lead 230°C, Lead Free 245°C or 260°C*
- *Testing to Any Temperature – 150C to 260C Typical*
- *Convection Cooling to Ambient – Approx 2 min.*

IST Testing

- *Resistance is Measured Continuously on Each Circuit*
- *10% Increase in Resistance is Considered a Failure*
- *Data is written to various files for automatic reporting*

Test Coupon

- *The Coupon Must Reflect the Critical Attributes of the PWB*
  - *Coupon Reflects Thickness and Layer Count*
  - *Copper Weights used in the Construction*
  - *Holes Sizes that includes the Smallest Hole Size*
  - *Surface Finish that is Appropriate*
  - *Grid size*
  - *Construction*
  - *Designs are Required for Each Level of Technology*
- *All Above is Established by the Customers Requirements*

Test Coupon

- *The Line width is the One Variable that is adjustable by IST Design*
  - *Line Width is Determined by IST Coupon Design Requirements*
  - *Power Circuit Line widths are Adjusted to Assure the Resistances are Optimized for Heating Efficiency*
  - *The Sense Circuit Line Widths are Adjusted to Assure the Maximum Sensitivity*

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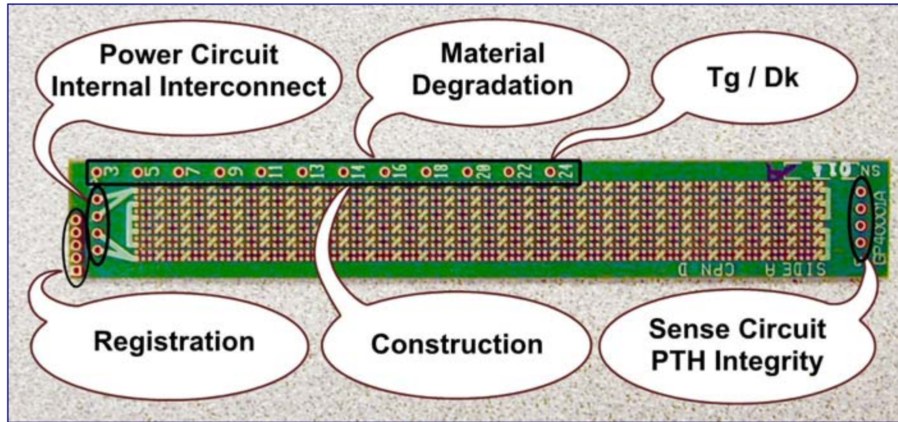
Test Coupon



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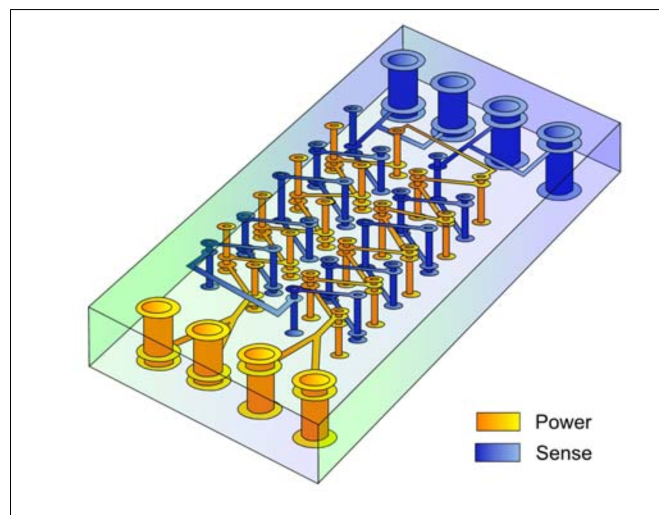
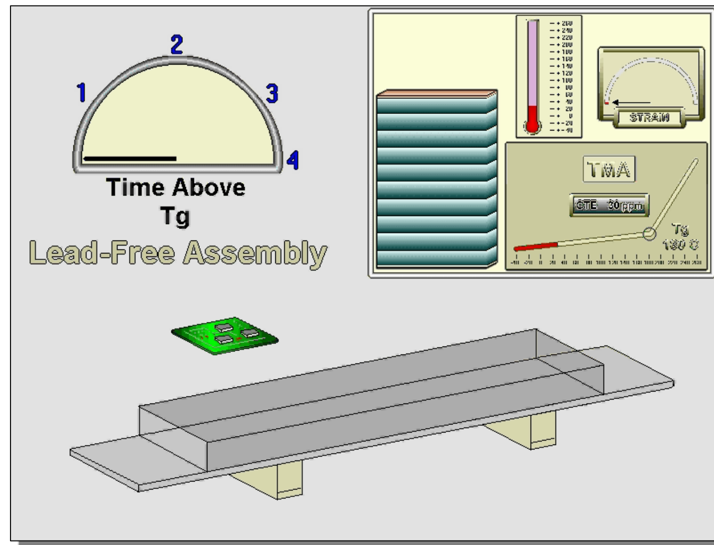
Test Coupon



Thermal Expansion



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Test Method

- *Test to 150°C (Microvia 190°C) +*
- *Test in Three Minutes +/- Three Seconds*
- *Cooling in Approximately Two Minutes*
- *Determines Relative Reliability*
- *Allows Ranking of Process, Materials etc.*
- *Uses Standard and Weibull Statistical methods*
- *Tests the Interconnect and PTH integrity at The Same Time*

Test Temperatures

- *Performance and Baselines =150°C*
- *Microvias = 190°C*
- *Flex Circuits are Tested at 210°C*
- *Polyimide = 220°C*
- *Survivability Testing Tin Lead = 230°C*
- *Survivability Testing Lead Free = 260°C*
- *Preconditioning Tin/Lead Assembly = 230°C*
- *Preconditioning Lead Free = 245°C or 260°C*
- *Acceleration Testing Typically 150°C, 160°C and 170°C*
- *Test Temperatures Can Be Adjusted as Required*

IST Methodology

- *Rejection Criteria is a 10% Increase in Resistance*
- *A 10% Resistance Established by Military Specifications*
- *Failures can happen abruptly, or progressively*
- *Failures can occur on the sense or power circuit*
- *Material Damage is a Rejection Criteria*
- *Material Damage is Based on Capacitance (-4%)*

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Plot of Damage Accumulation

- *Plot of Damage Accumulation at 150°C*
- *Resistance at Temperature for Each Cycle*
- *Damage is caused by cracks in copper*
- *Damage is Express as Increase in Resistance*
- *A 10% Increase is a Failure = Top of Graph*
- *Review – Onset, Slope, Acceleration etc.*
- *Sense Circuit Shows Typical Wear Out*
- *Power Circuits Shows Typical Acceleration*

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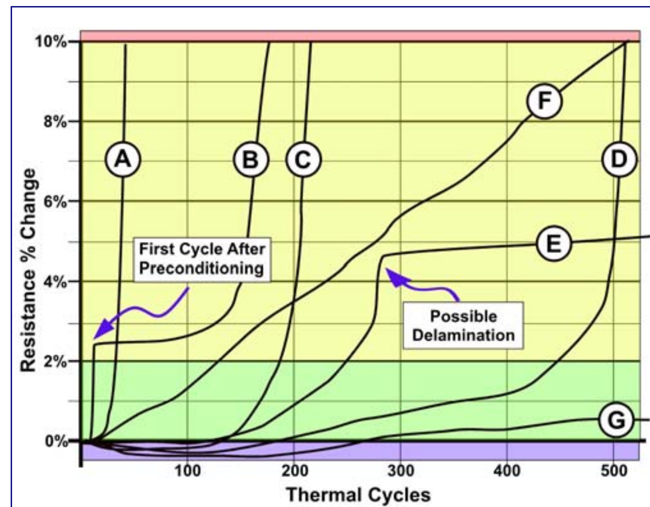
Plot of Damage Accumulation



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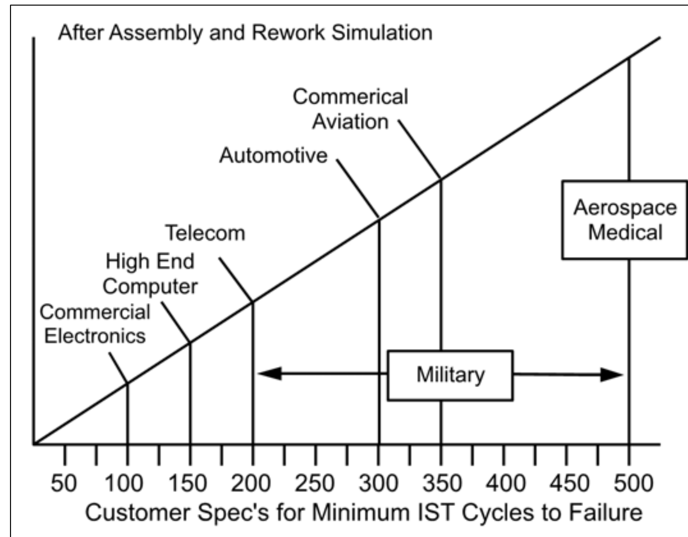
Minimum Cycle by Industry



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Reliability Testing of Medical Electronic Circuits using IST

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