Silicon Interposer Design: Architecture through Implementation

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MEPTEC Nov 2012

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Silicon Interposer Design

- Today's interposer serves as a bridge between the higher density of today's die, and the IC package
- Is interposer design an IC design challenge, or a IC packaging design challenge?

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Interposer: Bridges IC and Package design

Interposer Features	"Coarse"	"Fine"
Metal Line/Space	> 5um/5um	< 1um/1um
Provider	Package house, using RDL manufacturing	Foundry, using IC manufacturing
RDL Metal	Cu	Al, Cu
RDL Thickness	3-5um	<1um
Passive Devices	Yes	Yes
Cost	Lower	Higher
Application	Low I/O Count	High I/O Count
Design Rules	*Package-Like*	*IC-Like*
Design Tool	*APD/SiP (EDI/VLE for Validation)*	*EDI/VLE (APD/SiP for Feasibility)*

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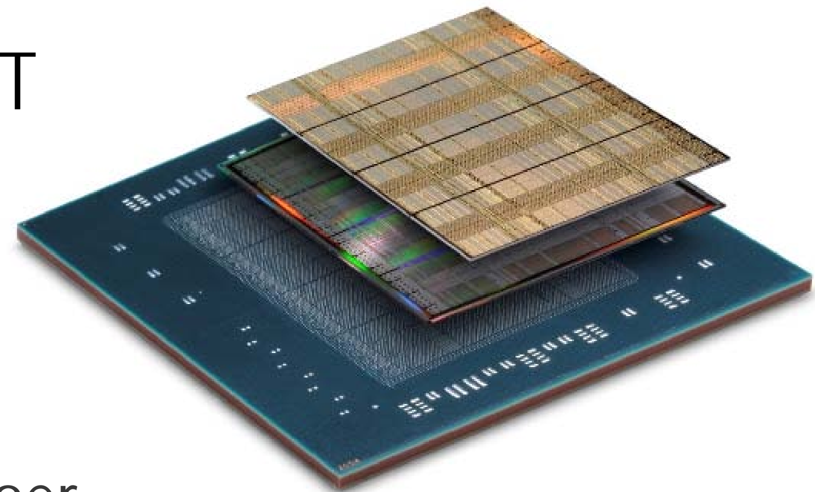
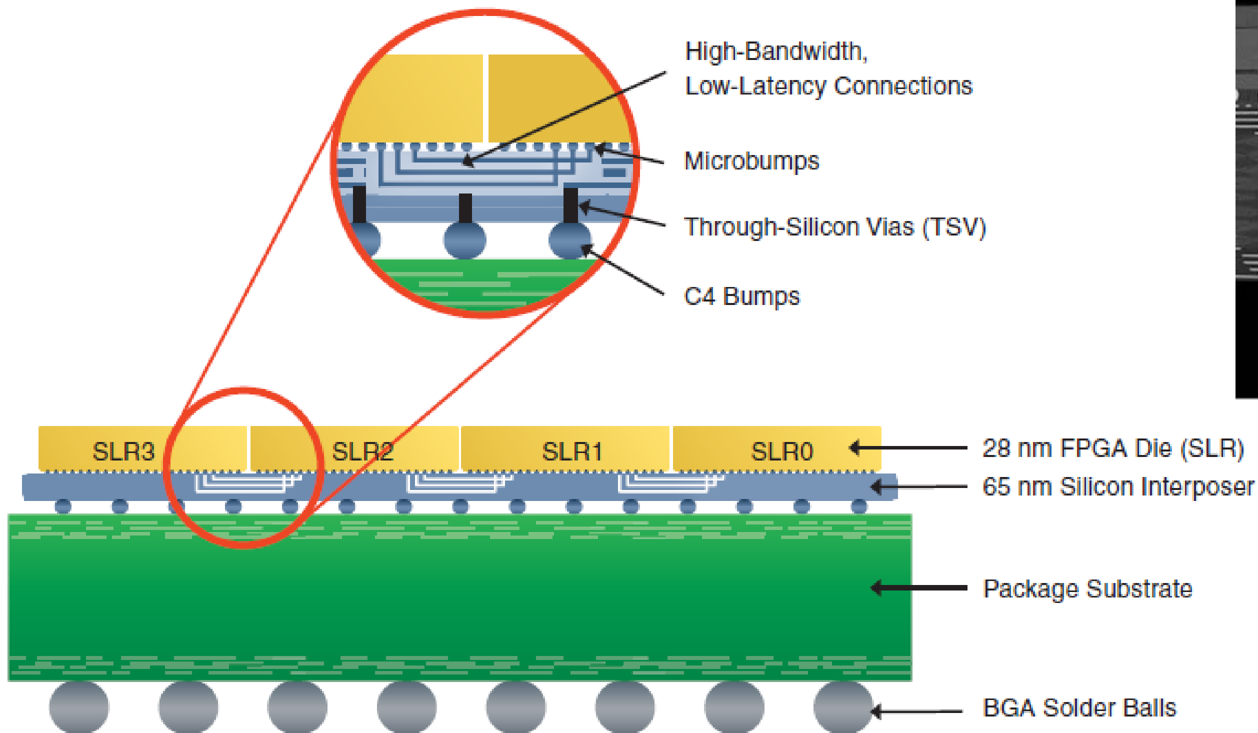
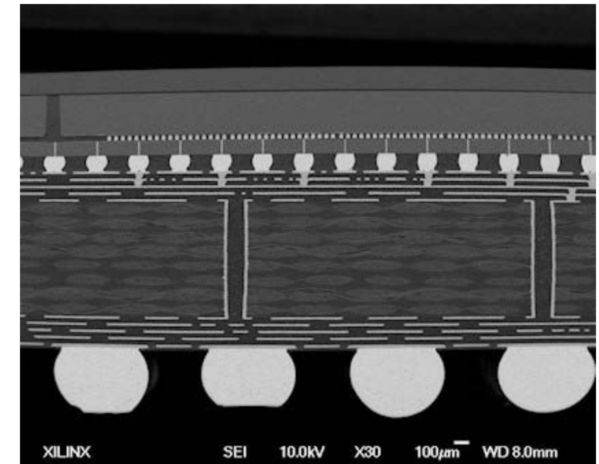
"Classic" Interposer: Virtex-7 2000T



- "Stacked Silicon Interconnect"
- 6.8 Billion transistors
- Four 28nm die on a "fine" Interposer





Source: Xilinx

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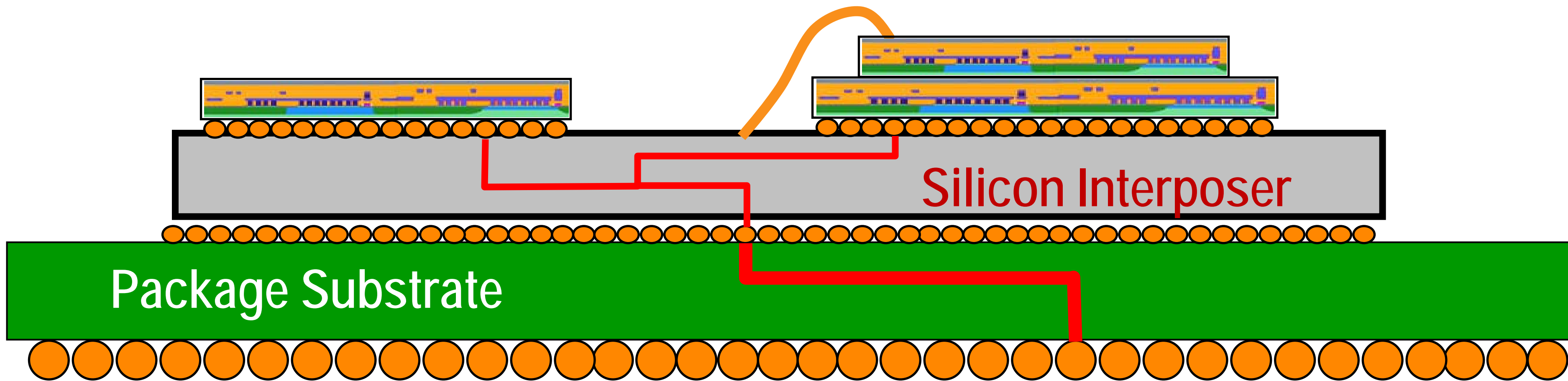
IC-Based 2.5D vs PKG-Based 2.5D



- IC Technology-Based Solution
  - Analysis include Core logic
  - Design for TEST
  - Timing Analysis (STA)
  - Manufacturing ready DRC
  - TSV implementation
- PKG/PCB Technology-Based Solution
  - System Interconnect Analysis
  - System Optimization thru all domains
  - Package Routing Technology
  - Core areas could be Black box
  - TSV proposal

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Perfect World: Interposer Design

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Reality

- Who “owns” the design (IC team, PKG team)? What tools are available?
- What design process node? Course or fine width? What geometry design rules? What IC design structures are needed (power stripes, redundant via)? What layer materials for metal and dielectric?
- Who is making the silicon? (in house, external)
- What is required for IC implementation/mask generation ?

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Why use Packaging tools for Si Interposer Planning?

- **Sorting out the optimization**

  When considering fixed components on the board, the system (chip-interposer-package-board) can be optimized from the board up

- **Preliminary system analysis**

  – When System route planning validates the route-ability of the system
  – System Signal and Power Integrity can be analyzed early

- **Hand off the Interposer plan to IC tools**

  IC Packaging tools can create a representation of a silicon interposer that includes die placement, TSV locations, and feasibility routing that can be transferred to an IC tool for final detailed implementation using IC Design rules

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Possible Interposer Flows

- Design completely in IC Design Tool
- Prototype in IC PKG design tool, Complete in IC Design
  - Use separate databases for interposer and package
  - Use one unified “substrates” database

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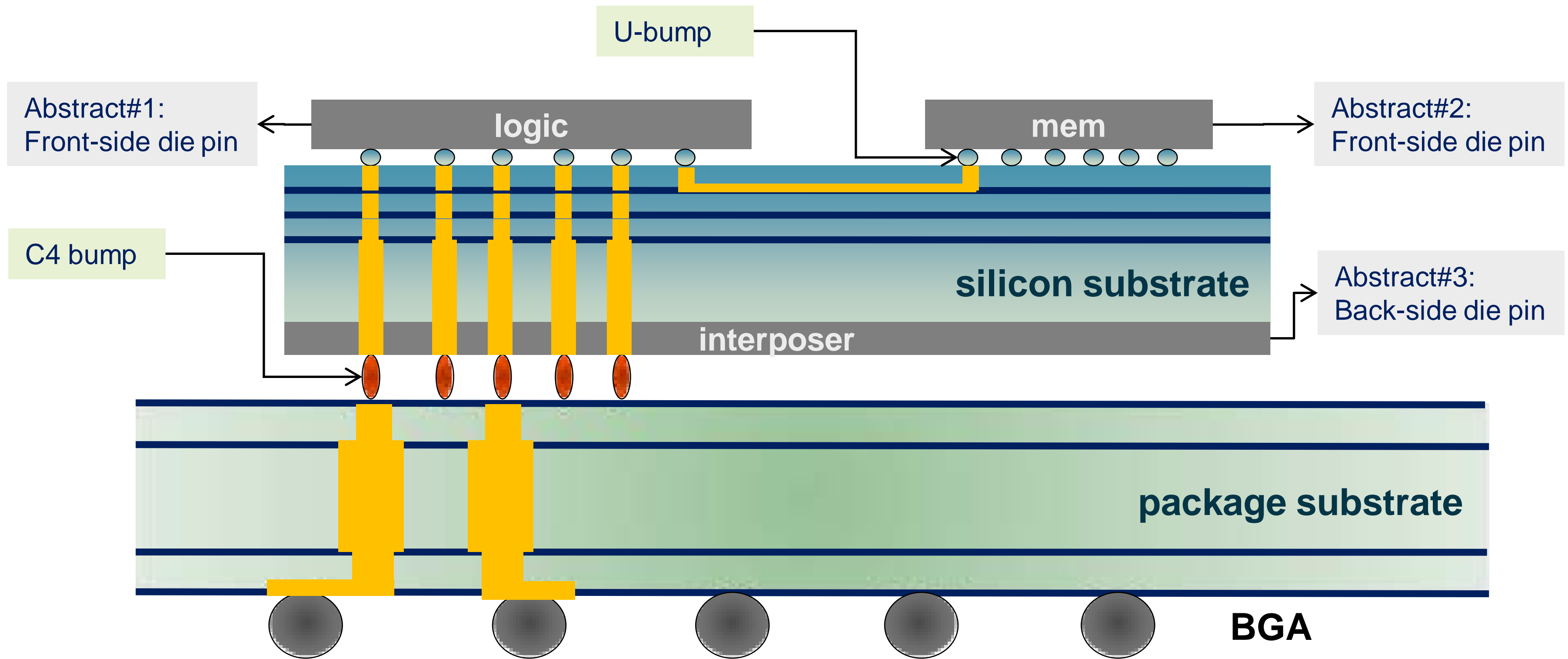
Common Database: Design Overview



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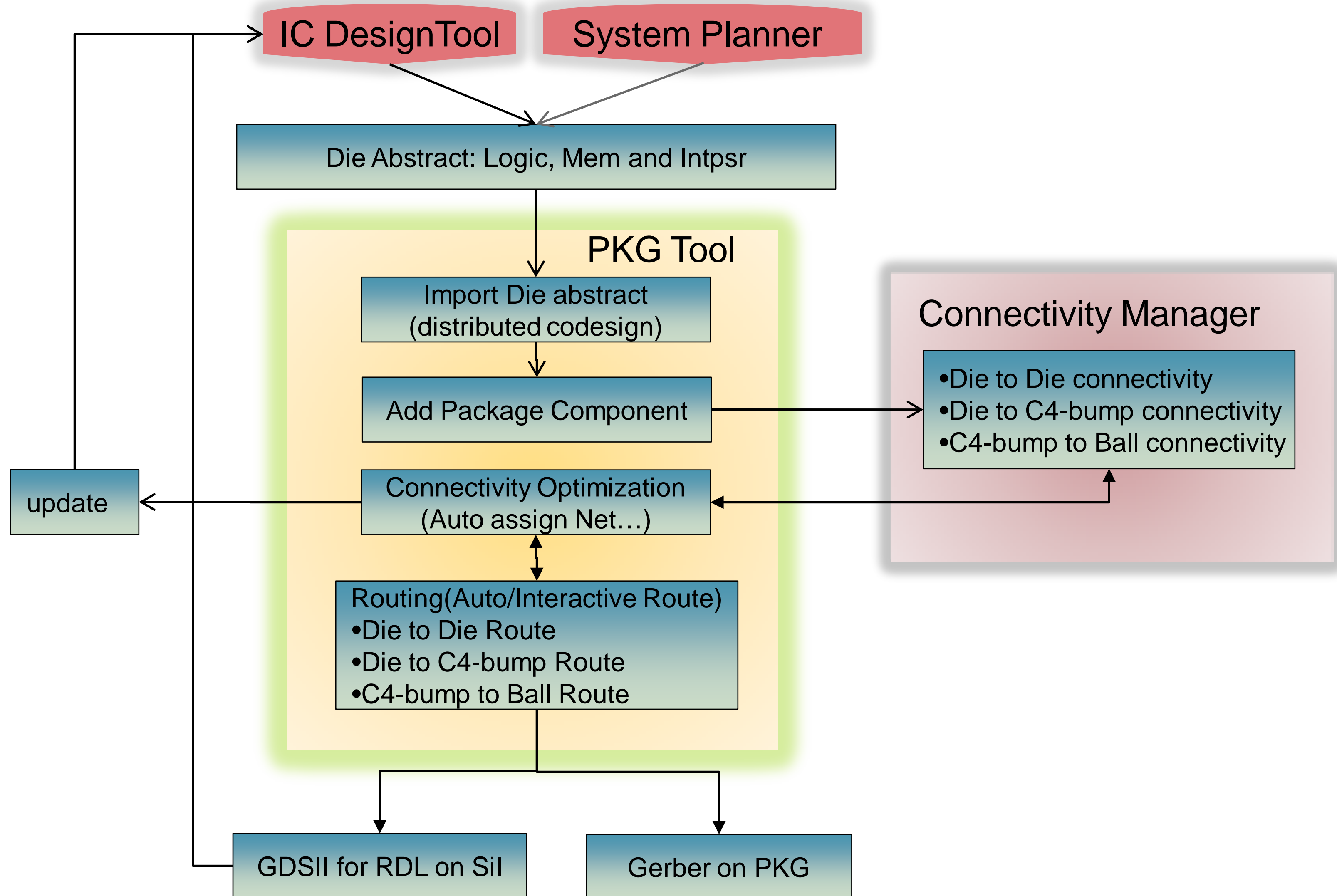
Interposer/Package Co-design Planning Flow



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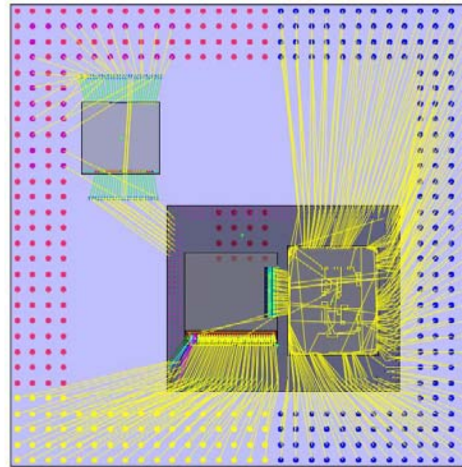
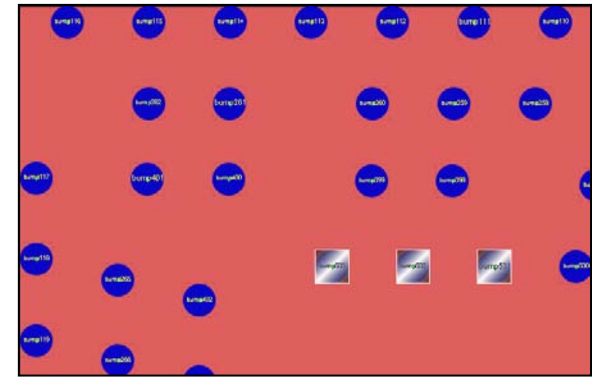
Co-Design and System Feasibility Planning

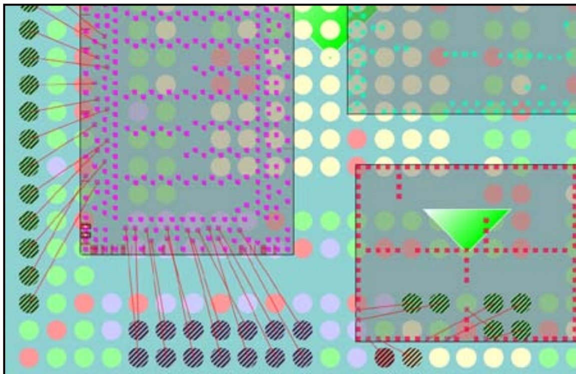
IO Pad Ring Construction



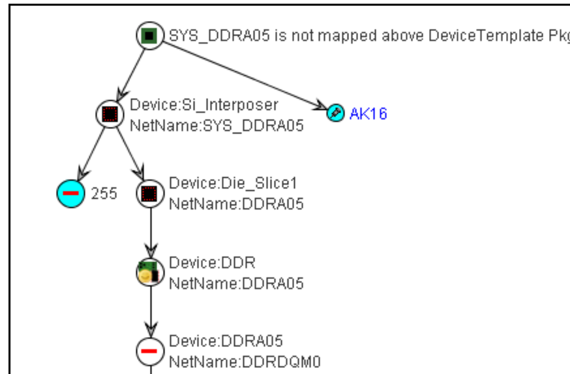
2.5D & 3D Planning



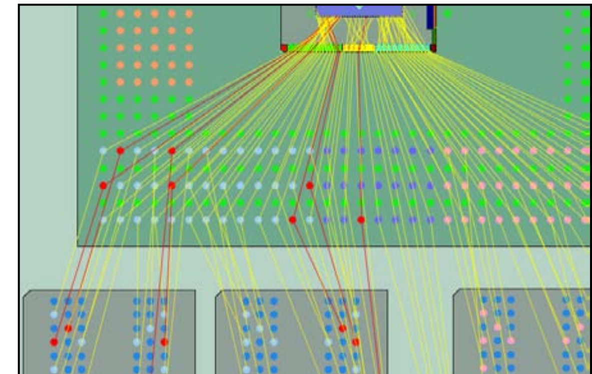
Bump Pattern Development



Multi-Die Support



Net Management



System Connection Planning

Single Canvas Optimization of Chip-Interposer-Package-Board

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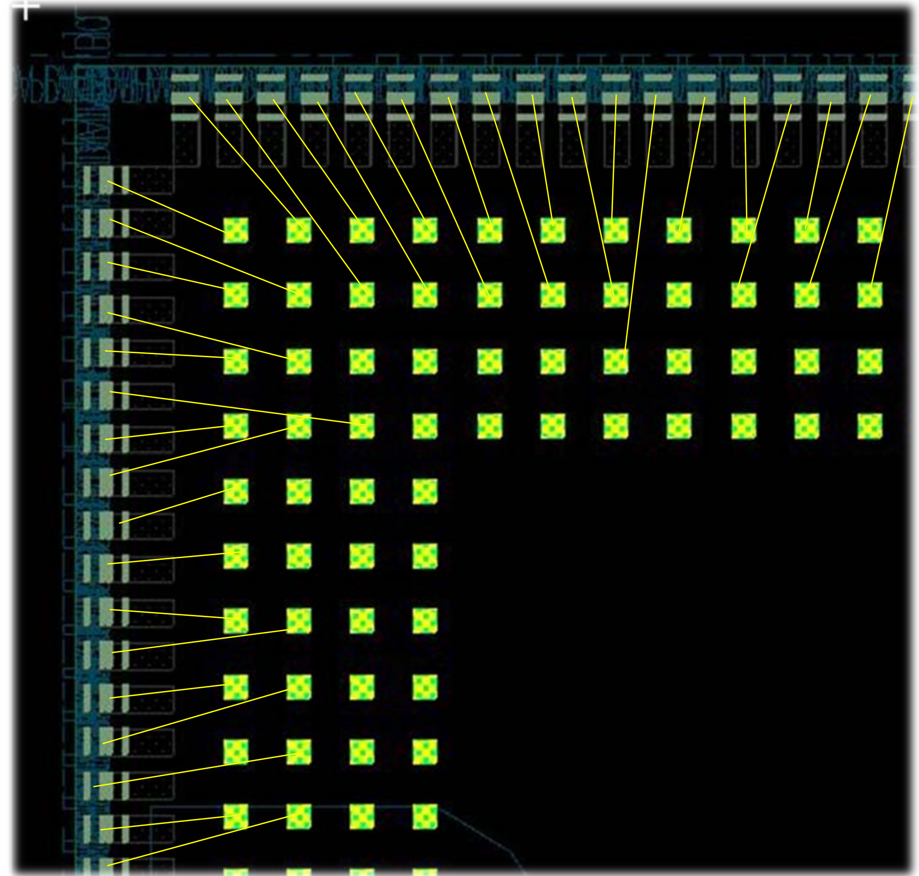
Die Abstract is Self-contained with …

- IC technology information
- Library
  - I/O drivers
  - I/O pins
- Netlist
  - IC Net name inherited from Verilog
  - Flight line between bumps and I/O drivers
- Physical
  - Bumps
  - IC Cells/Pins
  - Die boundary



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Connectivity Management

Net management over multiple domains

SiP Digital Architect GXL - System Connectivity Manager - D:\Allegro_PE_Team\Product\3DIC\inter...\interposer_top.cpm - [sil_pkg [In Master]]

Status		Object	Logical Design(sil_pkg)	Physical Design(sil_pkg_qbus_routed.sip)
Component Differences (3/3)				
✓	ⓘ	MEM#1 (mem)	✗	✓
✓	ⓘ	LOGIC#1 (logic)	✗	✓
✓	ⓘ	INTERPOSER#1 (interposer)	✗	✓
Net Differences (792/792)				
✓	ⓘ	QBUS[270]	✗	✓
✓	ⓘ	QBUS[271]	✗	✓

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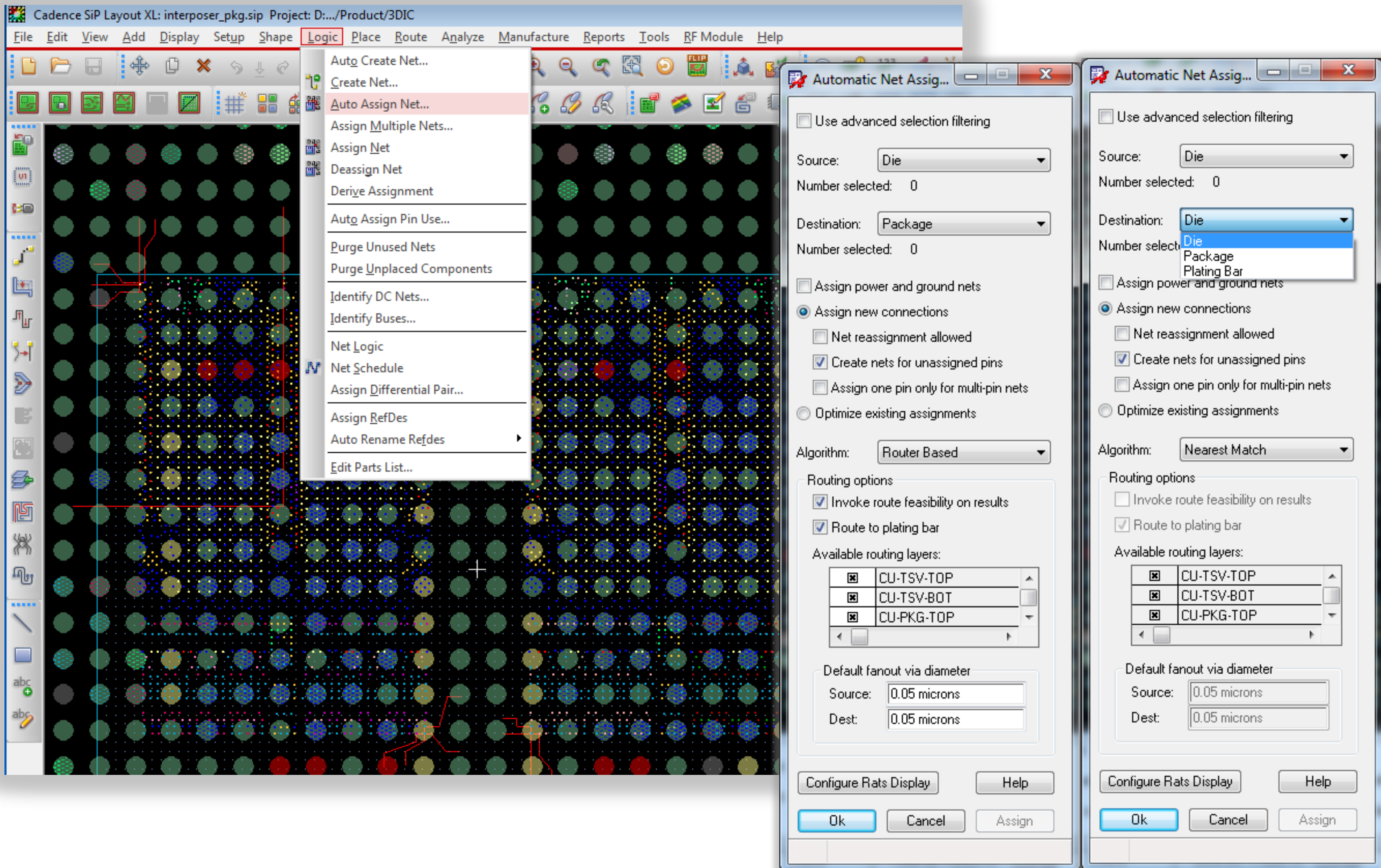
Automatic Die micro-bump → Interposer C4-bump →Package Ball Connection Optimization



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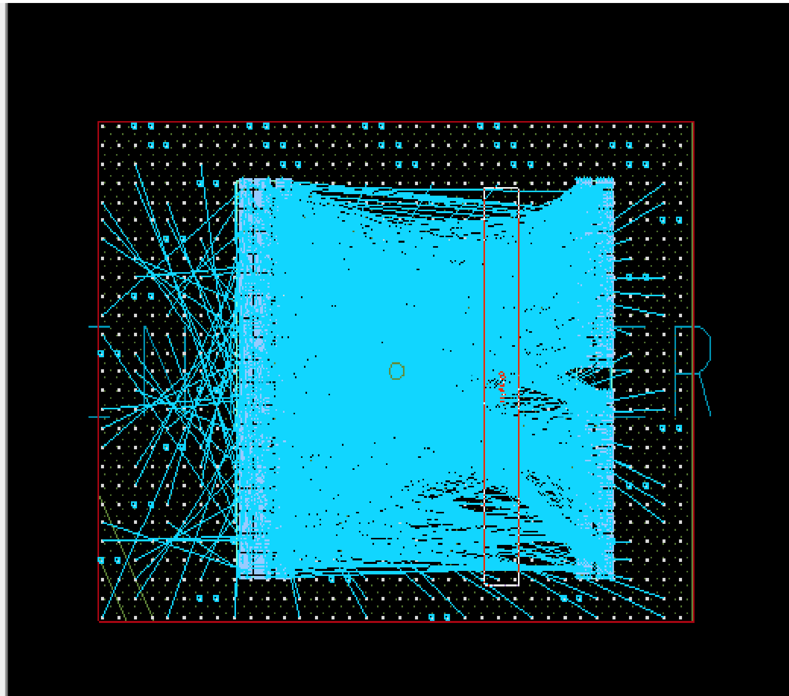
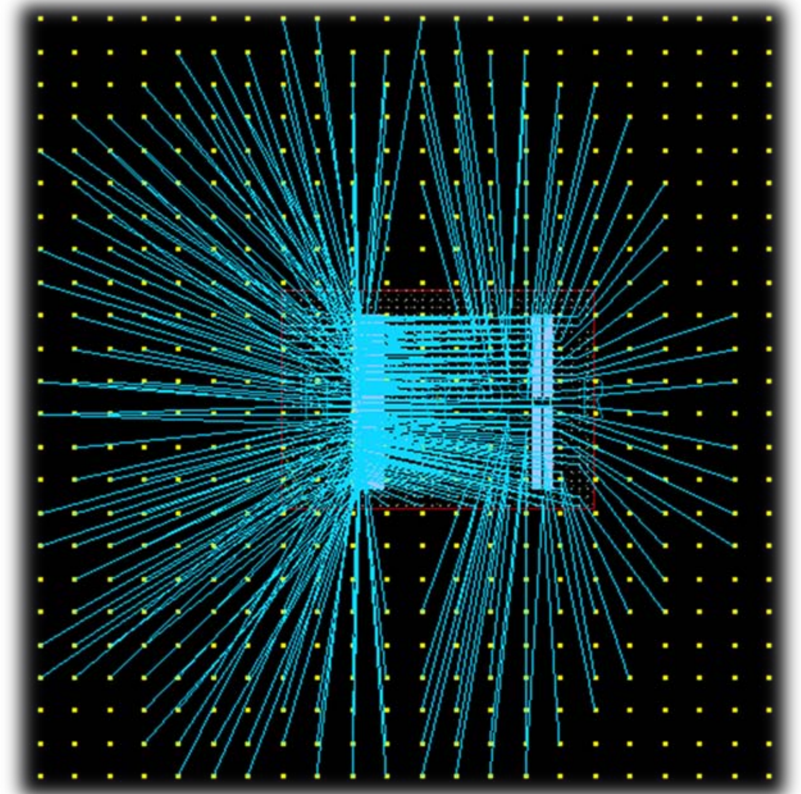
Bump and Micro-Bump Assignment Optimization



Before auto-assign net



After auto-assign net

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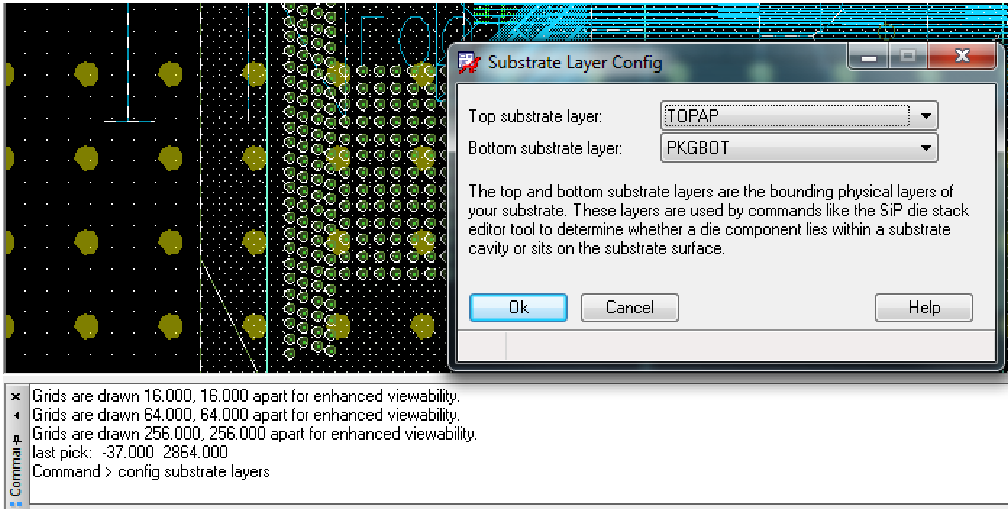
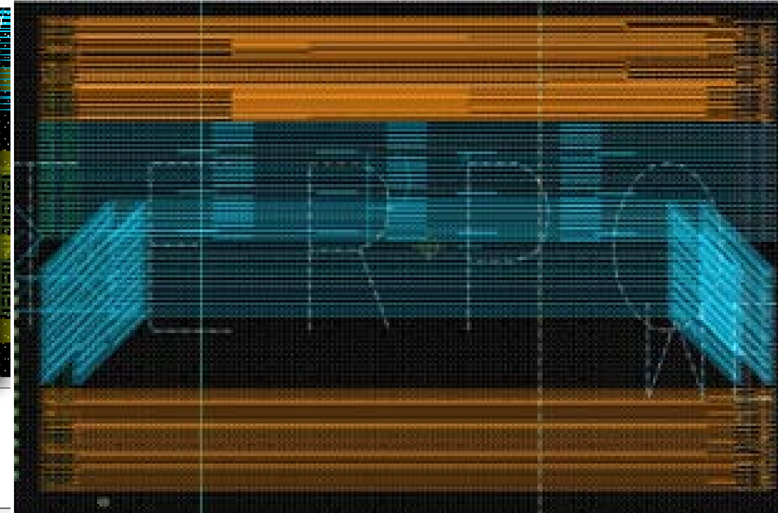
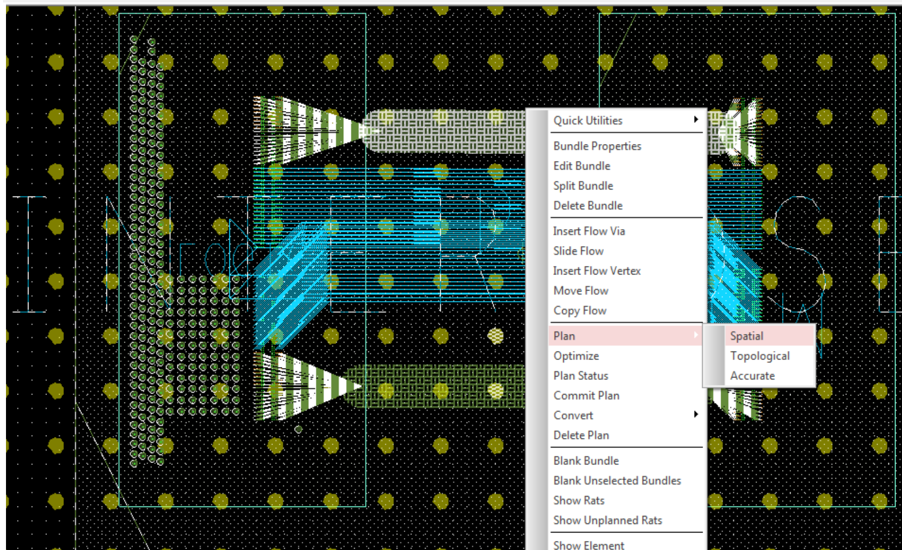
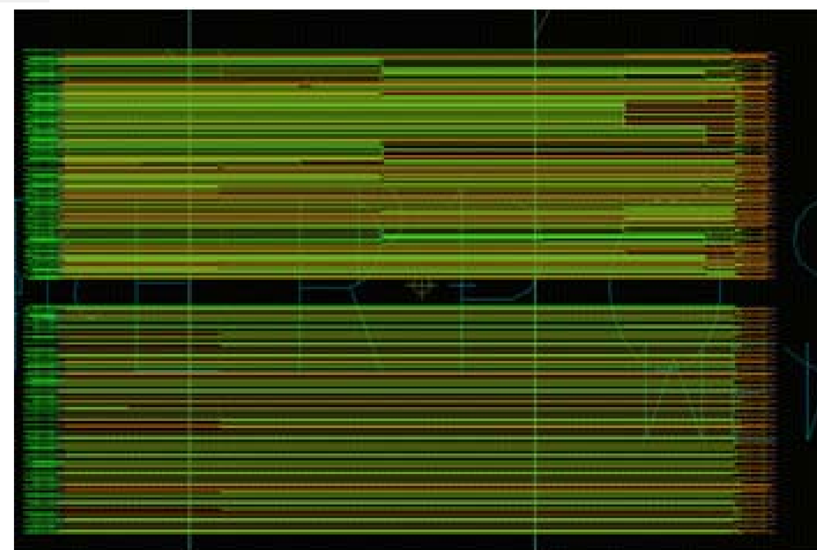
Auto RDL Routing Feasibility









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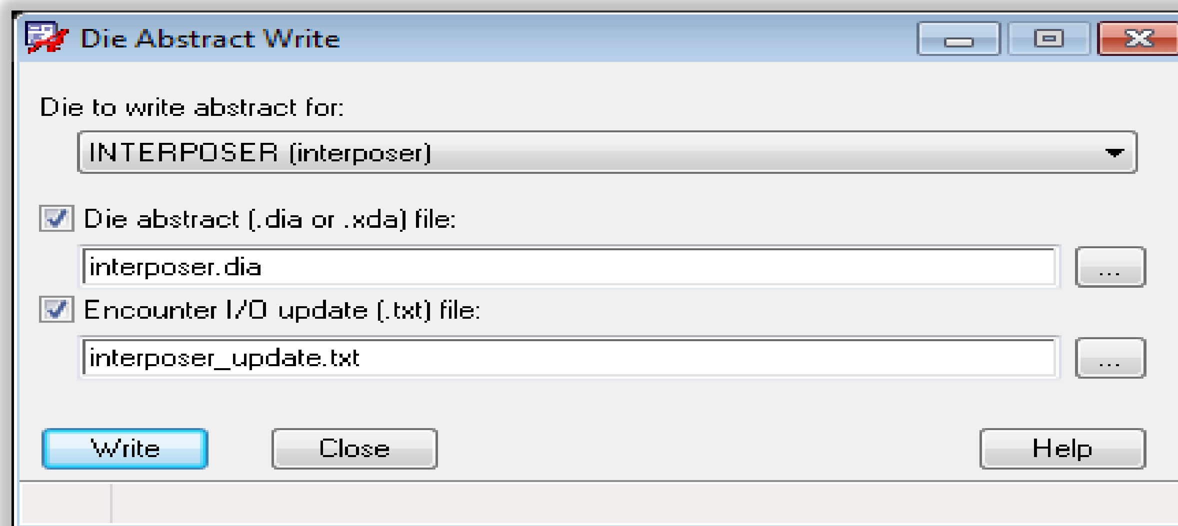
Export Modified Bump Assignment back to IC Tool

- While optimizing bump to bump connection, micro-bump assignments in logic and memory die and C4-bump assignments in the interposer could change.
- Updated die abstract file and IO location file can be written to update floor planning in IC tool.



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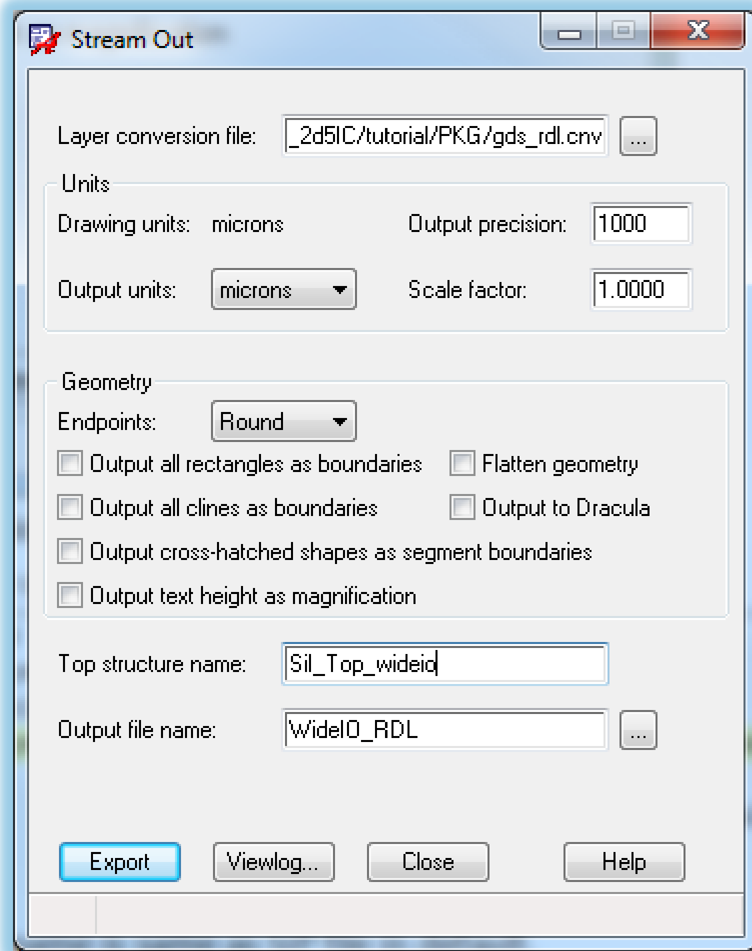
Export GDSII to combine RDL routing data in IC tool




```
# This layer conversion file is used to map
# Stream layers and their data types to SiP
# class/subclasses.
#[stream layer]    [data type]    [class]      [subclass]
1                  -1             pin           SiLap
2                  -1             via_class     Siivia23
3                  -1             conductor     SiLap
```

Layer mapping between package & IC layout tool

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Extend Co-design into a "Single-Canvas View"

- Generate netlist
- Create flat view of
  - PCB
  - Package/Interposer
  - IC
- Optimize interfaces between fabrics

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Chip Scale Review Article on System Interconnect Path Optimization

- New integrated design process concept
- Co-Design bridging of design teams
- Creates a global view and facilitates an early identification of problem areas
- System-wide co-analysis is now possible for SI, PI and timing closure prior to die fabout

Co-design Optimizes System Interconnect Paths from ASIC to Package to Board

By Real Pomerleau [Cisco Systems, Inc.] and Carlos Moll [Cadence Design Systems]

Historically, a semiconductor chip and the package and PCB that house it have all been designed independently. One design is completed and "thrown over the wall" to the next design team. Quite often, the PCB designer is challenged with the task of untangling interconnect that would

electrical and physical domains. When designs are "thrown over the wall," the design is typically done by someone with little knowledge of the overall system constraints. With such a "siloed" design, the IC package designer may be forced to deal with a die design where the pad-ring and bump array (for flip chips) or passivation openings (for wire-bonded chips) are located sub-optimally from a packaging perspective. Package-level signals routed underneath and straight across core— potentially causing signal and integrity problems — and parallel erfaces may have different routing —causing signal skew across the bus. wires may be scattered around the e footprint with little regard to return causing more problems. Differential re also sensitive to skew. lly, these signals should have ed physical and electrical lengths. er interface speeds, there's enough margin to overcome such mismatches, th GHz+ signaling rates, there is ly no margin to correct these tches on the PCB. Signal quality, lk, and timing are all significant -level challenges even with an zed package. Trying to correct the on the board of a poorly designed kage on GHz+ interface speeds is o impossible.

n power-delivery systems at the ckage, and board levels are designed tely by different design teams, there pportunity to optimize the power- ry network (PDN). Lack of, or per use of package decoupling tors can possibly be fixed with nal PCB decoupling for slower- board designs, but today's high- systems require far better, more ted PDN design to avoid severe blems. Separately designed PDNs PCB, package, and die levels can e some unexpected results once they're coupled together. Integrated co-design of all three PDNs is clearly the right approach.

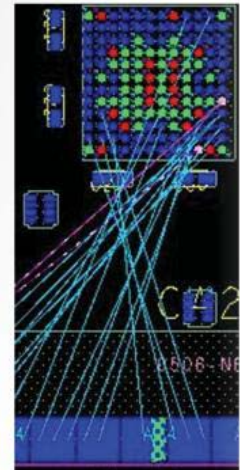

Figure 1. Un-optimized connectivity between a BGA package and a connector on a PCB

Co-Design Reduces Package Costs

Integrated co-design at the die, package, and board levels can also help reduce the IC packaging cost. ASIC packages come in two types: ceramic and organic. Ceramic packages have a large number of layers to distribute die signals, but they cost more and are generally single-sourced. In contrast, cheaper organic substrates are typically limited to fewer signal layers, complicating the efforts to break signals out of the die.

There are also practical limits to the number of PCB layers. Engineering teams often find themselves up against the maximum number of layers for a given board thickness or cost. High ASIC pin counts complicate matters because the

Chip Scale Review, March-April 2011 p 20

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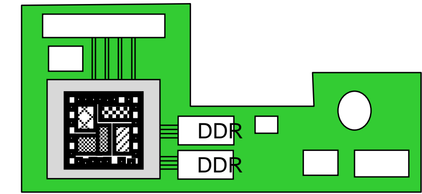
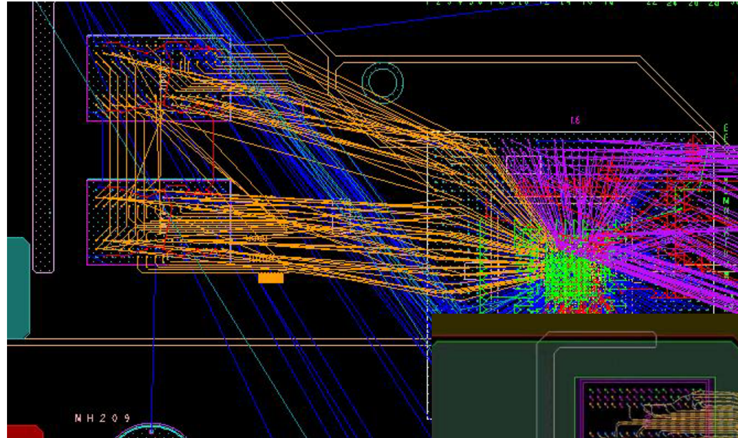
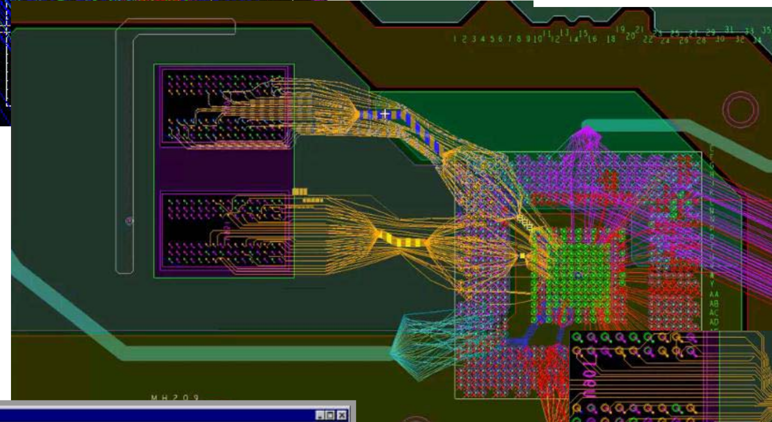
IC-IPSR-PKG-PCB Optimization



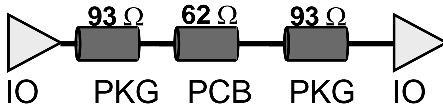


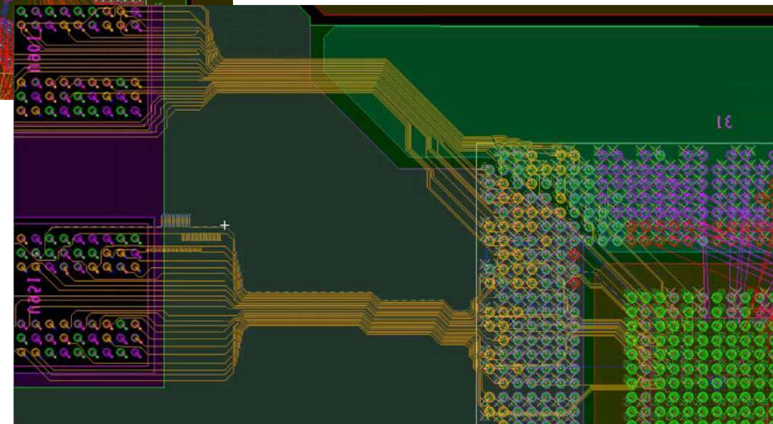
Rats based Pin Assignment Throughout

Define routing path and sequencing



Route Instantiation





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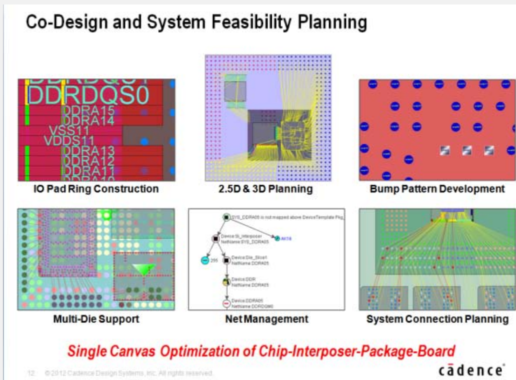
System Planning & Single Canvas: Complementary Solutions



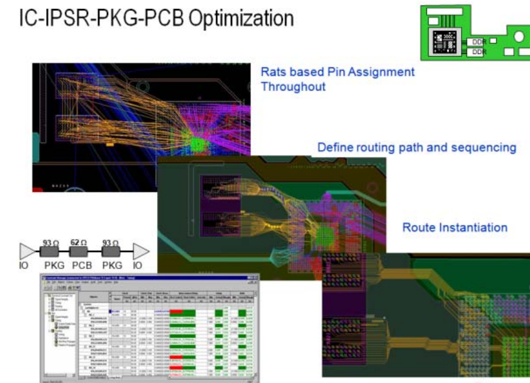
Planner

- Lightweight, rapid prototyping environment for chip, package, board planning

Plan | Prototype | Optimize Interconnect | Implement | Analyze & Refine

Single Canvas

- Detailed co-design with greater awareness of constraints and routability



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Single-Canvas Extraction and Analysis

- Leverage SI analysis tools with common view
- Co-simulation of chip-package-board system view
  - n-fabrics
  - n-layers
  - Board routing, package routing, RDL routing, vias

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Package-Driven Si Interposer Benefits

Problem

- Lack of optimization between the Silicon Interposer and adjacent fabrics adds cost to the overall system and reduces system performance

Solution: Interposer planning

- A comprehensive system view and pin assignment optimization function will reduce the number of signal crossovers in the overall system
- System route feasibility and system SI and PI analysis validates that the Interposer will meet design specifications

Result

- A system optimized Silicon Interposer plan that can be handed off to IC implementation tools for final manufacturing prep

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