Considerations in High-Speed High Performance Die-Package-Board Co-Design

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October 2014
Why Co-Design?

- Complex Multi-Layer BGA Package
  - Horizontal and vertical design optimization

- PCB Adds ~ 5 dB Degradation
  - Package-PCB transition design

- Die Parasitic Adds ~ 5 dB More Degradation
  - Die parasitic compensation

- Power Distribution Needs Co-Design
Outline

- Transceiver Channel
  - Channel loss
  - Reflection
  - Channel cross talk
  - Material dispersion

- Transceiver Power Distribution Network (PDN)
  - Power supply induced jitter (PSIJ)
  - Channel IR drop
  - Electromigration (EM)

- System Jitter Break Down and Improvement
Die-Package-PCB Co-Design Flow

- Silicon loading
- Protocol
- Electrical spec
- PKG stack up
- Substrate material
- PKG RX/TX impedance
- Electrical spec
- Electrical design rules
- Physical design rules
- Correlation
- Methodology
- Physical design
- Simulation
- Co-design
- meet spec?

Finish

YES

NO
Managing Transceiver Channel Loss

- **Loss Sources**
  - Material loss
  - Material surface roughness
  - Conductor surface roughness
  - Channel length

- **Loss Control**
  - Using low loss material
  - Material with good surface roughness
  - Advanced chemical treatment of conductor surface
  - Control of trace length and use of thick wide traces
Managing Transceiver Channel Reflection

In Package (Multi-Layer BGA Package)

- Reducing geometry/impedance discontinuity
  - Smaller BGA ball pitch, via pad, PTH/ball pad
  - Bump/PTH/BGA ball pattern optimization
  - Coreless package

- Design of proper target impedance

- Control of layer to layer coupling

- Optimization of vertical transition (US patent 8502386)
Managing Transceiver Channel Reflection

- **At Die-Package Interface**
  - Silicon pin capacitance causes the major discontinuities
  - Use of on-die inductor to compensate Silicon pin capacitance (US patent 8368174)

- **At Package-PCB Interface**
  - Control of BGA pad capacitance (US patent 8841561)
  - Control of PCB cap pad capacitance
BGA and PTH are the biggest contributors to package discontinuities.
Die-Package Interface

On-die compensation inductor

- **How much compensation inductance needed?**
  \[ Zo = \sqrt{\frac{L_{\text{comp}}}{C_{\text{die}}}} \]

- **How to realize the compensation inductance?**
On-Die Compensation Inductor

- on-die inductor
- bump pad
- bump
- package

Die

Inductor

Package

(not to scale)

US Patent 8368174
Optimized Differential Return Loss

Magnitude, dB

freq, GHz

CEI SPEC

TX_SDD

No compensation

Ideal inductor

On-die inductor

Magnitude, dB

freq, GHz

CEI SPEC

RX_SDD
Optimized Differential Insertion Loss

Magnitude, dB

TX_IL

freq, GHz

Magnitude, dB

RX_IL

freq, GHz

No compensation

Ideal inductor

On-die inductor
Optimized Common Return Loss

- Magnitude, dB
- Optimized Common Return Loss
- CEI SPEC
- TX_SCC
- RX_SCC
- No compensation
- Ideal inductor
- On-die inductor
Package-PCB Co-Design

- Integrating Package and PCB
  - Very time consuming

- Separating/Cascading Package and PCB
  - How to accurately model the interface?
  - How accurate comparing to the unified model?
Package + PCB + Connector
Package-PCB Co-Modeling

- Package
- PCB
- BGA
- ground
- truncation plane
- Package simulation
- PCB simulation
- de-emb
Package-PCB Co-Modeling Verification

SDD11, dB
seen from bump side

SDD22, dB
seen from connector side

SDD21, dB
unified package/PCB
cascaded package + PCB

Zc_diff, Ohm

TDR
Transceiver Channel Cross-Talk

- Cross-Talk Between Transceiver Channels
  - Properly coupled differential pair
  - Proper separation /shielding of channels
  - Use of smart bump and BGA pattern

- Cross-Talk From Lower Speed Memory Interface to Transceiver Channels
  - Hard ground to shield transceiver IO from lower speed IO
PKG + PCB Cross Talk Induced Jitter

- PCB via cross talk is more dominant than PKG cross talk when via length is large
Transmit jitter increases when the number of lower speed IOs and PCB via depth increase.

Hard ground effectively reduced coupling from lower speed IO to TX.

Ball #1 hard ground, toggle 2-6 with deep PCB via.
Material Dispersion

- Material Dielectric Constant Varies with Frequency
  - Group delay
  - ISI (Inter Symbol Interference) jitter
Managing Transceiver Power Design

- **Power Supply Induced Jitter (PSIJ)**
  - Reduce on-chip supply noise
    - Improve PDN impedance
      - Use on-chip capacitors to improve high frequency PDN impedance
      - Use PCB capacitors to improve low frequency PDN impedance
    - Use power supply regulator on critical power rails
  - Reduce jitter sensitivity to power supply noise
    - Only dependent upon circuit implementation
Managing Transceiver Power Design

- **Channel IR Drop**
  - Power consumption
  - Co-design to balance IR drop budget for die package and board

- **Electromigration (Max Current on BGA Balls)**
  - Manufacturing reliability
An Example of IR Drop and EM Simulation in A Package
Transceiver Channel Jitter Sources

- **Inter-symbol interference jitter (ISI jitter)**
  - Transceiver channel discontinuities
  - Material dispersion and loss

- **Cross talk induced jitter (XTIJ)**
  - Package horizontal trace coupling
  - Package vertical transition (PTH, BGA)
  - PCB via, socket, connectors

- **Power supply induced jitter (PSIJ)**
  - Supply noise
  - Jitter sensitivity
- Discontinuities dominant in short traces
- Material dispersion dominant in long traces
Summary of Transceiver Channel Jitter Improvement

- **Inter-Symbol Interference Jitter (ISI jitter)**
  - In short trace design, focus on reducing package discontinuities
    - Fine ball pitch
    - Coreless
  - In long trace design, consider low dispersion and low loss material
  - Constrain trace length for very high data rate
  - Control silicon pin capacitance
  - Optimize package/PCB transition

- **Cross-Talk Induced Jitter (XTIJ)**
  - Physically separate transceiver channels
  - Design more confined and shielded PTH
  - Design more electrically isolated BGA ball (coax ball) and PCB via
  - Avoid use of socket

- **Power Supply Induced Jitter (PSIJ)**
  - Identify contribution of supply rails to system jitter
  - Reduce supply noise and jitter sensitivity to noise through co-design
Thank You