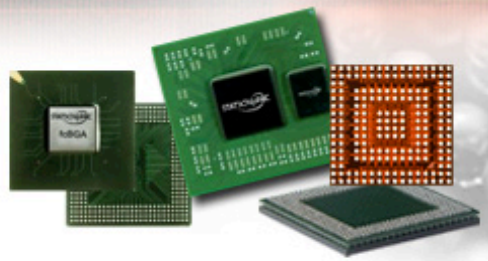
Critical Technologies for Thin Wafer Handling in 2.5D & 3D Integration



Steve Anderson
STATS ChipPAC

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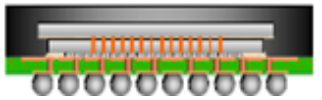
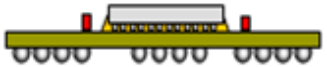
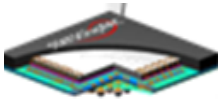
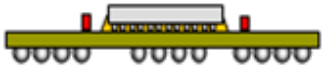
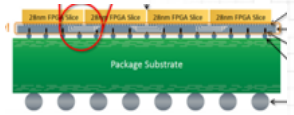
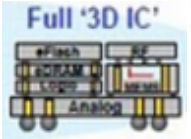
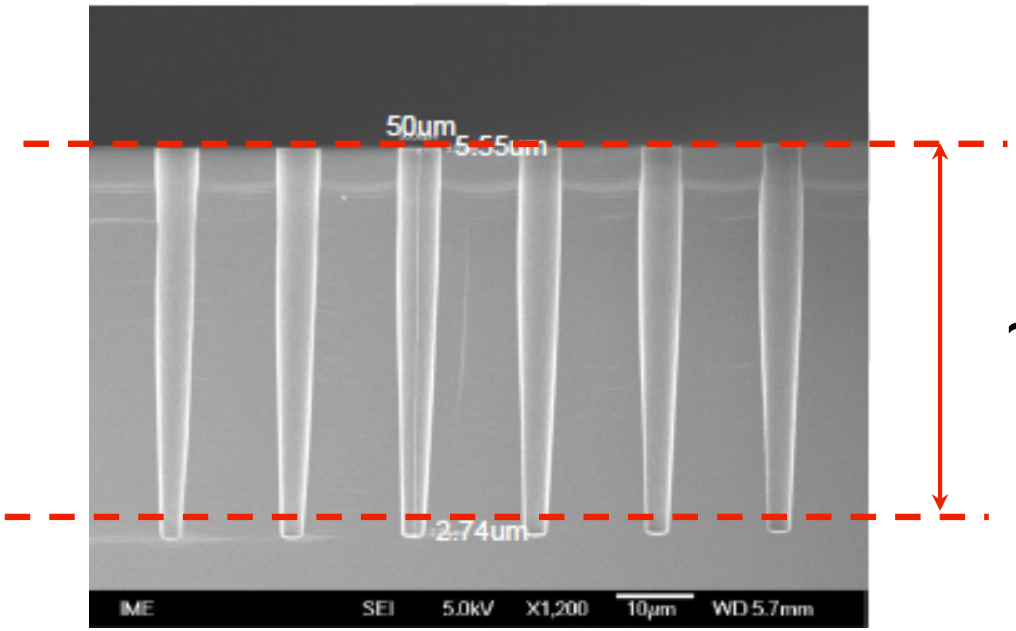
- Markets for 3D/2.5D Die Stacking using TSV
- Integrated Process Flows for 2.5D/3D
- Thin wafer handling challenges and Solutions
  - Edge Trimming
  - **Temporary Bonding/Debonding**
    - Technology Comparison
    - Progresses in Temp bond/debond
  - Dicing a thin wafer
- Chip attachment
- Summary

3D/2.5D Driver - Target markets

	Market	Device Types	Current Configuration	Future Configuration with TSV	Approximate Intro. Timing
3D	**Memory**	DRAM	 **DIMM**		2011~2012
3D	**Mobile Application Processor**	Application Processor AP (+ BB)			2013~2014
2.5D	**Logic with memory using TSV interposer**	GPU, Gaming Console			2013~2014
2.5D	**Logic + Analog using TSV interposer**	Network, Telecommunication			2012~2013
2.5D	**Partition of IP blocks with TSV interposer**	FPGA			2012~2013
3D	**High Performance Computing**	CPU, MCM, etc			2016~

Why do we need a thin wafer for 3D/2.5D?

- TSV depth is limited by TSV diameter and aspect ratio in the process and design
- Wafers need to be thinned to expose a tip of the TSV from the back side



~50um after back-grind and via reveal

5um dia via and 50um depth, AR~10

Who will handle thin wafers?

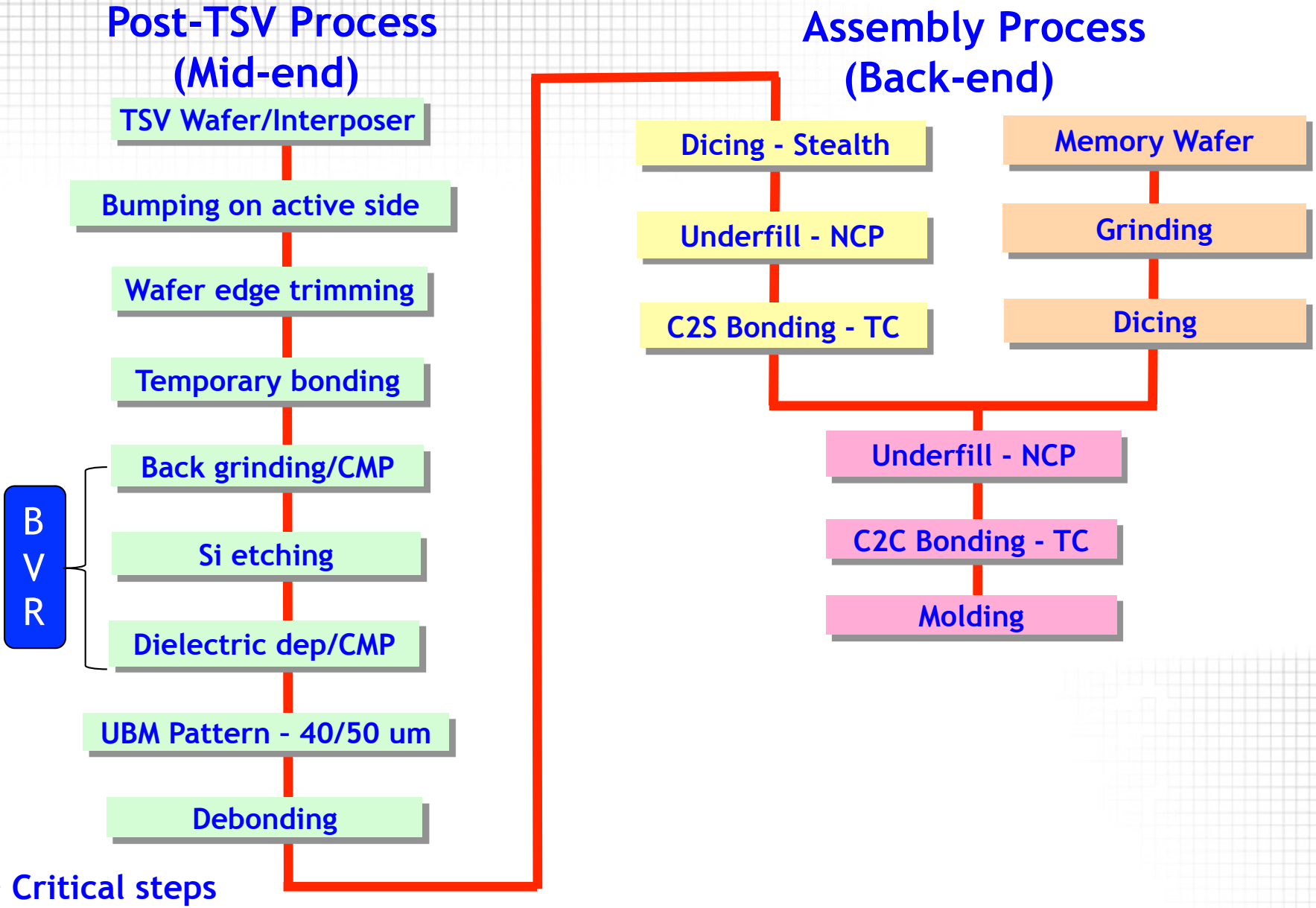
Business Models and Foundry/OSAT Collaboration- Material flow and infrastructure evolution:

	Device	TSV Fab	Post-TSV process	TSV Assembly	Typical Application
Via-First Via-Middle	Fab	Fab	✓ Fab/OSAT -Via exposure & capping; wfr thinning - RDL, uBump	✓OSAT - CtC/CtW/CtS bond - fine gap ufill	• AP + Memory
TSV Inter-poser	Fab	✓FAB/OSAT - Passive Si via fabrication	✓FAB/OSAT -Via exposure & capping; wfr thinning - RDL, uBump	✓OSAT - CtC/CtW/CtS bond - fine gap ufill	• Si partitioning (e.g. FPGA, GPU + Mem) •Logic + Analog

OSAT's Positions:

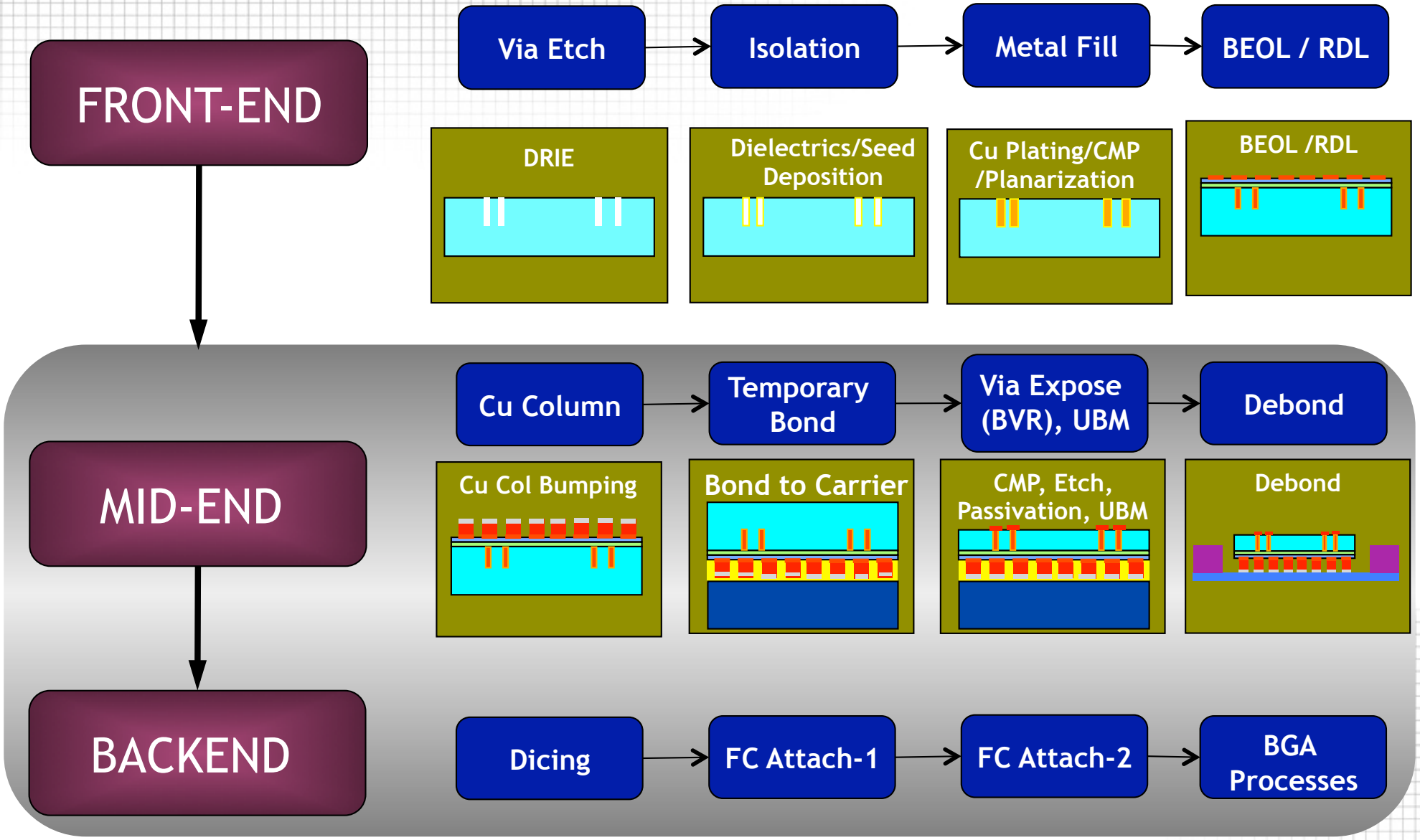
- Mid-end process and Back-end assembly for Via-Middle Application Processor in Mobile Market
- Mid-end process for TSV interposer and Back-end assembly for GPU/MPU and network processor market
- TSV fabrication of TSV interposer for Heterogeneous Integration of less demanding 2.5D market

TSV Assembly Process Flow – Example 1



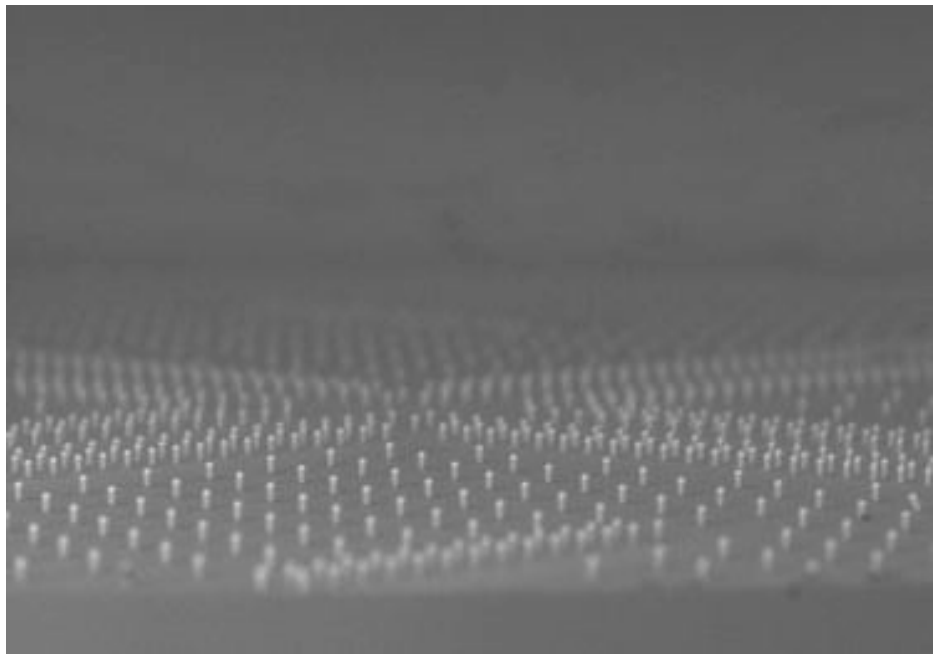
- Critical steps
  - Bumping, Wafer thinning & handling, Planarization & via Exposure
  - Micro-bump Flip Chip Assembly (FCA)

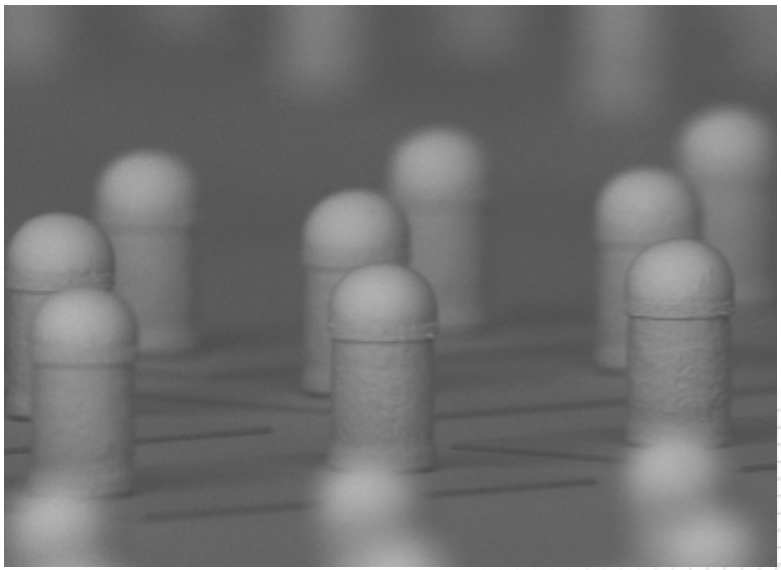
Front, Mid and Backend Processes



Micro-bumps

- Bumped and thin wafer handling
- Bumping at the active (FRONT) side of a wafer
  - Lead-free solder (SnAg)
  - Cu column (Cu/SnAg) for micro-bumps

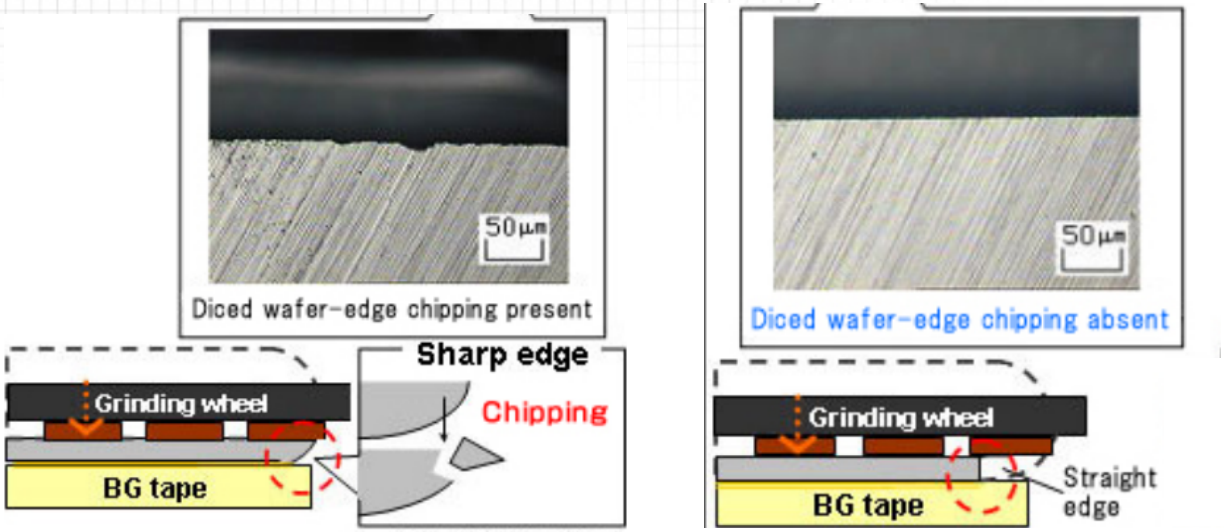




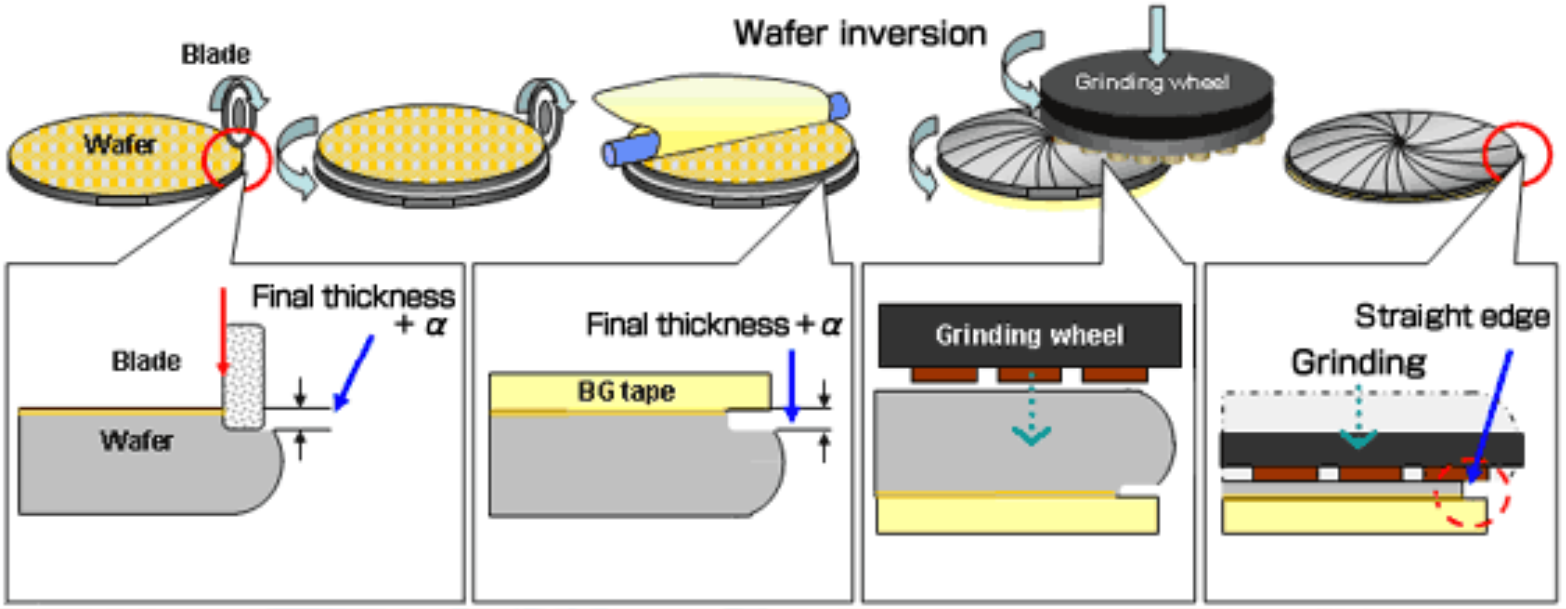
Cu column (Cu/SnAg)

Edge Trim

- Reduce edge chipping and wafer cracking during or after back-grinding



Source: Disco



Temporary Bonding and Debonding

Method	Thermal cure + Thermal release	Thermal cure + Room temperature release	UV cure + Laser Release
Carrier	Glass or Silicon	Glass or Silicon	Glass
Bonding method	1. Coat adhesive on carrier 2. Bond device wafer to carrier	1. Coat pre-cursor + release layer on device wafer 2. Coat elastomer on carrier 3. Bond device wafer to carrier	1. Coat a polymer on carrier 2. Coat adhesive on device wafer 3. Bond carrier to device wafer
Curing	< 200degC	< 200degC	UV cure
Debonding method	1. Apply heat and slide off carrier from device wafer 2. Use solvent to dissolve adhesive from device wafer	1. Mechanically tilt carrier and remove from device wafer 2. Clean and rinse device wafer.	1. Apply laser to remove LTHC layer 2. Remove glass 3. Peel off adhesive from device wafer
Debonding temperature	<200degC	Room temp	Room temp

Adhesive Requirement for Temporary Bond/Debond

- High Temperature resistance
- Chemical resistance
- High mechanical strength during process between temporary bonding and debonding
- Protect bumps
- Void free and Residue free
- Low out-gassing and easy to clean
- Capability for low TTV and ultra thin wafer processes
- Low stress removal of a carrier
- Compatible with the integrated process flow of mid-end and back-end
- Low Cost, high throughput and high yield

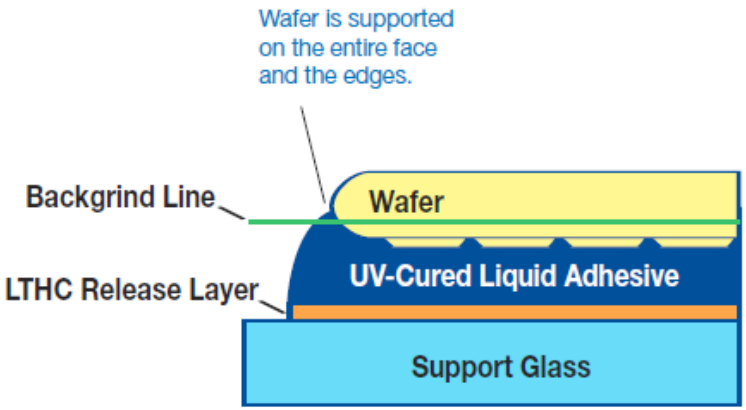
Thickness and TTV Control

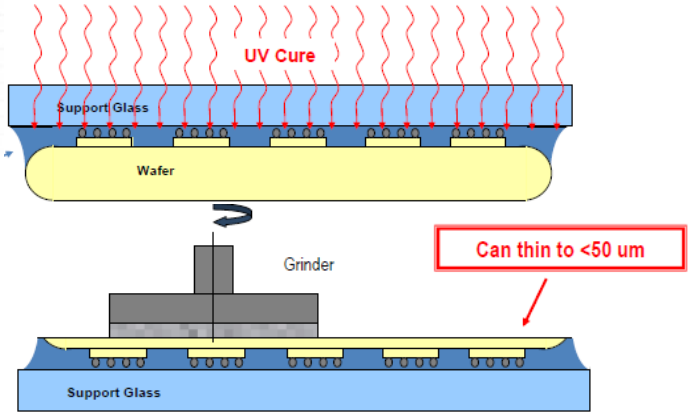
- Carrier thickness and its TTV
- Adhesive thickness and its TTV
- Total stack thickness and TTV

- Voids in the Adhesive
- Bonded wafer bow and warpage

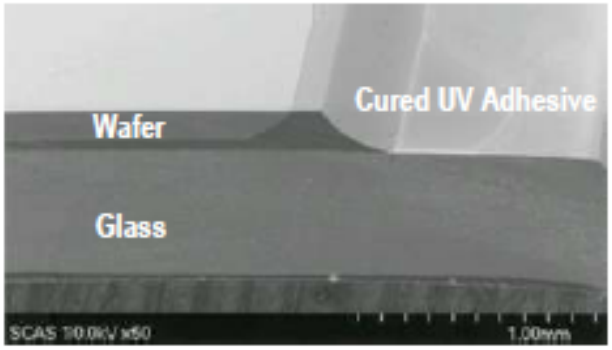
- In-line Metrology for Temporary Bond/Debond Process

Various Temporary Bond/Debond Options – UV Release

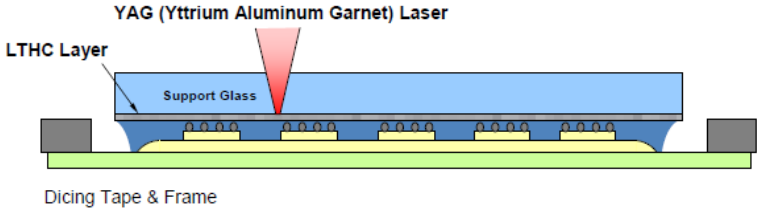


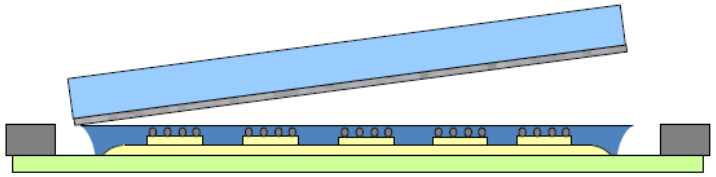


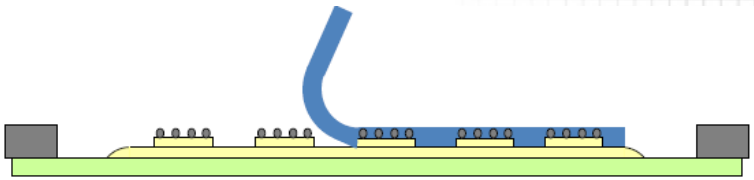
Before and after back-grinding



Source:3M



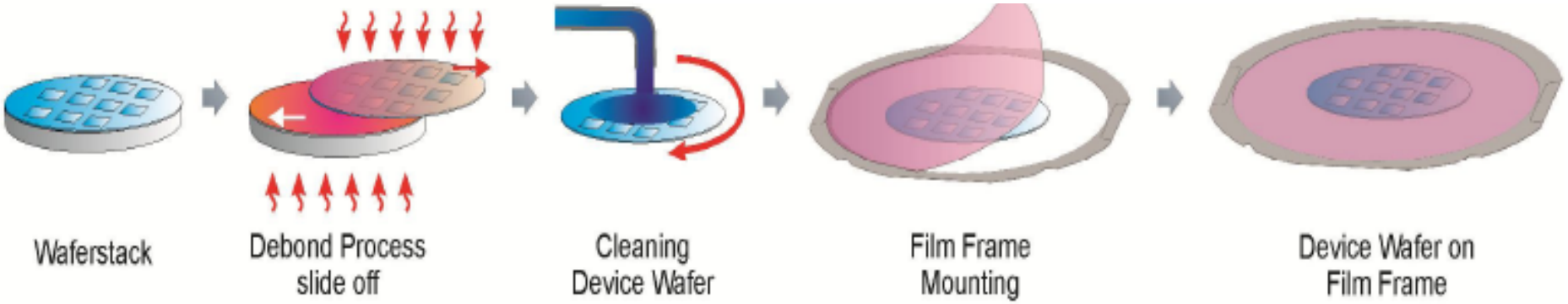




Various Temporary Bond/Debond Options – Thermal Release

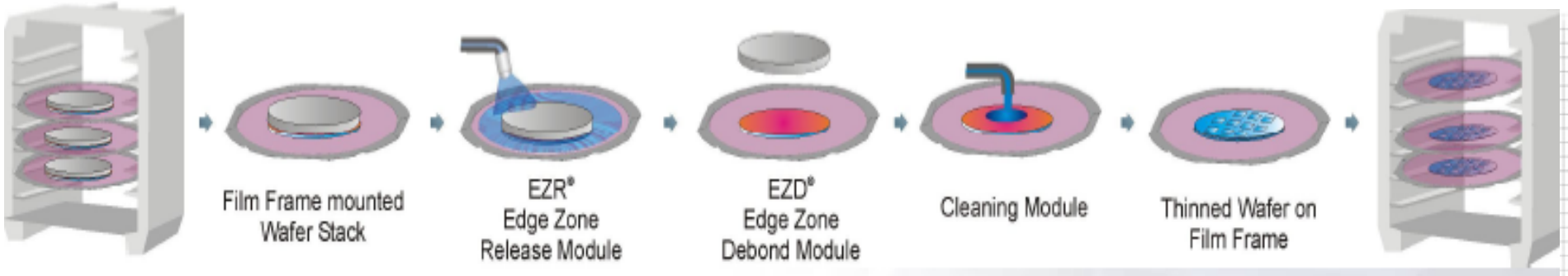
Thermal Slide-off Release

Source: EVG



ZoneBOND™ Release

Source: EVG



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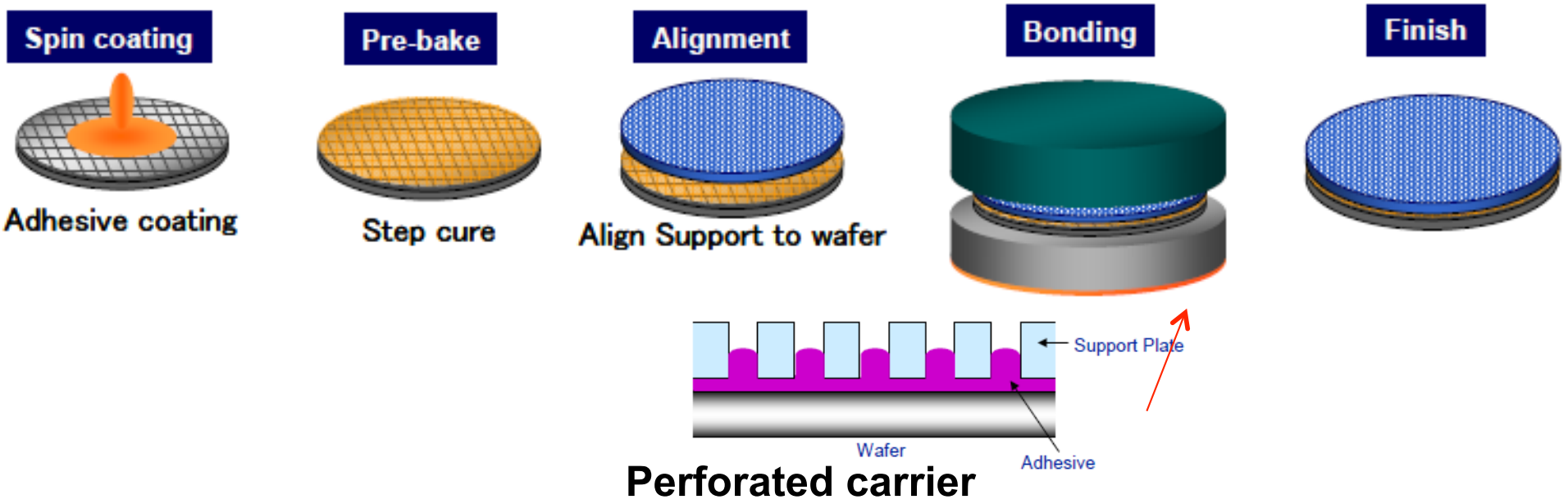
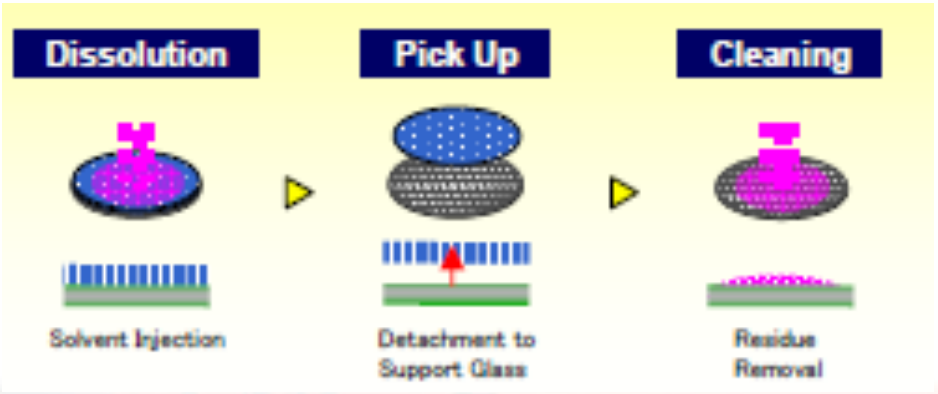
Various Temporary Bond/Debond Options – Solvent Release



Wet debonding with solvent followed by cleaning

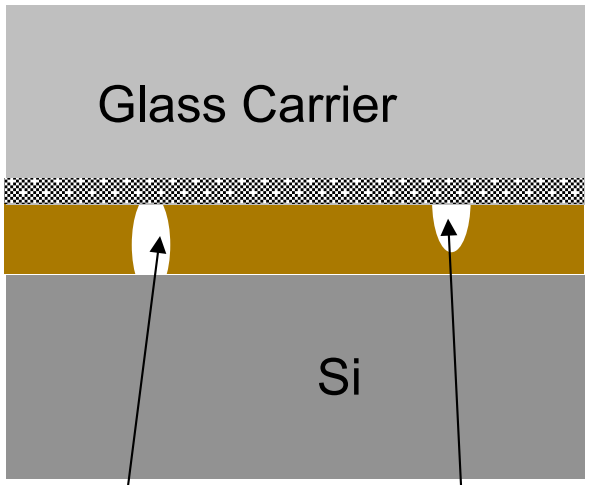


Source: TOK

Typical Defects after Temporary De bonding

- Remove the defects using optimized processes and materials

After Bonding



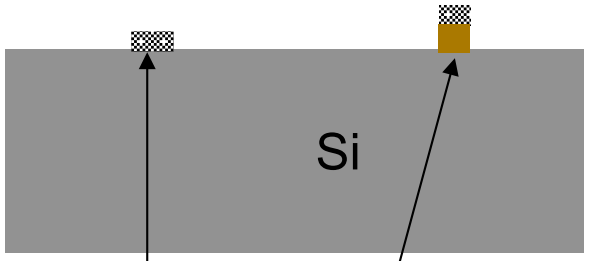
(1) bubble extended between wafer and glass

(2) bubble at adhesive top surface

After Laser Debond & Glass Removal

Detached particles on adhesive and on wafer.

After Adhesive Peeling

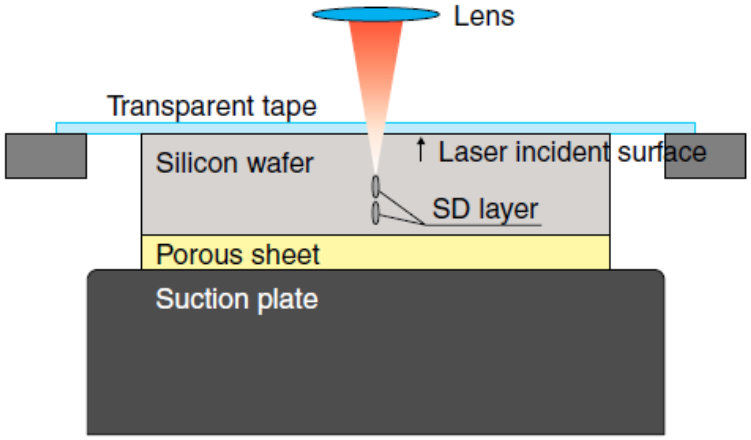


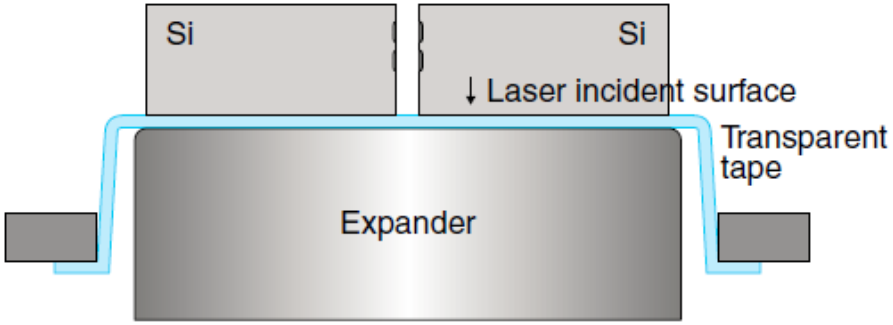
Residue

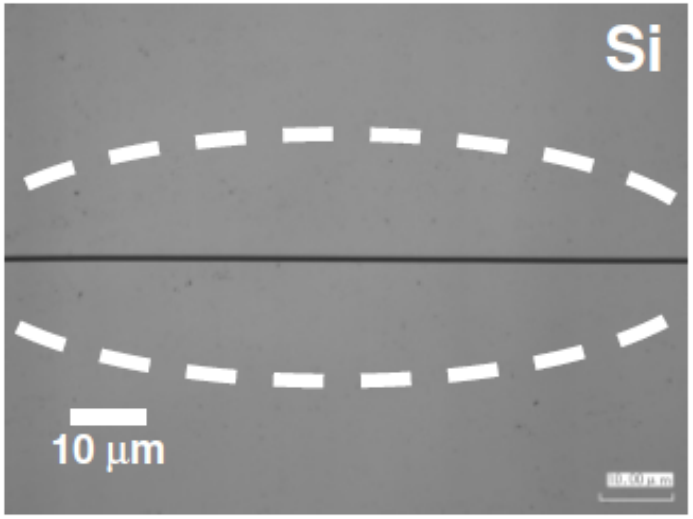
Broken Piece of Adhesive Residue and on top

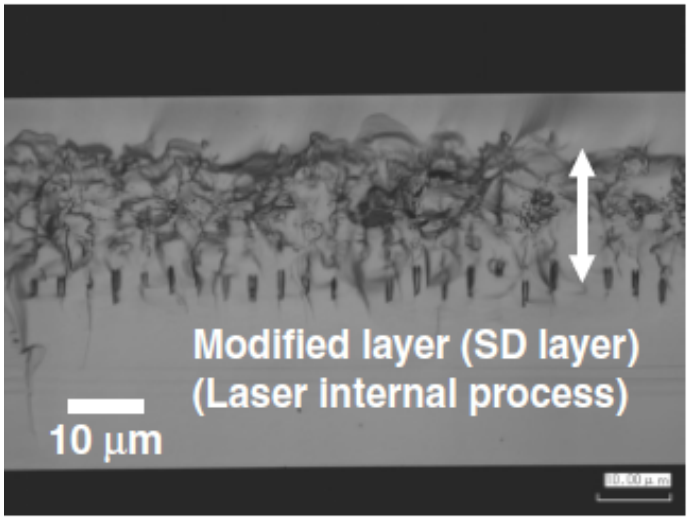
Stealth Dicing

- Internally focused laser process and internally damaged zone
- No water cooling and no heat affected zone
- Great chip yield and high throughput for ultra-thin wafers





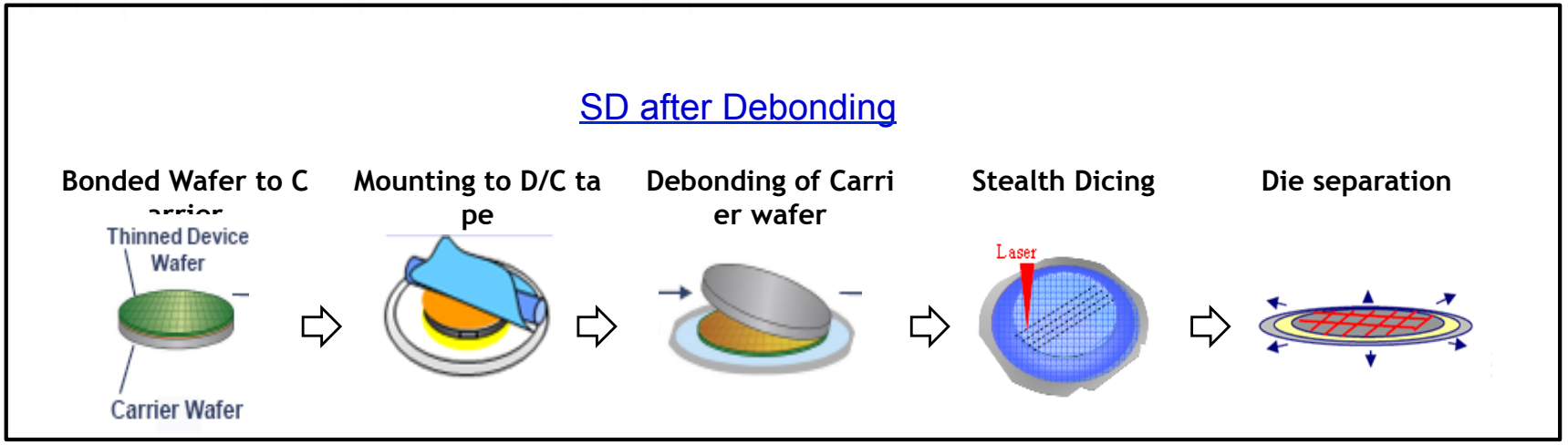


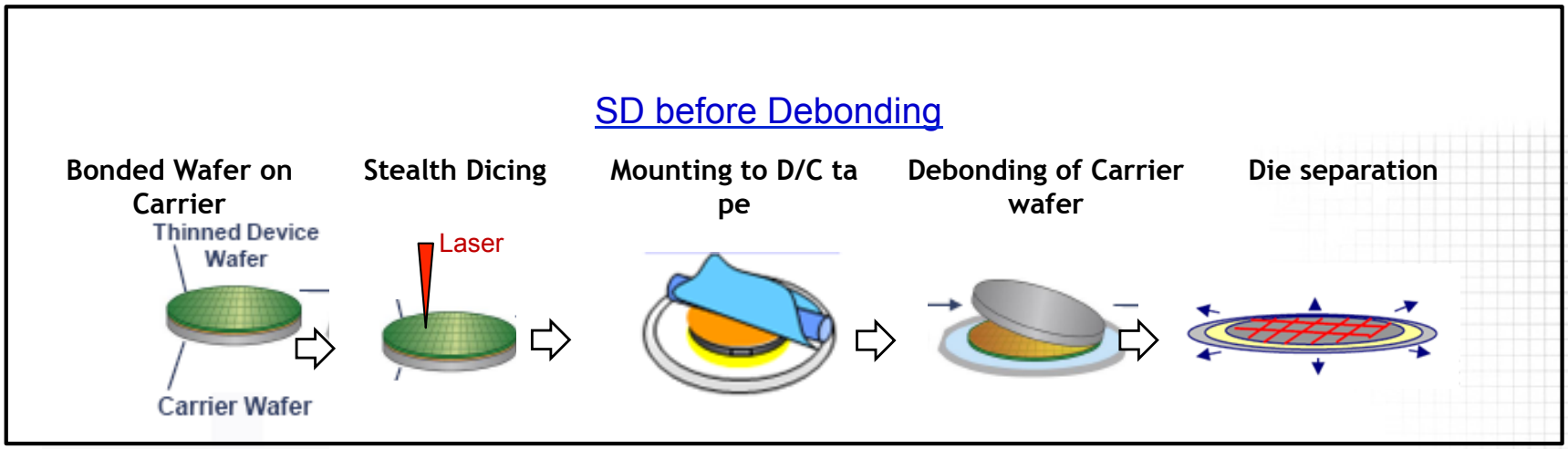


Courtesy of Hamamatsu)

Stealth Dicing

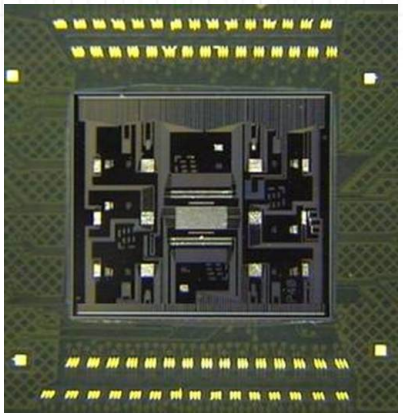
- Option 1 : Stealth Dicing after Debonding : Laser through dicing tape
- Option 2 : Stealth Dicing before Debonding : Laser directly to wafer backside

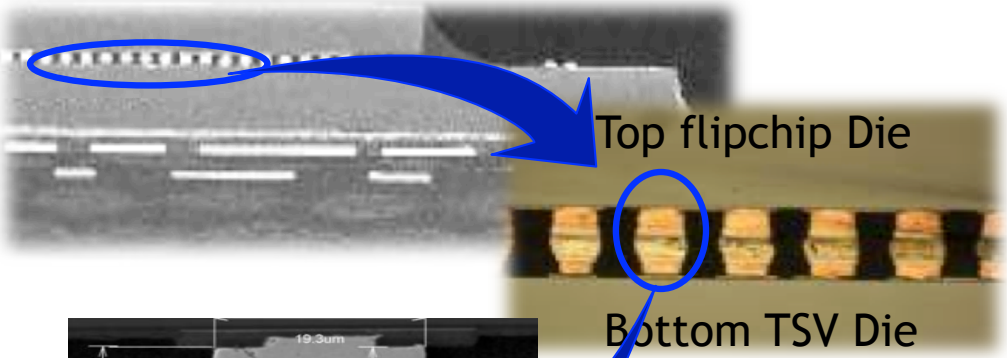


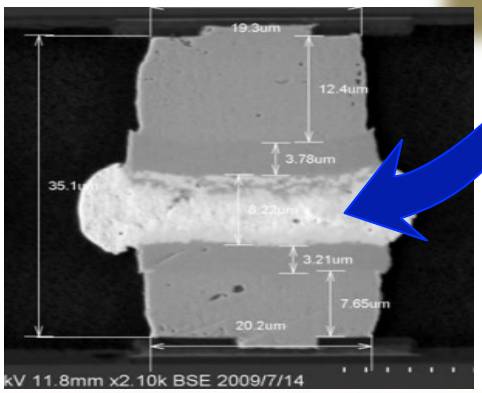


Thin Die Flip Chip Attachment

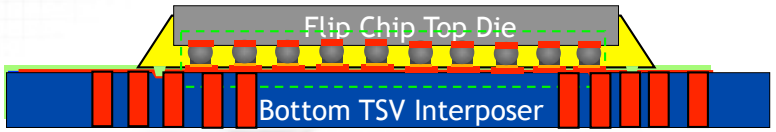
Chip-to-Chip/Substrate (CtC,CtS)

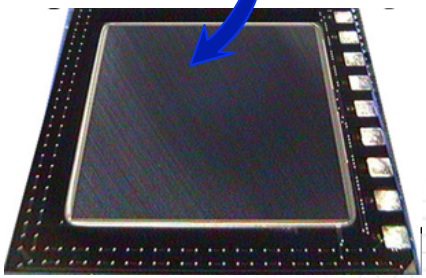


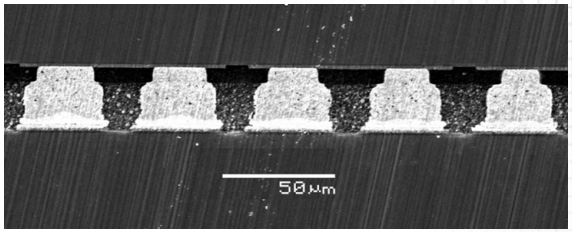




Chip-to-Wafer (CtW)



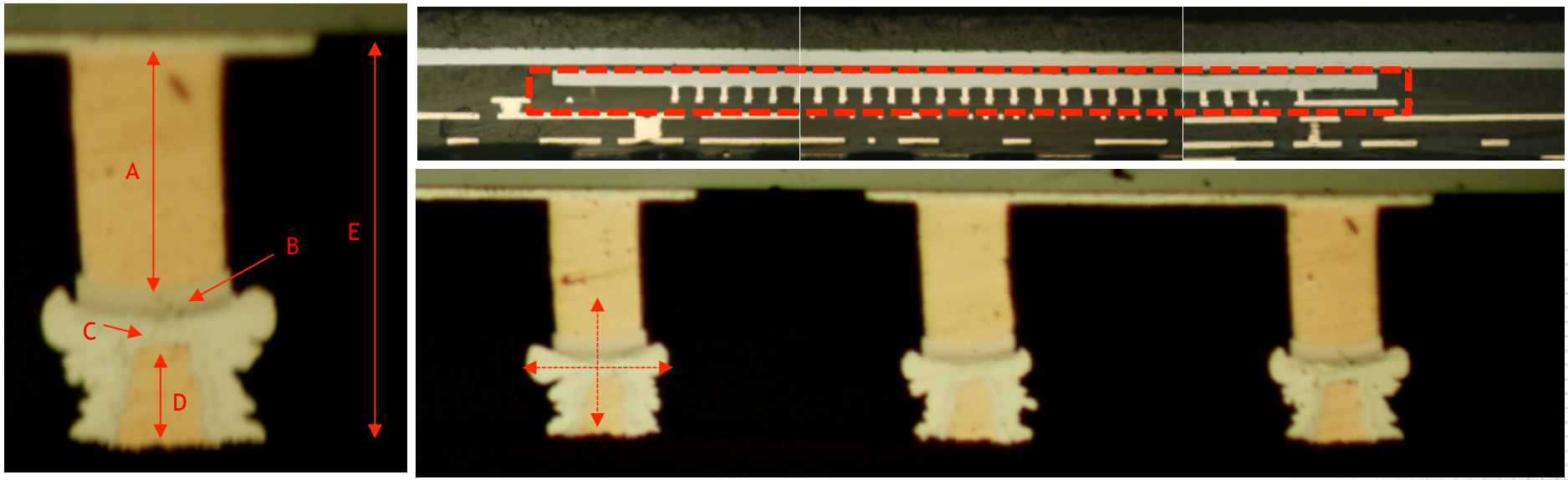




Thermal Compression Bonding - thin die to Substrate

- Alignment Control of a thin die
- Minimize warpage
- Stand-off height: Minimize variation

✓ **Tier-1 Die to sub X-section & stand-off image**



(Unit: um)

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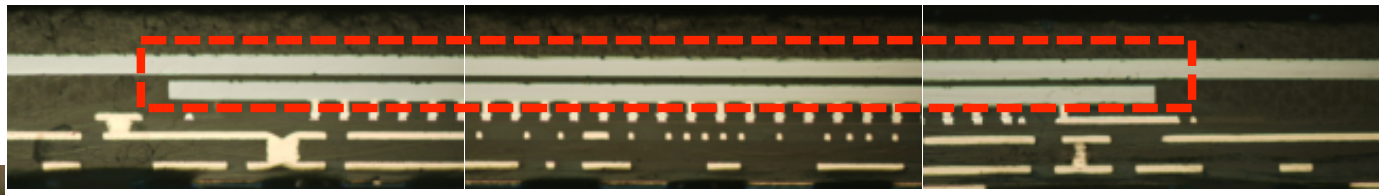
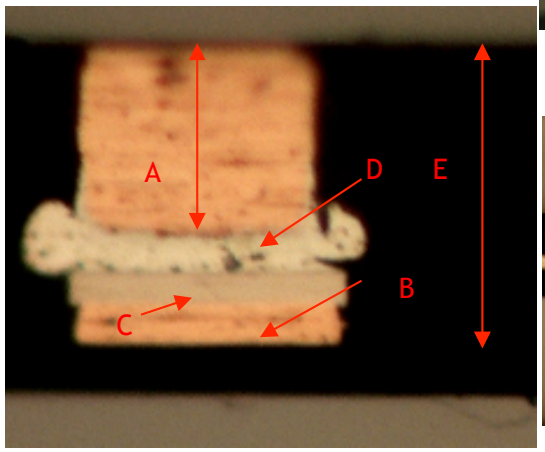
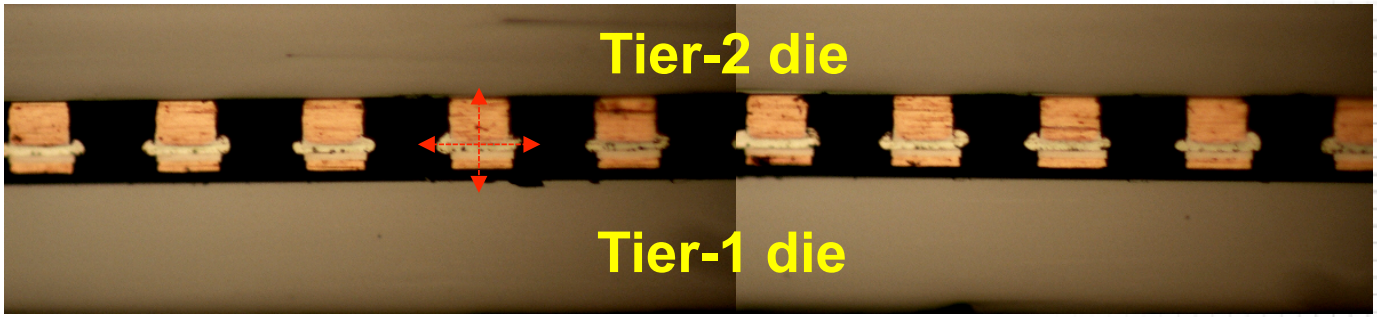
Thermal Compression Bonding - Thin die to die

- Alignment Control of a thin die
- Minimize warpage
- Stand-off height: Minimize variation

✓ **Tier-2 Die to Tier-1 Die X-section & stand-off image**







(Unit: um)

SUMMARY

- 3D/2.5D with TSV markets are emerging in mobile and high performance device areas.
- OSATs can play a major role in mid-end and back-end processes with experiences in wafer bumping, thin wafer handling and back-end processes.
- All vehicles with TSV need thin, bumped wafer handling.
- New technologies have been developed to prevent wafer cracking and edge chipping
- Temporary bond/debond tools have been developed. There are a few options. It has to be optimized in the integrated process flow of mid-end and back-end processes
- A great deal of progresses have been made in equipments, materials, design and process optimization.