3D & 2½D Test Challenges
Getting to Known Good Die
&
Known Good Stack

Known Good Die 2102
San Jose, CA

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Any Multi-die Product Must Consider the Accumulated Yield

Assume Test Can Provide 99% Die Coverage.....

Even assuming a perfect interposer – 5 die stack could have 4-5% final yield loss
Conventional Test Holds Many Challenges

Conventional Flow

- Wafer Process
- Wafer Test
- Back Grinder
- Dicing
- Packaging
- Final Test

TSV uPillar Wafer Test Challenges

- TSV Check
- High Pin Count
- Fine Pitch
- Low Contact Pressure
- Drive-ability 0.4pF
- ESD
- Die Level Completeness

Added Test Yield Concerns
Test Challenges
The Via Itself: Interposer

Example:
If TSV PPM = 0.1
If 1 Die = 50,000 TSV
Die Yield = 99.5%

Limitation:
- Lowest cost device (can’t afford to test); no access until after thin.

Countermeasures:
- Very good yields; parametric samples, visual & Xray inspections.

Issues:
- PPM can have big effect. And … Active interposers are coming.

Source: Optimized TSV Filling Process Reduces Cost, Nexx Systems
Do We Access on the TSVs uPillars or Test Pads?

Limitation:
- Probe Cards have architectural limitations for contacting uPillar

Countermeasures:
- Use Test Pads and IEEE Standards (1149.7/1149.1/1500/P1687)
- Use Non-Contact Probing

Issues:
- Will Test Pads + Structural Test give enough coverage?
- Non-Contact Probing requires transmitters/receivers, power delivery still requires physical contact.

= Added Test Yield Concerns
Thin Wafers

- **Limitation:**
  - Advanced Probe Card lowest contact forces ~ 2g per contact
  - Thin Die may require <1g

- **Countermeasures:**
  - Probe before backside processes (BG, CMP, Etch)
  - Use Non-contact probing? Film Frame? Backside Probe on Carrier?

- **Issues:**
  - Backside processes *induce defects* that go untested.
  - Many Questions with debonding Alternatives & substrates

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**Added Test Yield Concerns**
Lack of Buffers at 0.4pF I/O

**Limitation:**
- Lack of buffers in device creates drivability problem to ATE.

**Countermeasures:**
- Active probe cards with supplemented buffer amp circuitry.
- Dedicated Test Pads with weak drivers

**Issues:**
- Probe cards require high density circuitry, unproven architecture.
- Design and Power requirements for drivers (6mm distance)

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Added Test Yield Concerns
**Limitation:**
- TSVs create paths to internal nodes of IC not previously exposed.
  - Circuit loading may be issue with ESD structures.

**Countermeasures:**
- Limit ESD < machine model
- Weak, small size ESD flip-flop circuits on IC (B-scan circuits)
- Other: Extreme care in handling & flow equipment

**Issues:**
- No redundant signaling TSVs, “very small leakage” test

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**Source:** ESD Protection of Through Silicon Via Signals Utilizing Temporary Backside Metallization, IBM
Repartitioning: EDA and I.P.

Limitation:
- If logic is partitioned on different layers, single die may not be fully testable. If Homogeneous memory – treated as multi-bank die.

Countermeasures:
- Design recommendations; GSA and IEEE Standards
- Comment: IDMs can go this route, but will fabless design model support with software & design complexities? EDA/IP issues.

- 3D clock tree for optimized length and power (example)
- Utilization of different process nodes/different suppliers with truly heterogeneous die.

Source: Test Strategies for 3D Die-Stacked Integrated Circuits
Lewis & Lee, Georgia Institute of Technology

+ TSV Check + High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness
There are possible solutions to allow continued use of conventional wafer test architecture. They mostly require:

- Silicon Solutions (Test Access Ports, Direct Access & DFT)
- Direct Docking & improved coverage at wafer sort
- New Probe/Contact Solutions

These may come at a Test Yield penalty. “Probably Good Die” could become “Maybe Good Die” and \textbf{unacceptable yield loss at stack}, especially with expensive components added later to the stack.

- There is limited thermal coverage and no die interaction coverage
Manufacturing Process Example

Process for Device with TSV

Wafer Process → Wafer Test → Back Grinder → Dicing → Stack → Packaging → Final Test

- Deep VIA
- Surface PAD
- Thin Wafer
- Backside Bump

Each Interim Product must be “Known Good” Product

Must consider many options for Suppliers vs OSAT vs IDM

ASET® = Association of Super-Advanced Electronics Technologies / Advantest is member of ASET
Partial Assembly: OSAT
Downstream integration

Limitation  - Limited test access from outside; landscape height variations

Countermeasures  - IEEE & Jede test ports; new test insertion points in the flow

Issues  - Multiple suppliers; yield loss = scrap $$ assy
KGD will be essential to making 2.5D and 3D stacking cost effective

Some Considerations......

- Wafer vs. Singulated Die Test
- Zero Force Contacting
- Carrier Technologies
- Combined Electrical & Non-Electrical Test
- TSV Top/Bottom Contacting
- ATE close to the DUT (drive)
- Flexibility for Multi-pass
- Thermal Management

⇒ A Non-conventional test methodology that enables KGD

Yield of single-chip
Commodity Success Challenge

• MUST achieve cost targets even though there is value added with reliability and KGD.

• Supply chain management gets complicated.
  - Who is responsible for 3D/2.5D/TSV quality/yield?
  - KGD guaranteed? How?

• Also manufacturing process depends on business model.
3D Innovation Into Commodity: Cost, Profit, Risk
Contact solutions in development

Contact features
- < 1gram force
- 2500 probes
- <50um pitch capable
• Separated control for Insertion force and die force
  - Enables different height control
  - Die force control enable to avoid edge crack

* Die and Memory
  • Height A > B
    - Control die force for Die
    - Control balancing force at contact press
Active Thermal in Real Time

- This is scalable: DRAM, DFT Asics, even Power CPUs

Excursion of Tjc

Stepping the device’s power consumption at 30W steps
Technology for Test/Handling

Process for Device with TSV

- **Wafer Process**
- **Singulated Die**
- **Partial Assembly**
- **Packaging**
- **Final Test**

**Vision Alignment**
- Camera + Contact
- LED Lights
- Device

**Die Level Testing solution**
- High Performance to Burn In

**93K SoC Test System**

**Burn-In Test System**

**T5xxx Memory Test System**

**T2000 SoC Test System**

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**MEPTEC KGD 2012**
Summary for 2.5D & 3D Test

• New test points – IEEE and IMEC Erik Jan and team
  – Many new test points- but they will be selectively implemented
  – Each flow will use different points; **No** flow will use all points

• Optimized flows and test economy

• Key is tooling flexibility & integration

• Yield, Yield, YIELD
Thank You
Coming 2.5D and 3D products pose new challenges to the production test environment. Providing a commodity viable 3D product demands implementation of unique test and handling solutions. Yield is the foremost concern but cost sensitivity and test economics are critical to any successful commodity. Manufacturing (back end) flows and new insertion points will be described. The presentation will also outline challenges of 2.5D and 3D implementation, highlight limitations with today’s monolithic solutions, and offer alternatives for a high yield, integrated Die Level Handling environment.