The Future of Packaging ~ Advanced System Integration

RELIABILITY & TRUST

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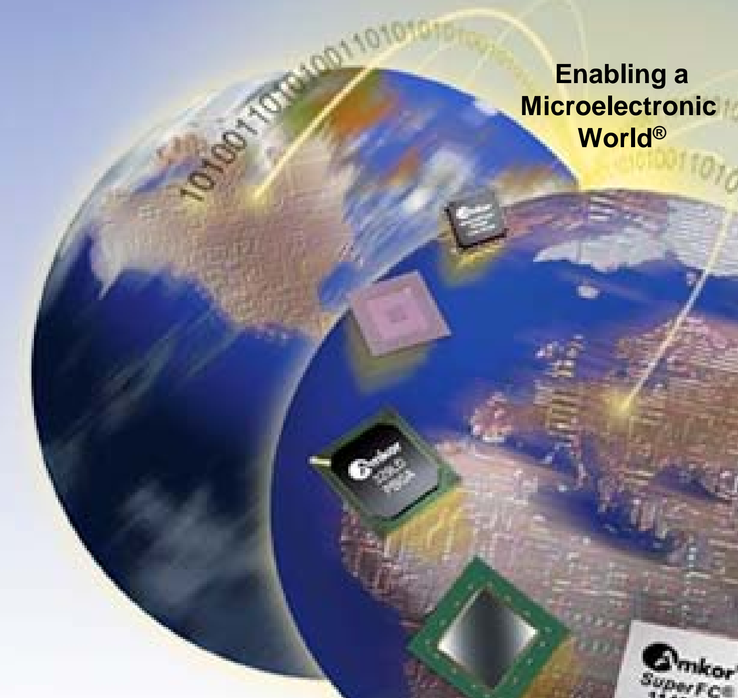

Product Segments

End Market % Share Summary

Communications 46%	Consumer 22%	Computing 12%	Networking 11%	Automotive & Industrial 9%
Smartphone	Gaming	PC / Laptop	Server	Infotainment
Tablet	Television	Hard Disc Drive	Router	Safety
Wireless LAN	Set Top Box	Peripherals	Switch	Sensors

Note: Percentages represent share of LTM 3Q12 Net Sales

New Product Technology Focus

Market	Highlights	Customers
Smartphone	▪ Cumulative 5.3 Billion Unit Sales from 2012-2016 (18% CAGR)[1] ▪ 59% of Handsets by 2016[1]	Qualcomm, Texas Instruments, Intel (Intel Mobile Communications)
Tablet	▪ Cumulative 1.1 Billion Unit Sales from 2012- 2016 (27% CAGR)[1] ▪ 2016 Tablet Traffic at 1.1 Exabytes per Month (Equal to Entire Global Mobile Network in 2012)[2]	Samsung, Micron, Toshiba
Consumer Electronics	▪ Gaming Consoles ▪ "Always Connected" Devices ▪ Digital Home	Sony, Texas Instruments, Broadcom, Toshiba, Entropic Communications
Networking	▪ 2016 Global IP Traffic at 110 Exabytes per Month (29% CAGR from 2011)[2] ▪ 2016 Global Mobile Data Traffic at 11 Exabytes per Month (18-Fold Growth from 2011)[2]	LSI, Altera, Broadcom, Xilinx, Texas Instruments

[1] Gartner. Mobile Devices Forecast Update. September 2012
[2] Cisco Visual Networking Index Forecast. May 2012 and February 2012

Market Direction & Drivers

Mobile Phones and Tablets to Drive Nearly 50% of Semi Industry Growth Thru 2017 ($43B of $88B total)

Segment	2012	2017F	Growth	CAGR
Mobile Phones & Tablets	$69	$112	$43B	10%
Consumer	$36	$42	$6B	3%
Computing	$68	$74	$6B	2%
Networking	$47	$62	$15B	6%
Automotive	$25	$32	$7B	5%
Other*	$47	$58	$11B	4%

Semiconductor Market Revenues ($ in billions)

2012 - $292B
2017F - $380B
Growth - $88B
CAGR - 5%

Source: Prismark Partners. February 2013

* Other includes Medical, Industrial, Military and Aerospace

Foundational Blocks for Advanced Integration

Cu Pillar

TSV

Advanced Materials

WLFO

Advanced Flip Chip

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Advanced Flip Chip

Interconnection Evolution (Wide Pitch to Fine Pitch)

Standard Solder Flip Chip

- Typically uses electro plated bumps redistributed in an <u>area array format</u>
- <u>Mass reflow</u> bonding
- Suited for High I/O, High Power, Very high speed, High thermal applications

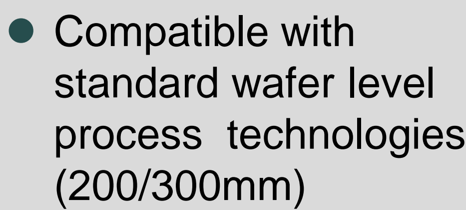
Wide Pitch Cu Pillar Flip Chip

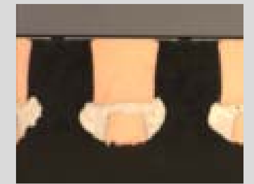
- <u>Utilizes</u> common wafer bumping <u>infrastructure</u>
- Alternative to Standard Solder FC
- <u>Mass reflow or thermal compression</u> bonding capability

Fine Pitch Au Stud

- Primarily developed and used in Japan
- Stud typically applied with a modified wire bonder, formed directly on the Aluminum bond pad
- Thermal sonic or compression bonding
- <u>Stand-off</u> <u>defined by bump height</u>

Fine Pitch Cu Pillar

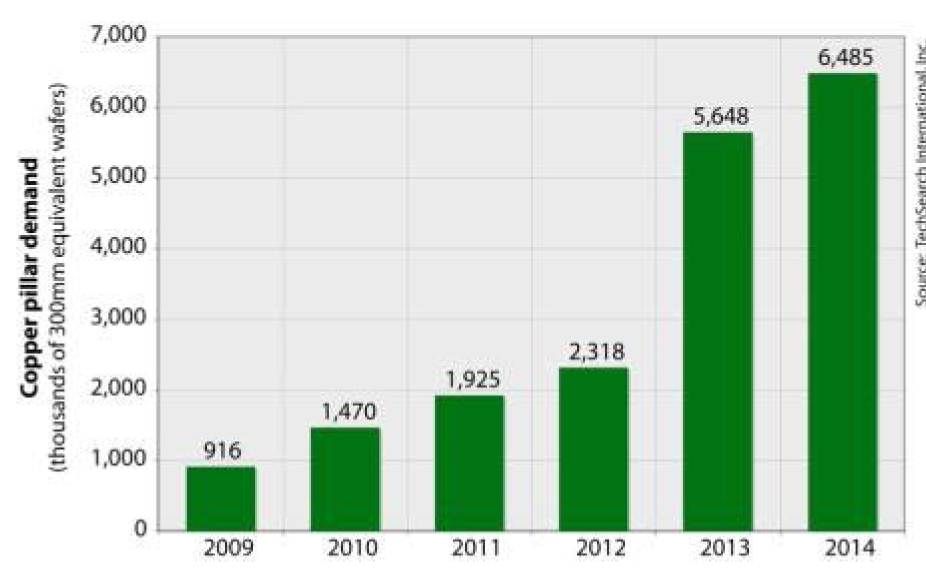


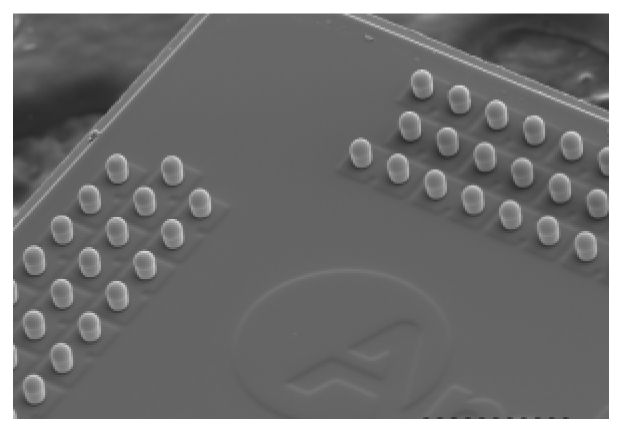


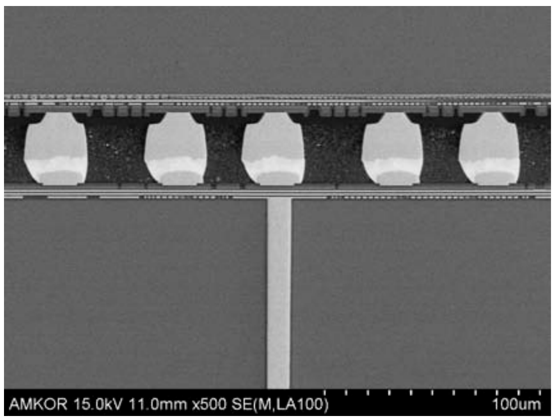
- Compatible with standard wafer level process technologies (200/300mm)
- Bump redistribution not required
- Adaptable from wirebond designs
- Less costly for high bump densities due to the wafer level bump process

Interconnection : Fine Pitch Cu Pillar

- **Copper Pillar Platform**
  - ✓ Fine pitch CSP
  - ✓ Area array fine pitch BGA
  - ✓ μBump F2F - TSV
- **Production Status**
  - ✓ HVM since Q2 2010
  - ✓ 40/80um 3-row CuP pitch
  - ✓ 28/22nm under development
  - ✓ Bonding method : TC/NCP, TC/CUF, TC/NCF







Foundational Blocks for Advanced Integration

Cu Pillar

TSV

Thermal & Adv. Materials

WLFO

High-End FC

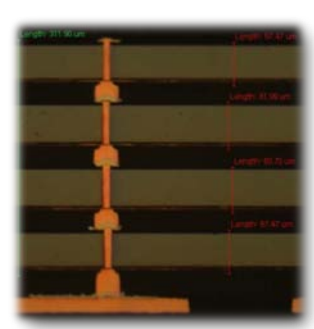
Integration : Through Silicon Via (TSV)

- **Current Status**
  - ✓ World's first production of fully integrated TSV package platform completed
    - "Logic dies on Si interposer" product is being produced
  - ✓ Large number of customers engaged in active TSV development
  - ✓ Target devices
    - Logics on Si interposer
    - Logics + memories on Si interposer
    - Memory / Memory stack
    - Memory / Logic combination

2.5D MCM Interposer Supply Chain

- **High End Products : Networking, Servers**
  - Silicon interposers ; < 2um L/S, < 15nsec latency, > 25k µbumps per die
  - Several foundries delivering silicon interposers today
  - Others in consideration of adding capability to make use of unused assets
- **Mid Range Products : Gaming, Graphics, HDTV, Adv. Tablets**
  - Silicon or Glass interposers ; < 3um L/S, < 25nsec latency, ~10k µbumps/die
  - Glass *may* provide cost reduction path in future
  - Glass interposers infrastructure still immature, but improving
- **Lower Cost Products : Lower End Tablets, Smart Phones**
  - Silicon, Glass or Laminate interposer ; < 8um L/S, low resistance, ~2k µbumps
  - Must provide cost reduction path to enable this sector; thick copper traces
  - No laminate substrate ; So don't underestimate the reach & desire of the organic substrate manufacturers to survive

Memory



- **Sources**
  - End customer choosing memory supplier
  - 2 different sources today – Elpida (Micron) & Hynix
- **Logistics**
  - Plan is to receive memory as 'KGM' on tape and reel
- **Activity**
  - Multiple programs in progress with stacked memory in wide I/O format
  - Shipping single die, 2 die stacks and 4 die stacks
  - Most development being completed with single memory in wide I/O

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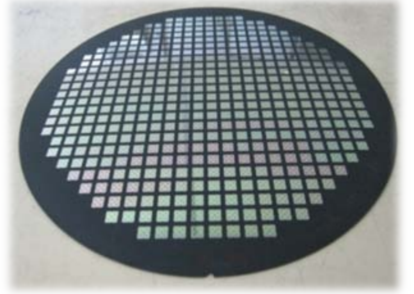
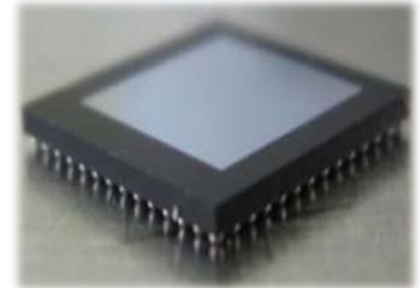
Advanced Flip Chip

Advanced Platform : Wafer Level Fan Out (WLFO)

- **WLFO is now established as a viable alternative to conventional laminate-based and wafer-based packages**
- **The elimination of a conventional laminate substrate and utilization of wafer-level packaging's superior design and feature size capabilities provide many benefits for WLFO, including:**
  - Increased I/O density
  - Reduced form factor (including z-height)
  - Improved electrical and mechanical performance
  - Multi-chip capability
  - Outstanding cost/ performance capability
  - Scalability within a heterogeneous assembly platform
  - Opportunity for advanced 3D structures





Wafer Level Fan-Out Revenue Forecast

Yole Developpement © October 2012

FO-WLP Revenues (M $)

Intel Mobile / IFX eWLB driven

CAGR > 50%

Transition phase

CAGR ~ 0%

Ramp-up with fab-less wireless IC players and wide FOWLP infrastructure / supply-chain

CAGR > 30%

	2008	2009	2010	2011	2012F	2013F	2014F	2015F	2016F	2017F	2018F	2019F	2020F
TOT FOWLP (M$)	$13M	$48M	$75M	$107M	$114M	$107M	$118M	$195M	$280M	$374M	$477M	$571M	$641M

- **WLFO reached the $100M market valuation in 2011**
- **Predicted by Yole to reach $250M market valuation in the 2015/16 timeframe once demand moves from IDMs to fabless wireless IC players and the OSAT supply chain expands**

Wafer Level Fan-Out Wafer Forecast

Breakdown by IC type (12"equiv wafers)

Yole Developement © October 2012

Wafer count (12"eq. wafers) Millions

3.0
1.5
0.0

2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020

DRAM
Touchscreen Controller
RF Connectivity Combo
PMU
NAND Flash Memory
Memory Controller
MEMS & Sensors
NFC
RF Tranceiver
ASIC / FPGA
Audio/Video Codec
Digital Baseband Processor
BB/APE wireless SoC

- **Yole's wafer forecast model predicts 30% CAGR in the 2010-2020 time frame, leading to a ~ $1B market in 2020**
- **This equates to nearly 500,000 wafers shipped in 2015 and more than 2.8 billion shipped in 2020**
- **Time will tell if the infrastructure for this emerging package technology will be strong enough to support this anticipated demand**

Advanced Platform : Wafer Level Fan Out (WLFO)

- **Customer Interest**
  - Hybrid Packages, RF Connectivity, Audio modules & Sensor Applications

No Wire or Substrate

Die Shrink Continuing

Entry — **Large I/O Count Without Die Increase**

Face to Face

PoP/Sensor Application

Expand — **3D PKG Platform Creation**

Cost Reduce — **Core Technology Development**

Customer / Product Base Widens

Evolution of WLFO

- **Key enabling technologies for extensions into 3D**
  - Thru Mold Via (TMV®)
  - Fine pitch copper pillar
  - CoC possum™

3D PoP

TMV®

3D Die on Pkg

Die

Die

Die

Die

3D F2F

3D Stacking

Standard WLFO Structure

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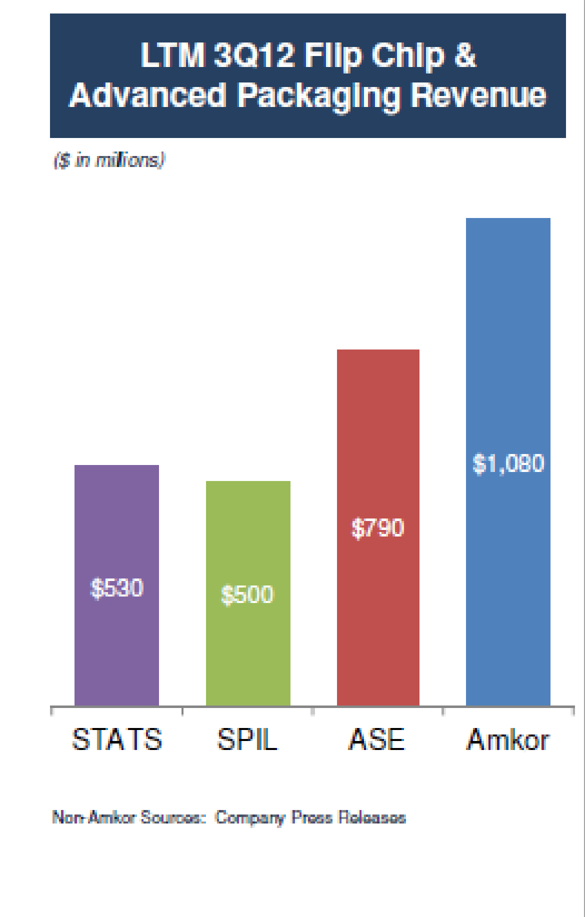
Advanced Flip Chip Continuing to Drive Growth

- Migration to Flip Chip, 3D and Advanced Packaging Continues to Accelerate
- Driven by Strong Demand for Smartphones, Tablets, Gaming Devices, Network Infrastructure
- Enhances Device Performance, Reduces Power Consumption and Form Factors
- Higher Gross Margin and Returns Versus Wirebond

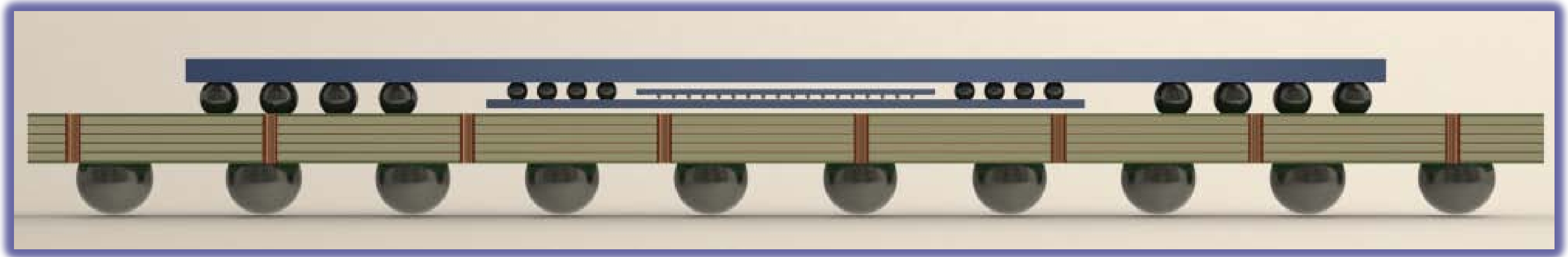


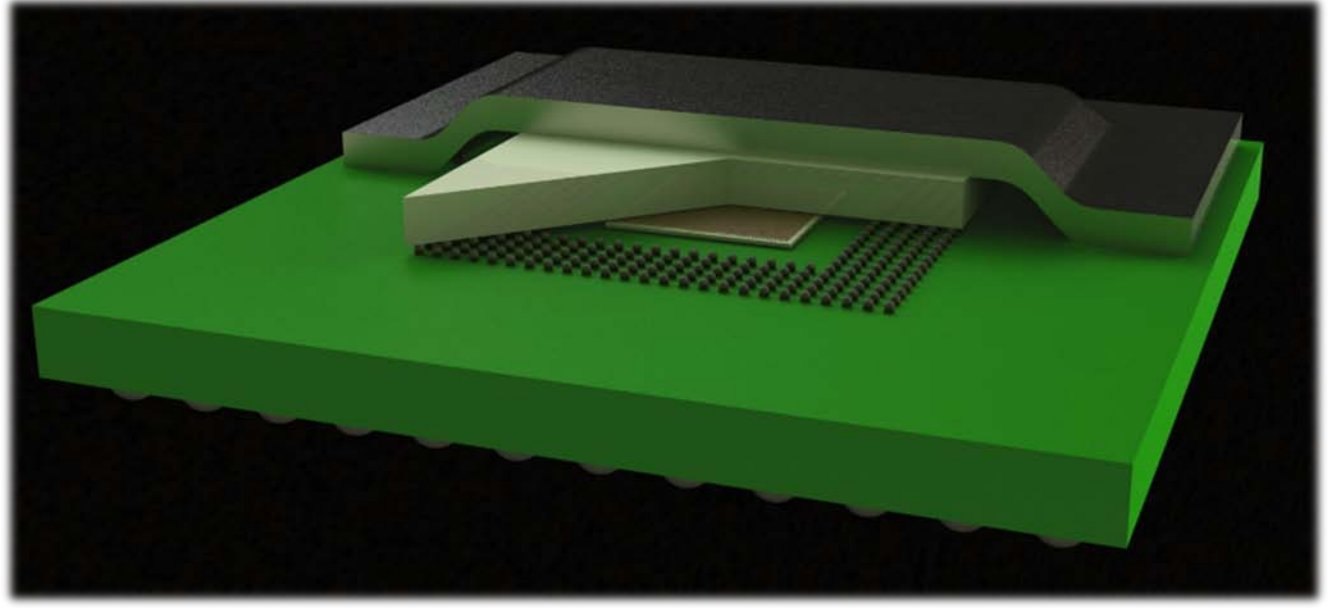
High Performance Flip Chip

- **Industry Direction**
  - ✓ Increasing body size (>55mm BD)
  - ✓ Increasing die size (>26mm)
  - ✓ 32/28nm in production with 20nm qualification in progress
  - ✓ Cu Pillar to enable density / pitch below 150um bump pitch
  - ✓ Coreless substrates in use for 32/28nm
  - ✓ Multiple die per package …. With die count continuing to increase

Advanced FC Packages : Chip on Chip

- **Next Generation of FC – CoC$_{\text{POSSUM}}$**
  - MEMs, Automotive, Networking





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Foundational Blocks for Advanced Integration

Die Attach

Substrate

Underfill

Thermal

Material & Equipment
Technology
Enabling System Integration

Advanced Packaging & Technology Integration

Copper µPillar Bumping

Die Joining

Underfill

Adaptive Learning Required

Silicon

Interposer

Substrate

Thermal

Sha-1 on DDR stack top and underfill

Tc=85.8C

Tj=110.9C

Cu lid
Sha-1
underfill

Assumed Lid touchdown structure along the gap

Sub-assembly & Package Warpage

Foundational Blocks for Advanced Integration

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Advanced Materials

WLFO

Advanced Flip Chip

Amkor Advanced Package Integration

Larger — Form Factor — Smaller

Board Level

Embedded die
Single chip
Embedded MCP
Embedded PoP
Embedded SiP

Wafer Level

FO PoP
FO SiP
FOWLP
1st generation

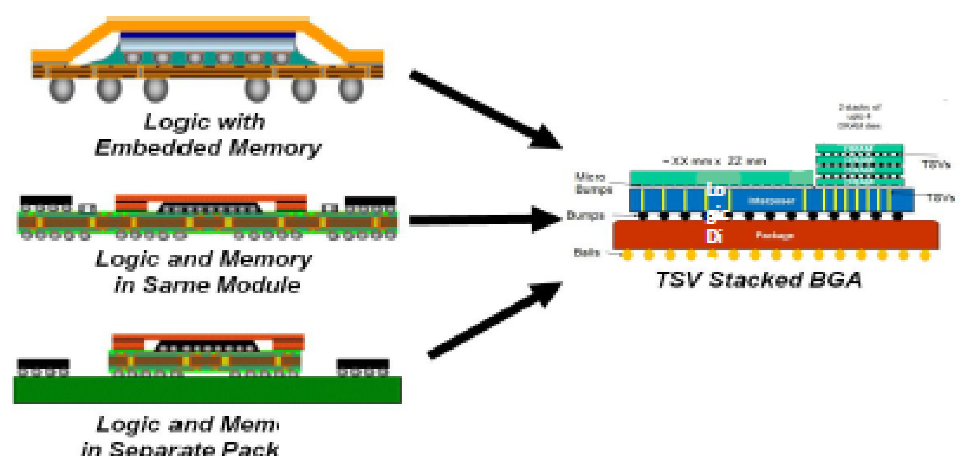
CoC
possum™
LOGIC
ASIC

Die Level

DRAM
DRAM
DRAM
DRAM
TSVs
ASIC
Interposer
TSVs
Package

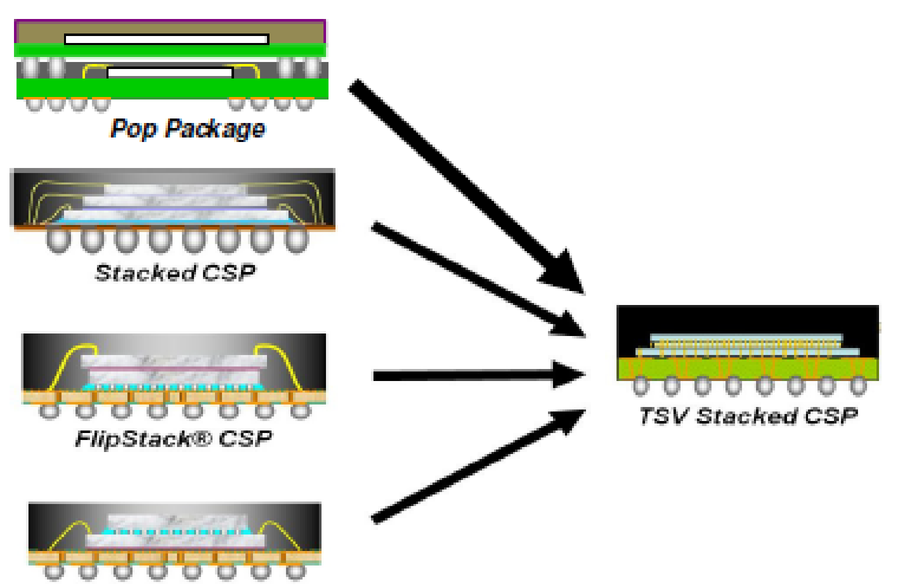
Interconnect Density & Functionality : Increasing

Package Migration to SiP - MCM Integration



2.5D MCM - CPU, GPU, Networking

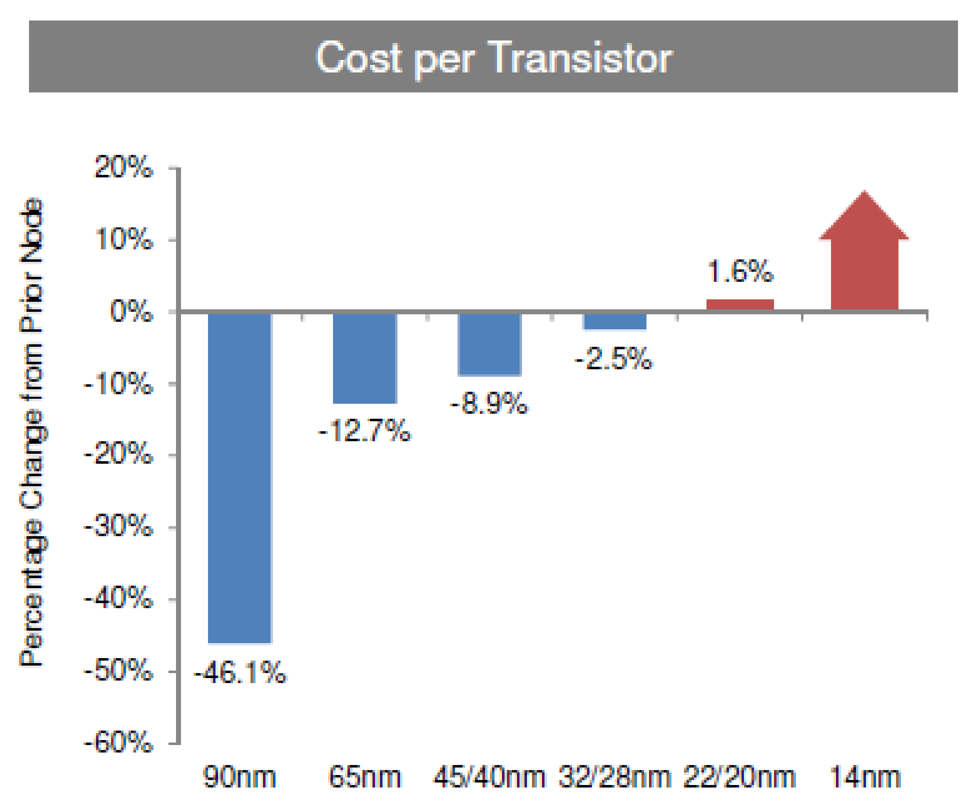
- 100X Improvement in Inter-Die Bandwidth / Watt
- 50% Power Savings
- 5X Latency Reduction
- 20X denser Wire Pitch



3D - Smartphones, Tablets, Memory

- 8X Performance in Bandwidth
- 50% Power Savings
- Profile Improvement

Advanced Silicon Nodes Driving Higher Costs



- For the First Time Ever, Wafer Price Increases Eliminating Scaling Benefits at 22/20nm
- Substantial Process R&D
- Increased Equipment Costs
- Lithography Now 50% of Wafer Costs

Use Advanced Packaging to Minimize or Reduce the Number of Layers of Circuitry that Need to Be Created on the Wafer

Sources: IBS and Nvidia

SOC to 2.5D TSV MCM SiP Drivers

Monolithic
22nm SOC
Type 1

Logic 1
Logic 2
Logic 3
Logic 4

Logic 1
Logic 2
Logic 3
Logic 4

Multi-Die
Interposer
SiP

Monolithic
22nm SOC
Type 2

Logic 1
Cache
Analog
Logic 2
Logic 1
Logic 2
Logic 1

Logic
1
Cache
Logic
2
Analog

Multi-Die
Interposer
SiP

- **Focus Process Node Development on Specific Application Functionalities**
  - ✓ Reduces complexity and mask layer count of process node
  - ✓ Improves wafer yield
  - ✓ Reduces wafer start cost
  - ✓ Improves performance, power, and area of each application

Industry Advanced Package Integration Roadmap

Current / Future Tool-Box for 3D Packaging

TSV Silicon/Glass
WLP
Embedded die
BGA/PoP

I/O Count

> 1,000
500
300
120
50
15
5

3-D Flip-Chip
3-D Logic SiP
DRAM
DRAM
Processor
Memory / Other
Fn A
Fn B
3D Active & Passive Circuitry
Low Cost Package
3D Silicon PoP
3D RF-SiP
Logic & Analog 3D SOC
Logic
eFlash
sDRAM
Analog
RF + I/Os
Interposer
FO PoP
FO MCP
Embedded MCP Module
FO SiP
FO WLP 1st gen.
PoP 'Bottom Package' evolution:
→ Face to Face
→ TMV
MEMS & sensors WLP
Embedded Die
WLP Fan-in

Commissioned report September 2011 courtesy of Amkor Technology and Yole Développement

Chip / Package Size

$2mm^2$ $30mm^2$ $50mm^2$ $80mm^2$ $100mm^2$ $500mm^2$

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Amkor Advanced Package Integration Roadmap

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Thank You!