Near Term Solutions for 3D Memory Stacking (DRAM)

- Wael Zohni, Invensas Corporation

Contents

- DRAM Packaging Paradigm
- Dual-Face-Down (DFD) Package
- DFD-based 4R 8GB RDIMM
- Invensas xFD™ Technology Platform
- Memory Applications
- Summary

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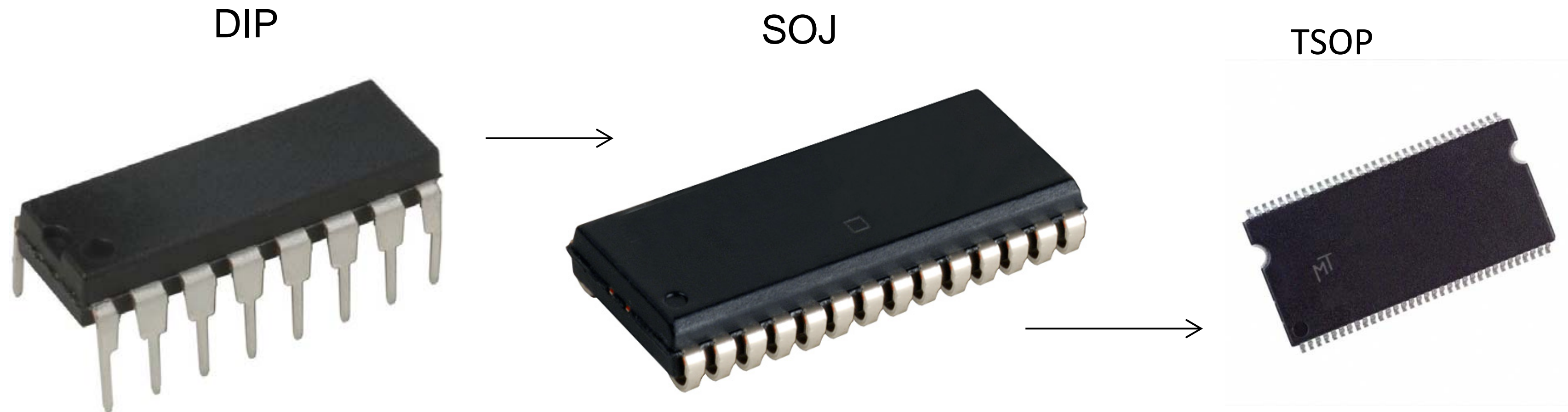
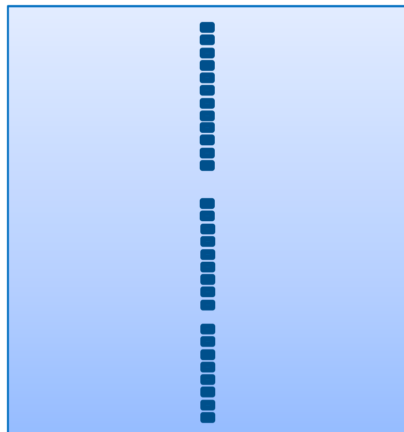
Evolution of Single-Device DRAM Packaging

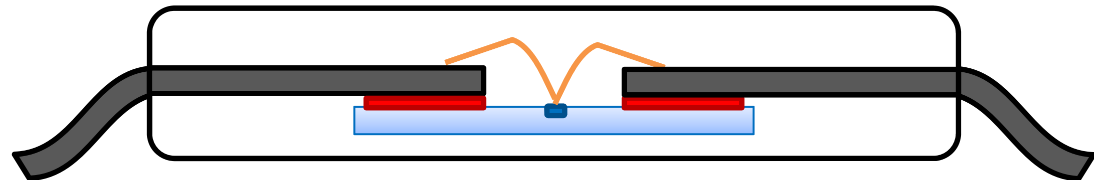


DRAM Device Layout
(top view):



Centered Bond Pads

Single DRAM in TSOP
(Cross-Section)



Wide-body Plastic Leadframe
Wirebonded Package

CSP
...

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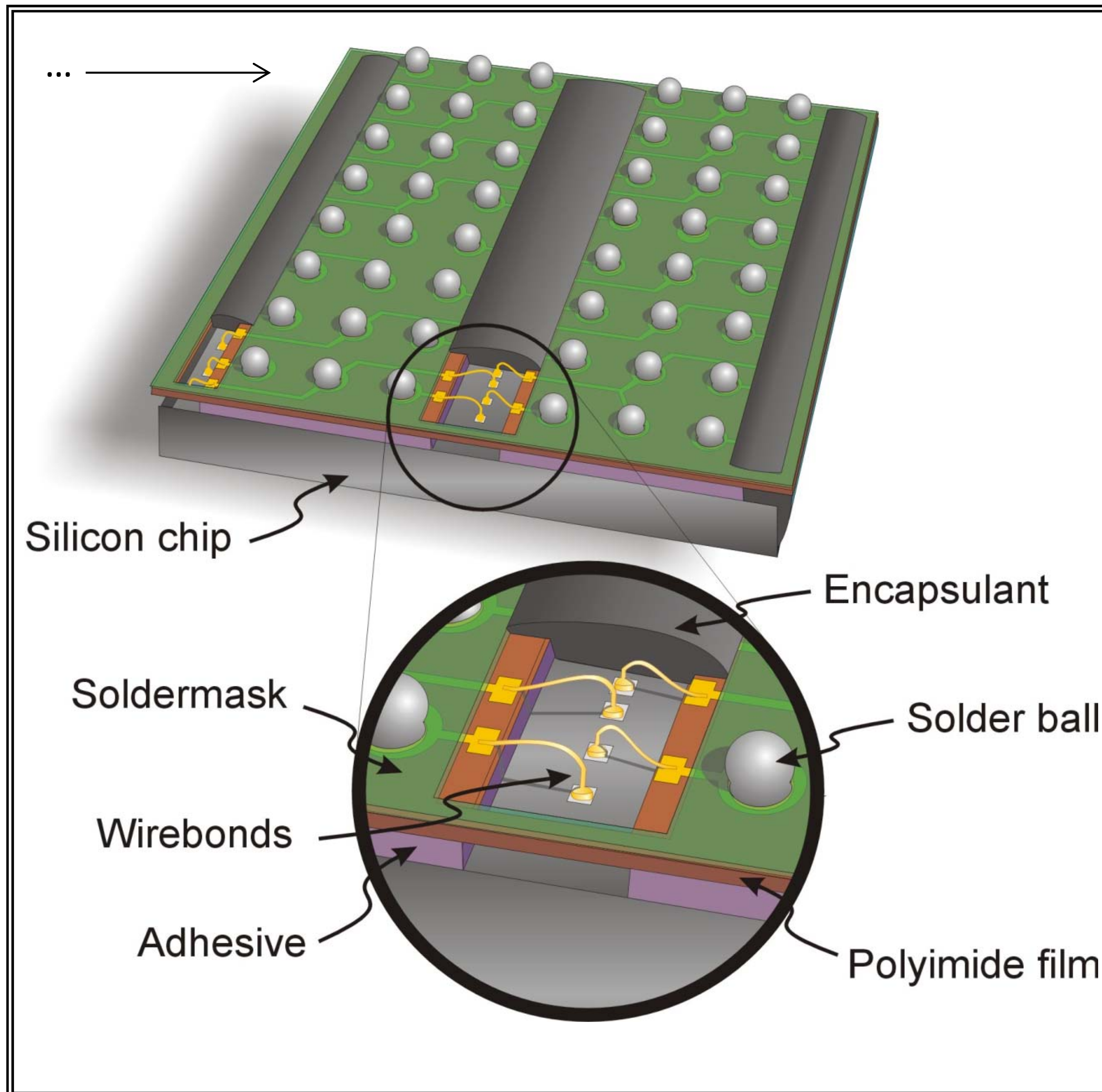
TSOP to Window BGA Chip-Scale-Package (CSP)



- Entered production ~2000
- Current "De facto" standard for single-device DRAM packaging
- Reduced size (Chip-Scale)
- Higher performance

- Over 10 years of infrastructure development
- Established reliability
- Reduced material cost
  - Flex → BT
  - Film → Print Adhesive
  - SnPb → Pb-free
  - Increased volume
  - Short wirebonds

- Demonstrated High Volume Manufacturing
- More than ***40 billion*** units shipped over last 6 years
- Infrastructure forms basis for xFD implementation

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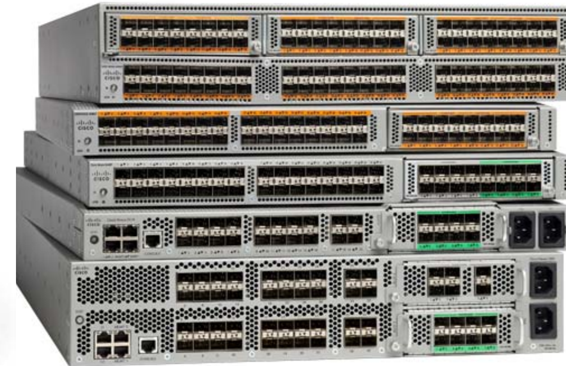
The Governing Paradigm

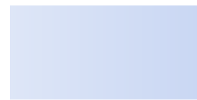


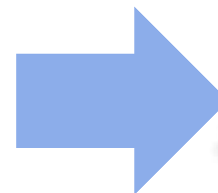
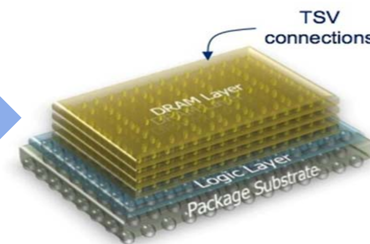
<u>Denser:</u>
"Higher Capacity/mm^3"

<u>Cheaper:</u>
"Lean and Green"

<u>Faster:</u>
"Quicker Data Access"

<u>2012</u>



<u>2017?</u>

Source: Samsung & Micron Images

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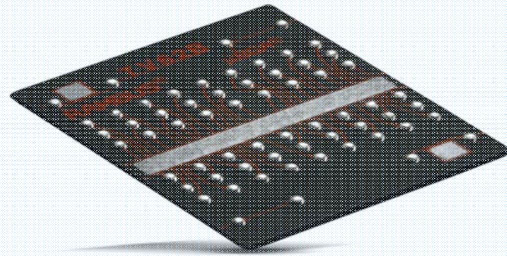
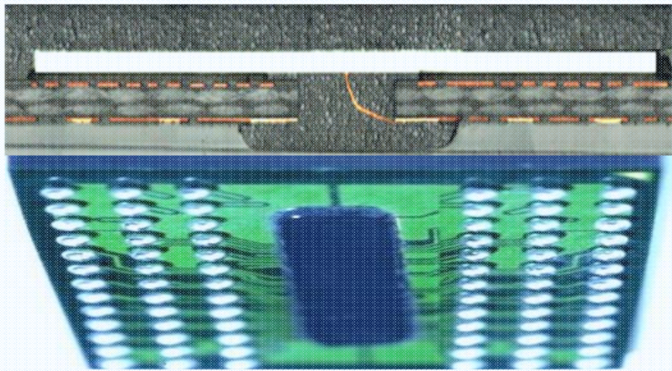
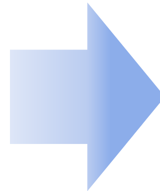
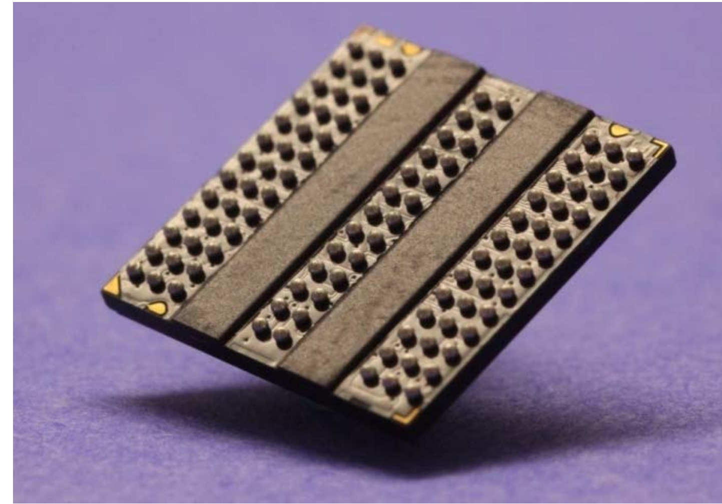
Invensas xFD™ Solution



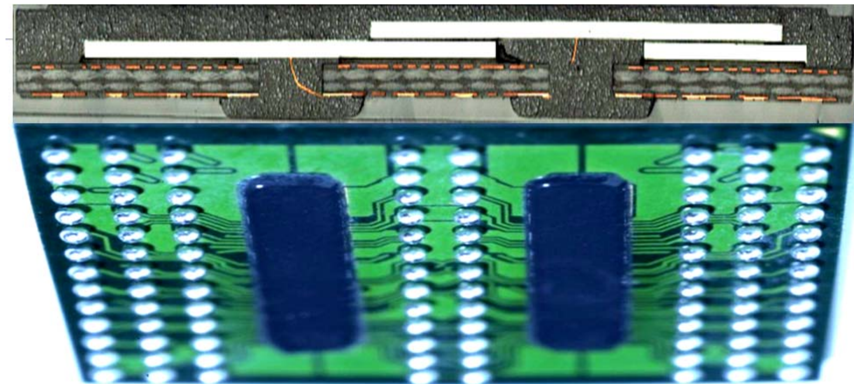
Single Die DRAM Package
>Decade HVM, Billions of Units







2011 – DFD: Dual Face Down Package



Full Leverage of Established Assembly Infrastructure for High-Performance Multi-DRAM Package

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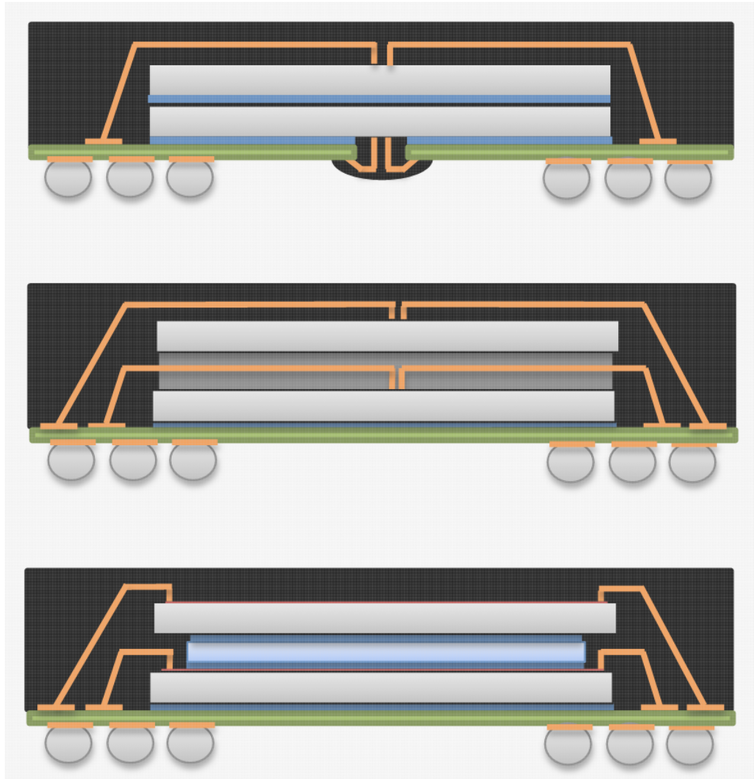
Comparison with Conventional Dual DRAM Packages

Dominated by Gold Cost



Opposing-Face DDP
Long wires, unbalanced top/bottom signal length, thermal challenges

Face-Up DDP with FOW
Balanced signal length but at significant gold wire cost, difficult and cost Film-over-Wire material/process, thermals

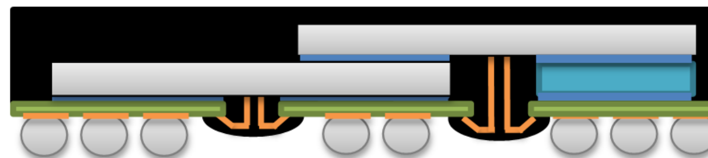
Dominated by RDL Cost

Face-Up DDP with RDL
Balanced signal length, reduced gold wire but requires expensive re-distribution layer process, thermal challenges

Conventional structures: Two Passes Through Wirebond Line

Invensas: Single Pass through Wirebond Line (much less gold wire, no RDL) = lowest cost

Invensas Dual Face Down (DFD):



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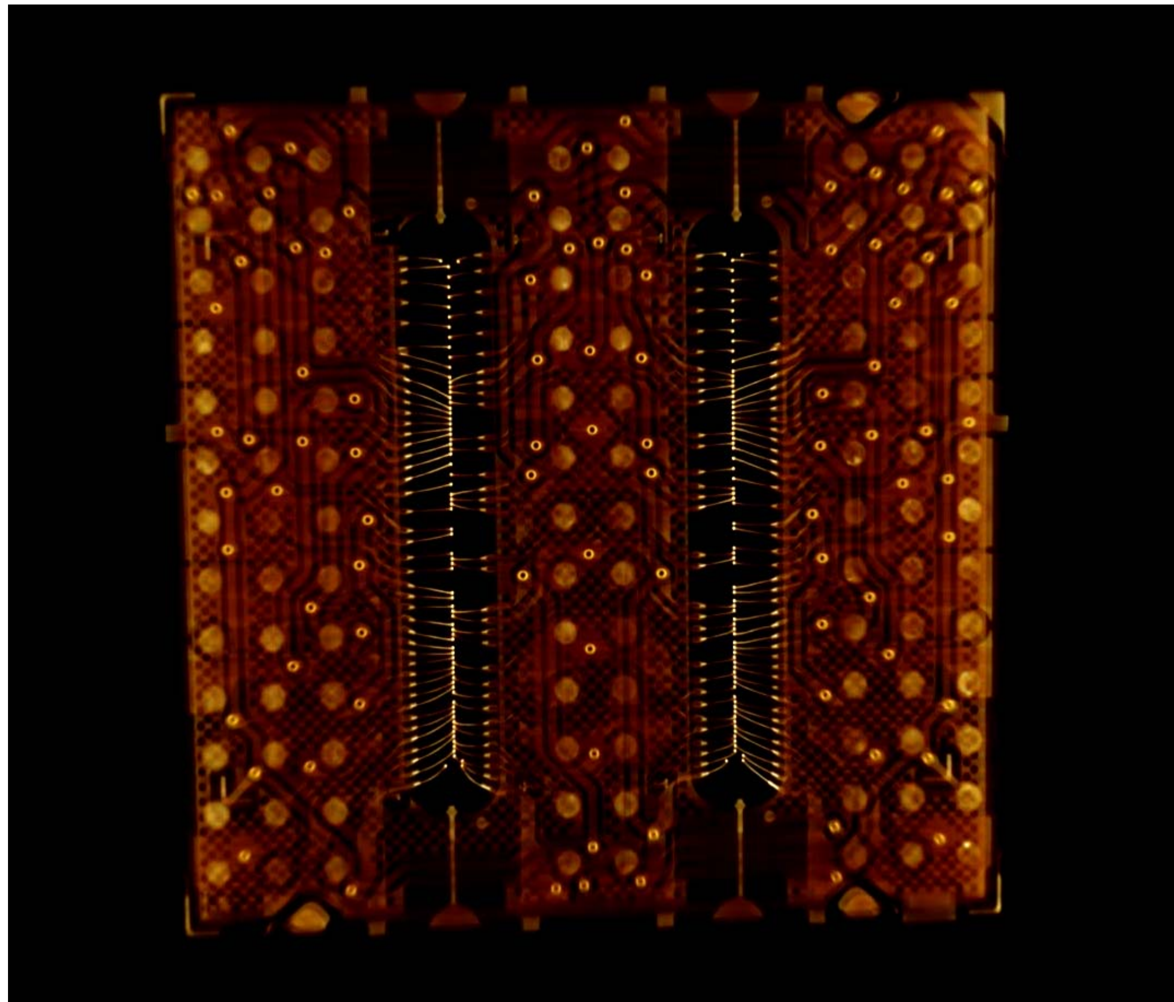
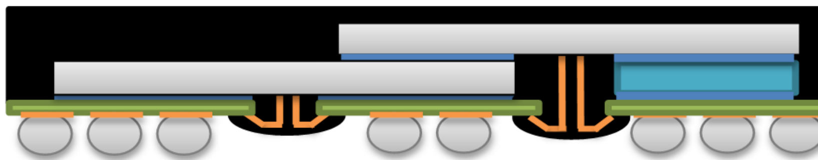
DFD Package Highlights



3D CT scan



- Brings single-device electrical performance to multi-DRAM packaging
- Verified volume manufacturing process with existing equipment
- Less than half packaging cost of RDL-DDP
- About 25% improvement in thermal performance
- Implications extend to module-level design optimization and cost reduction

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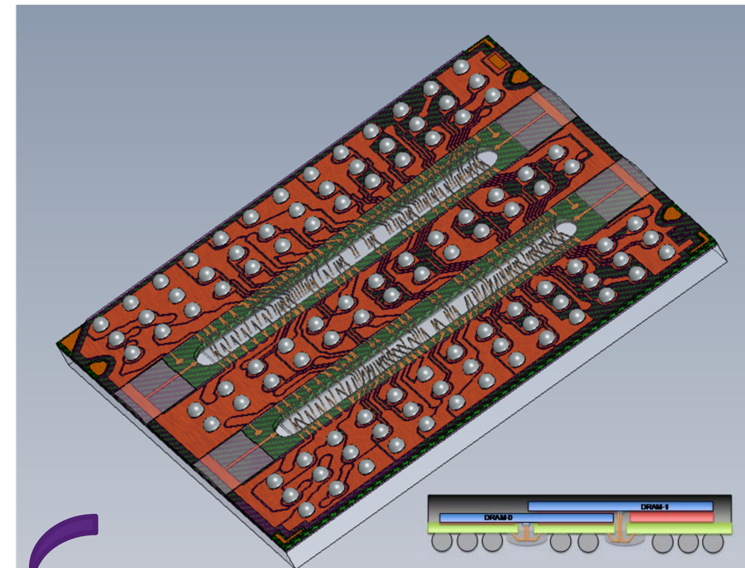
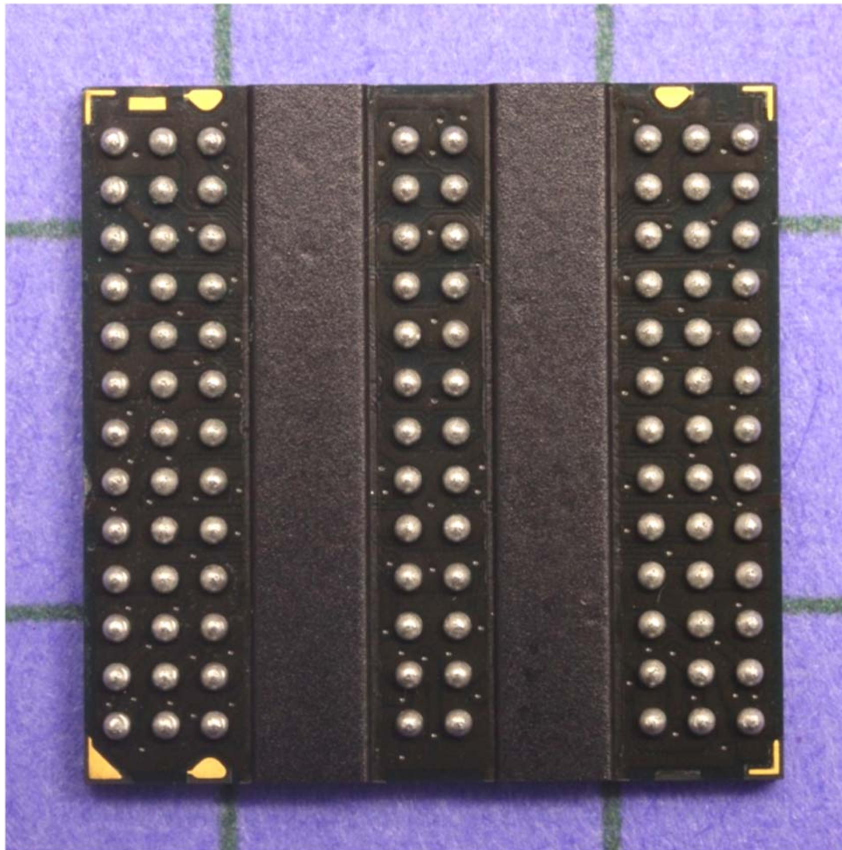
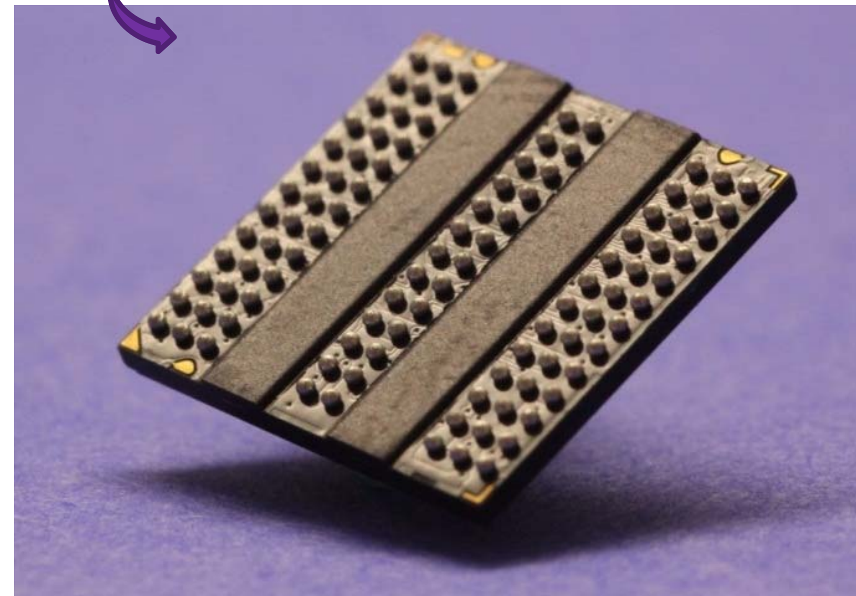
2x1Gb DFD Package Prototyping

- 2x1Gb DFD Engineering at HVM facility
  - 1500+ prototypes completed
  - Verified HVM assembly process
  - Generated electrical test yield data
  - Utilized 1600Mhz+ Micron 1Gb DDR3 device
  - Prototypes assembled into functional RDIMMs







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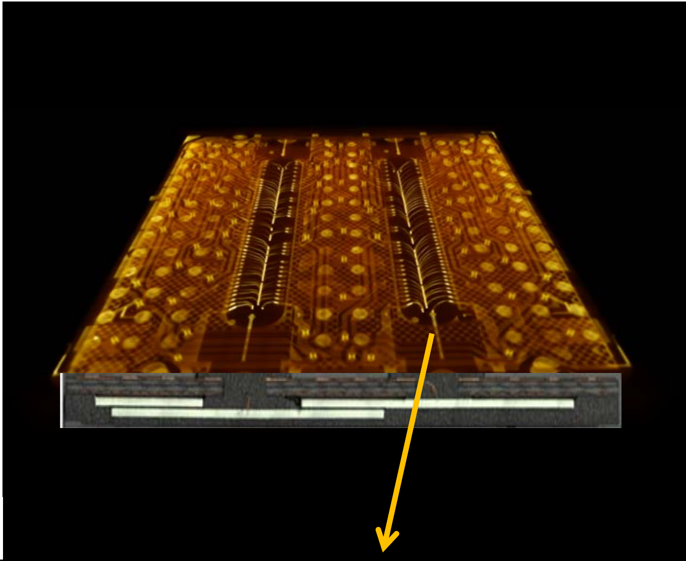
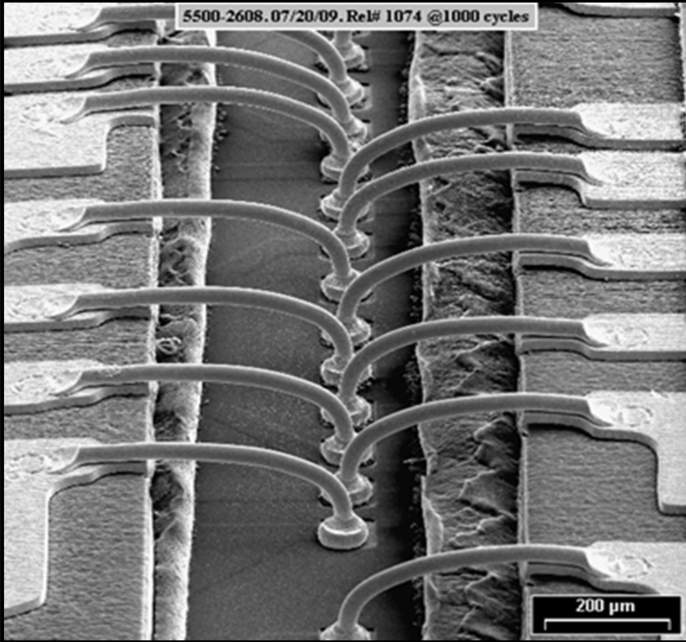
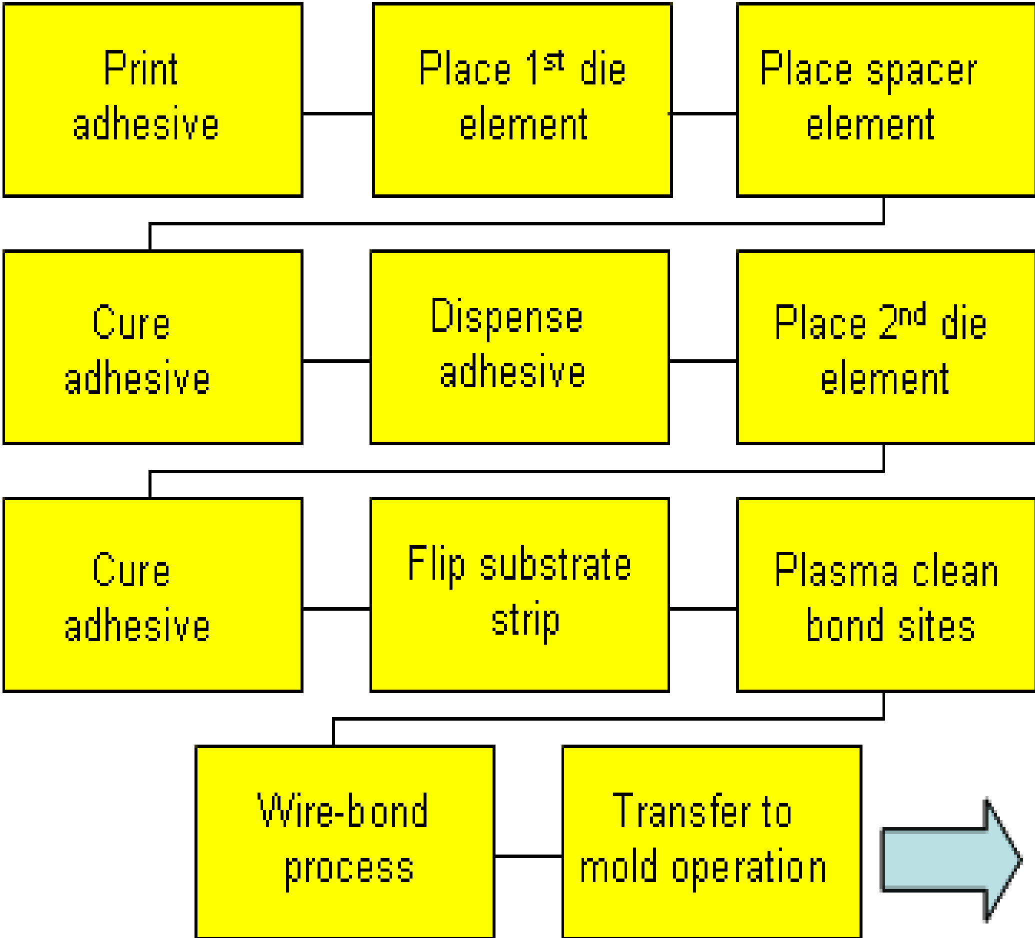
DFD Package Assembly Process Flow







Two narrow slots are provided in the substrate to access the die bond pad pattern and accommodate the through-window wire-bond process

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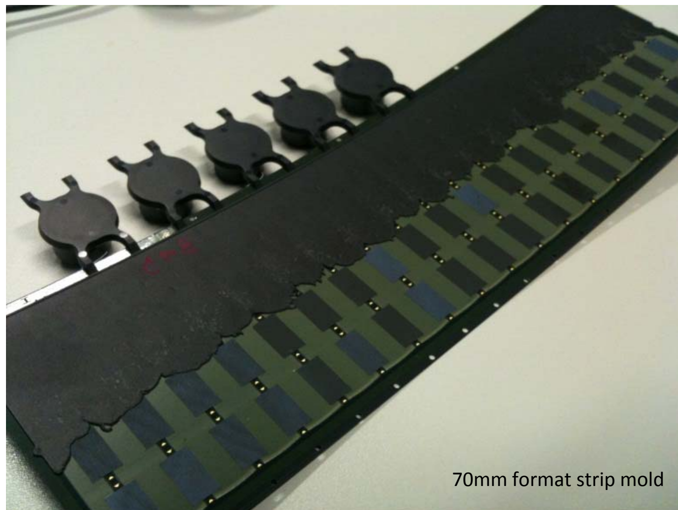
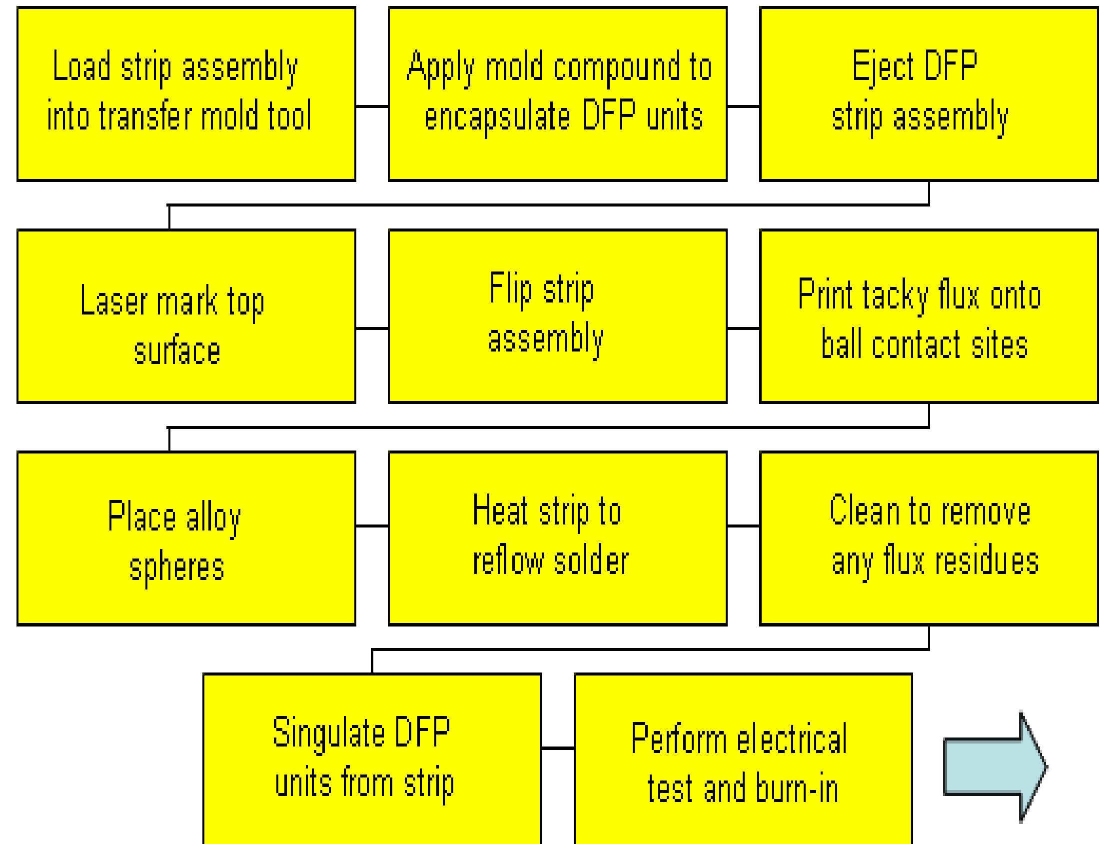
DFD Package Assembly cont.





Conventional BGA reflow

- Final phase of the package assembly includes an injection molding process, laser marking, ball attach, singulation, electrical test and burn-in.

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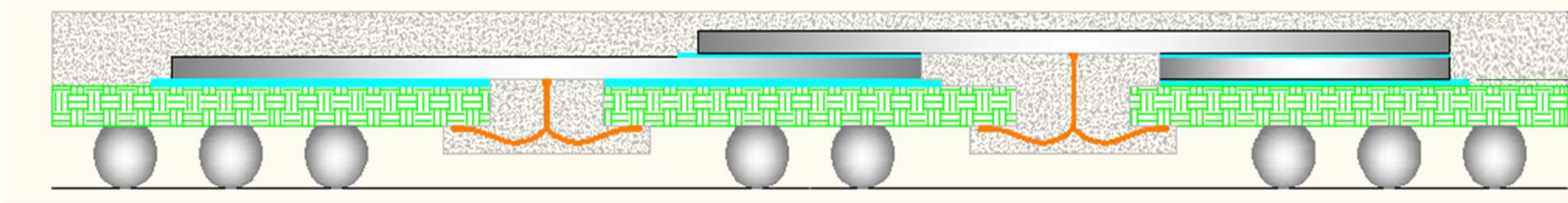
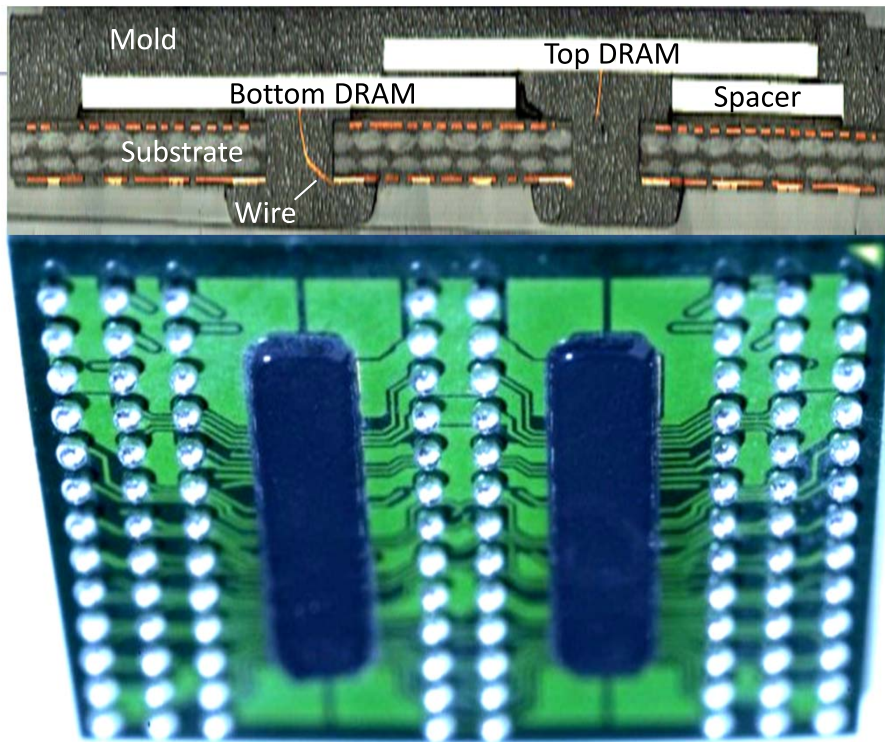
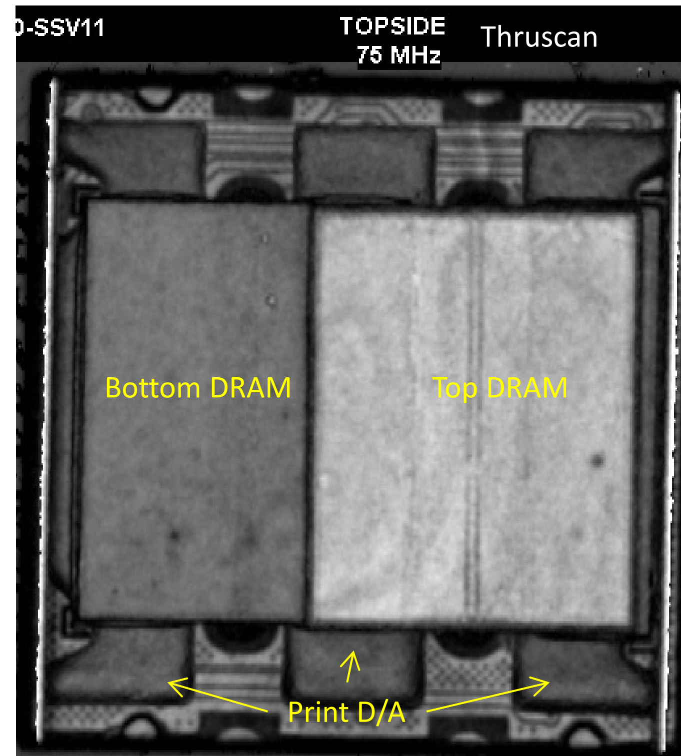
Invensas DFD Prototype

Cross-section Drawing:







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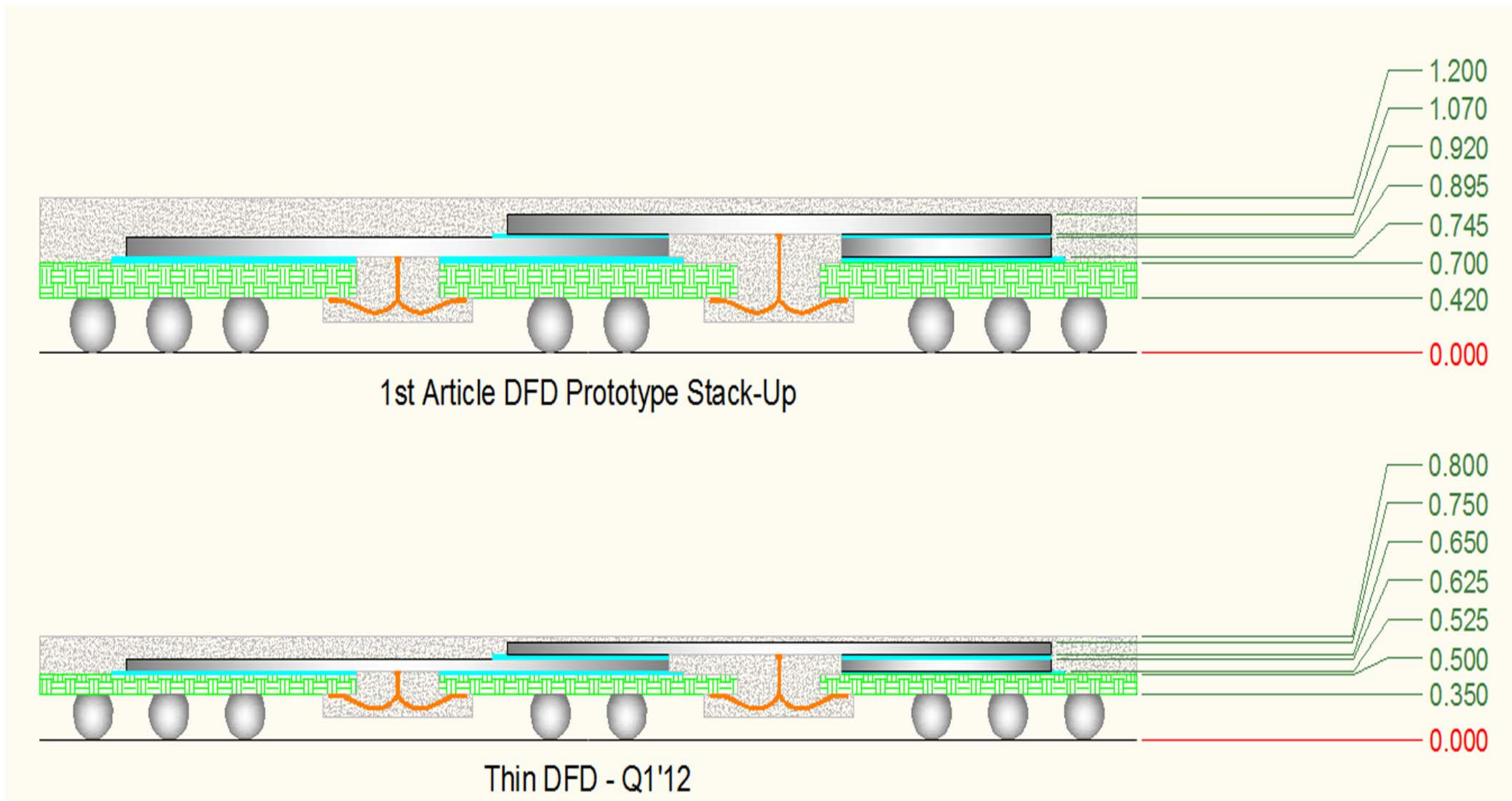
DFD Package Stack-Up



Next stage DFD Prototyping to demonstrate 0.8mm package height

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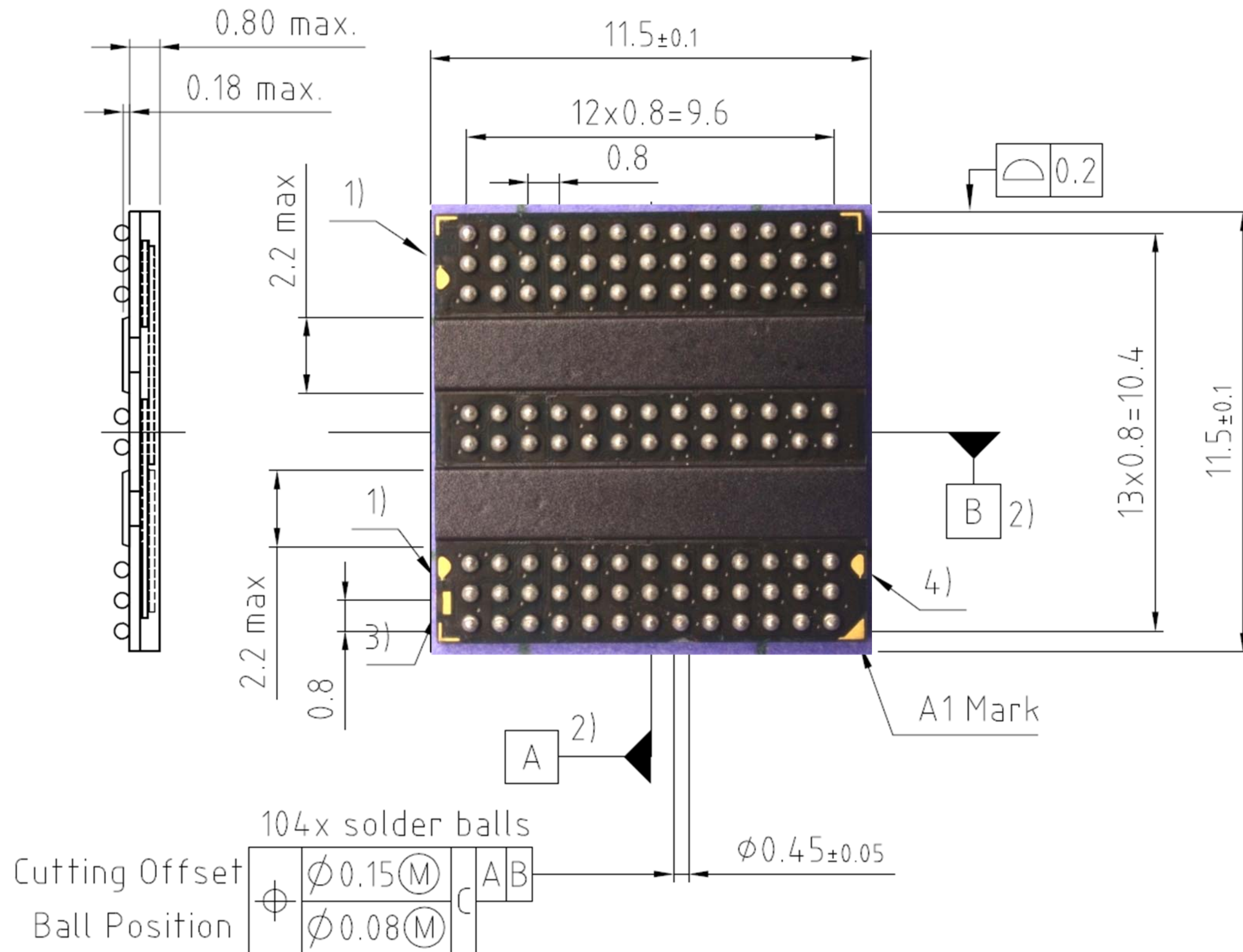
2x1Gb DDR3 DDP Prototype – Package Outline



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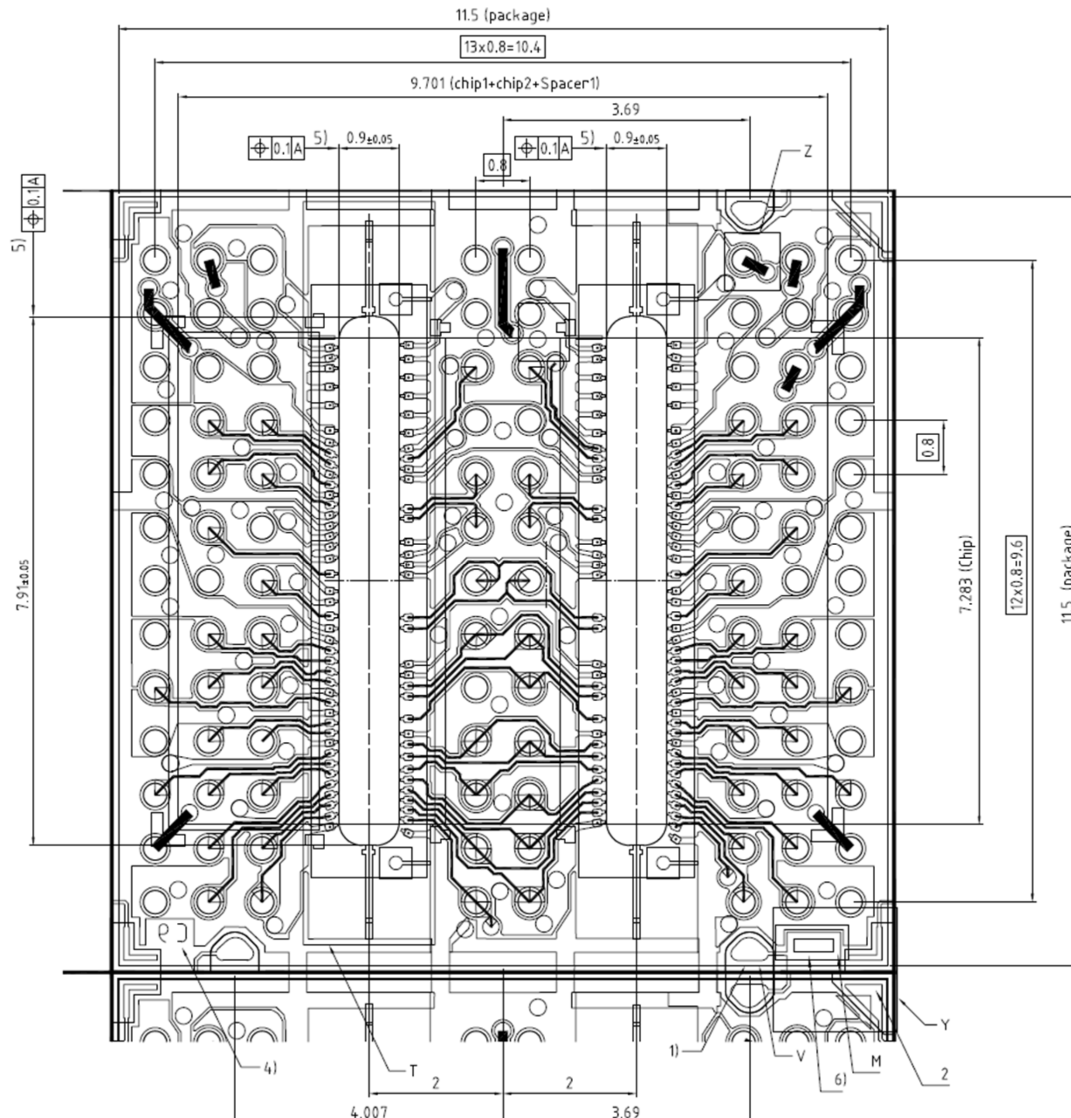
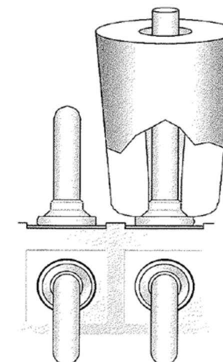
DFD Prototype Package Materials

2ML BT substrate with dual bond windows



Materials:

- Substrate – BT – 280um thk
- Gold wire – 20um diameter
- Print die attach adhesive (bottom device)
- Dispense die attach adhesive (top device)
- Silicon Spacer
- Mold
- Pb-free solder ball



- 20um gold wire diamter
- Standard and deep well bonding with conventional wire bond capillary and equipment

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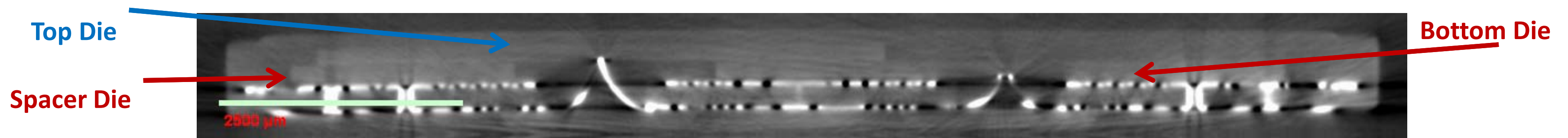
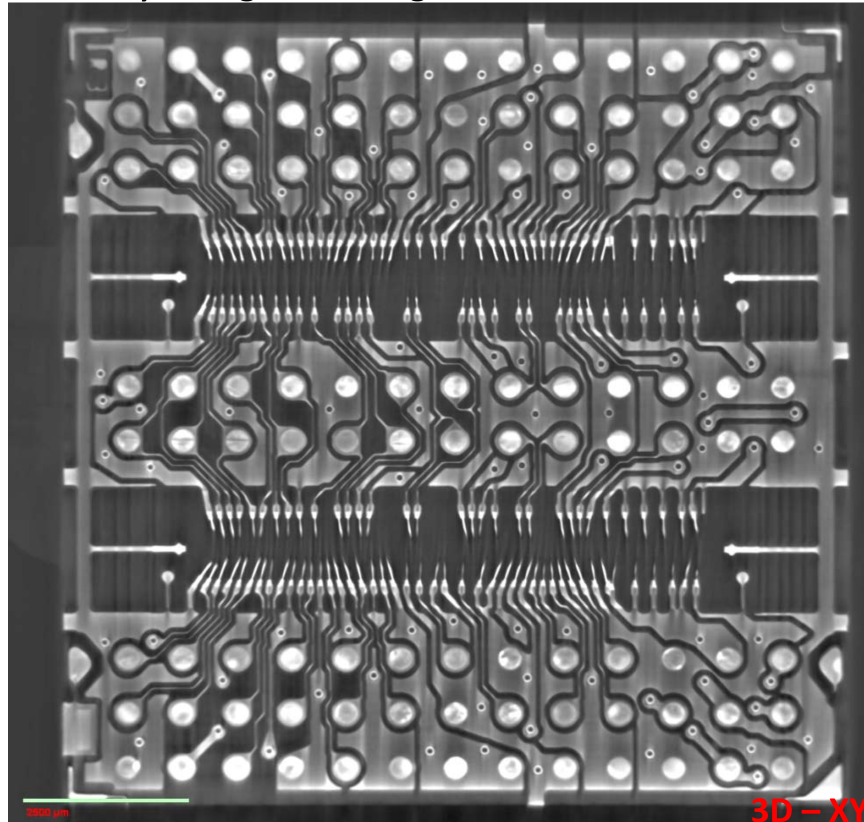
Invensas DFD: XRAY 2D CT Scan

Invensas Dual Face Down package: High Resolution Computerized Tomography – 2D Slices

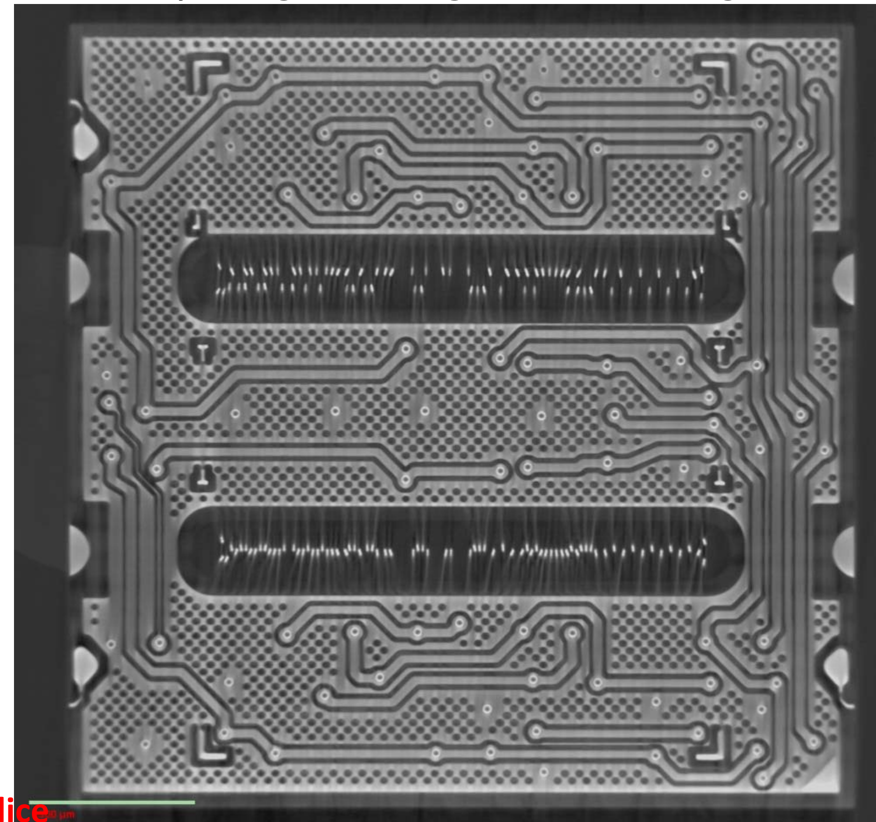
YZ Slice



XYSlice; Z height showing bond wires



XYSlice; Z height showing substrate routing



3D – XY Slice

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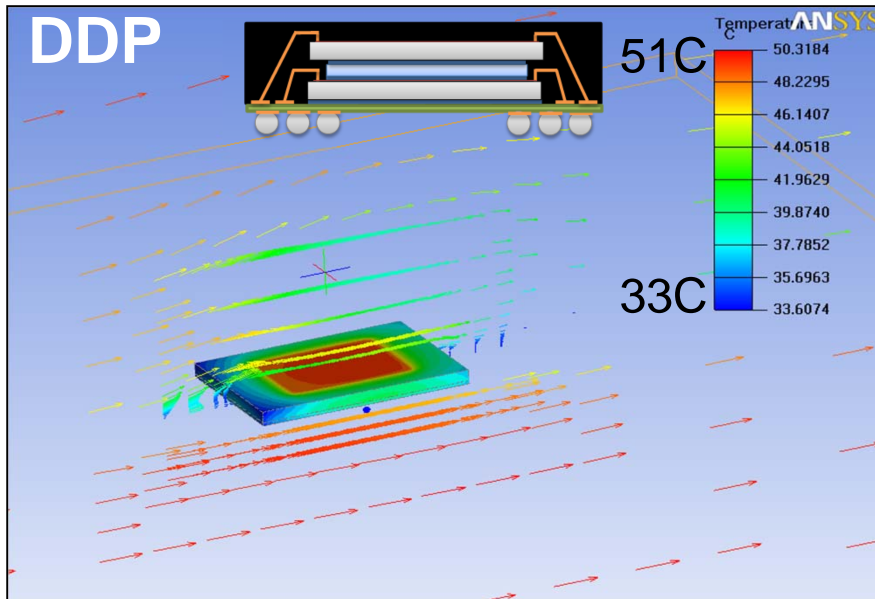
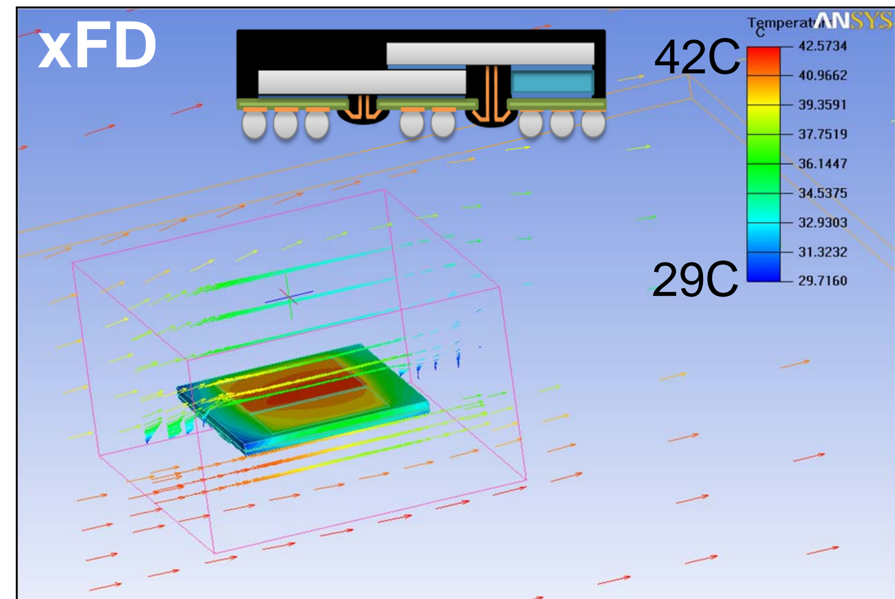
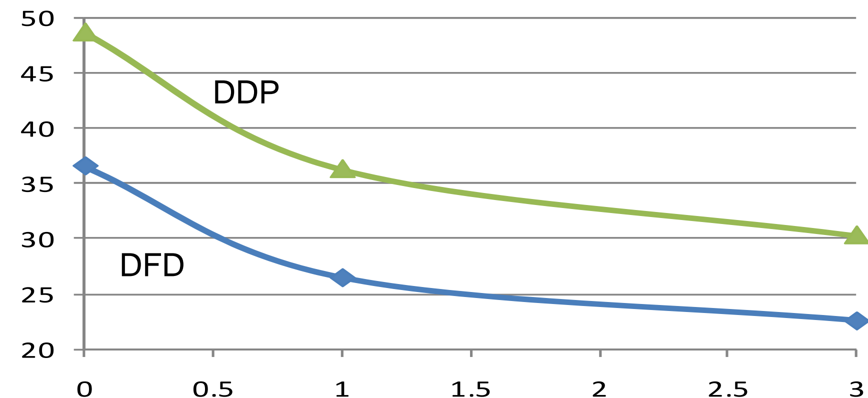
Denser: Thinner = Better Heat Transfer





Natural and Forced Convection

degC/W	Standard DDP	Invensas DFD	Difference
Rth-ja, 0 m/s	48.7	36.6	-25%
Rth-ja, 1 m/s	36.3	26.5	-27%
Rth-ja, 3 m/s	30.3	22.6	-25%



- **Thin + 25% Heat Transfer Gain = 40% Cooling Cost Reduction in Data Center.**

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DFD Package Reliability Test Data

- Component-level environmental test completed on functional DFD packages:
  - Moisture pre-conditioning – JEDEC level III
  - Highly-Accelerated-Stress-Test (HAST) – 240 hours
  - Temperature Cycling – 1000 cycles

Test	Quantity	Conditions	Results
Level 3 Pre-conditioning (MSL3)	60 units	TC: -55°C/+125°C (5x) Baking: 125°C (12hours) Soaking: 30°C / 60%RH (192hours) Reflow: 3x 260°C	Pass
HAST	29* units	MSL3 + (Ta=+130°C; 85%Rh) 240 hours	Pass
Temperature Cycling	30 units	MSL3 + 1000 cycles 55°C/+125°C	Pass

* 1 unit removed due to handling damage

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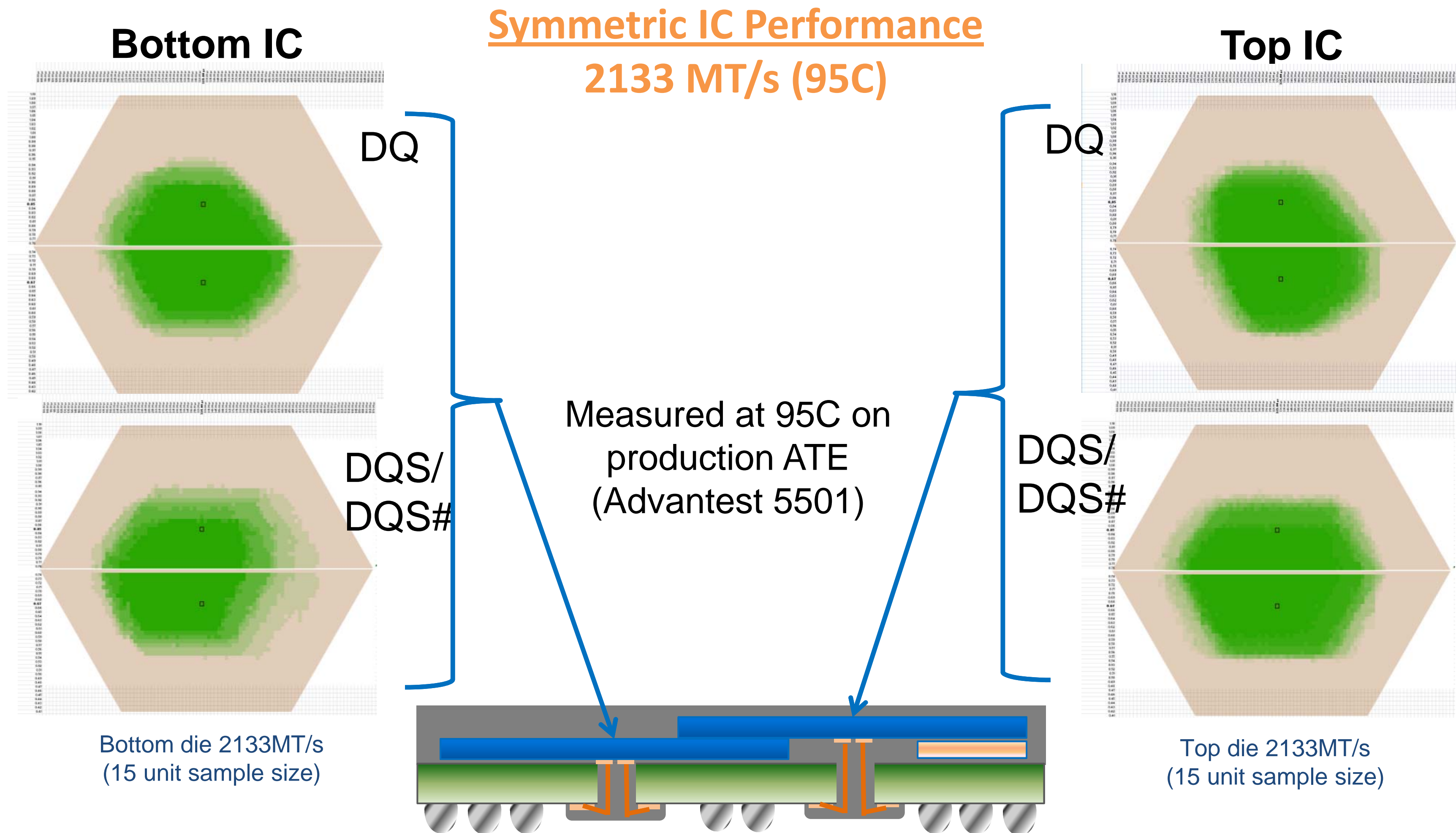
Faster: Monolithic Performance from All Die



Bottom die 2133MT/s
(15 unit sample size)

Top die 2133MT/s
(15 unit sample size)

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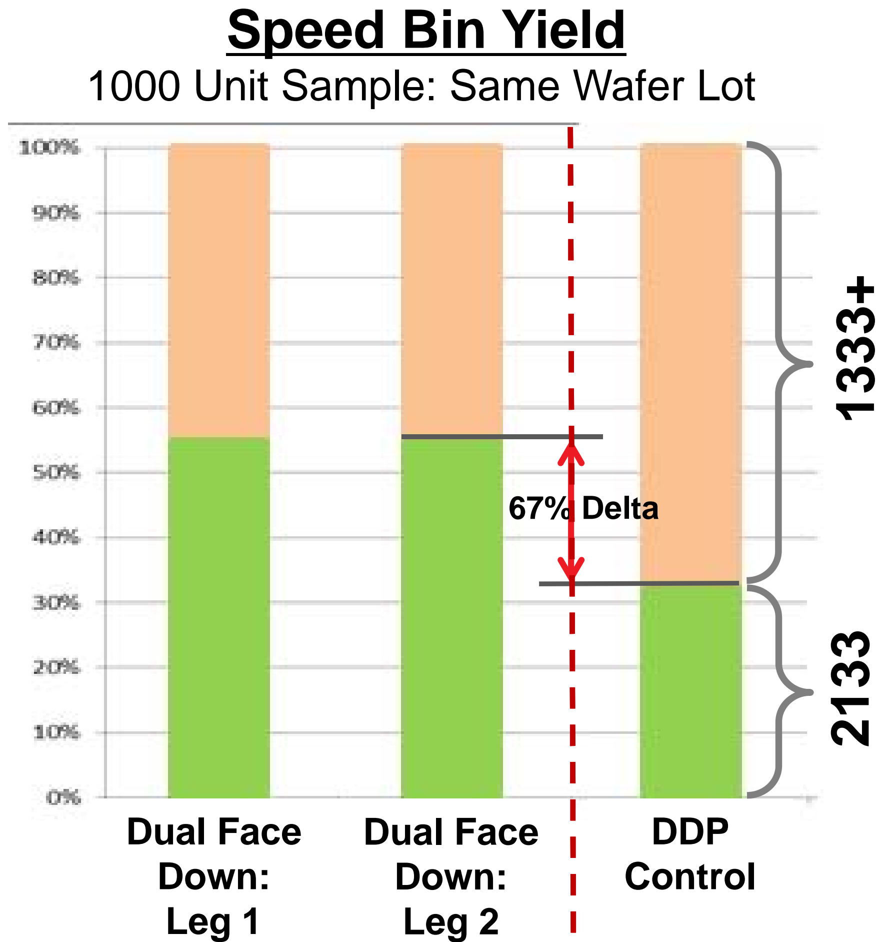
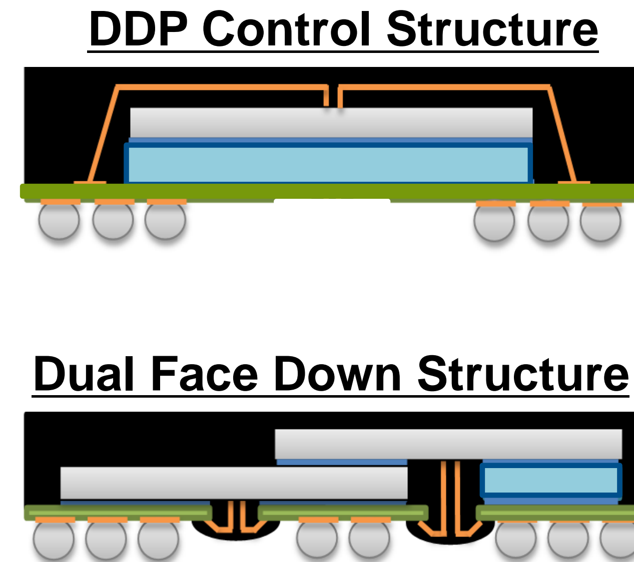
Faster: Significant Speed Bin Yield Gain





- **67% gain in 2133MT/s speed bin yield vs. control DDP using same wafer lot.**

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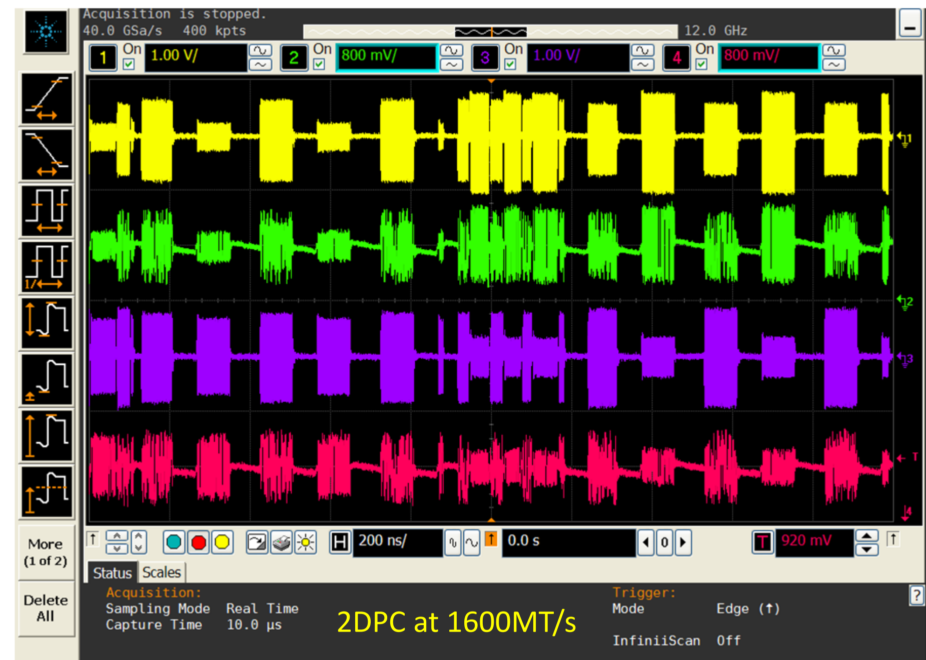
4-Rank 8GB RDIMM using 2x1Gb DFDs



- Produced functional 8GB RDIMMs using 2x1Gb DFD packages; undergoing evaluation

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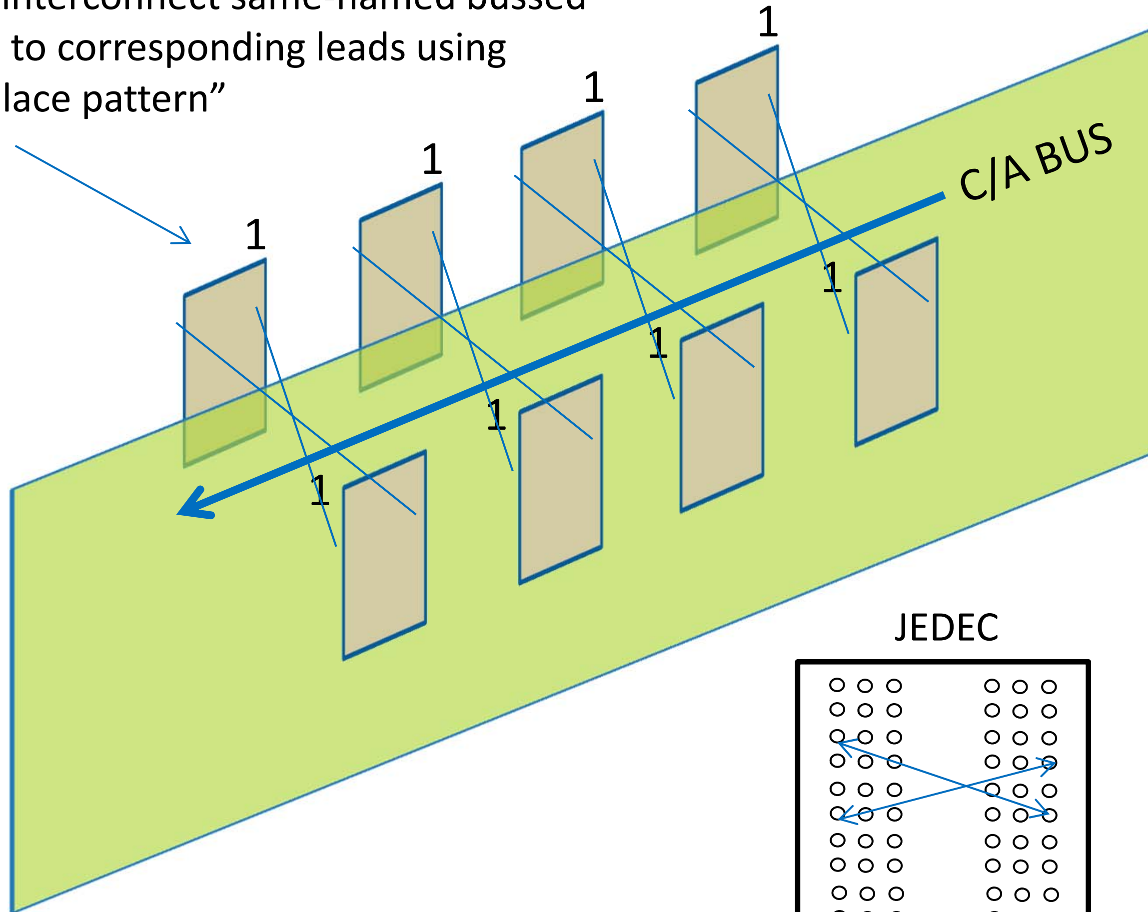
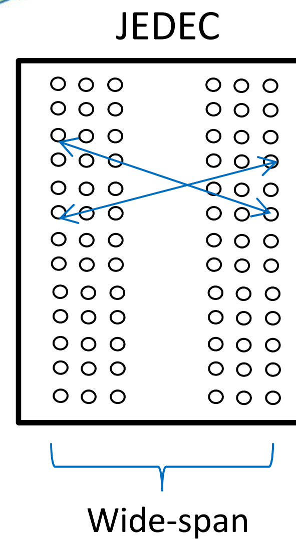
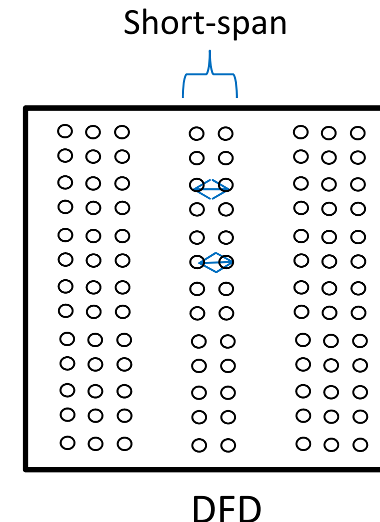
High Capacity DIMMs: Double-Sided Assembly







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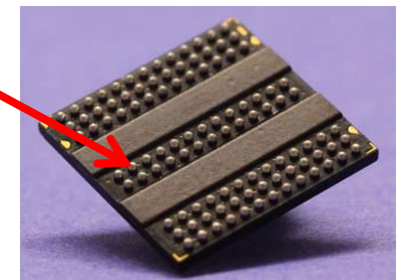
DFD Solves the C/A Stub issue elegantly

	1	2	3				7	8				12	13	14
A	VDD	DM_1	VSS				VDD	VDD				VSS	DM_0	VDD
B	VSS	DQ0_1	DQ2_1				CK	CKB				DQ0_0	DQ2_0	VSS
C	VDD	DQ1_1	DQ3_1				RASB	CASB				DQ1_0	DQ3_0	VDD
D	VSS	DQSB_1	DQS_1				A10	WEB				DQS_0	DQSB_0	VSS
E	ZQ_1	VDD	VSS				A15	BA2				VSS	VDD	ZQ_0
F	VDD	VSS	VDD				BA0	A12				VDD	VSS	VDD
G	VSS	ODT_1	VSS				BA1	A0				VSS	ODT_0	VSS
H	VREFDQ_1	CKE_1	VDD				A3	A1				VDD	CKE_0	VREFDQ_0
J	VDD	CSB_1	VSS				A4	A2				VSS	CSB_0	VDD
K	VREFCA_1	VSS	VDD				A5	A11				VDD	VSS	VREFCA_0
L	VSS	VDD	VSS				A6	A9				VSS	VDD	VSS
M	VDD	VSS	VDD				A7	A14				VDD	VSS	VDD
N	VSS	VDD	RSTB_1				A8	A13				RSTB_0	VDD	VSS

C/A signals in dead center of package in the traditional “No Man’s Land”



C/A region has simple breakout

C/A Bus Signal ordering matches DDR3 register perfectly

DQs and DQS signals close to package edge

Most other signals only need simple through-hole connections to backside components

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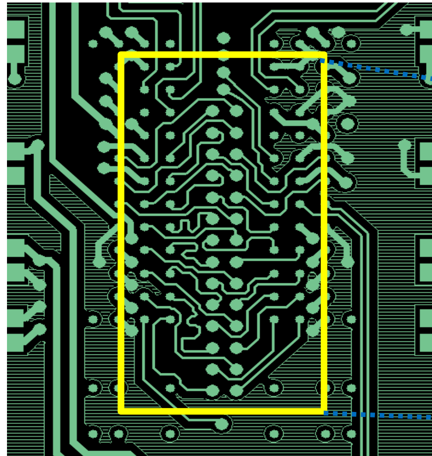
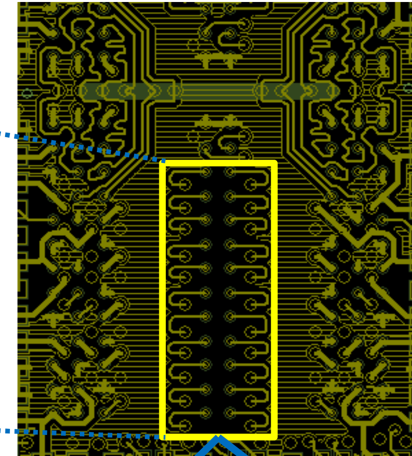
Faster: Ultra-Short, Matched DIMM Breakout

JEDEC Address/Command



xFD Address/Command



4X reduction in C/A stubs

- **Efficient Address/Command breakout minimizes stub lengths & DIMM layer-count.**

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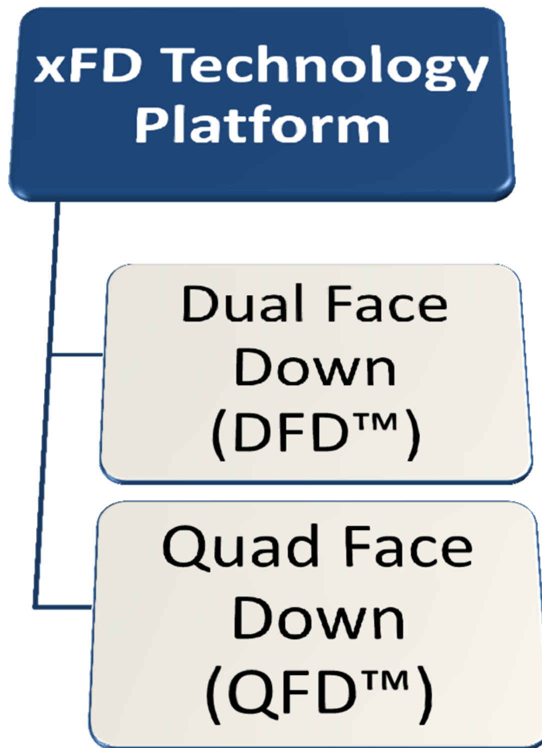
xFD Technology Platform



- xFD technology is a platform
- Two die in a single package (server, mobile)
- Four die in a single package (mobile)

Flexible platform that accommodates any number of multi-die packaging implementations

<u>All manufacturable in a standard wirebond line</u>

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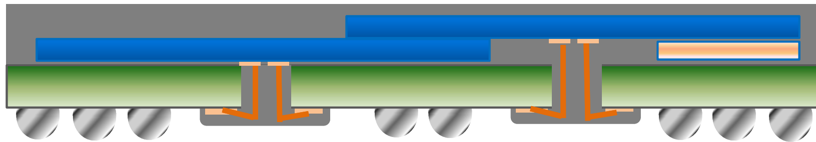
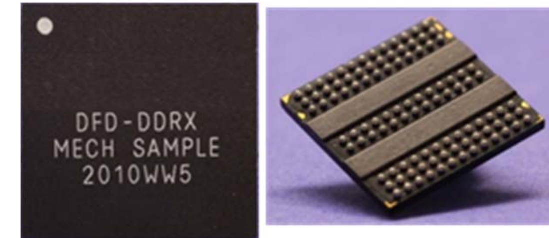
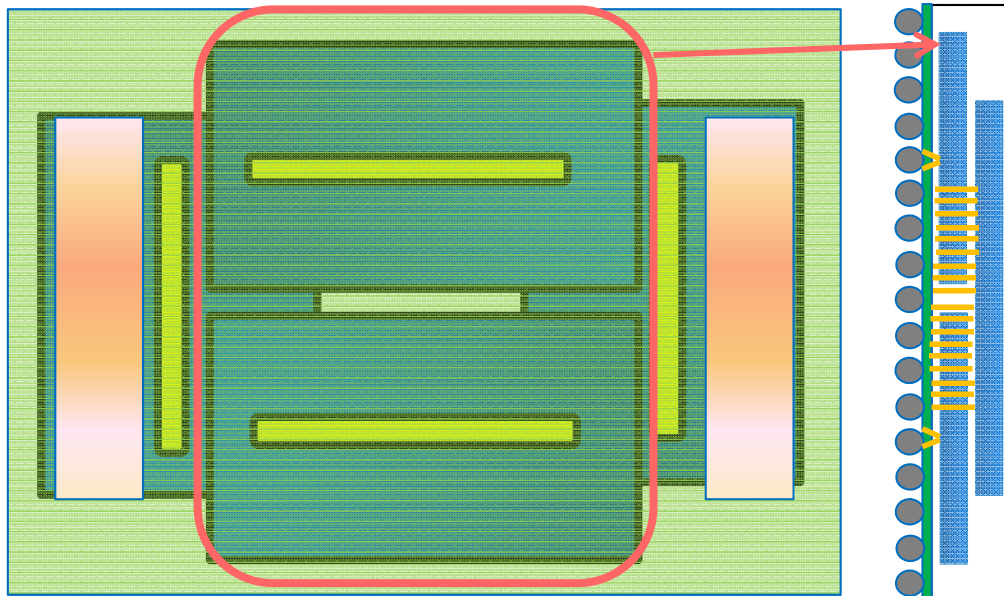
Invensas DFD and QFD DRAM Packages



Dual Face Down (DFD)
(side view)



Dual x4, dual x8 DRAM die:
104 balls: 11.5 x 11.5mm
Dual x16: 136 balls;
11.5 x 11.5 (0.8 x 0.65 pitch)



Quad-Face Down (QFD)
(bottom view/side view)

Quad x 8, Quad x 16 DRAM die:
16.2 x 16.2 mm, 256 balls
(0.8 x 0.8 pitch)

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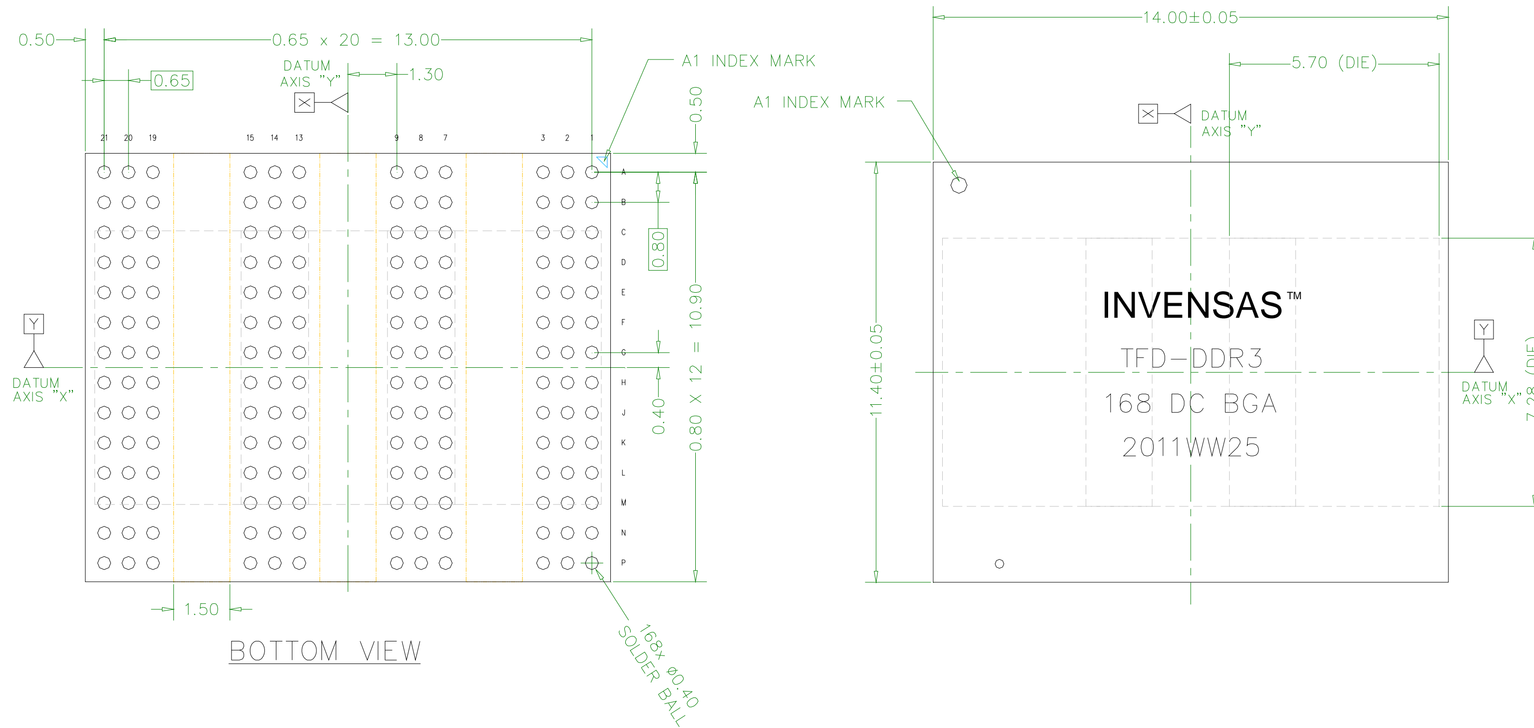
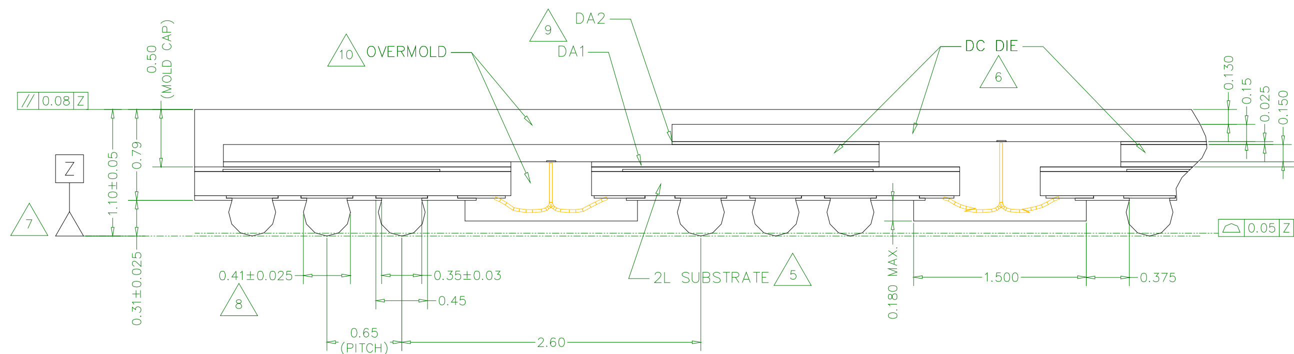
TFD (Tri-Face-Down) Package Test Vehicle

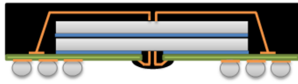
- 11x14 mm package with 3-devices; 0.65x0.80mm BGA pitch





Assembly Process Steps Comparison – DDP vs DFD

Opposing Face DDP



1. Print 1st adhesive
2. Place 1st die
3. Dispense adhesive
4. Place 2nd die
5. Wirebond 1st die
6. Invert Strip
7. Wirebond 2nd die*
8. Mold
9. Ball attach
10. Singulate

FOW DDP

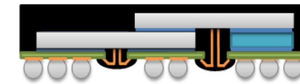
1. Print 1st adhesive
2. Place 1st die
3. Wirebond 1st die
4. Dispense FOW ***
5. Partial cure of FOW
6. Place 2nd die
7. Wirebond 2nd die
8. Mold
9. Ball attach
10. Singulate

***Costly material/ process

RDL DDP

1. RDL wafer**
2. Print 1st adhesive
3. Place 1st die
4. Wirebond 1st die
5. Dispense adhesive
6. Place spacer die
7. Dispense adhesive
8. Place 2nd die
9. Wirebond 2nd die
10. Mold
11. Ball attach
12. Singulate

Invensas DFD



1. Print 1st adhesive
2. Place 1st die + spacer
3. Dispense adhesive
4. Place 2nd die
5. *Single-pass wirebond*
6. Mold
7. Ball attach
8. Singulate

DFD offers consolidated assembly process with reduced material use resulting in less cost

Wafer RDL process

1. Dielectric Deposition
2. Mask , Etch Dielectric
3. Metal Deposition
4. Mask , Etch Metal
5. Dielectric Deposition
6. Mask , Etch Dielectric
7. NiAu plating

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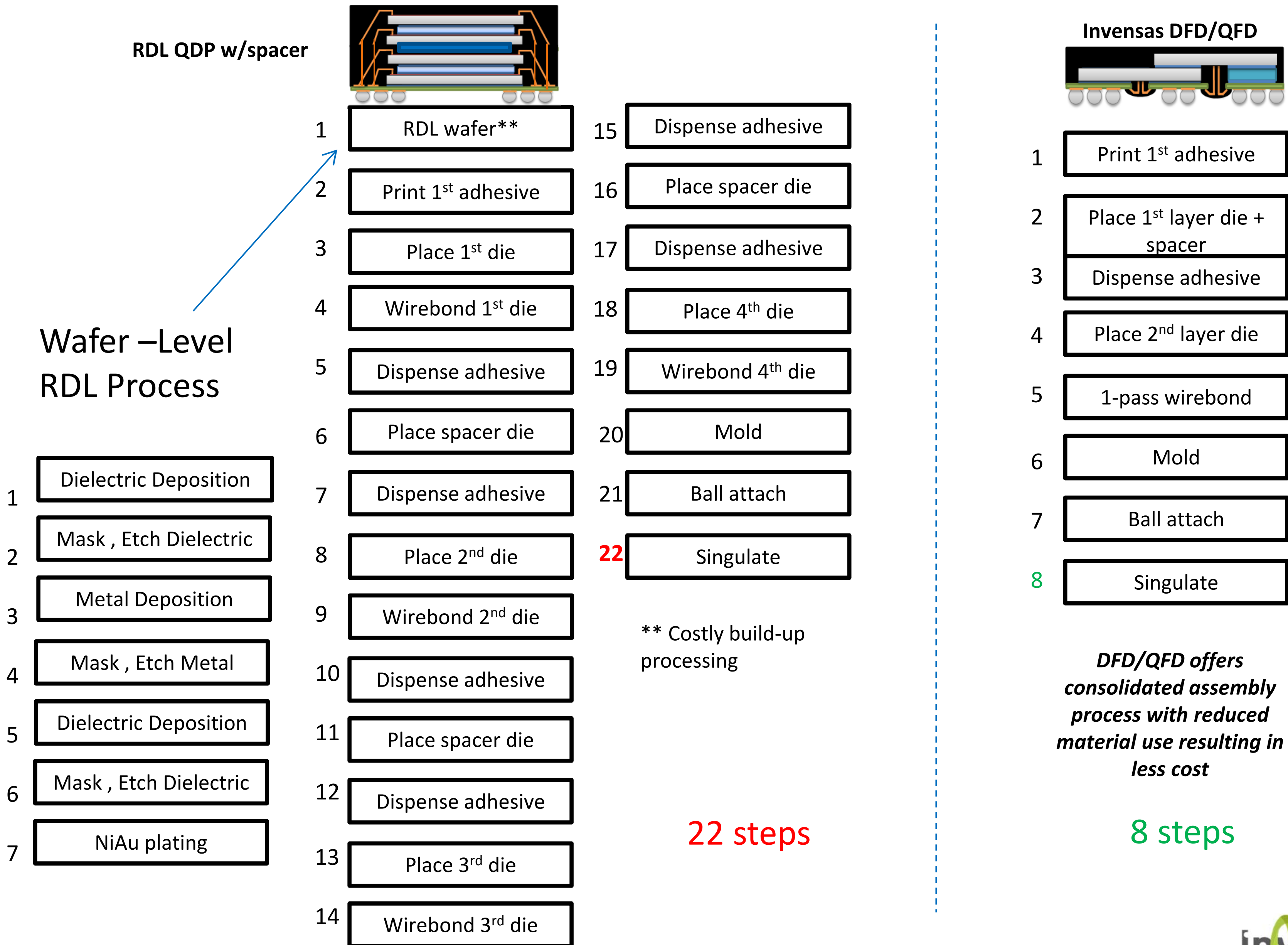
Assembly Process Steps Comparison – QDPs vs DFD/QFD



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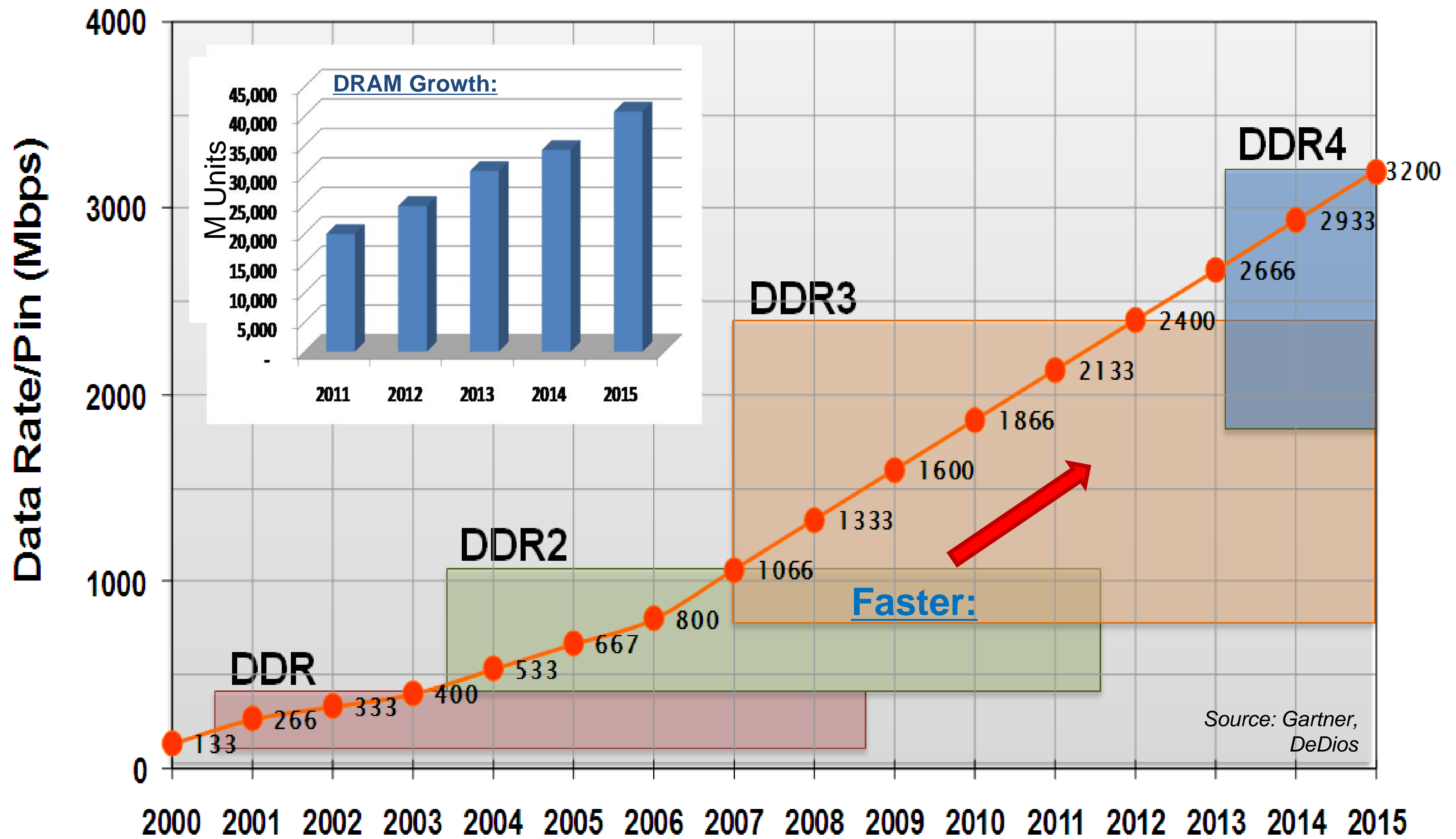
The DRAM Challenge: 2012-2017



xFD addresses performance and cost

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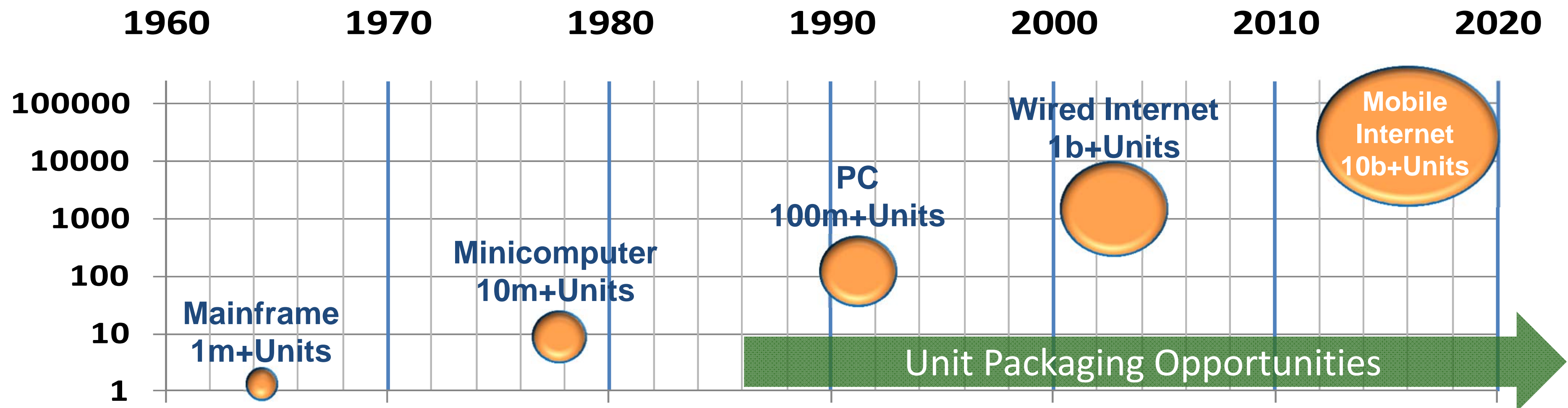
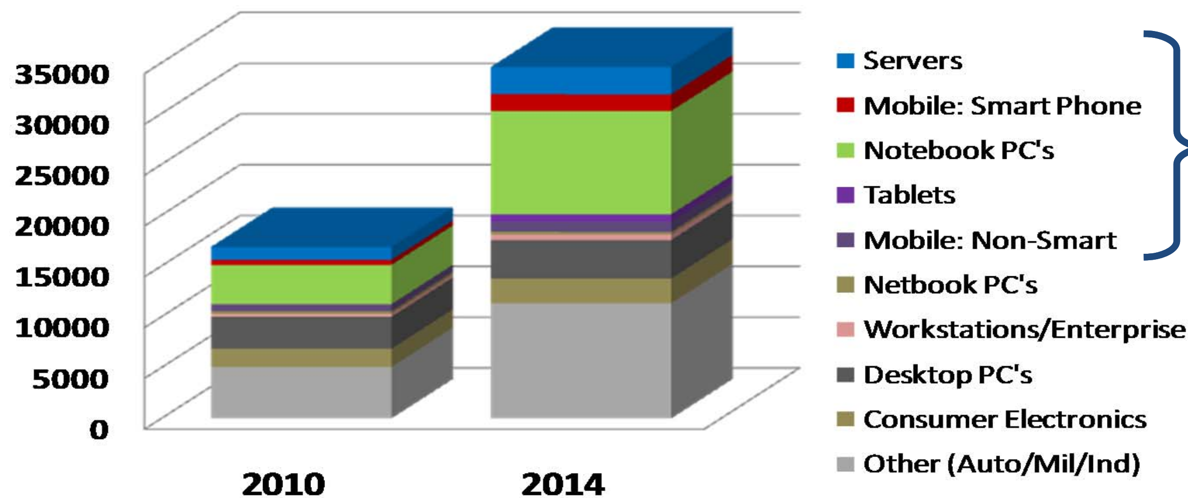
Mobile & Memory: Exponential Unit Growth





Focus on Growth:

Servers: 30.5% CAGR

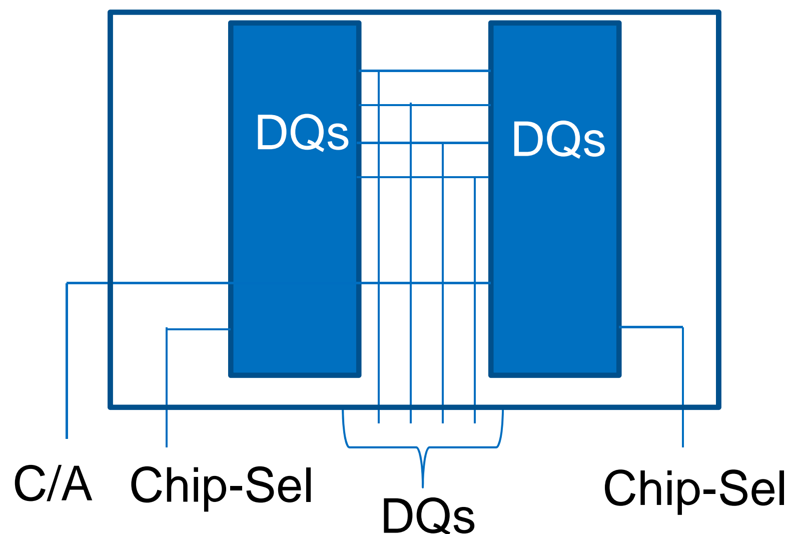
Smart-Phone: 34.5% CAGR

Tablets: 67.1% CAGR

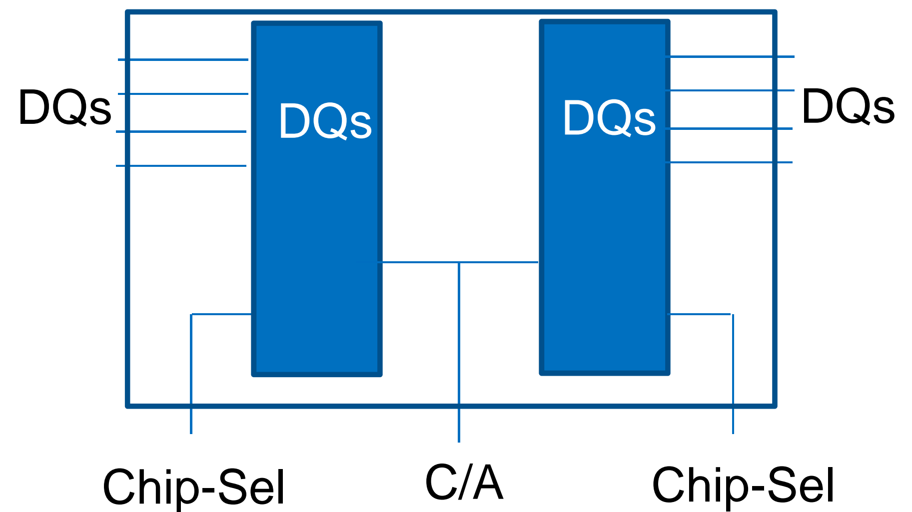
Source: Gartner Q1.11
Data in Millions of Units

Faster: Bandwidth (Wide-IO) Expansion

Conventional DDP
(Depth Expansion, Common DQs)

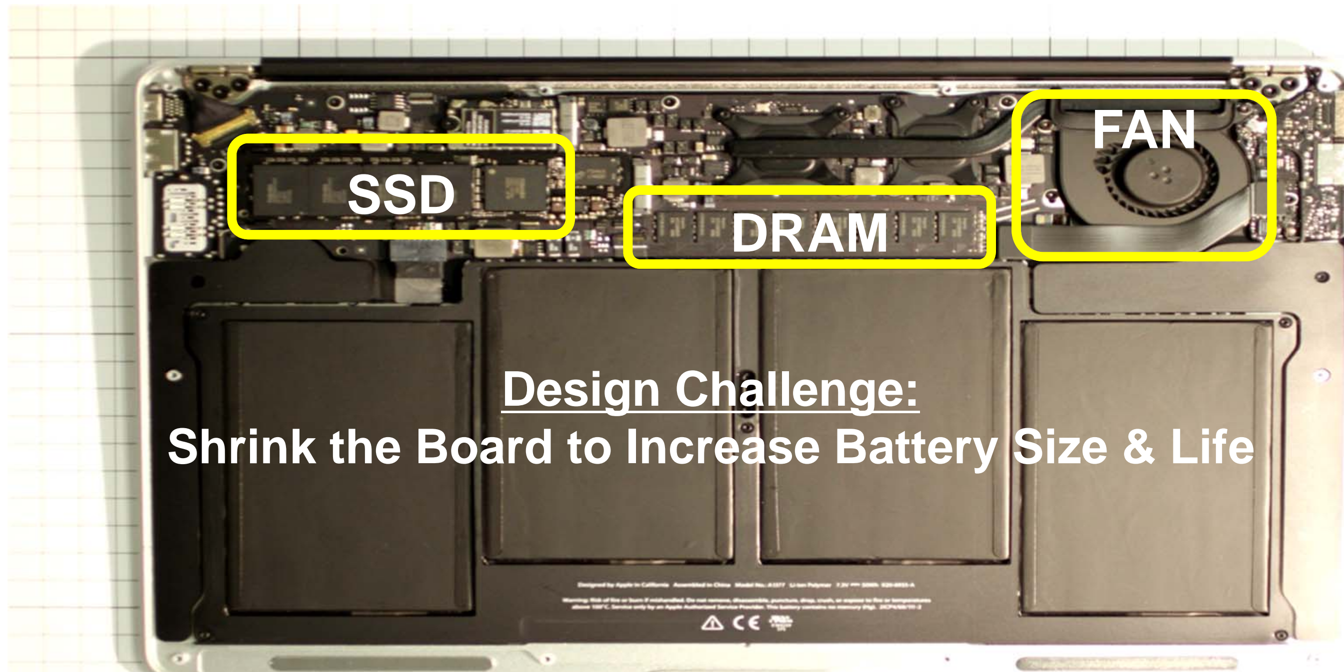


Width-Expanded DDP
(Bandwidth Expansion via Separate DQs)



- **xFD technology accommodates conventional "Depth Expansion" but uniquely is also designed for "Bandwidth Expansion" or Wider-IO.**

Denser: "Ultra-Book" Memory Form-Factor



Existing Solution: SO-DIMM

SO-DIMM in a Package

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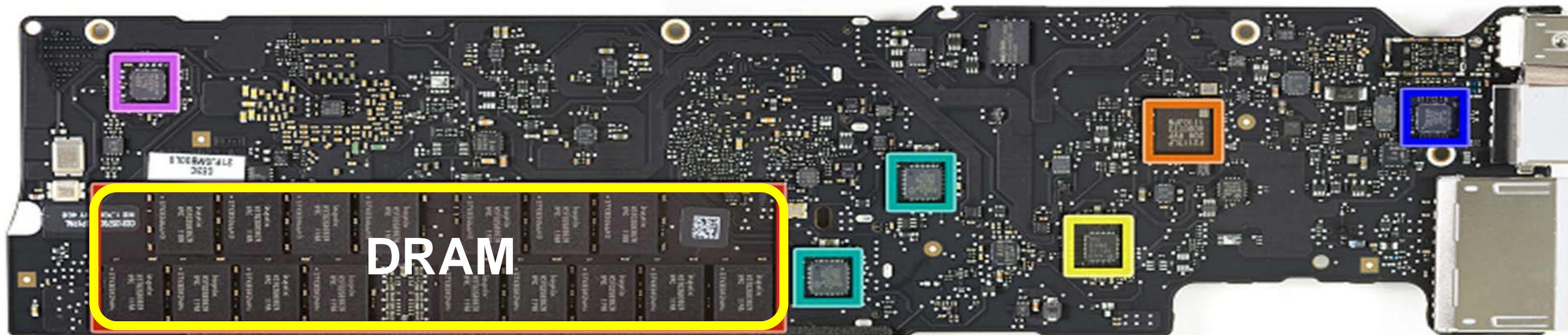
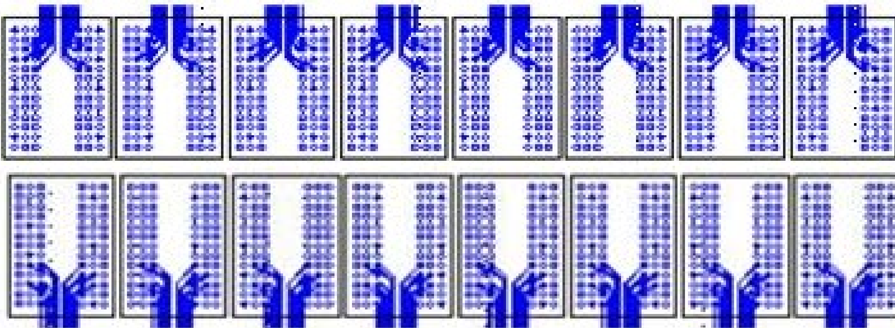
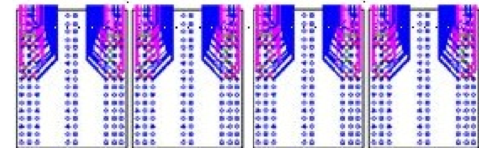
Denser: Substantially Reduced PCB Footprint



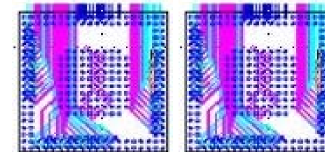
Single Die Package PCB Footprint



Dual Face Down



Quad Face Down



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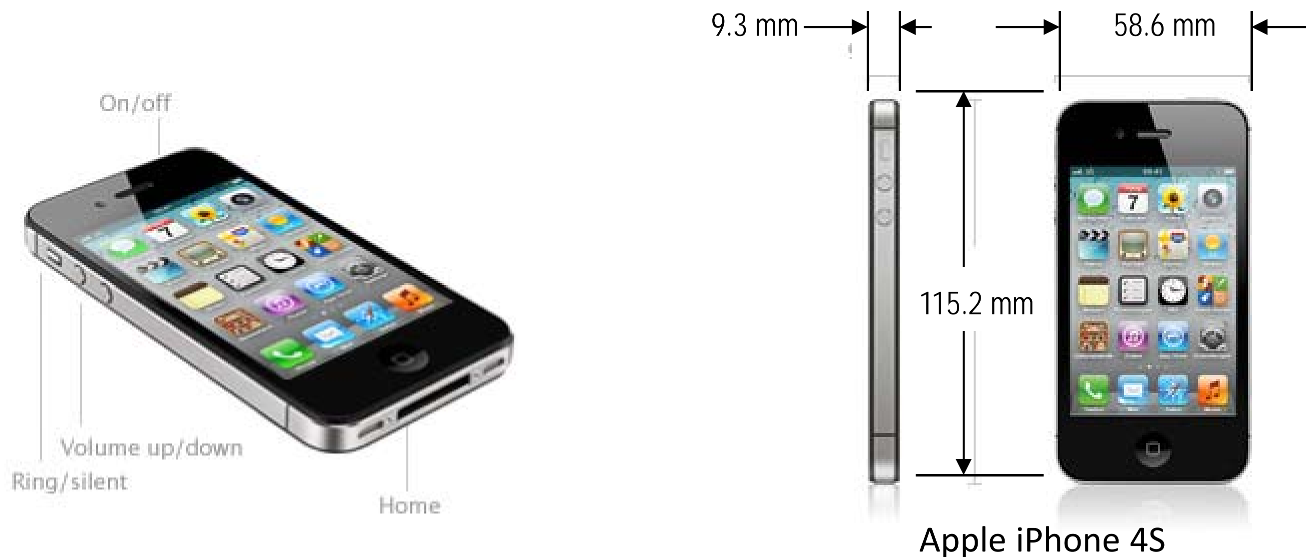
Package Profile Concerns

- Excessive package height can be a critical roadblock for a number of electronic products.

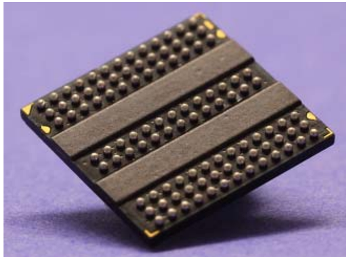


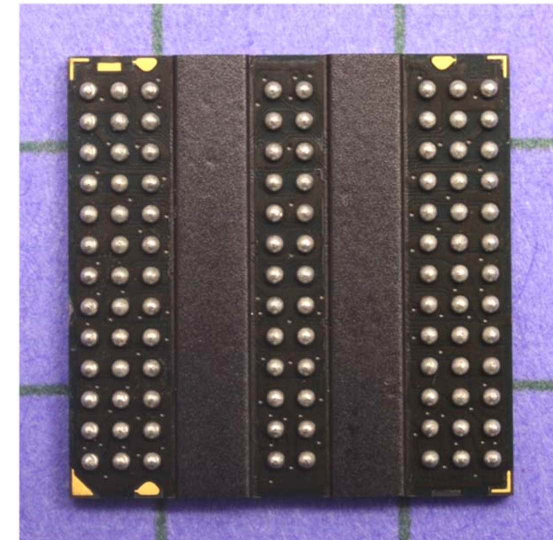
Apple iPhone 4S

- Even though the die elements can be made very thin, the accumulated stack-up height of the resulting package assembly may not be acceptable for specific product applications.

Example source: Apple, Inc

Summary of xFD Technology: Denser, Faster, Cheaper





- ***Denser*** than single die packaging
  - Two die in the footprint of one
  - Smaller PCB footprints for given memory capacity
  - Thinner package with no topside wire loops
- ***Faster*** than conventional double die packaging
  - Single die performance in Double Die Package
  - Streamlined PCB layout, better electrical design optimization
  - Significantly improved thermal characteristics
- ***Cheaper*** than conventional DRAM packaging
  - xFD: lowest assembly cost per DRAM die for single, double and quad die packages
    - Simplified process flow: fewer process steps
    - Minimal gold usage
    - No expensive redistribution layer process (RDL)
    - Manufactured on existing wirebond lines
  - Significantly improved split yield to higher frequency bins

Thank you