SMTL™ ,Advanced Transmission Lines for High Speed 3D Packaging Applications

Advancing the High Speed Interconnect Ecosystem…™

For MEPTEC

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Overview

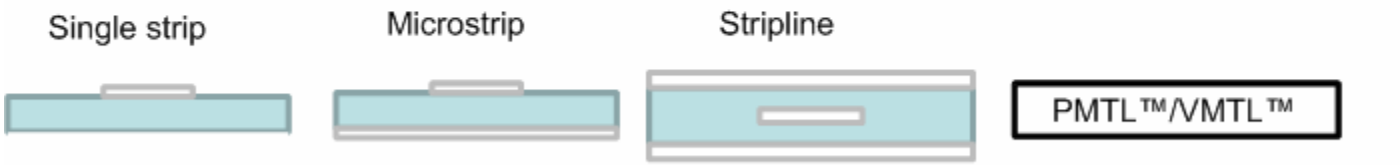
- Disruptive technology Patent Pending
  - PMTL™ , Periodic Micro Transmission Lines
  - VMTL™ , Via Micro Transmission Lines
  - SMTL™ , Shaped Membrane Transmission Lines

High Speed Packaging Challenges

- Wire Bonding Is
  - Limiting High Speed Performance
  - Limiting Die Stacking
- Need One time Multi die Bonding Process
- Signaling is approaching microwave and millimeter wave spectrum.
- High Speed Digital signals limited by traditional plastic packaging…

Transmission lines

EVOLUTION OF INTERCONNECT STRIPS FROM SIMPLE TRACE TO MORE ADVANCED FULL BANDWIDTH TRANSMISSION LINES

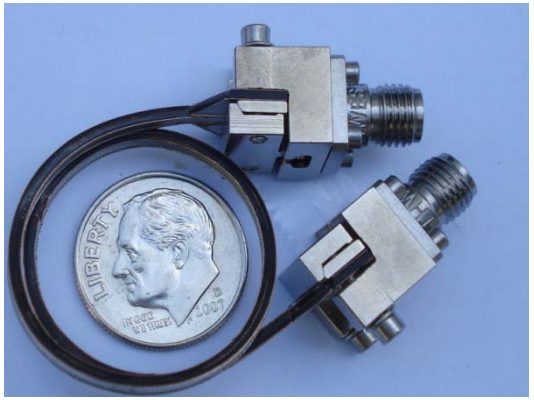


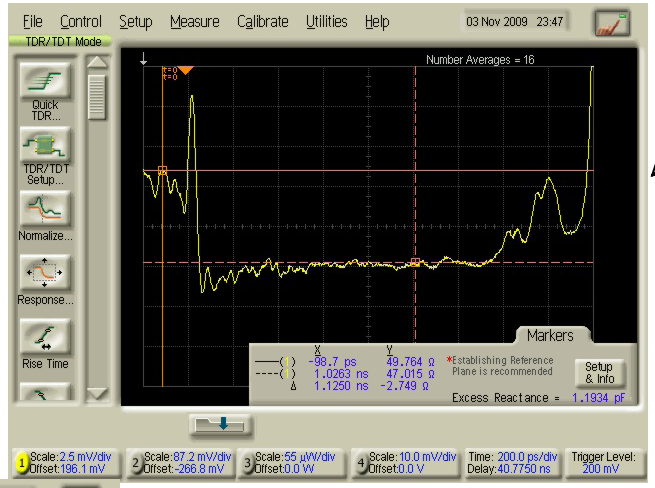
Wire bond like coonection

Transmission lines currently used in CMOS, Packaging, and PCB industry

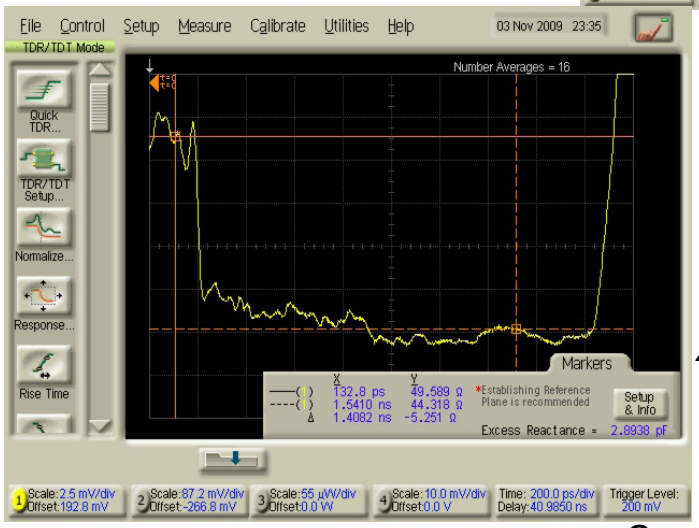
Advanced Transmission Lines

PMTL™ on Flex, TDR,

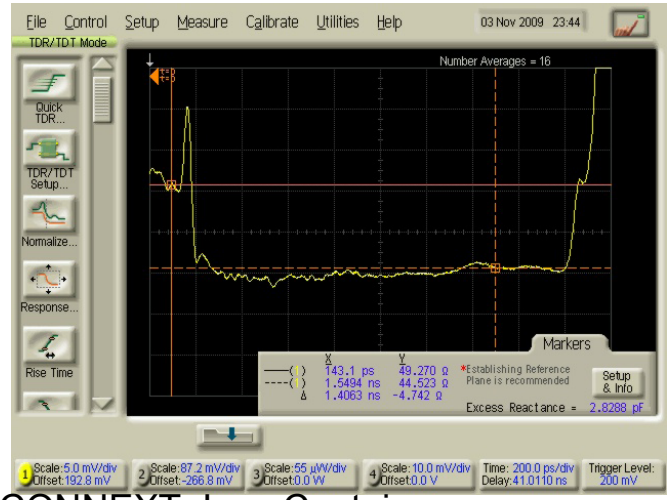




6”, 3 Layer PMTL, designed for 20GHz, Kapton, SMA Connectors, Sample S1



6”, 4 Layer PMTL, designed for 50GHz, Kapton, 2.92mm Conn., Samples 1A and 3A



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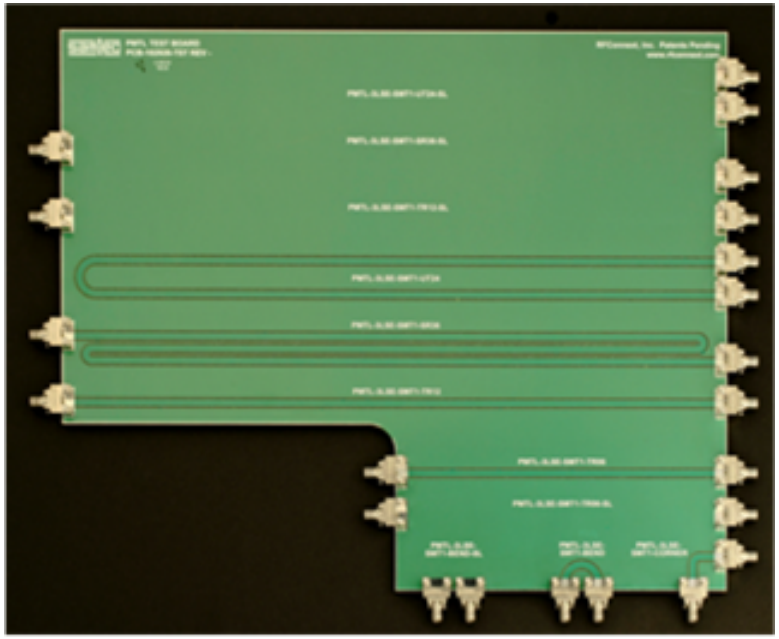
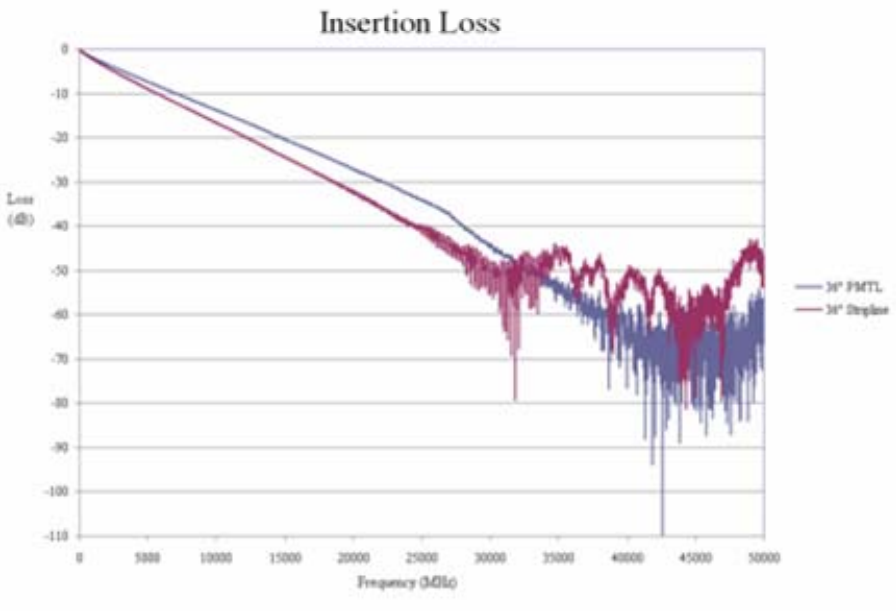
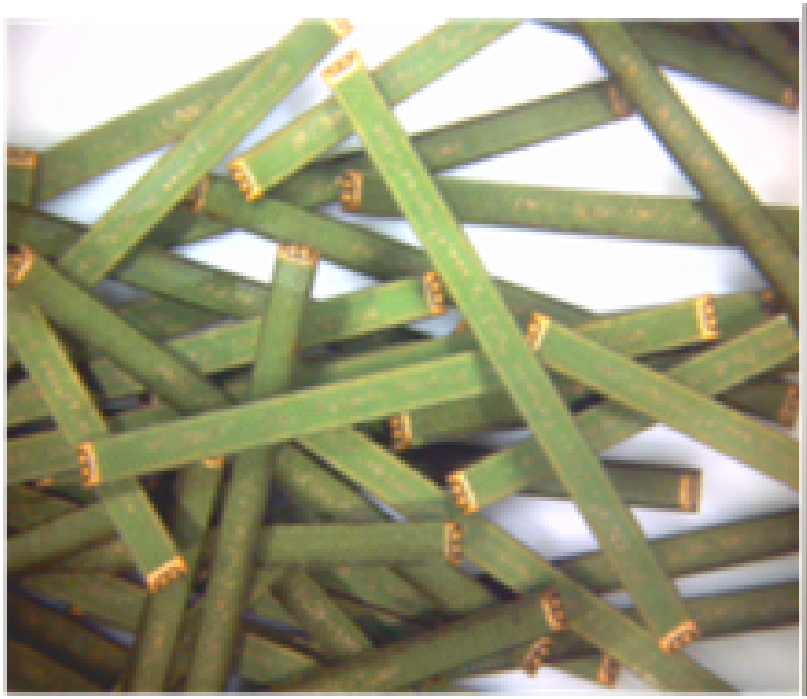
PMTL™, On FR4

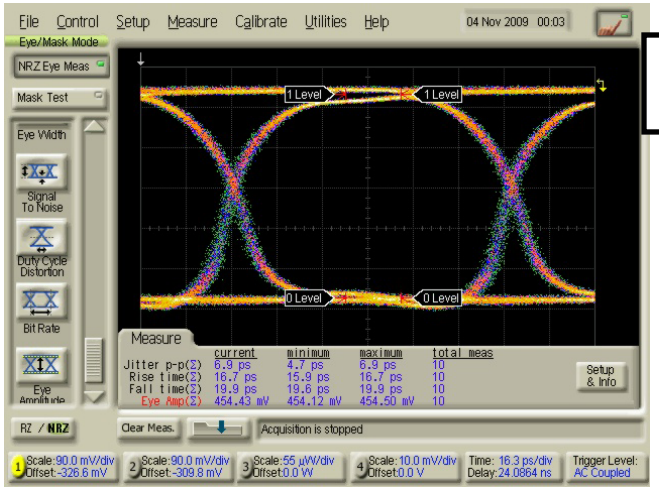




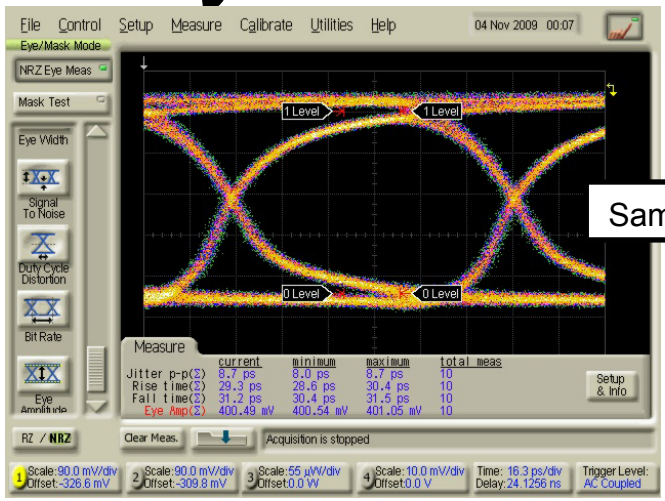
SMTL™,



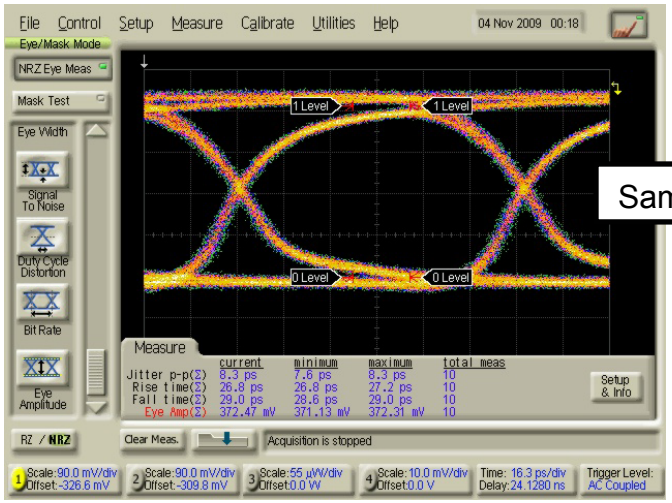
10Gbps,6” PMTL’s Samples 1S, 1A, and 3A Eyes



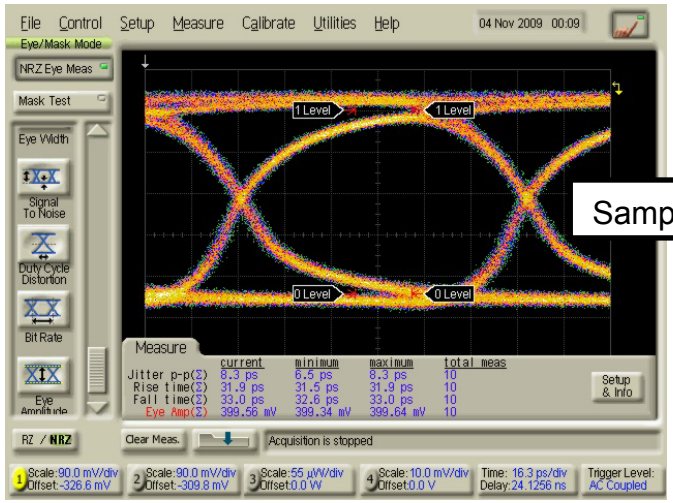
Ref. TP1 Instrument



Sample 1A



Sample 1S



Sample 3A

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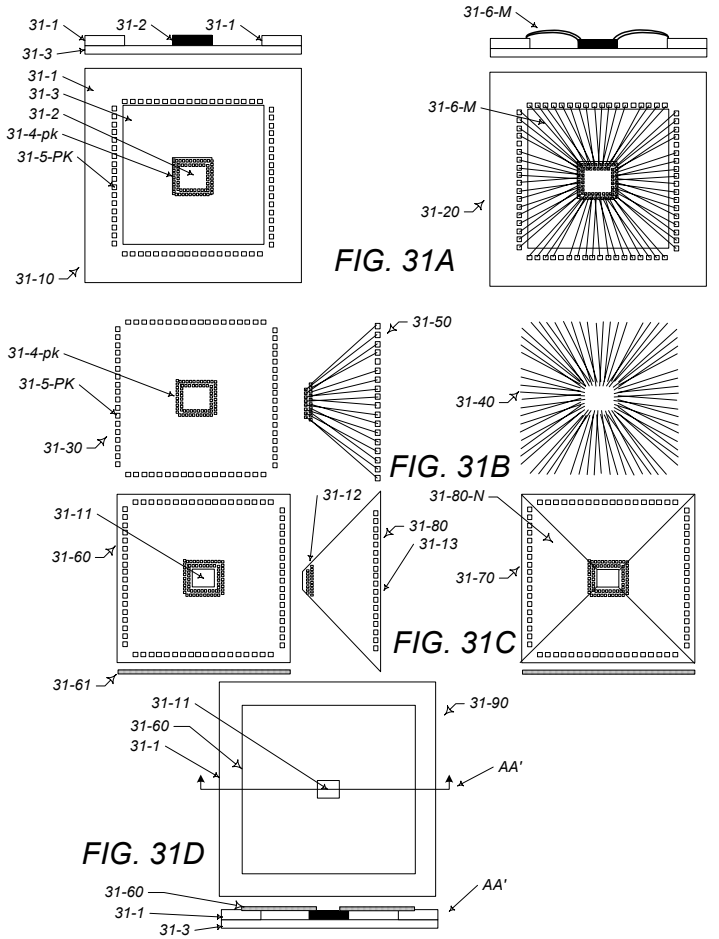
Patent Pending SMTL™ Shaped Membrane Transmission Lines

- Total High Speed Packaging Interconnect Solution
- Match the bumps on Chips to Fan out bumps on package
- Multi-layer Membrane PMTL™ arrays up >100GHz
- Single Action bonding/Adhesion
- Reliable/Shaped



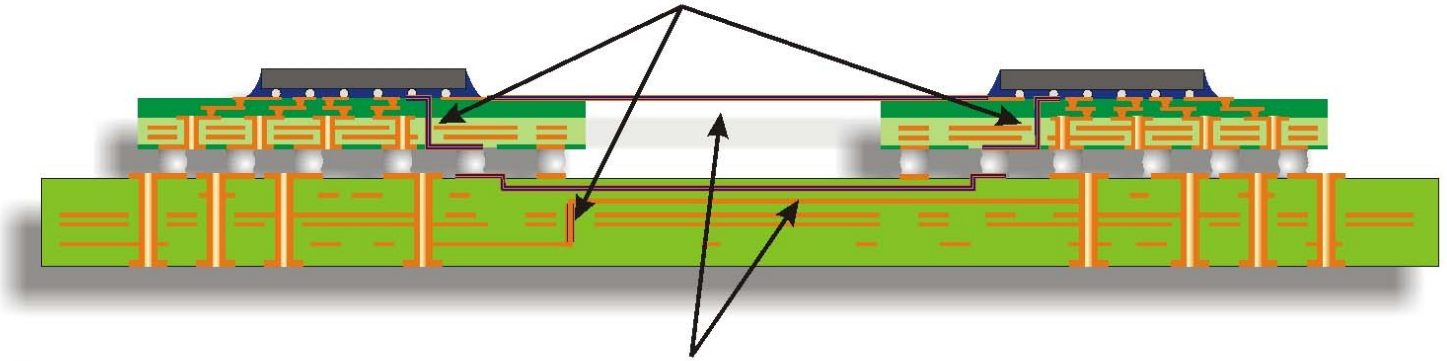
SMTL™ supports/improves

- Flip Chip, Micro bumping, Wafer thinning
- SiP (System in Package)
- SxS (Side by Side Package)
- PoP/PiP (Package on Package, Package in Package)
- PuP (Package under Package)
- MCM (Multi Chip Modules)
- Extends Bandwidth and High Speed limits…
- The Sky is the limit…

3D IC Packaging using PMTL™/VMTL™/SMTL™

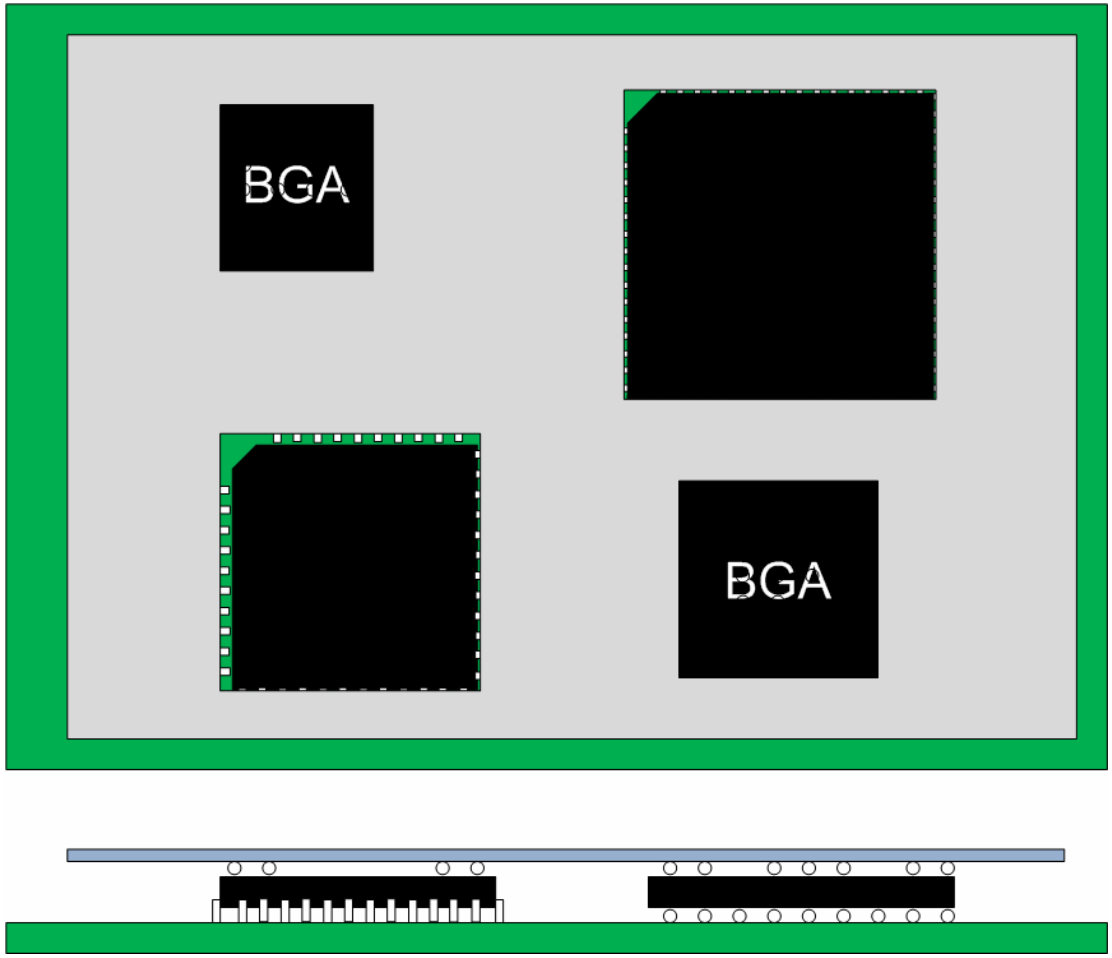
From joint paper with Joe Fjelstad, at PCB007.

Embedded VTML interconnections through package and in PCB

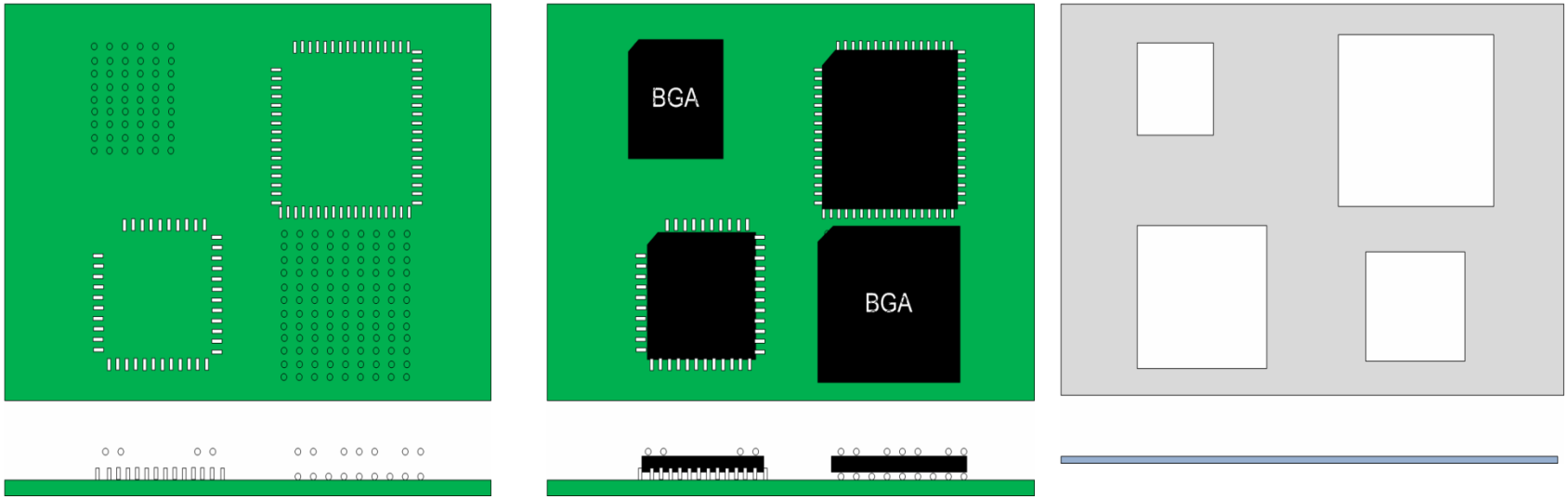


OTT and embedded PTML interconnections between chips and packages

SMTL™, Shaped Membrane Template with embedded PMTL™/VMTL™



Various Layers of SiP, Package System



Some Advantages of SMTL™(1)

- Matching Length, no Skew due to Bonding
- Controlled Impedance
- No Parasitic Inductance
- No significant Length Limit
- Confined Field, TEM Transmission Lines
- Full Bandwidth
- No Cross Talk
- Noise immunity
- Reduced Power Loss
- No EMI/EMC/ issues

Some Advantages of SMTL™(2)

- One time Connection,
  - Reflow Solder, Epoxy micro bumps, die/membrane attachment, stacked
  - Thermo-sonic or Tap bounding
  - Thermo-Compression Bonding, single tool
  - Using existing Die/Wire Bonding machines
- Precise Z Control, Skyscraper stacking
- Accommodates uneven Bonding Pad Levels

Some advantage of SMTL™(3)

- No more Wire bond stitching…
- Uses 90% Less Metal Use, Au,Ag, Cu..
- More precise control of routing and Placement
- Use inexpensive PCB layout/Fabrication precision
- Precise control of Pitch, uniformity
- Deployable in large scale arrays
- Can be mass manufactured with existing PCB/Packaging Processes
- Scalable

Example for High Speed Packaging

DC-70 GHz Die to Package Interconnect

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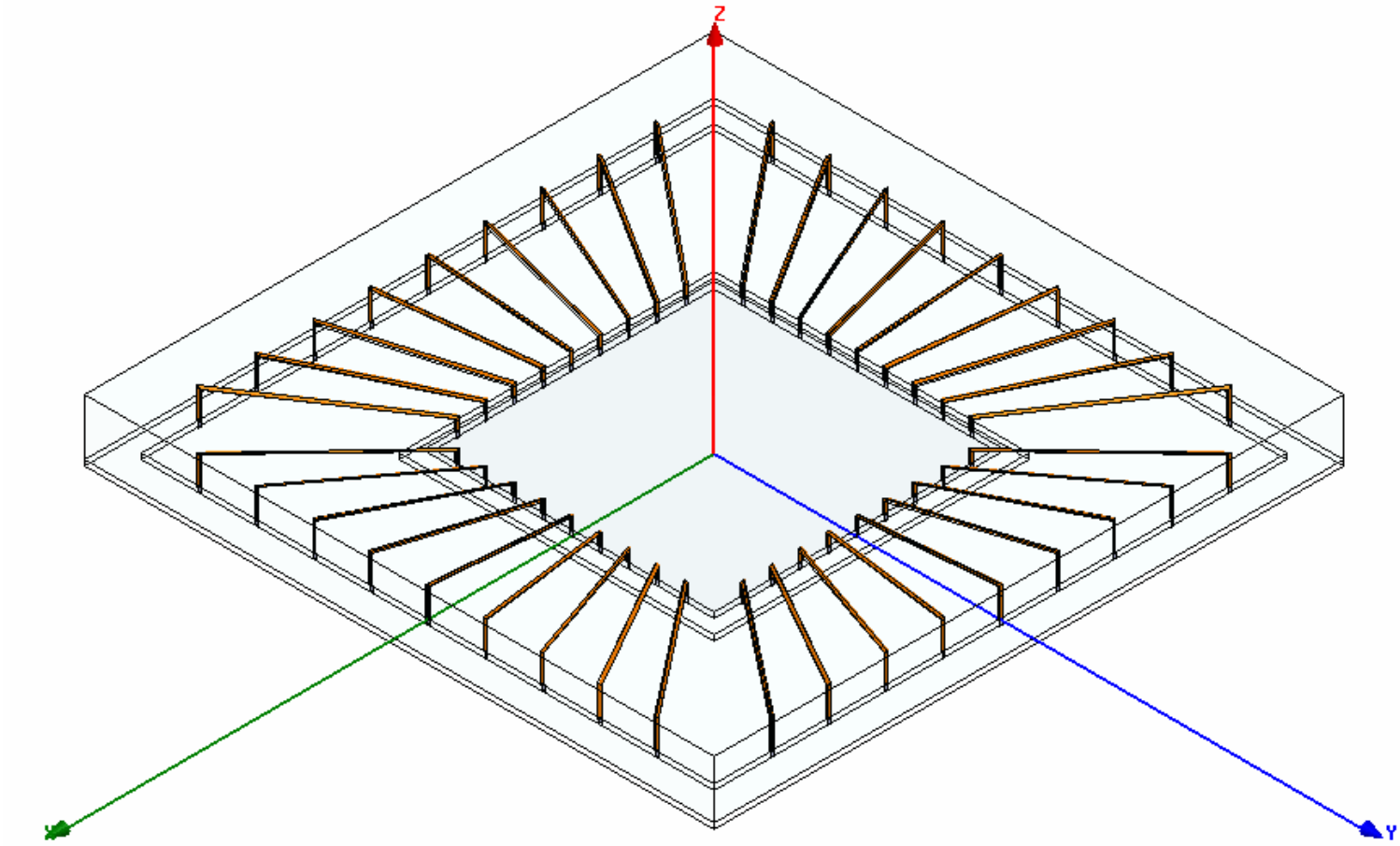
Comparison

- Electromagnetic(EM) Field Simulation of a Typical High Speed Electronic Package at 10GHz
  - With traditional Gold Wire bonds
  - With SMTL™ Interconnects, replacing the Gold Wirebonds

Basic Information

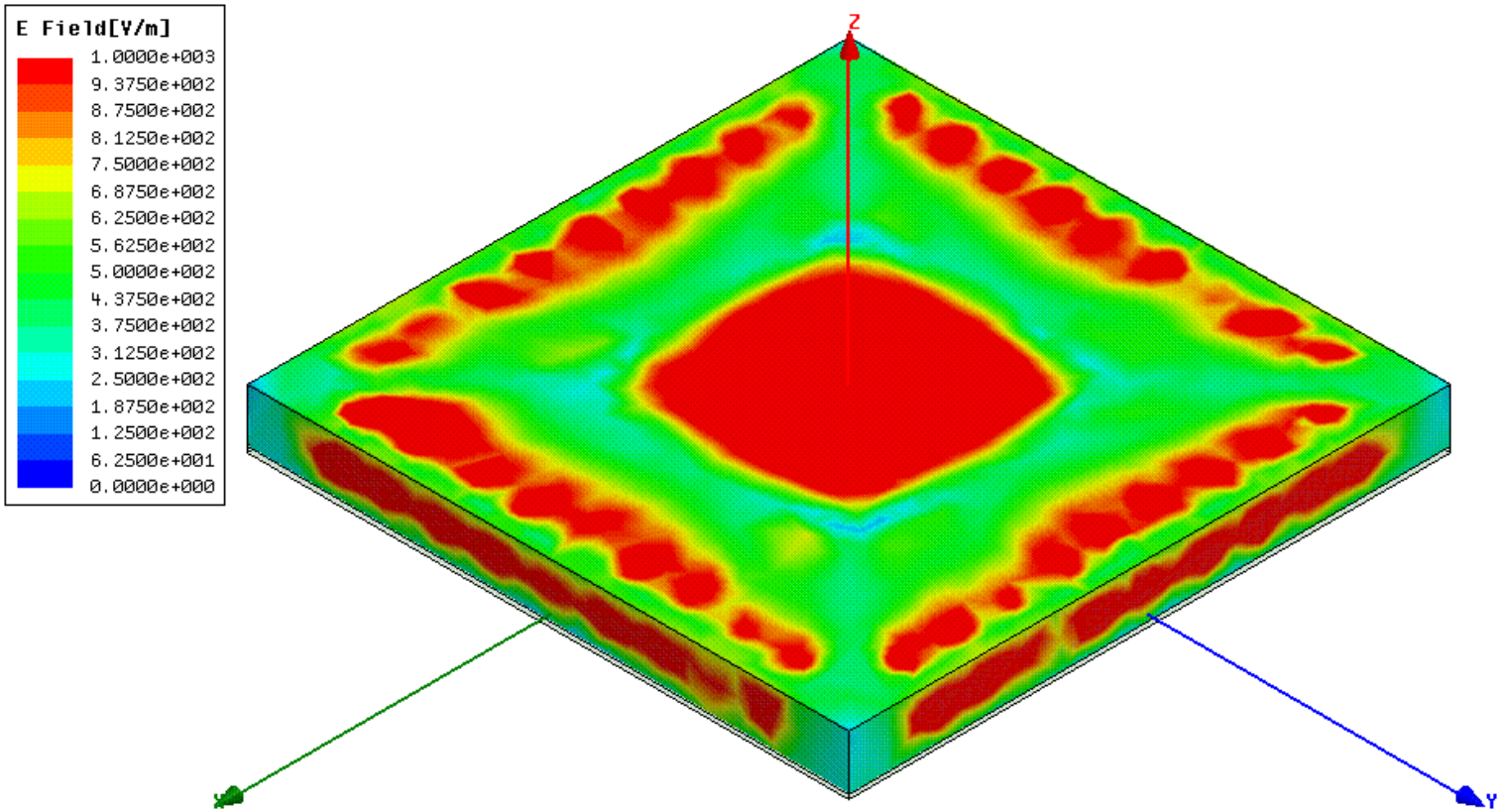
- A 5mm die is attached to a 10mm package
- Magnitude of Electric Field is displayed on the epoxy resin surface
- The scale for all simulations are 0-1000v/m, linear display(except as noted to zoom in)
- There are 9 wire bonds, on each side, each with 2 i/o ports
- 1W power is distributed equally in all ports, for display comparison

Geometry of Package with Gold Wire Bond



Magnitude of E Field, on Package, With Gold Wire Bonds

(animated)



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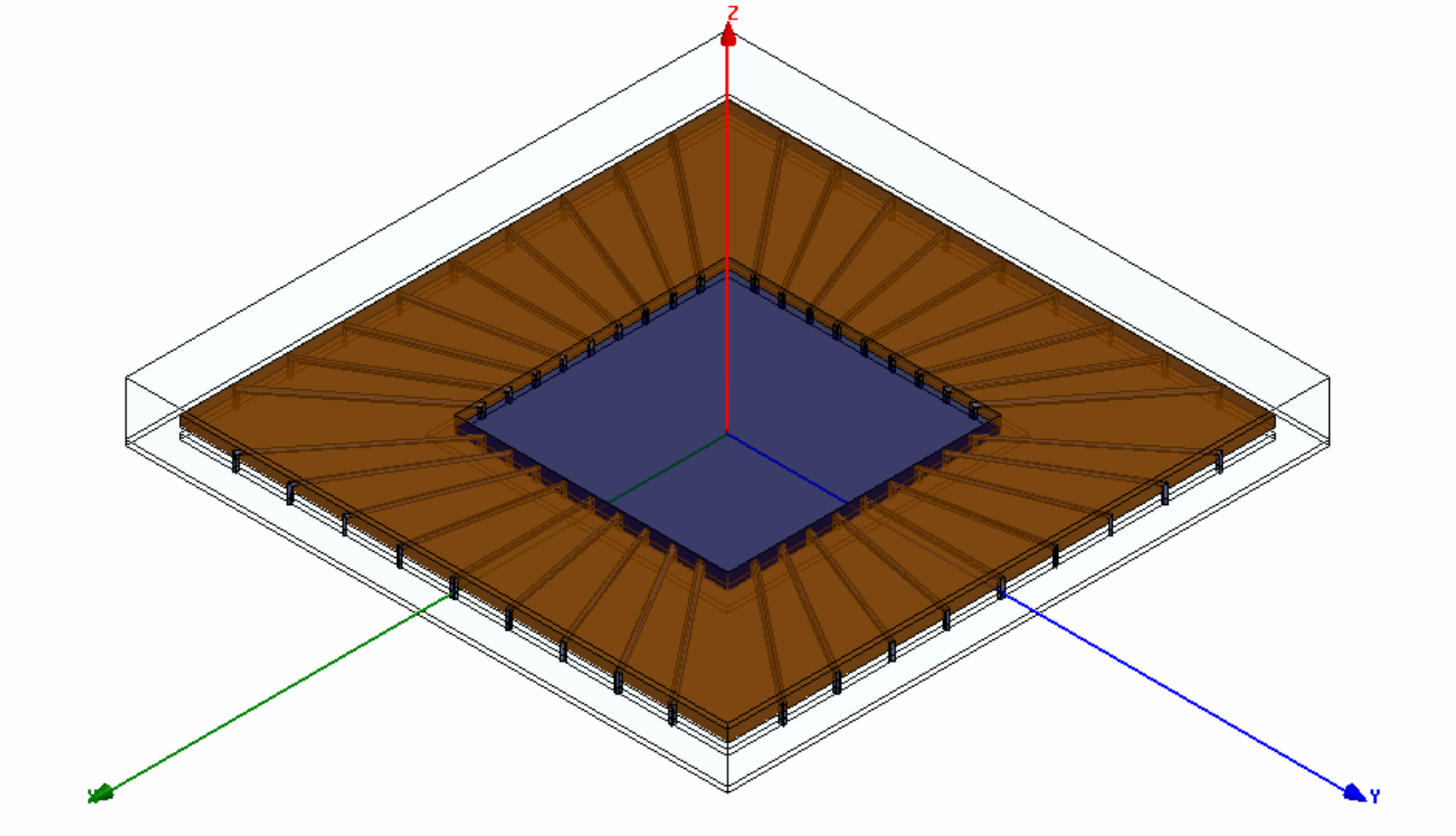
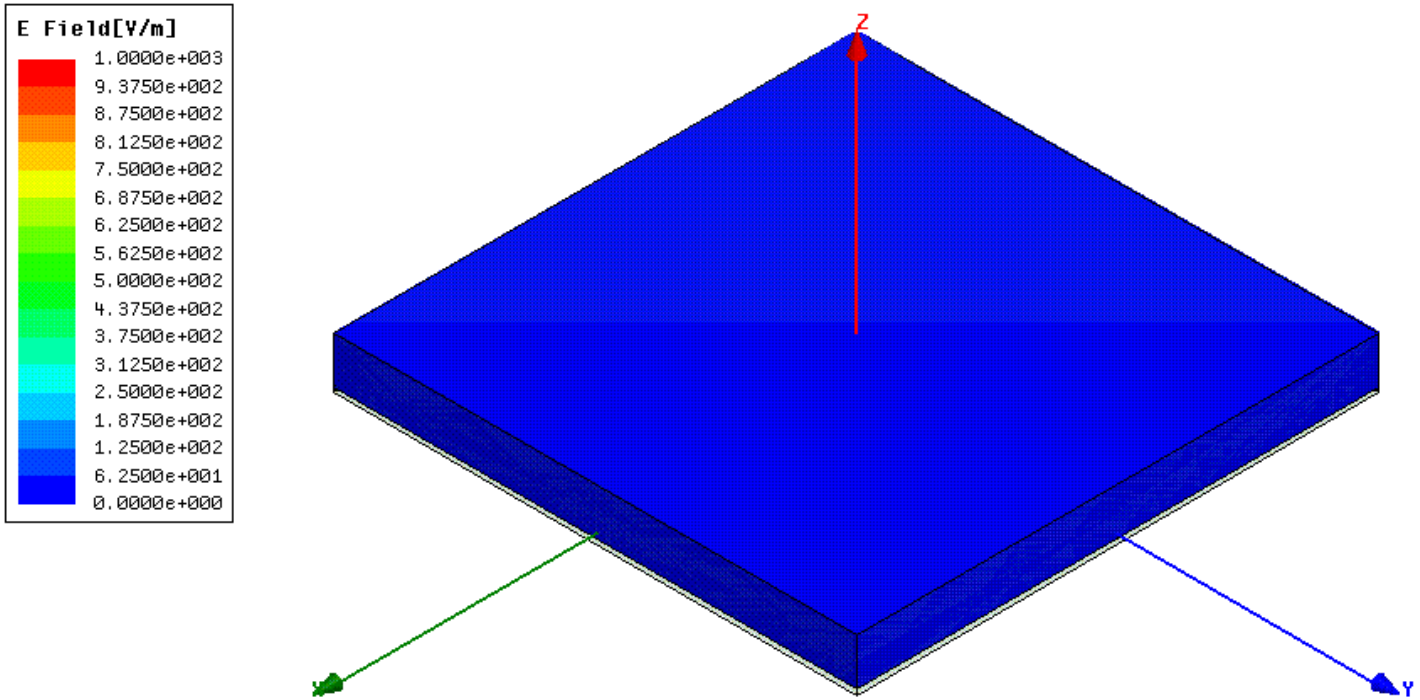
Geometry of Package with SMTL™ interconnect



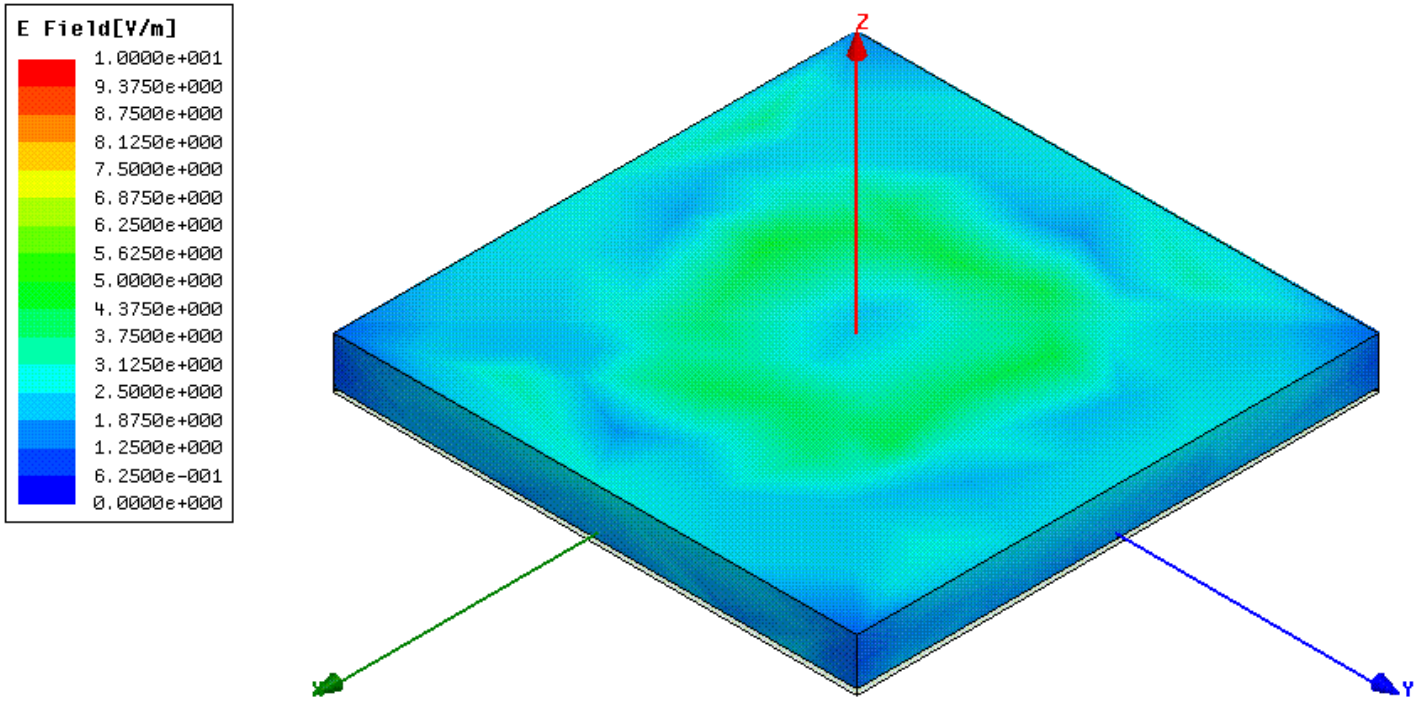
Magnitude of E Field, on Package, With SMTL™

(animated, at same scale, too small to see)



Magnitude of E Field, on Package, With SMTL™

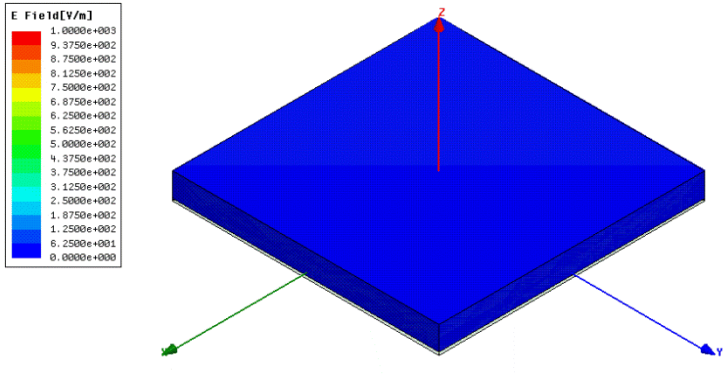
(animated, scale reduced by 100x to see low fields of SMTL™)



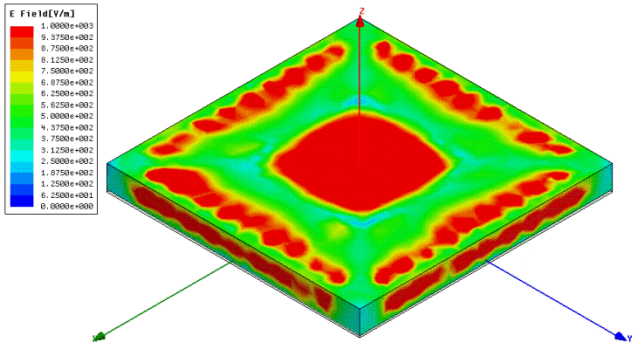
Side by Side Comparison of SMTL™ and Wirebond

(animated)

Scale 0-1000



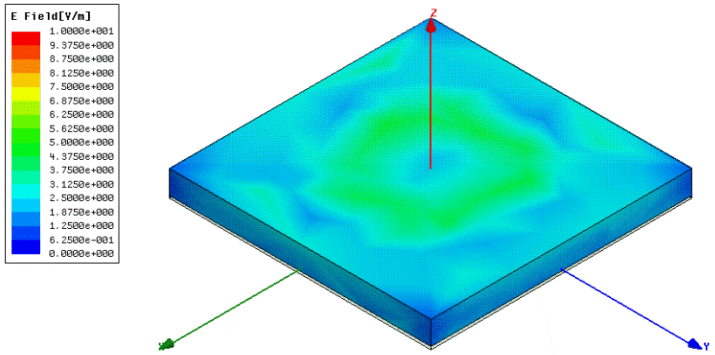
Scale 0-1000



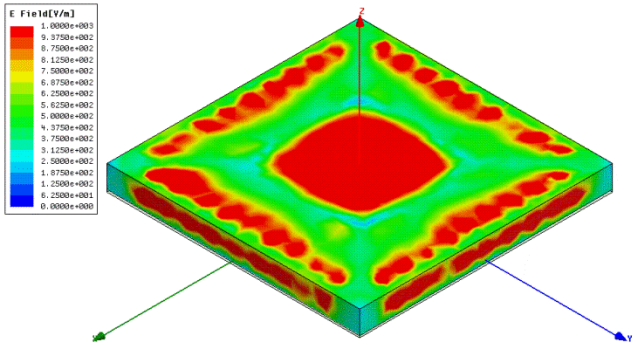
Side by side Comparison of SMTL™ and Wirebond

(animated)

Scale 0-10



Scale 0-1000



No Need for Ceramic Packages to Achieve High Speed

With SMTL™, inexpensive PCB materials and plastic molding encapsulation can be used

Conclusions

- Traditional Wire bond
  - Is open field, has parasitic
  - No impedance control
  - Has high crosstalk
  - No noise immunity
- SMTL™ interconnect
  - has confined fields, no parasitic
  - Has perfect impedance control
  - Has very low or no crosstalk
  - Has high noise immunity
- Wire Bonding Can be Replaced by SMTL™ interconnect
  - Uses 90% less precious metal and copper.
  - Can be implemented for mass low cost manufacturing…

More on SMTL™

You may ask yourself!

I work with only a few Gbps, is SMTL™ an overkill???

SMTL™ Can Also be used at low frequencies and at low data rate too…

READ ON…

Example for Memory Stacking

TSV (Through Silicon Vias)

Are Expensive, for most multiple die stacking to Achieve “More than Moore”

Patent Pending SMTL™ Can server is an inexpensive PCB alternative solution…

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EXAMPLE: SMTL™ for uSD(1)

- SMTL™ can be made as thin as die
  - Can be used for interconnect
  - Can be used for spacer/support/die attachment base
- X,Y,Z, die dimension, 400u x 200u x 25u
- Support thinner polished die, 10u instead of 25u
- Chip is fully supported, no die hangover or breakage
- No more wire bond loop height issues
- Increase the capacity of a single uSD ,
  - 16GB capacity, by stacking of 8x16Gb dice
  - 32 GB capacity, by stacking of 16 x16Gb dice
    - But with almost same stack height
- This Process Could be extended by SMTL™
  - To provide even 64GB , 128GB, 256GB, ultimately limited by MC(Memory controller chip???), and other components…

EXMAPLE: SMTL™ for uSD(2)

- For SxS, SMTL™ can achieve at least a 2x2 array (For uSD and TOP package)of above chips stacks thus providing 4x 32GB=128GB or 4x 64GB=256GB (depending on the die size)
- SMTL™can mitigate thermal issues too by use of thermal vias…,
- SMTL™ eliminates height limits and die breakage due to WIRE BOND…
- The size and location of MC control chip can be optimized
- The loss and thermal effect of epoxy resin could be reduced, or ultimately eliminated.

Authors Biography

- Jamal S. Izadian, Ph.D. : Dr. Izadian is the cofounder and president of RFCONNEXT, Inc., As member of a development team, he has been instrumental in designing and promoting a new high speed interconnect ecosystem, using new TEM transmission line technologies. He is the innovator of the patent pending PMTL™, VMTL™, and SMTL™ transmission line technologies which are designed to mitigate the shortcomings of the modern interconnects systems to 50GHz and beyond. Prior to RFCONNEXT, Inc., Dr. Izadian was cofounder and CTO, and Later CEO of ANTENNEM COMMUNICATION,LLC, In this capacity, Dr. Izadian helped establish the company as a leading antenna development and engineering services company in the wireless industry. He has seven issued patents, and six pending. He is the author of numerous technical articles and conference presentations, including the book “Microwave Transition Design” published by Artech House. He obtained his BSEE from University of KY, MSEE form Ohio State University, and Ph.D. in EE with emphasis in Electromagnetic/Antennas, and Radio Communication, from Ohio State University. He finished a year of MBA programs at Santa Clara University’s Leavey School of Business.