Stacked Silicon Interconnect Technology (SSIT)

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Agenda

- Background and Motivation
- Stacked Silicon Interconnect Technology
- Summary
Background and Motivation
Background: FPGA

- **Building Blocks**
  - Configurable Logic Block (CLB)
    - Configuration memory
    - Programmable switches
    - Interconnect drivers
  - Hard IP (DSP, EMAC, etc.)
  - Block RAM
  - Configurable IOs
  - High-speed transceivers

Programmable SoC of logic, memory, and analog circuits
Customers Are Asking for More

• More than 2X today’s logic capacity…

• Many more high-speed serial transceivers…

• Many more processing elements…

• Much more internal memory to store data…
Insufficient IO Scaling

- Growing gap between number of logic gates and I/O
- Technology scaling favors logic density

Gates and Number of IOs

15x drop in I/O-to-logic ratio by 2020

Number of I/O per 1000 logic cell in the largest FPGA in each family

~60x decrease in I/O-logic ratio
Package Technology is Limiting

- **The packaging chasm:**
  - Two orders difference in package trace/width vs silicon metallization: connection BW is limited
  - I/O also isn’t scaling due to bump pitch and chip to chip loading issues
  - Leads to increased area, power and complexity

- **Board chasm is even worse…**

![Graph showing package via diameter, package trace width, and chip top metal dimensions over time from 2005 to 2010.](image)

- Pkg via dia
- Pkg trace width
- Chip top metal

To scale in X dimension

Major “gearing” problem
Challenge 1: Availability and Capability
Largest FPGAs only viable later in the life cycle
Challenge 2: Power and Bandwidth
Traditional mitigation techniques are no longer adequate

Chip-to-Chip via
Standard I/Os and SerDes
More total gates, sooner, but...

Resources Not Scaling
1. Not enough I/Os
2. I/O latencies too high
3. Wasted I/O power

Innovation Needed
Introducing Stacked Silicon Interconnect Technology
High Bandwidth, Low Latency, Low Power

Xilinx Innovation

- Massive number of low latency, die-to-die connections
- Earlier in time
- No wasted I/O power
- Over five years of R&D

Delivers the Best of Both Worlds: High and Usable Capacity
Enables High Bandwidth, Low Power FPGA to FPGA Connectivity

100x bandwidth / Watt advantage over conventional methods
Delivers Resource-Rich FPGAs

Largest Device with Transceivers

Logic Cells

- Xilinx
- Nearest Competitor

90nm, 65nm, 40nm, 28nm

3.5x, 2.8x
For the Most Demanding FPGA Applications

Next Gen Wired Communications

Next Gen Wireless Communications

High Performance Computing

Industry’s Highest System Performance and Capacity

Aerospace & Defense

Medical Imaging

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Summary

- **SSIT Addresses IO Bottleneck**
  - 100X lower BW/W over traditional IOs/SerDes

- **Can offer Next Generation Density Now**

- **SSIT Platform Enables**
  - Optimal Partitioning
    - Digital and analog blocks
    - IP/IC reuse
  
  - Heterogeneous Integration
    - Digital, mixed signal, & optical
    - FPGA & memory
Stacked Silicon Interconnect Technology

- Technology Overview
- Design & Implementation Flow
- Path to Production
Xilinx FPGA Architectural Innovations
At the Heart of the Technology

ASMBL Optimized FPGA slice

FPGA Slices Side-by-Side

Silicon Interposer:
>10K routing connections between slices
~1ns latency
Harnesses Proven Technology in a Unique Way

Microbumps
- Access to power / ground / IOs
- Access to logic regions

Through-silicon Vias (TSV)
- Only bridge power / ground / IOs to C4 bumps
- Coarse pitch, low density aids manufacturability
- Etch process (not laser drilled)

Passive Silicon Interposer (65nm Generation)
- 4 conventional metal layers connect micro bumps & TSVs
- No transistors means low risk and no TSV induced performance degradation

Side-by-Side Die Layout
- Minimal heat flux issues
- Minimal design tool flow impact

New!

28nm FPGA Slice
Silicon Interposer
Through-Silicon Vias
C4 Bumps
Microbumps
BGA Balls
Package Substrate
Benefits from Collaboration with Other Technology Leaders

- Leading fabless & fablite companies
- Equipment manufacturers
- Fabs and OSAT
- Industry consortia

- Requirements alignment
- Industry standards setting
- Best practice sharing
Design & Implementation Flow
Design Methodology Scales to Largest Devices

- One project
- Transparent routing
- Standard timing closure flow
- Single FPGA bring-up & debug

- Multiple projects
- I/O multiplexing & other “tricks”
- Timing closure across multiple designs
- Bring-up & debug of multiple FPGAs
Optimized ISE Design Suite Flows for Wide Variety of Users

1. Push-button flow
   - Ease-of-Use
   - High performance

2. Block-based flow
   - Floor planning
   - Hierarchical design
     • Team design
     • Incremental builds
   - Additional performance tuning

Hierarchical flow preserves portions of the design.
Path to Production
Technology Development Strategy

Test Vehicles

Modeling & Correlation

Benchmarking
- Consortium & Standards
- Supply Chain Manufacturing

• Shorter Learning Cycle
• Risk Mitigation
### Xilinx Is Well on the Way to Volume Production

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- Module Development
- Process Integration
- Reliability Assessment
- Supply Chain Validation
- Design Enablement
- Design Validation
- Process Qualification
- EA Design Tools
- Initial Sampling

**Today**
Reliability Assessment and Modeling

Reliability & Yield Assessment
- Temp Cycle B, Level-4 Preconditioning, and Electromigration
- Electrical tests of micro-bump and TSV

Stress Simulation
- Interposer functions as a stress buffer
- Improved C4 bump reliability

Thermal Simulation
- 40 watt design simulated
- < 2.5°C junction temperature difference

Test Vehicle
(Top View)
Xilinx leads industry with **Stacked Silicon Interconnect** technology delivering breakthrough capacity, bandwidth and power efficiency.

**Stacked Silicon Interconnect Technology**
- 2X FPGA capacity advantage at each process node
- Core part of Virtex-7 family
- Supported by standard design flows