Stacked Silicon Interconnect Technology (SSIT)

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Xilinx Inc.

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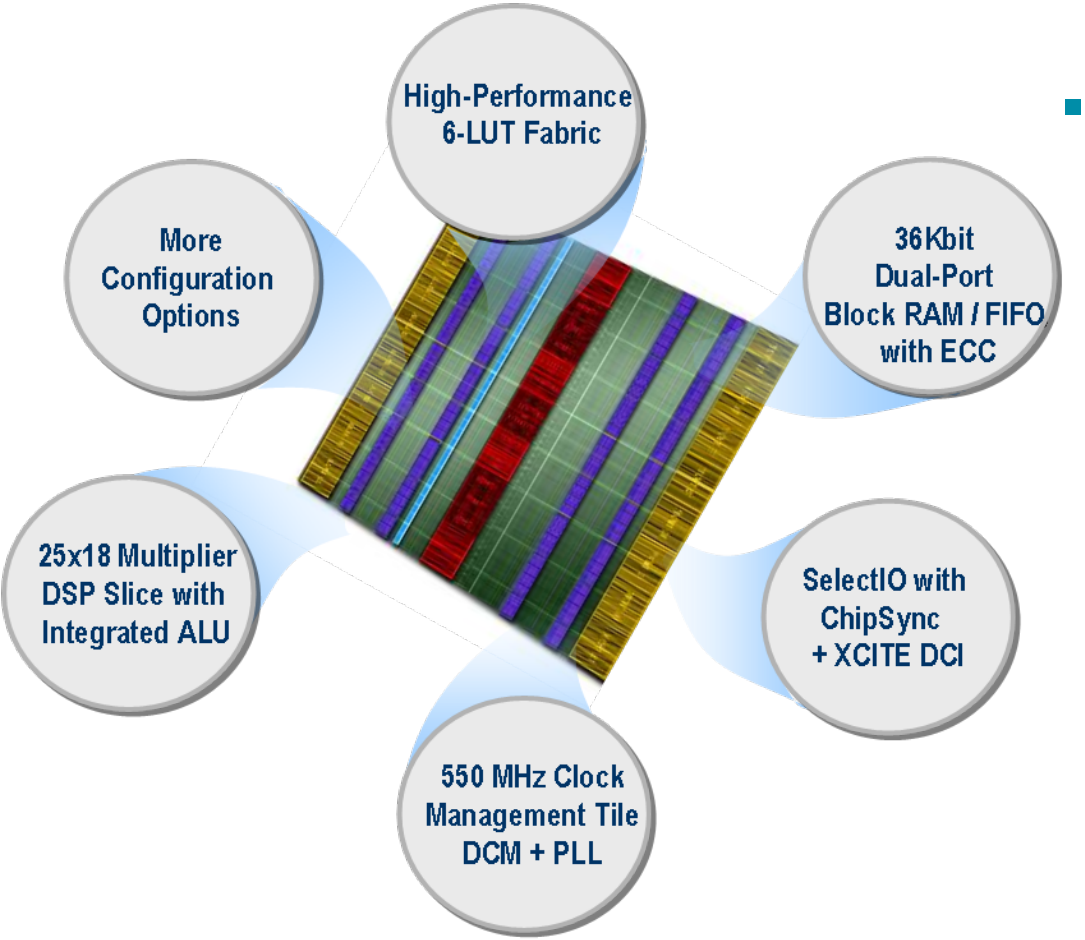
Agenda

- Background and Motivation
- Stacked Silicon Interconnect Technology
- Summary

Background and Motivation

Background: FPGA



- **Building Blocks**
  - Configurable Logic Block (CLB)
    - Configuration memory
    - Programmable switches
    - Interconnect drivers
  - Hard IP (DSP, EMAC, etc.)
  - Block RAM
  - Configurable IOs
  - High-speed transceivers

Programmable SoC of logic, memory, and analog circuits

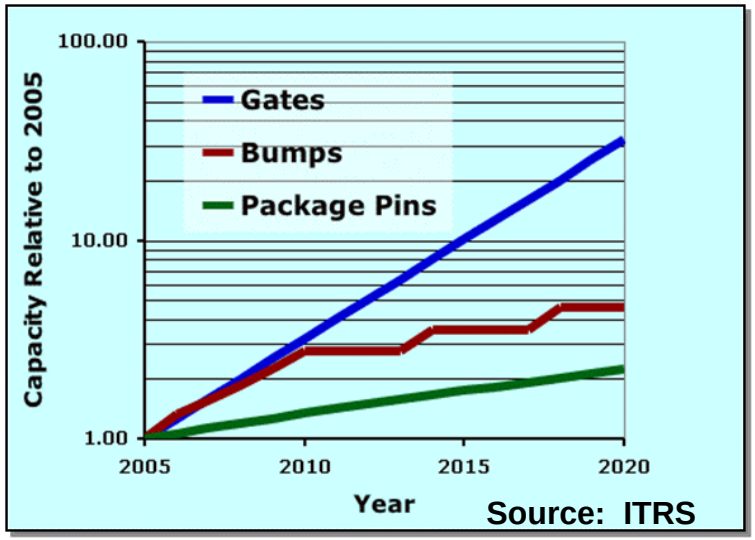
Customers Are Asking for More

- More than 2X today's logic capacity…
- Many more high-speed serial transceivers…
- Many more processing elements…
- Much more internal memory to store data…

Insufficient IO Scaling

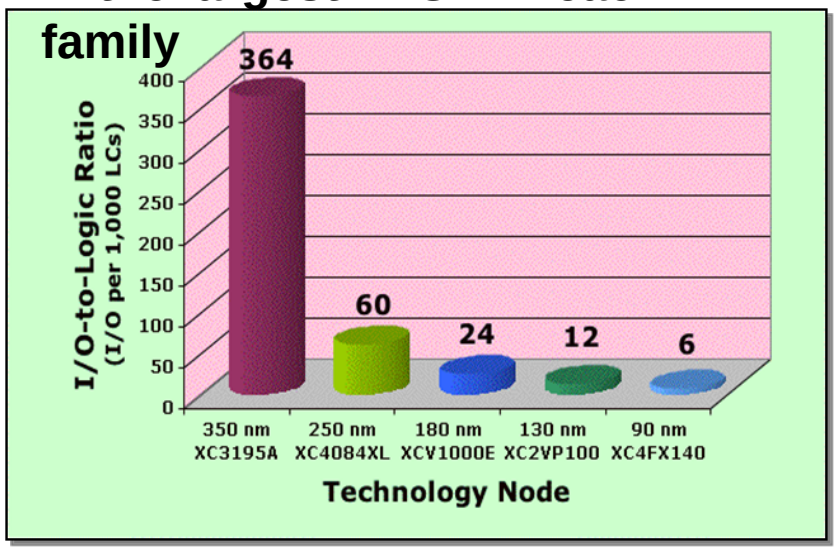
- Growing gap between number of logic gates and I/O
- Technology scaling favors logic density

Gates and Number of IOs



15x drop in I/O-to-logic ratio by 2020

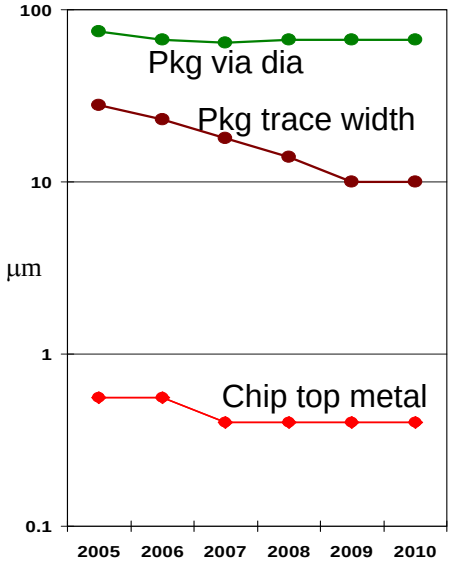
Number of I/O per 1000 logic cell in the largest FPGA in each family

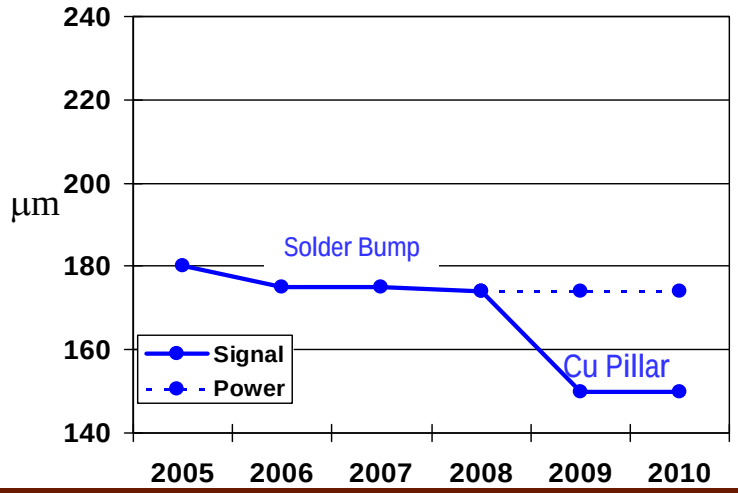


~60x decrease in I/O-logic ratio

Package Technology is Limiting

- **The packaging chasm:**
  - Two orders difference in package trace/width vs silicon metallization: connection BW is limited
  - I/O also isn't scaling due to bump pitch and chip to chip loading issues
  - Leads to increased area, power and complexity
- **Board chasm is even worse…**





Major "gearing" problem

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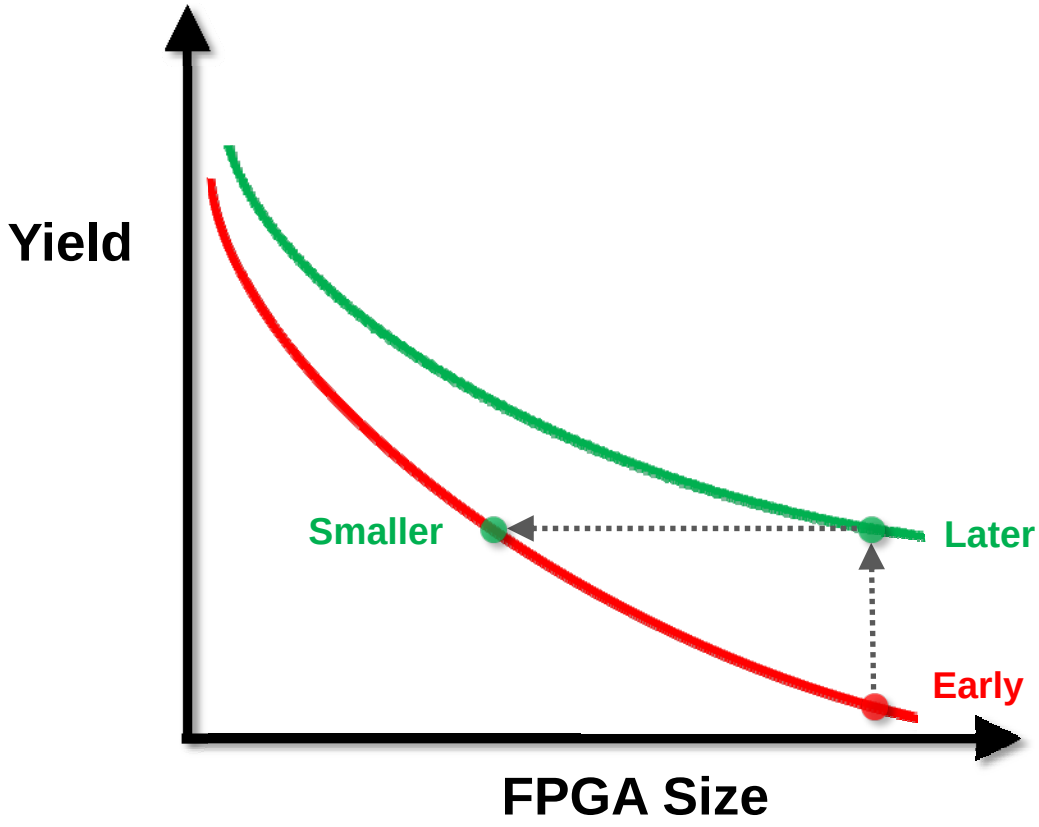
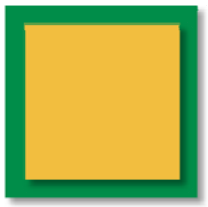
Challenge 1: Availability and Capability

Largest FPGAs only viable later in the life cycle

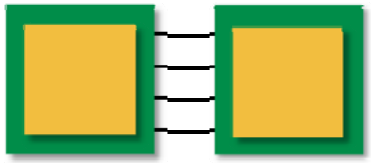


Challenge 2: Power and Bandwidth

Traditional mitigation techniques are no longer adequate



Large Monolithic FPGA



Multiple FPGAs on PCB or MCM

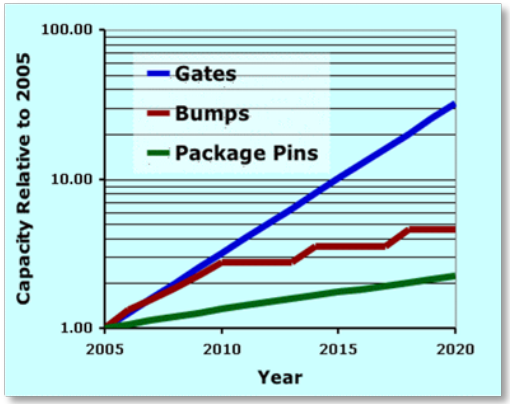
Chip-to-Chip via Standard I/Os and SerDes

More total gates, sooner, but…

Resources Not Scaling

1. Not enough I/Os
2. I/O latencies too high
3. Wasted I/O power

Innovation Needed



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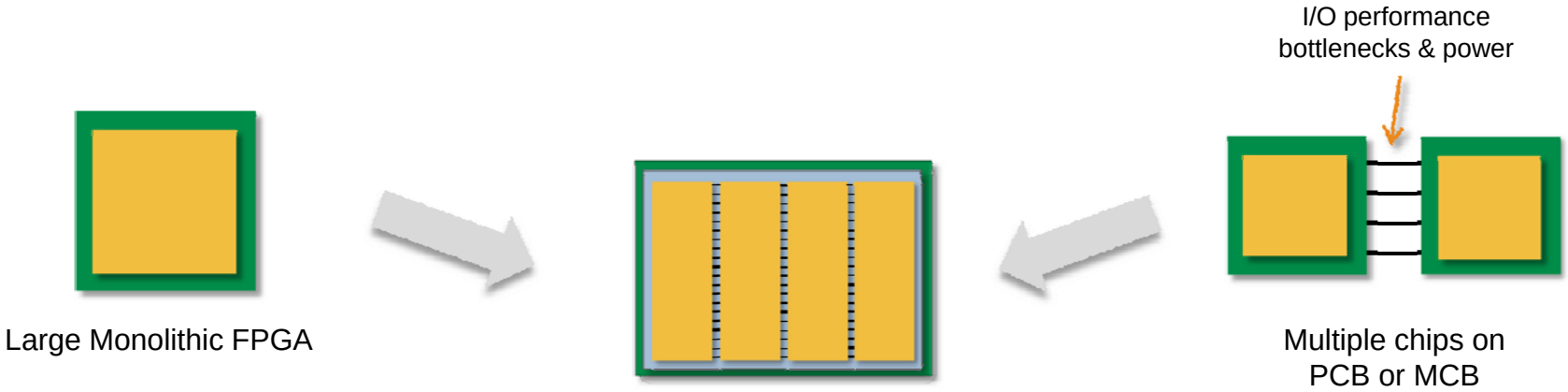
Introducing Stacked Silicon Interconnect Technology

High Bandwidth, Low Latency, Low Power

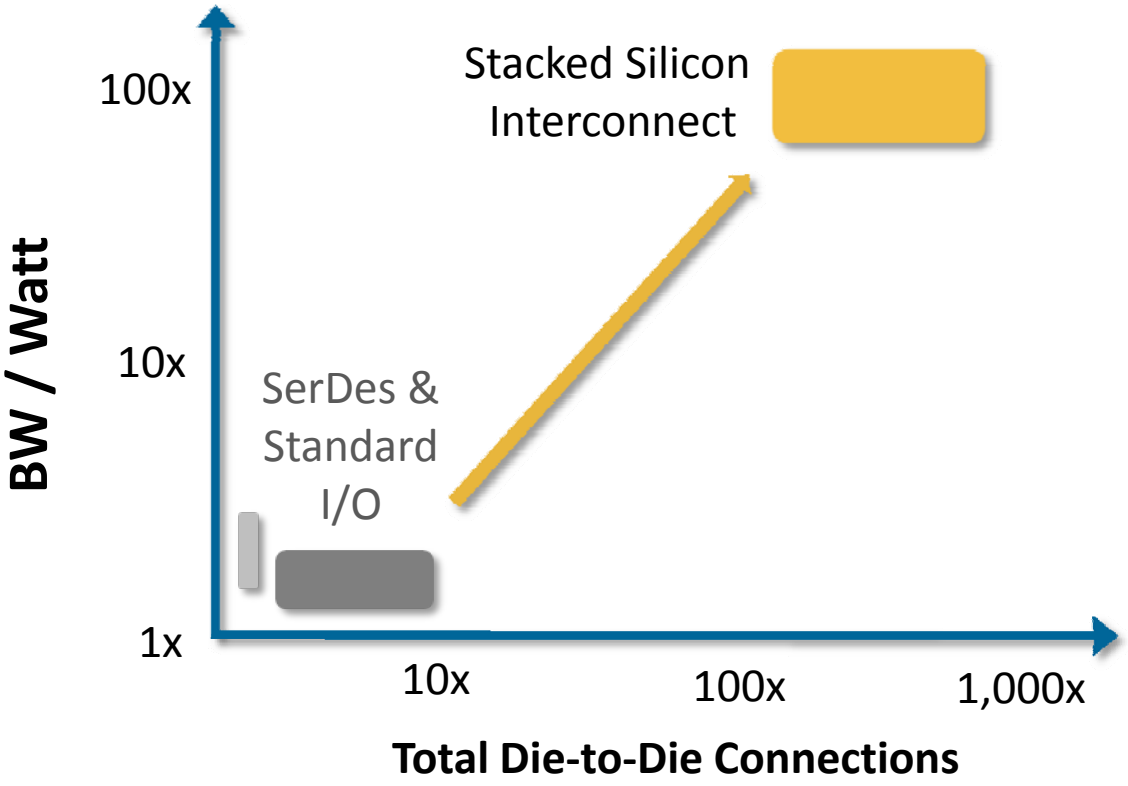


Xilinx Innovation

- ✓ Massive number of low latency, die-to-die connections
- ✓ Earlier in time
- ✓ No wasted I/O power
- ✓ Over five years of R&D

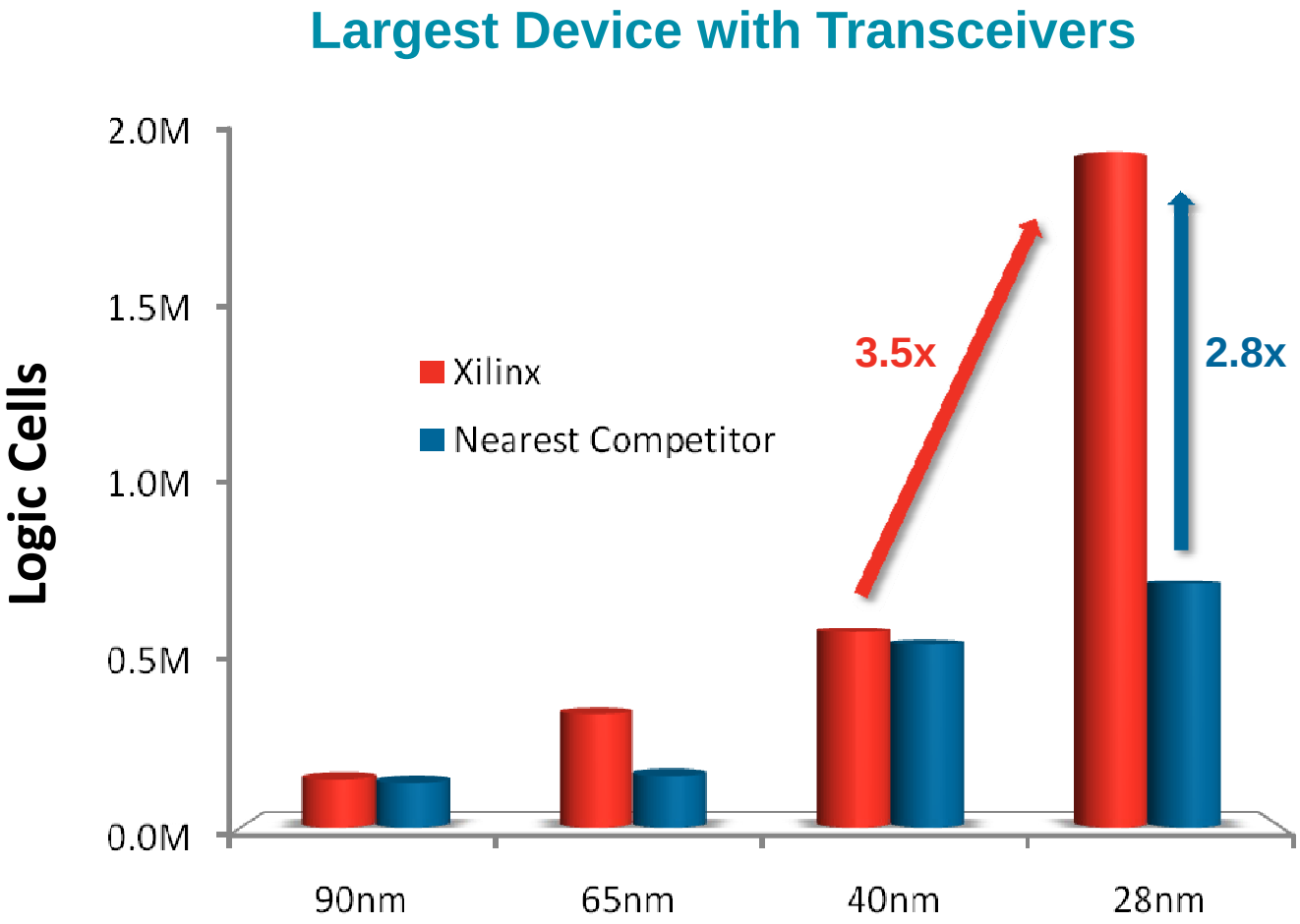
Delivers the Best of Both Worlds: High and Usable Capacity

Enables High Bandwidth, Low Power FPGA to FPGA Connectivity



100x bandwidth / Watt advantage over conventional methods

Delivers Resource-Rich FPGAs



For the Most Demanding FPGA Applications

Next Gen Wired Communications

Next Gen Wireless Communications

VIRTEX 7

Industry's Highest System Performance and Capacity

High Performance Computing

Medical Imaging

Aerospace & Defense

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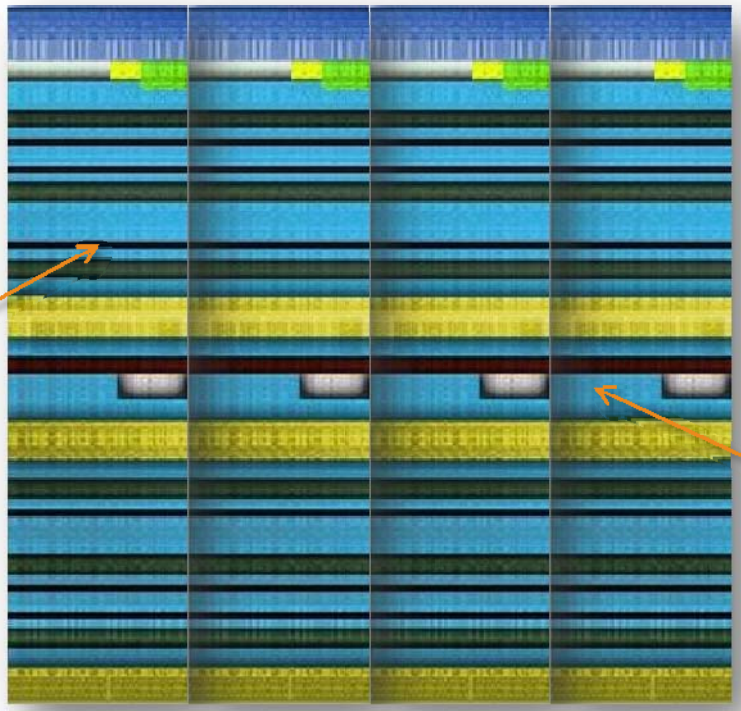
Summary

- **SSIT Addresses IO Bottleneck**
  - 100X lower BW/W over traditional IOs/SerDes
- **Can offer Next Generation Density Now**
- **SSIT Platform Enables**
  - Optimal Partitioning
    - Digital and analog blocks
    - IP/IC reuse
  - Heterogeneous Integration
    - Digital, mixed signal, & optical
    - FPGA & memory

Stacked Silicon Interconnect Technology

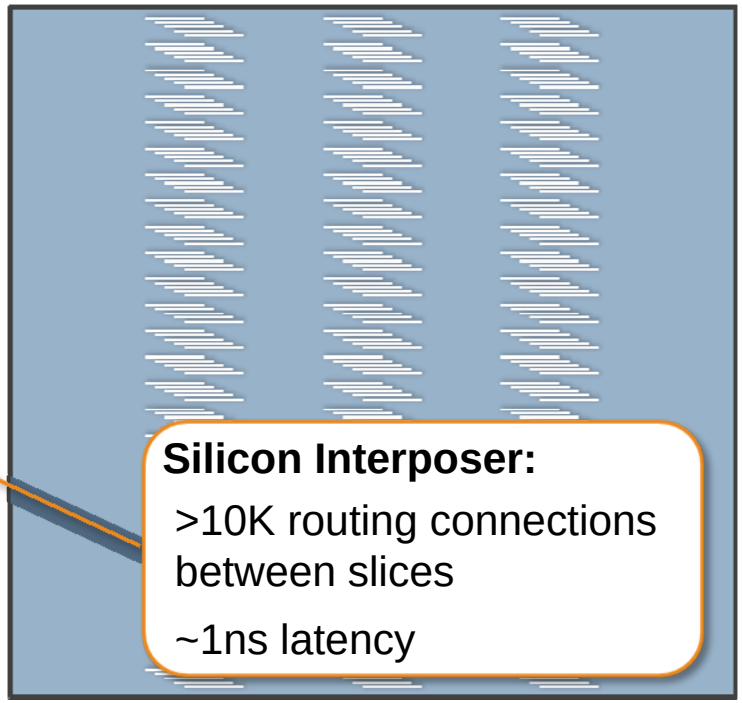
- Technology Overview
- Design & Implementation Flow
- Path to Production

Xilinx FPGA Architectural Innovations
At the Heart of the Technology



ASMBL Optimized FPGA slice

FPGA Slices Side-by-Side



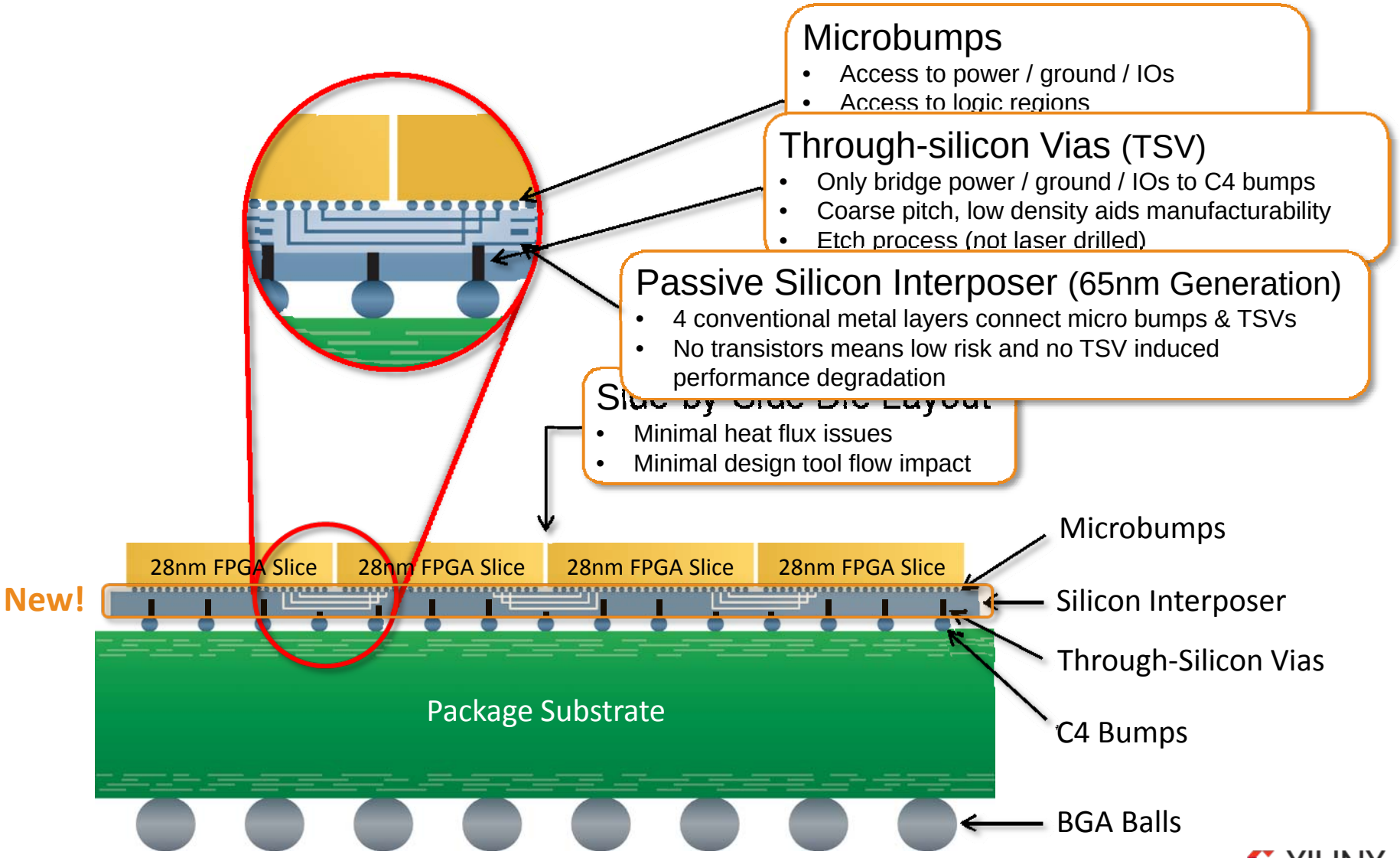
Silicon Interposer:

>10K routing connections between slices

~1ns latency

Silicon Interposer

Harnesses Proven Technology in a Unique Way



Benefits from Collaboration with Other Technology Leaders

- ✓ Leading fabless & fablite companies
- ✓ Equipment manufacturers
- ✓ Fabs and OSAT
- ✓ Industry consortia

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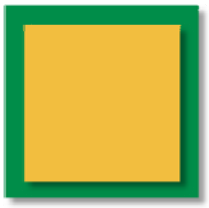
- Requirements alignment
- Industry standards setting
- Best practice sharing

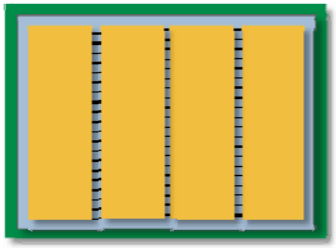
Design & Implementation Flow

Design Methodology Scales to Largest Devices

Monolithic FPGA

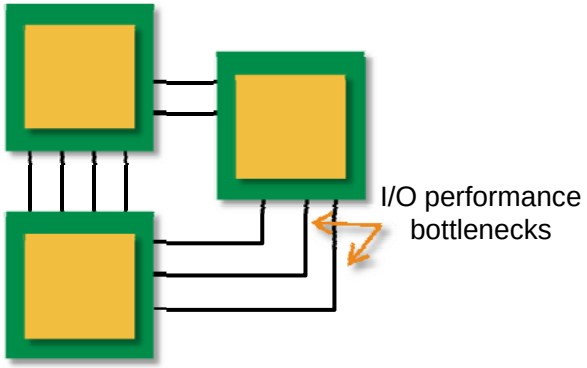


Stacked Silicon FPGA



- One project
- Transparent routing
- Standard timing closure flow
- Single FPGA bring-up & debug

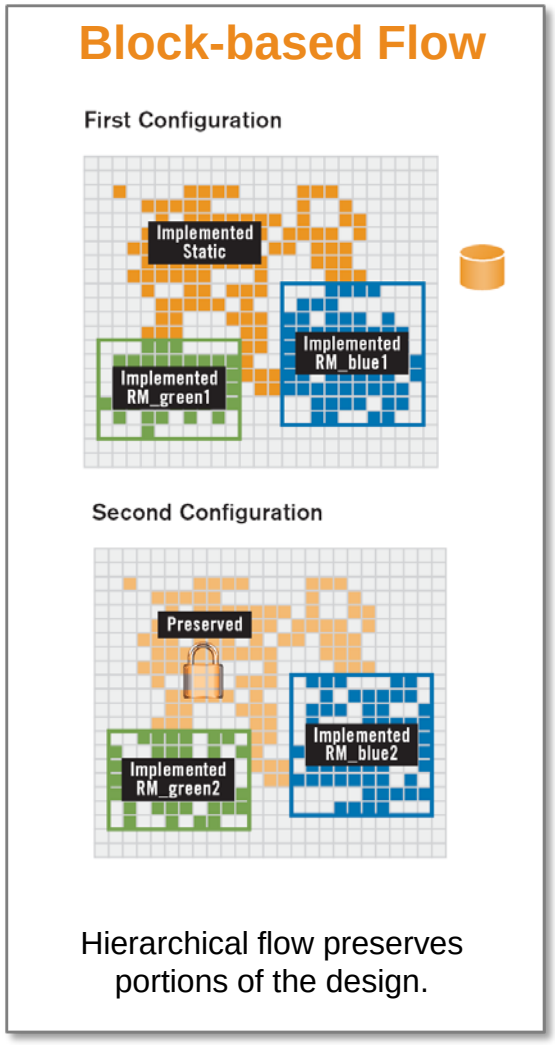
Multiple FPGAs



- Multiple projects
- I/O multiplexing & other “tricks”
- Timing closure across multiple designs
- Bring-up & debug of multiple FPGAs

Optimized ISE Design Suite Flows for Wide Variety of Users

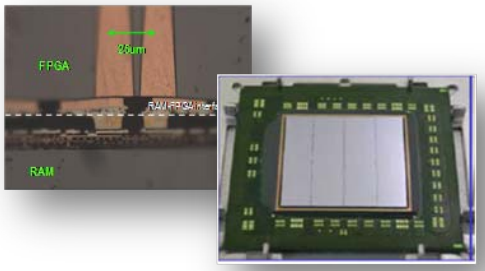
1. **Push-button flow**
   - Ease-of-Use
   - High performance
2. **Block-based flow**
   - Floor planning
   - Hierarchical design
     - Team design
     - Incremental builds
   - Additional performance tuning



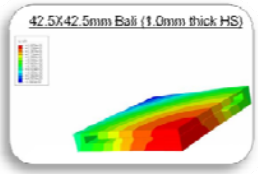
Path to Production

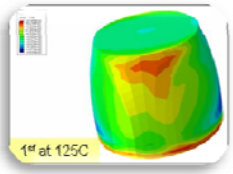
Technology Development Strategy

Test Vehicles



Modeling & Correlation





Benchmarking

- Consortium & Standards
- Supply Chain Manufacturing

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- Shorter Learning Cycle
- Risk Mitigation

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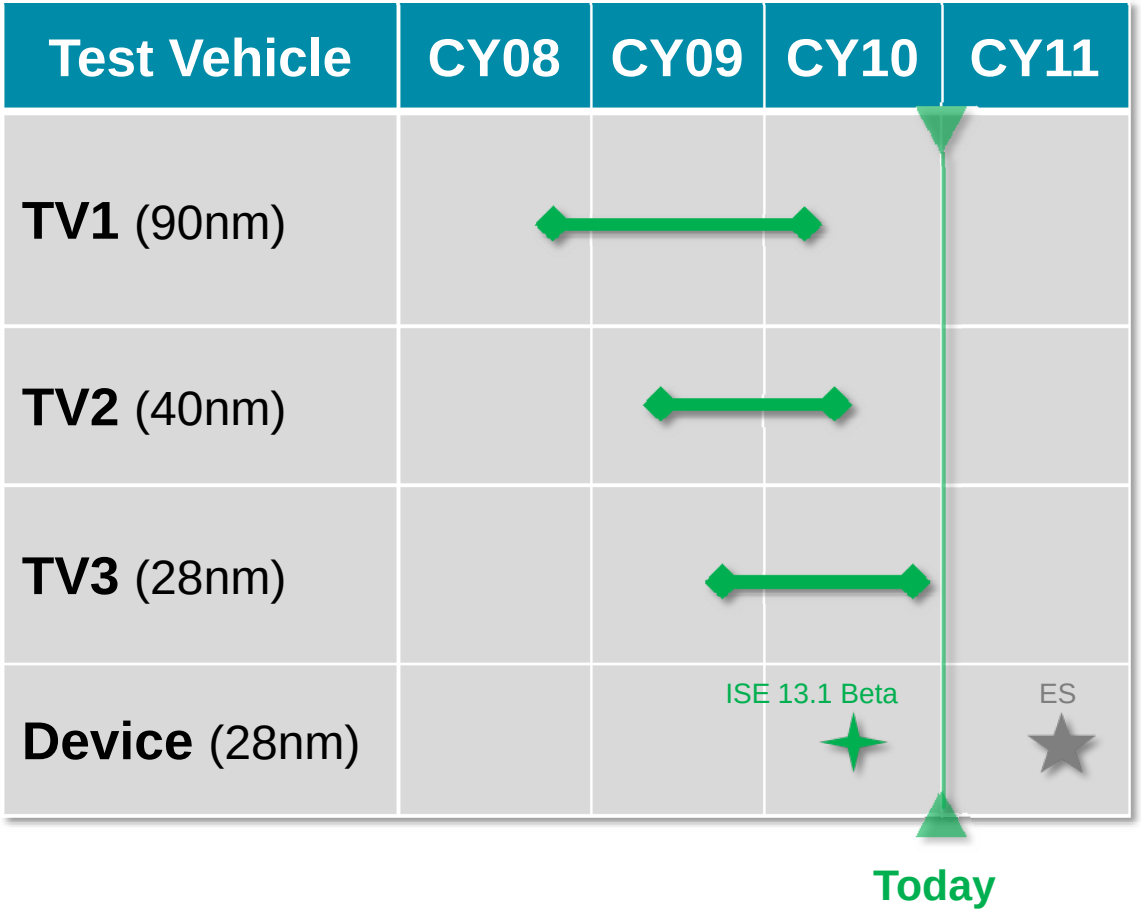
Xilinx Is Well on the Way to Volume Production



Module Development ✓
Process Integration ✓
Reliability Assessment ✓
Supply Chain Validation ✓

Design Enablement ✓

Design Validation ✓
Process Qualification

EA Design Tools ✓
Initial Sampling

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Reliability Assessment and Modeling

Reliability & Yield Assessment

- Temp Cycle B, Level-4 Preconditioning, and Electromigration
- Electrical tests of micro-bump and TSV

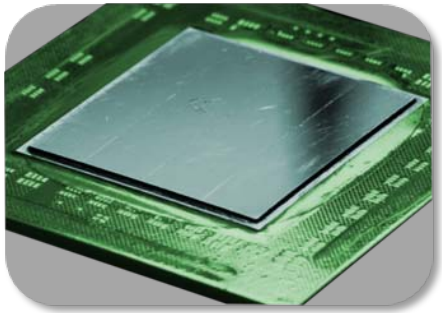
Stress Simulation

- Interposer functions as a stress buffer
- Improved C4 bump reliability

Thermal Simulation

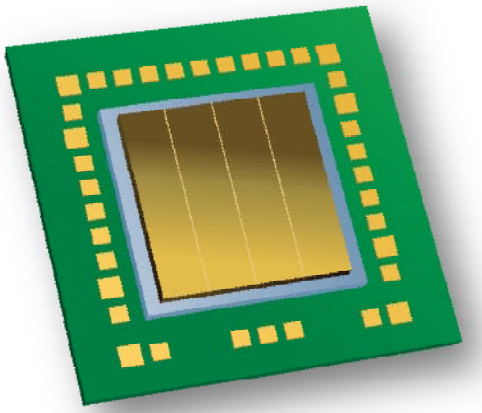
- 40 watt design simulated
- < 2.5^0C junction temperature difference

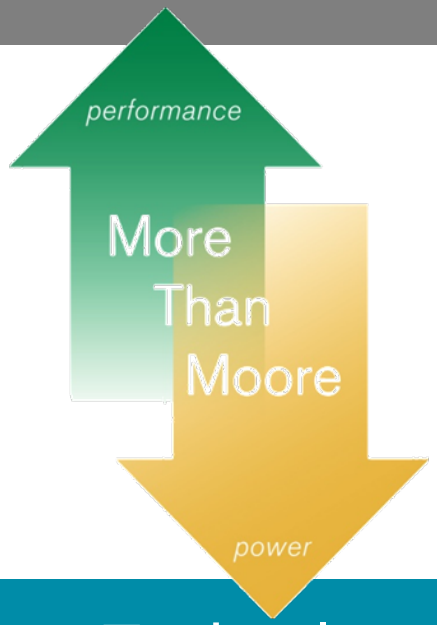
Test Vehicle
(Top View)



Summary

Xilinx leads industry with **Stacked Silicon Interconnect** technology delivering breakthrough capacity, bandwidth and power efficiency





Stacked Silicon Interconnect Technology

- 2X FPGA capacity advantage at each process node
- Core part of Virtex-7 family
- Supported by standard design flows