IC Packaging of the Internet of Things

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Outline

• IC Forecasts
• Bandwidth Demand and Forecasts of Things which use this bandwidth
• Stacked Package Market
• System-in-Package (SiP)
• Through Via Technology – 3-D and 2.5-D
• Interconnection / Flip Chip
• Conclusion
IC Unit Forecast, 2012-2016

- 2010: 195,932
- 2011: 190,289
- 2012: 198,968
- 2013: 216,895
- 2014: 233,678
- 2015: 249,728
- 2016: 270,500

IC Units (Million)
IC Revenue Forecast, 2010-2016
IC Units by Package Family, 2011 vs. 2016
Total OSAT Company Packaging Units, 2010-2016
Total OSAT Company Packaging Revenue, 2010-2016

Contractor Market Percentage of Total Worldwide Market (%)
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Web browsing, peer-to-peer file sharing, audio/video streaming are driving a 50 percent year over year growth of data volume on fixed networks and 100 percent on mobile networks.
IoT Goals is to Integrate heterogeneous technologies to achieve all these goals concurrently:

• Reduced power consumption by reducing losses. But more integration inevitably leads to thermal challenges too.
• Improved miniaturization.
• Improved end to end processing speed: receive stimulus from environment, record, process, communicate and respond back to environment with minimal power consumed.
Cellular Handset IC Unit Forecast, 2011-2016
Cellular Infrastructure IC Unit Forecast, 2011-2016

- 2011: 3,238 million units
- 2012: 3,595 million units
- 2013: 3,990 million units
- 2014: 4,429 million units
- 2015: 4,961 million units
- 2016: 4,961 million units
Tablet IC Unit Forecast, 2011-2016

- 2011: 4,288 units
- 2012: 6,198 units
- 2013: 8,650 units
- 2014: 10,779 units
- 2015: 12,894 units
- 2016: 14,781 units
Netbook and Notebook IC Unit Forecast, 2011-2016
Desktop PC IC Unit Forecast, 2011–2016
Important IC Packages for Bandwidth Consumption

Enablers for Stacked Packages, SiP, Through-Via Technology, Flip Chip:

• FBGA
• BGA
• WLP / Fan-Out WLP (FO-WLP)
• QFN/ Fan-In QFN (FI-QFN)
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Stacked Packages

Stacked packages are a vertically packaged multichip package (MCP).
The interconnection of the upper die can go:

- Around the lower die with wire bonds,
- Through the die below, as in 3-D, through via technology, or
- Through an interposer to the substrate, or 2.5-D interconnection.
Types of Stacked Packages

- Die stacks, on a common substrate
- PoP, or package-on-package, aka package stacks
- PiP, or package-in-package, back-to-back in a single mold compound
- Stacked TSOPs
- Stacked QFNs / QFPs
- Stacked MCMs
- Stacked WLPs
Stacked Package Units

<table>
<thead>
<tr>
<th>Year</th>
<th>Percentage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>71%</td>
<td>Die Stack: Die within a Single FBGA</td>
</tr>
<tr>
<td></td>
<td>15%</td>
<td>Package on Package (PoP)</td>
</tr>
<tr>
<td></td>
<td>7%</td>
<td>Package in Package (PiP)</td>
</tr>
<tr>
<td></td>
<td>3%</td>
<td>Stacked TSOPs or within a TSOP</td>
</tr>
<tr>
<td></td>
<td>2%</td>
<td>Stacked QFN/QFP or within a QFN/QFP</td>
</tr>
<tr>
<td></td>
<td>1%</td>
<td>Stacked WLPs</td>
</tr>
<tr>
<td></td>
<td>1%&lt;1%</td>
<td>Other Stacked Packages</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Year</th>
<th>Percentage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016</td>
<td>68%</td>
<td>Die Stack: Die within a Single FBGA</td>
</tr>
<tr>
<td></td>
<td>22%</td>
<td>Package on Package (PoP)</td>
</tr>
<tr>
<td></td>
<td>1%&lt;1%</td>
<td>Package in Package (PiP)</td>
</tr>
<tr>
<td></td>
<td>5%</td>
<td>Stacked TSOPs or within a TSOP</td>
</tr>
<tr>
<td></td>
<td>1%</td>
<td>Stacked QFN/QFP or within a QFN/QFP</td>
</tr>
<tr>
<td></td>
<td>1%&lt;1%</td>
<td>Stacked WLPs</td>
</tr>
<tr>
<td></td>
<td>1%</td>
<td>Other Stacked Packages</td>
</tr>
</tbody>
</table>
Applications Breakdown for Stacked Packages

2008

2011

2012

- Cell Phones
- Base Stations
- Tablets & PDAs
- MP3 Players
- Camcorders
- Digital Video Recorders
- Digital Cameras
- Netbook & Notebook Computers
- Desktop PCs
- Internet Routers/Switches
- Servers/Workstations
- Medical
- Other

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Interconnection of Stacked Packages

2011
- All Wire Bonded: 87%
- WB + FC: 3%
- All Flip Chip: 10%
- Other: 0%

2016
- All Wire Bonded: 72%
- WB + FC: 13%
- All Flip Chip: 9%
- Other: 6%
System in Package (SiP)

A system in package (SiP) is a customized package with multiple elements inside, creating a functional block within a standard JEDEC footprint. This JEDEC footprint differentiates it from an MCM.

A functional block in the electronics world is a system of electronics that combines functional units together onto a single substrate to enable the shortest electrical distance between parts for superior performance. This also enables a more simplistic PCB for the final product, thus potentially reducing system costs.
Applications Breakdown for SiPs, 2012
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TSVs, or Through Vias

- Through-silicon vias (TSVs) have been developed as an interconnection style for stacked packages or SiPs to address bandwidth issues.
- 3-D and 2.5-D methods of vertical through interconnection.
- Silicon, glass, and laminate interposers for 2.5-D interconnection.
3-D versus 2.5-D

- **2.5-D**: Chips are partitioned and placed side by side on an interposer with through-vias to a substrate below. The interposer and microbumps act as Redistribution Layer, or RDL.

- **3-D**: Die are stacked vertically, with through vias going through the bulk silicon to connect each one to the next.
3-D versus 2.5-D

2.5-D
• Avoids thermal issues of stacking the die
• Less complex; through vias go through an interposer, not active silicon
• Interposer and microbumps for routing between layers
• Silicon interposers accommodate the CTE mismatch between the layers in a stack, acting as a stress reducer, thus improving reliability

3-D Interconnect
• Higher thermal issues
• More complex, vias go through active silicon
• Interposer and microbumps for routing between layers
• More potential reliability concerns
• Highest degree of bandwidth, can achieve 100 times the connectivity or bandwidth, with less power consumption, when compared to wire bonding
• Has the shortest interconnection distance, enhancing the characteristics of high speed, low power consumption, reduced parasitics, and small form factor.
TSV Chip Partition Examples

Courtesy of Qualcomm and IWLPC
Xilinx’s 2.5-D Structure
Elpida’s 8-Gigabit TSV DRAM Package Outline and Cross Section
Altera Corporation and TSMC chip-on-wafer-on-substrate (CoWoS)

- Altera Corporation and TSMC jointly developed the world’s first heterogeneous 3-D IC
- Heterogeneous 3-D ICs include analog, logic, and memory devices
- The process flow is to attach the device silicon chips onto the silicon interposer wafer, dice the wafer, and then attach the stacked silicon onto the substrate (CoWoS)

<table>
<thead>
<tr>
<th></th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>CAGR (%)</th>
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<tbody>
<tr>
<td><strong>Potential Units (M)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MPUs</td>
<td>534</td>
<td>557</td>
<td>605</td>
<td>644</td>
<td>678</td>
<td>733</td>
<td>6.5</td>
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<tr>
<td>DRAM</td>
<td>16,087</td>
<td>16,570</td>
<td>18,144</td>
<td>19,849</td>
<td>21,576</td>
<td>23,691</td>
<td>8.0</td>
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<tr>
<td>Special-Purpose Logic:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Communications</td>
<td>7,772</td>
<td>8,549</td>
<td>9,832</td>
<td>11,257</td>
<td>12,799</td>
<td>14,655</td>
<td>13.5</td>
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<tr>
<td>PLD and FPGA</td>
<td>1,662</td>
<td>1,883</td>
<td>2,209</td>
<td>2,538</td>
<td>2,898</td>
<td>3,336</td>
<td>15.0</td>
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<tr>
<td>Graphics</td>
<td>753</td>
<td>778</td>
<td>849</td>
<td>909</td>
<td>967</td>
<td>1,038</td>
<td>6.6</td>
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<tr>
<td>Flash</td>
<td>10,213</td>
<td>10,948</td>
<td>12,328</td>
<td>13,709</td>
<td>15,162</td>
<td>16,829</td>
<td>10.5</td>
</tr>
<tr>
<td><strong>Total Potential Market</strong></td>
<td>37,021</td>
<td>39,285</td>
<td>43,966</td>
<td>48,906</td>
<td>54,080</td>
<td>60,282</td>
<td>10.2%</td>
</tr>
<tr>
<td>TSVs as a Percentage of the Total Potential Market</td>
<td>0.3%</td>
<td>0.6%</td>
<td>0.7%</td>
<td>0.9%</td>
<td>—</td>
<td></td>
<td></td>
</tr>
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Total Interconnection for ICs, 2011 vs. 2016

- 2011: 82% Wire Bonded IC Package Units
- 2016: 81% Wire Bonded IC Package Units

Legend:
- Wire Bonded IC Package Units
- Flip Chip IC in Package Units
- Wire Bonded DCA
- Flip Chip DCA and TAB
- WLP

NVR
Flip Chip Interconnection

• The die is flipped face down (or active side down) so that the circuitry faces the substrate
• Bumps, not wires, create the electrical path, and is an area array covering all or part of the face of the die
• Generally for packages with substrates, although a few designs utilize leadframes
• Leadframe designs can have the die oriented upwards, and the leadframe reach over the top
Solder Limitation to Fine-Pitch Flip Chip

- Pitch limitation (~140um)
- Collapsed low stand-off
- UF filling limitation
- Lower EM and thermal performance
- Multiple die stacking is unfavorable

- 60um pitch capability
- Higher stand-off height
- Easy UF filling / MUF possibility
- Higher EM and thermal performance
- Multiple die stacking is favorable

Courtesy of Texas Instruments, Amkor Technology Korea, Amkor Technology, Inc., and ECTC
### Solder Flip Chip and Fine-Pitch Flip Chip

*Courtesy of Texas Instruments, Amkor Technology Korea, Amkor Technology, Inc., and ECTC*

<table>
<thead>
<tr>
<th>Conventional Solder Flip Chip</th>
<th>Fine Pitch Gold Stud Flip Chip</th>
<th>Fine Pitch Cu Pillar Flip Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Conventional Solder Flip Chip Image" /></td>
<td><img src="image2.png" alt="Fine Pitch Gold Stud Flip Chip Image" /></td>
<td><img src="image3.png" alt="Fine Pitch Cu Pillar Flip Chip Image" /></td>
</tr>
<tr>
<td>140-180um minimum pitch</td>
<td>50um in-line pitch</td>
<td></td>
</tr>
</tbody>
</table>
Gold-Bumping Process
Courtesy of NEXX Systems and IMAPS
Copper Pillar Bumping Process Flow

1. UBM Sputter
2. Template Photo
3. Cu Pillar / Solder Plating
4. Template PR Strip
5. UBM Etching
6. Reflow
Copper Pillar Bump
Courtesy of Siliconware Precision Industries Co., Limited and ECTC
Devices which Utilize Flip Chip

- MPU
- MCU 32-bit
- DSP
- Gate Array
- Standard Cell & PLD
- Special purpose logic: consumer, computer, communications, auto, other
- DRAM
- SRAM
- Flash
- Analog: communications, computer
Percentage of the Total Worldwide I/O Count Range, 2011 vs. 2016
Conclusion

• Increased bandwidth is required to meet today’s and tomorrow’s Internet demand
• Front end nearing the end of its ability to continue shrinking
• Backend IC packaging is now key to increasing bandwidth capabilities, by putting devices closer together, shortening the distance the electron must follow, with fewer parasitics, straightening the electron path, with fewer material changes