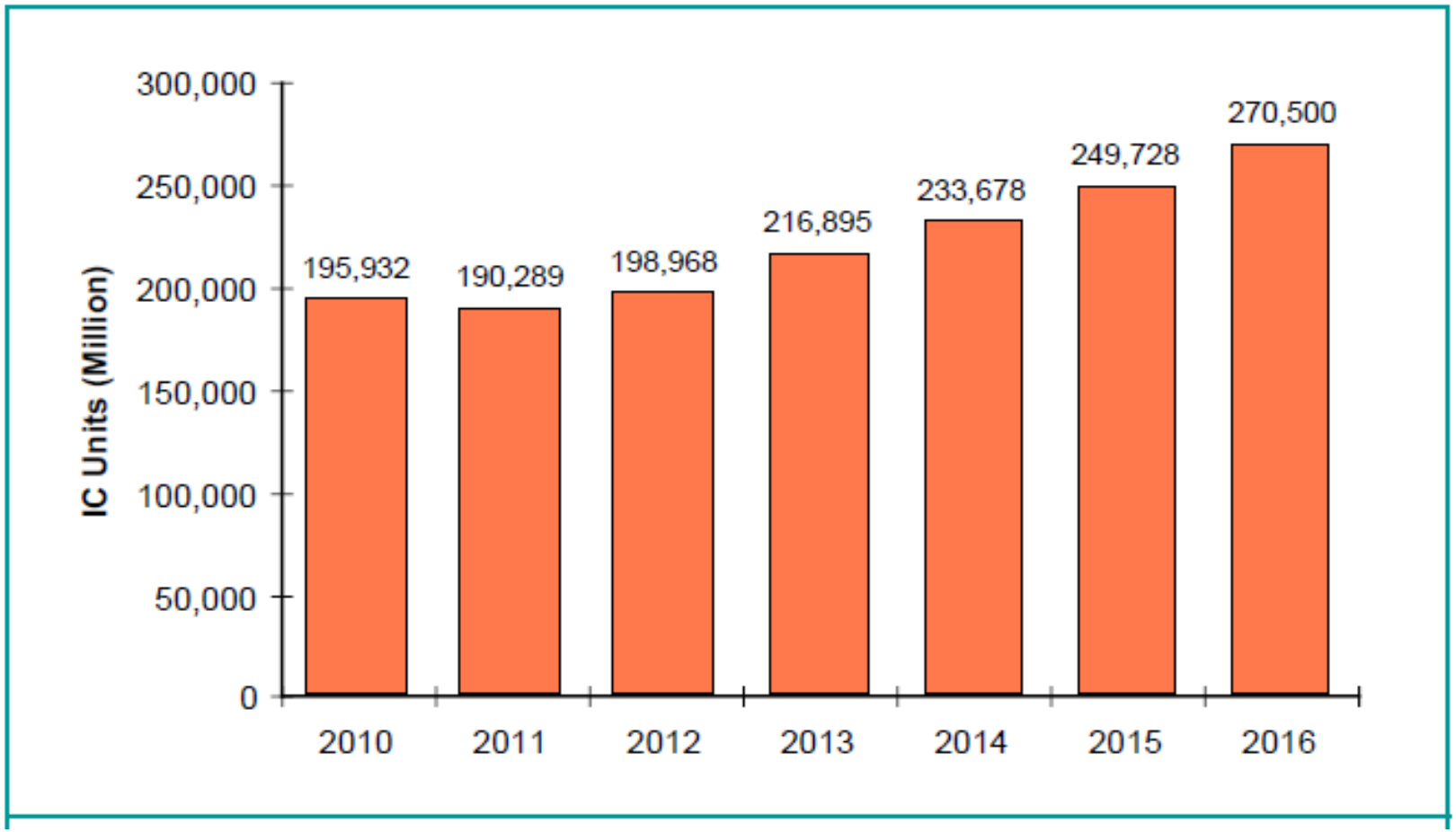
IC Packaging of the Internet of Things

Sandra L. Winkler
Senior Industry Analyst
New Venture Research
www.newventureresearch.com
slwinkler@newventureresearch.com

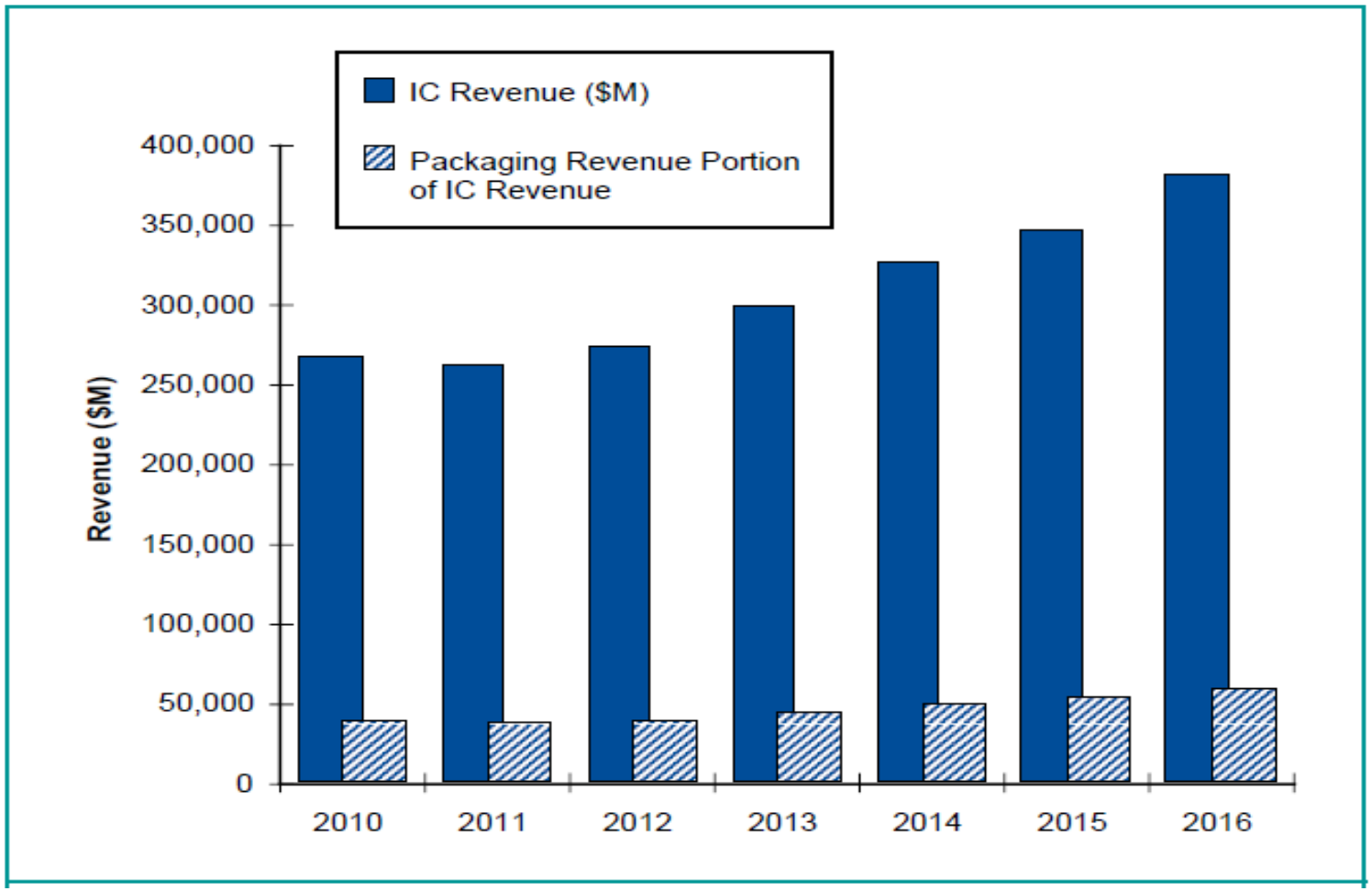
Outline

- IC Forecasts
- Bandwidth Demand and Forecasts of Things which use this bandwidth
- Stacked Package Market
- System-in-Package (SiP)
- Through Via Technology – 3-D and 2.5-D
- Interconnection / Flip Chip
- Conclusion

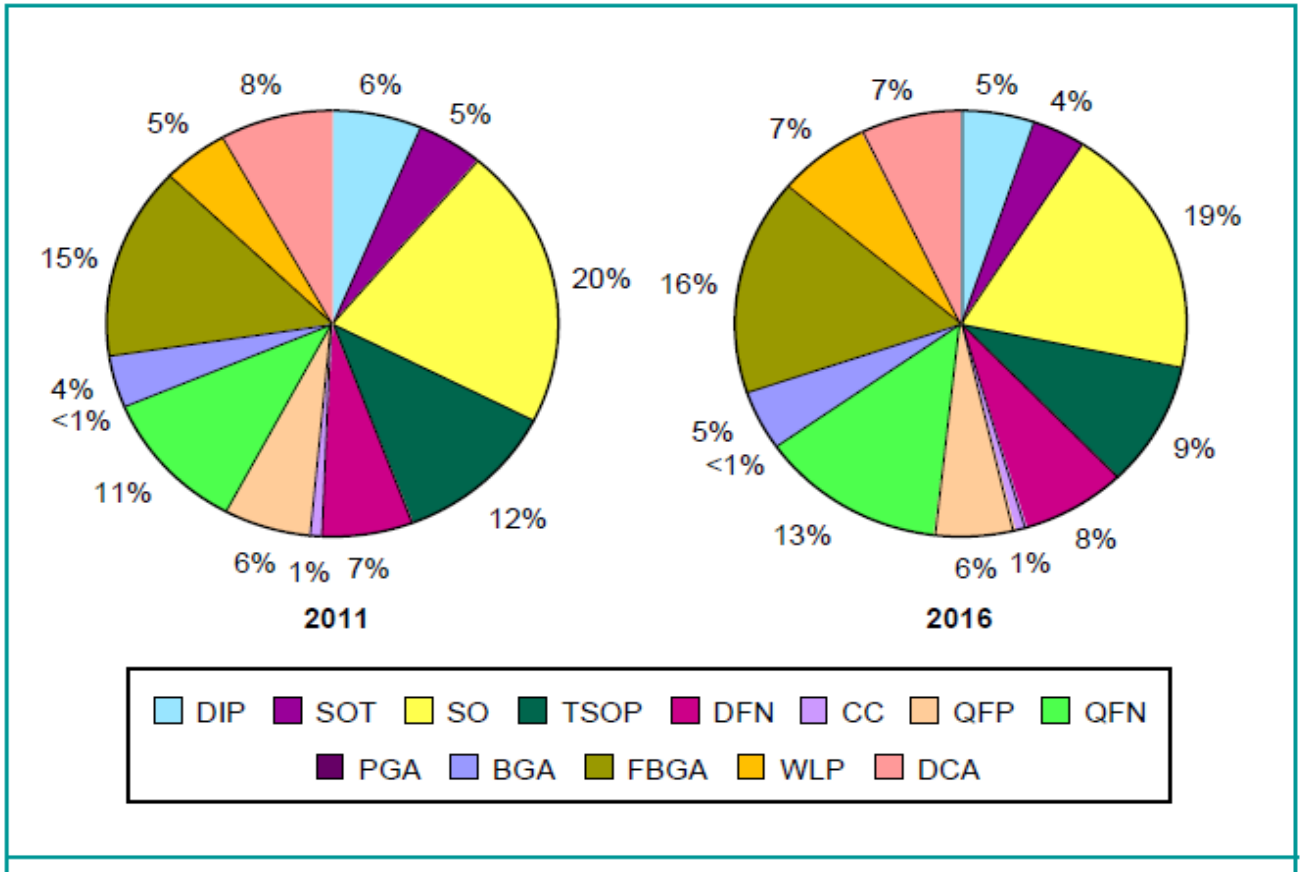
IC Unit Forecast, 2012-2016



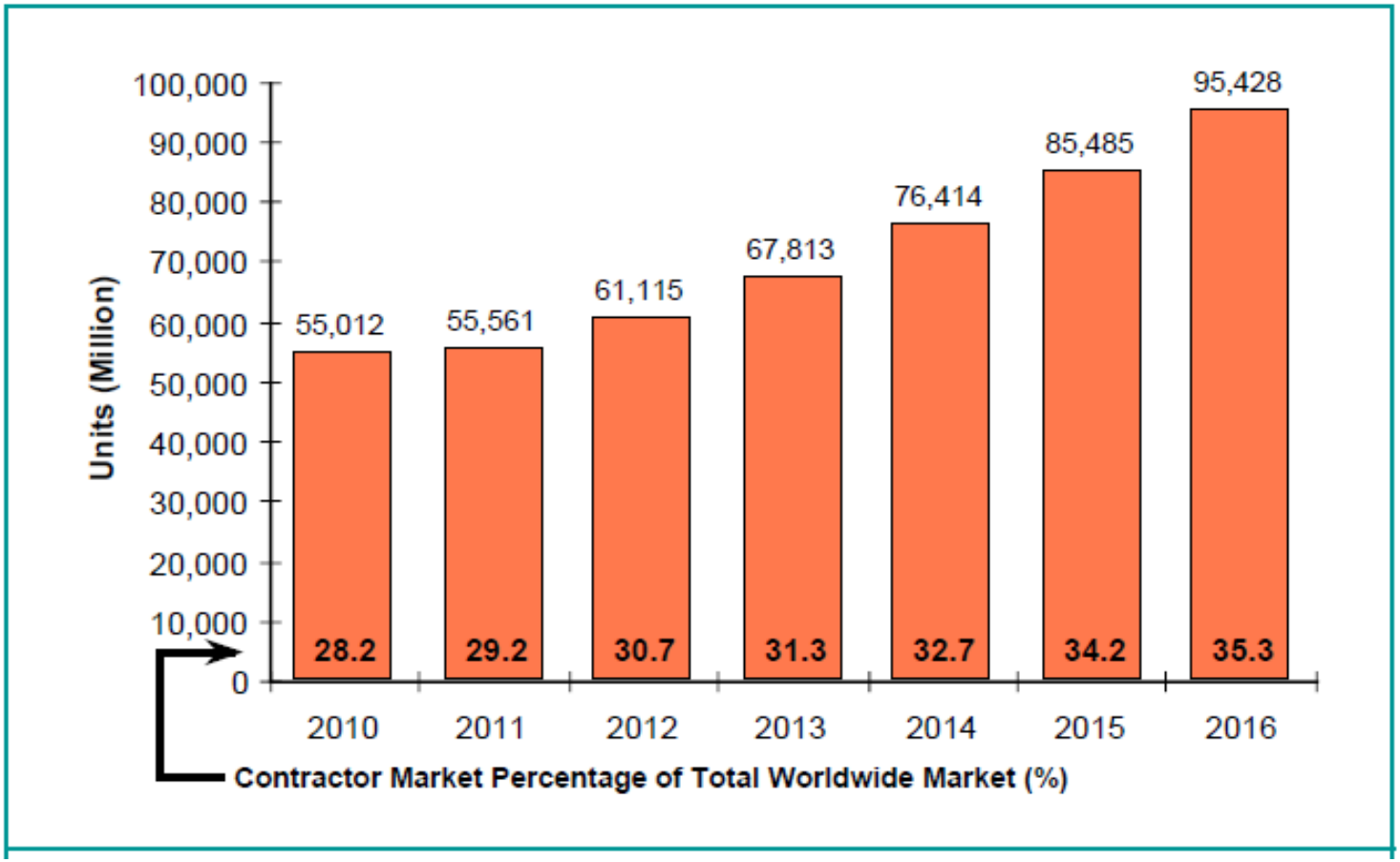
IC Revenue Forecast, 2010-2016



IC Units by Package Family, 2011 vs. 2016



Total OSAT Company Packaging Units, 2010-2016



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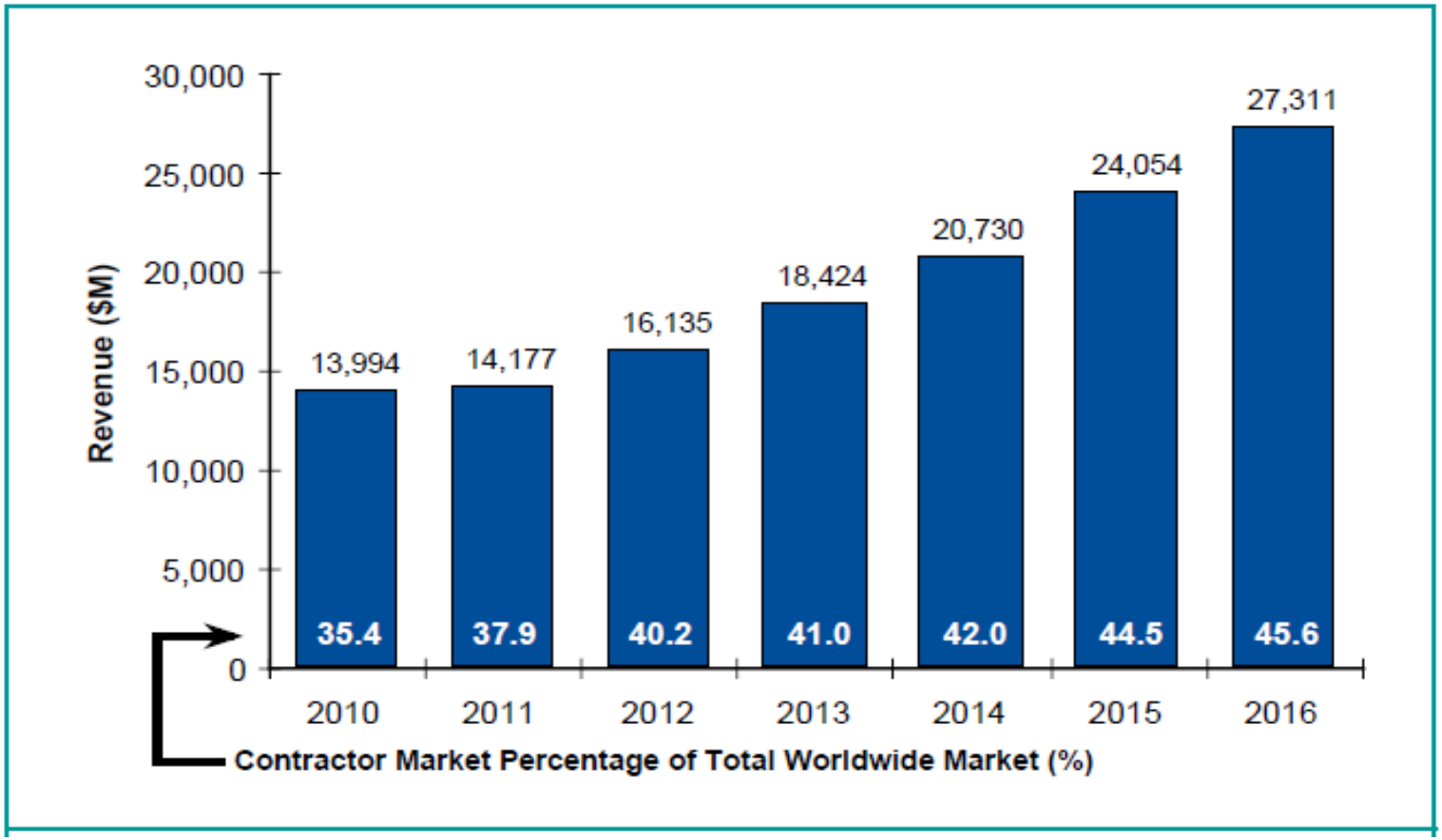

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Bandwidth Demand

Web browsing, peer-to-peer file sharing, audio/video streaming are driving a 50 percent year over year growth of data volume on fixed networks and 100 percent on mobile networks.

IDC March 15, 2012

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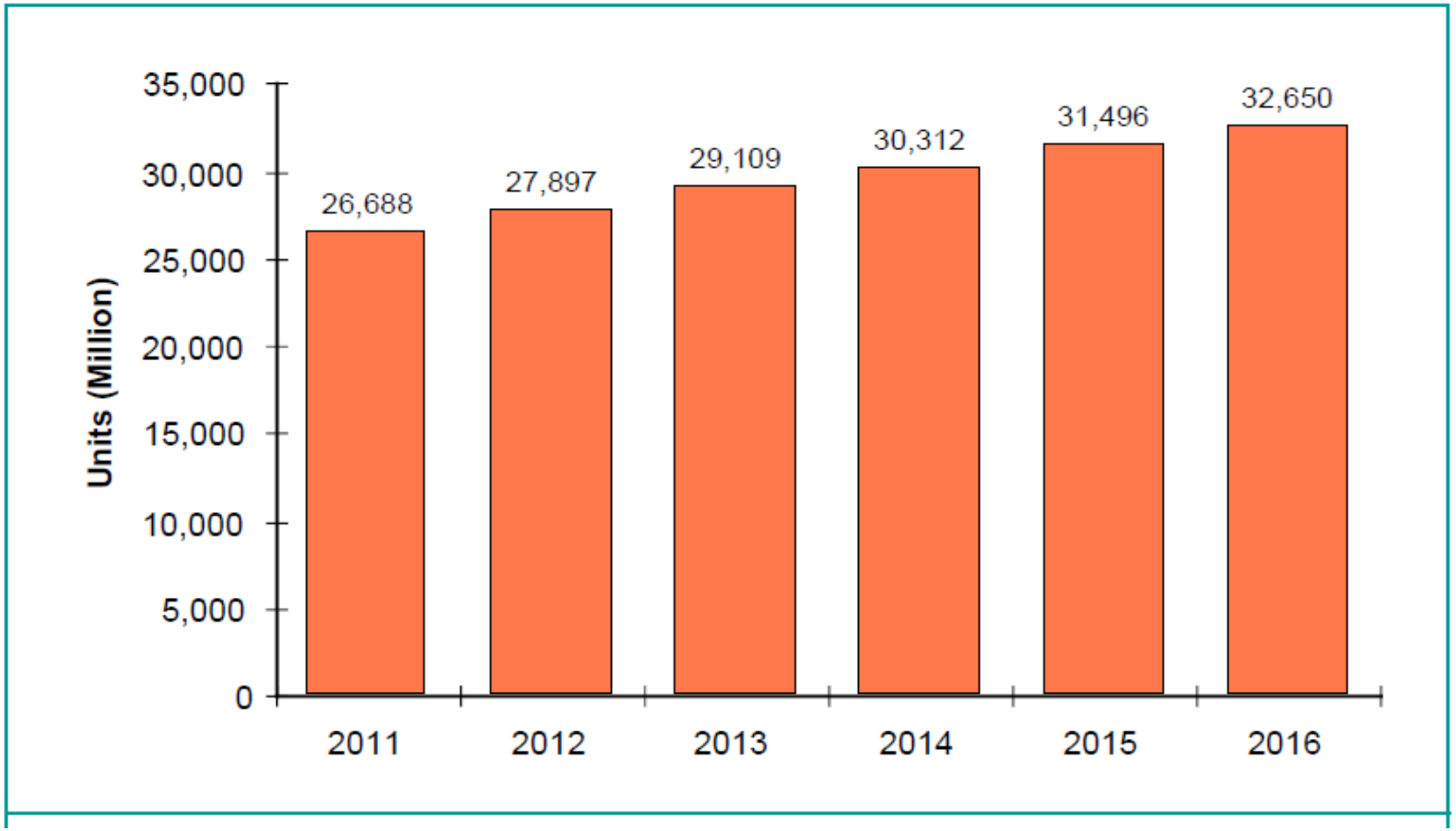
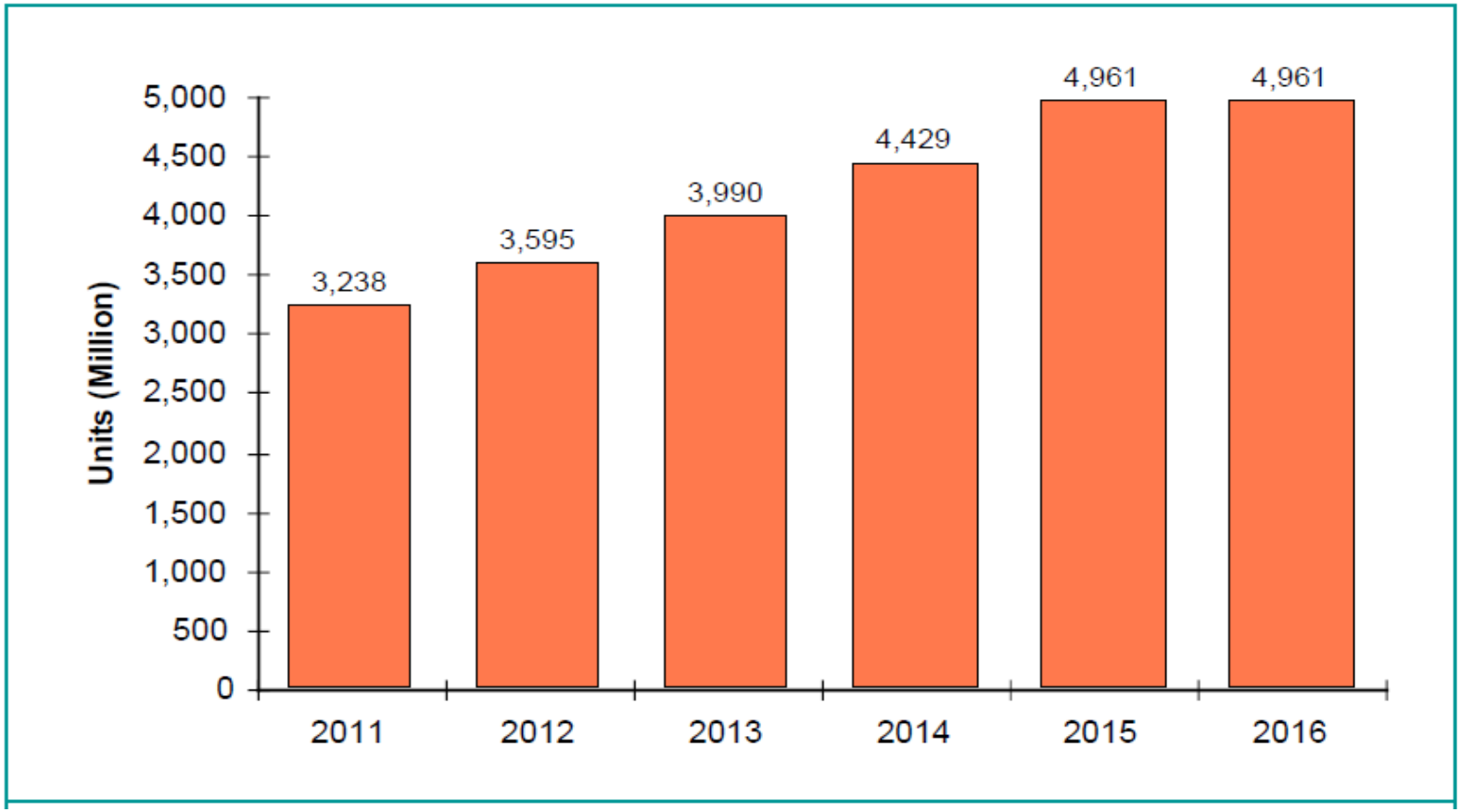
IoT Goals is to Integrate heterogeneous technologies to achieve all these goals concurrently:

- Reduced power consumption by reducing losses. But more integration inevitably leads to thermal challenges too.
- Improved miniaturization.
- Improved end to end processing speed: receive stimulus from environment, record, process, communicate and respond back to environment with minimal power consumed.

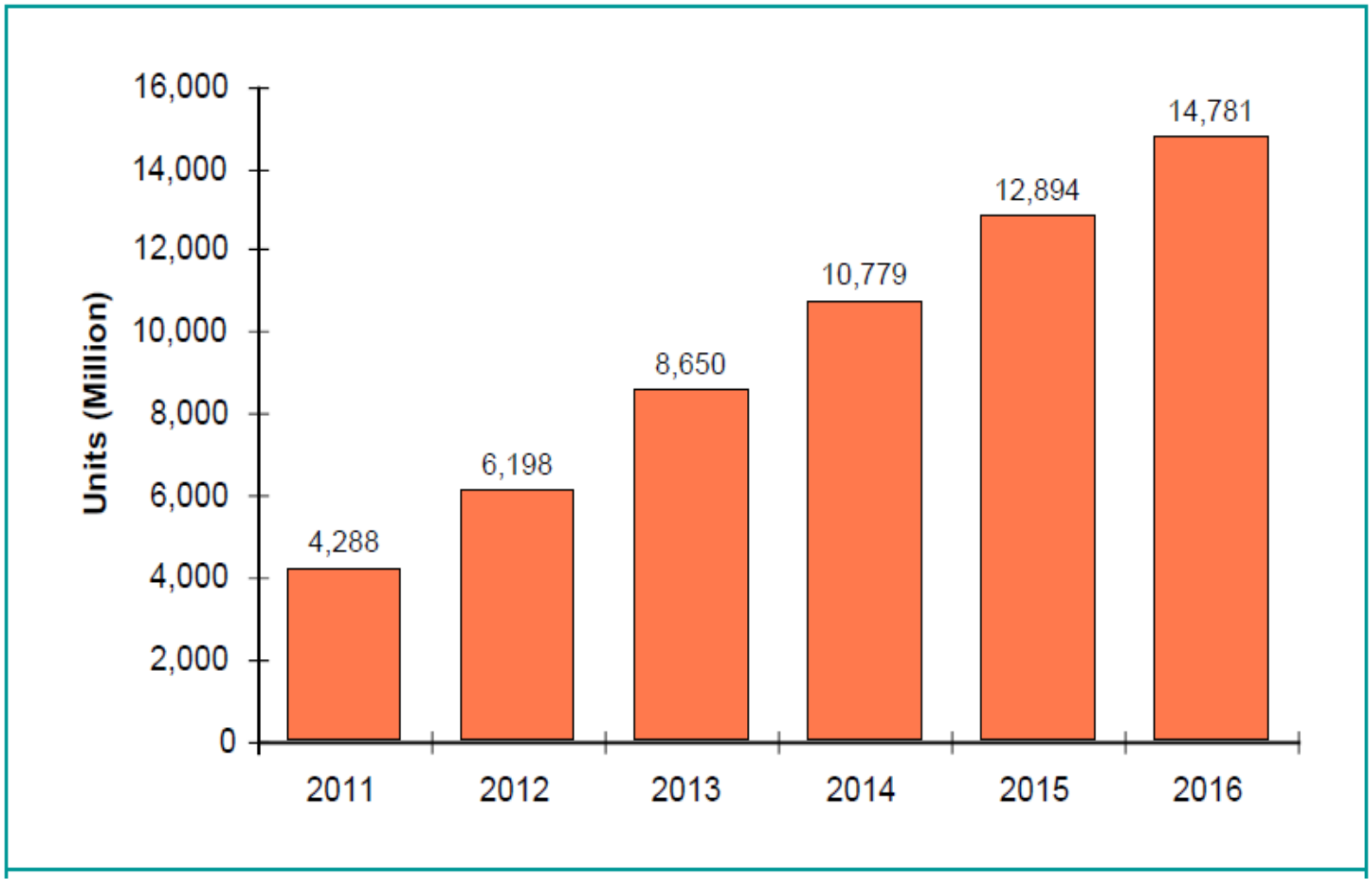
Cellular Handset IC Unit Forecast, 2011-2016



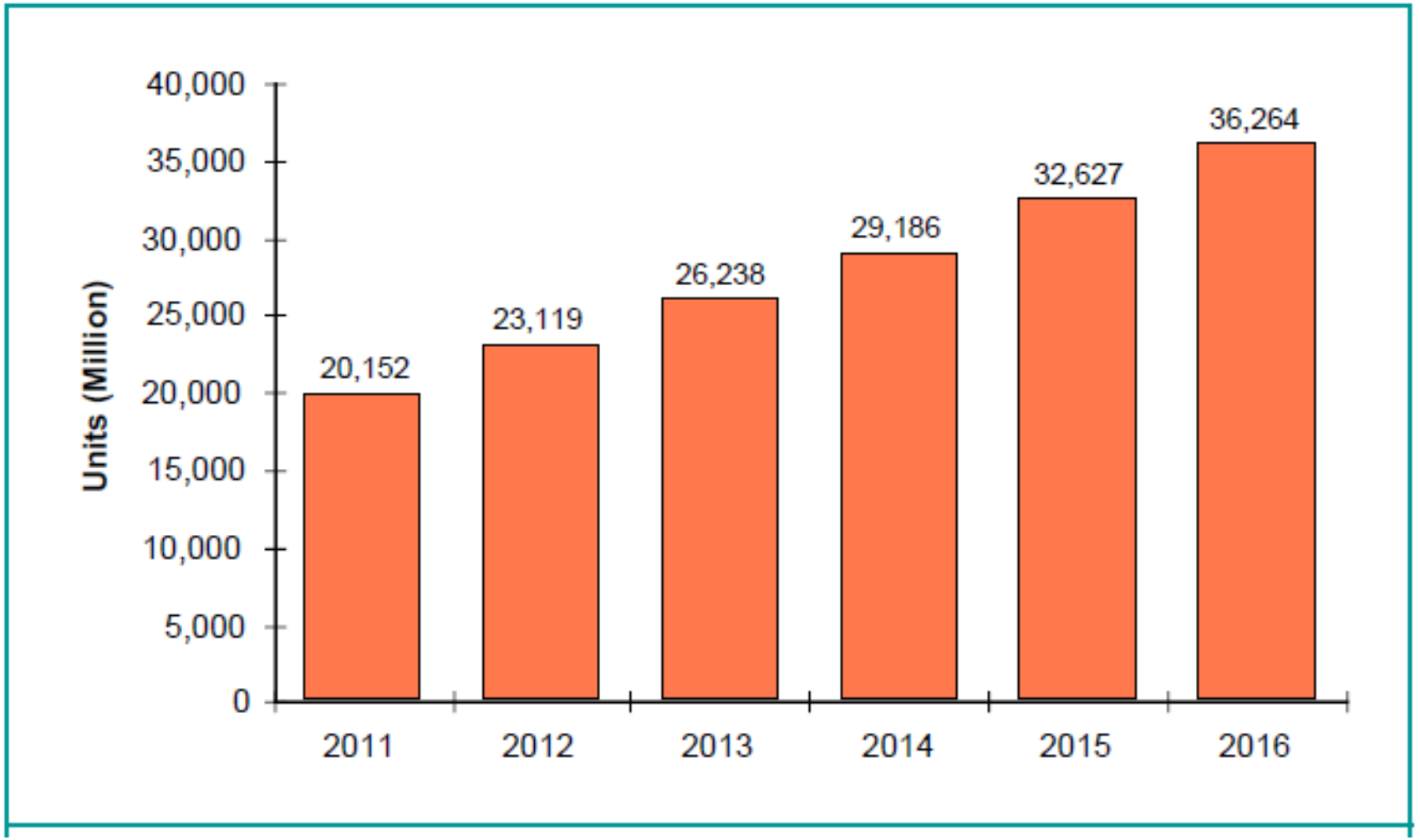
Cellular Infrastructure IC Unit Forecast, 2011-2016



Tablet IC Unit Forecast, 2011-2016



Netbook and Notebook IC Unit Forecast, 2011-2016



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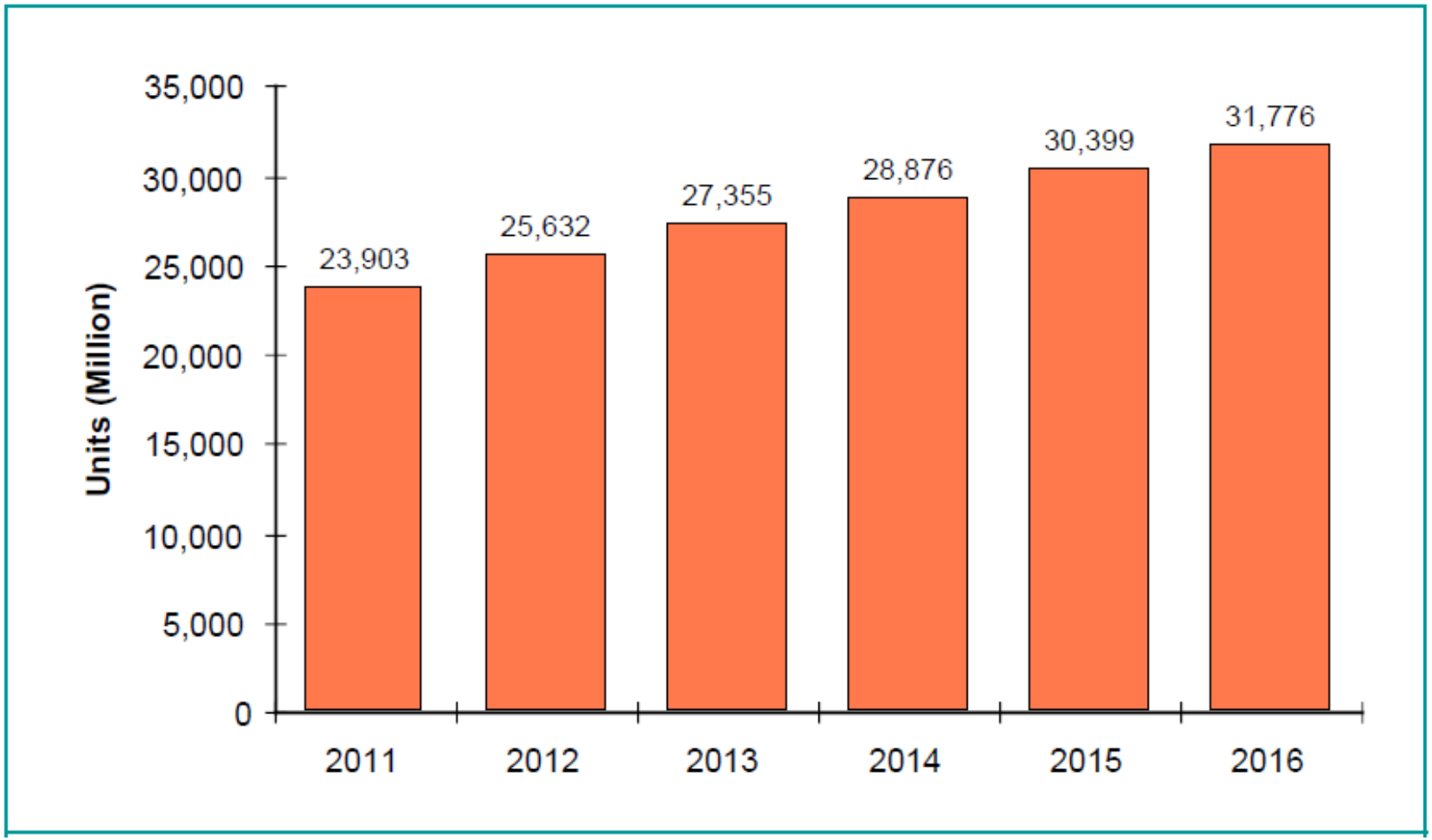
Desktop PC IC Unit Forecast, 2011–2016



Important IC Packages for Bandwidth Consumption

Enablers for Stacked Packages, SiP, Through-Via Technology, Flip Chip:

- FBGA
- BGA
- WLP / Fan-Out WLP (FO-WLP)
- QFN/ Fan-In QFN (FI-QFN)

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Stacked Packages

Stacked packages are a vertically packaged multichip package (MCP).

The interconnection of the upper die can go:

- Around the lower die with wire bonds,
- Through the die below, as in 3-D, through via technology, or
- Through an interposer to the substrate, or 2.5-D interconnection.

Types of Stacked Packages

- Die stacks, on a common substrate
- PoP, or package-on-package, aka package stacks
- PiP, or package-in-package, back-to-back in a single mold compound
- Stacked TSOPs
- Stacked QFNs / QFPs
- Stacked MCMs
- Stacked WLPs

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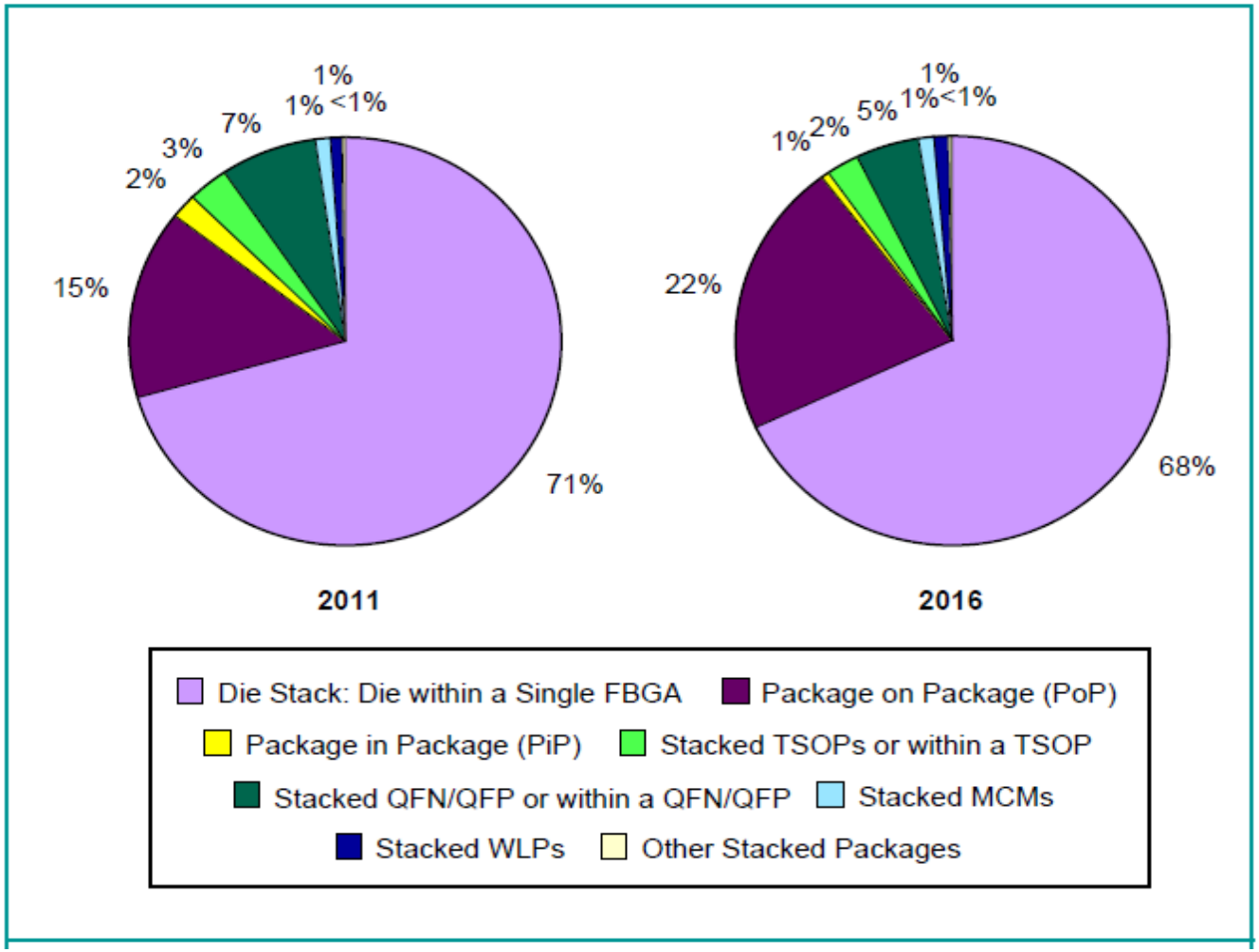
Stacked Package Units



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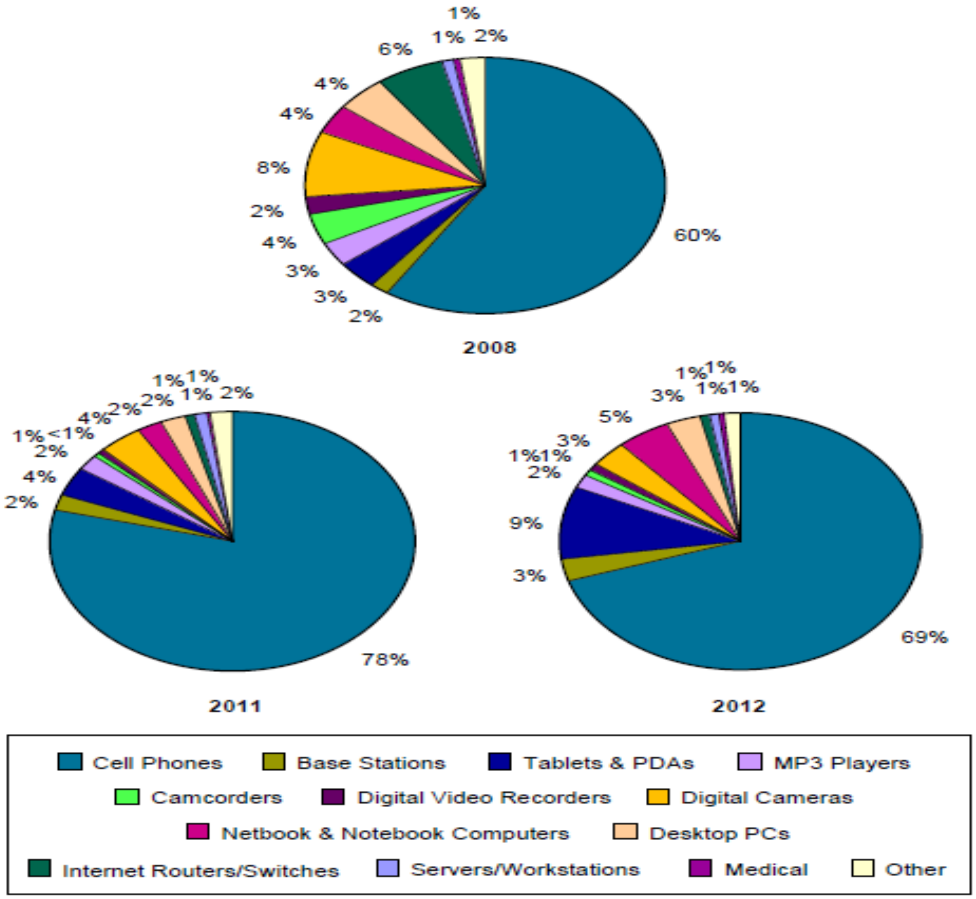
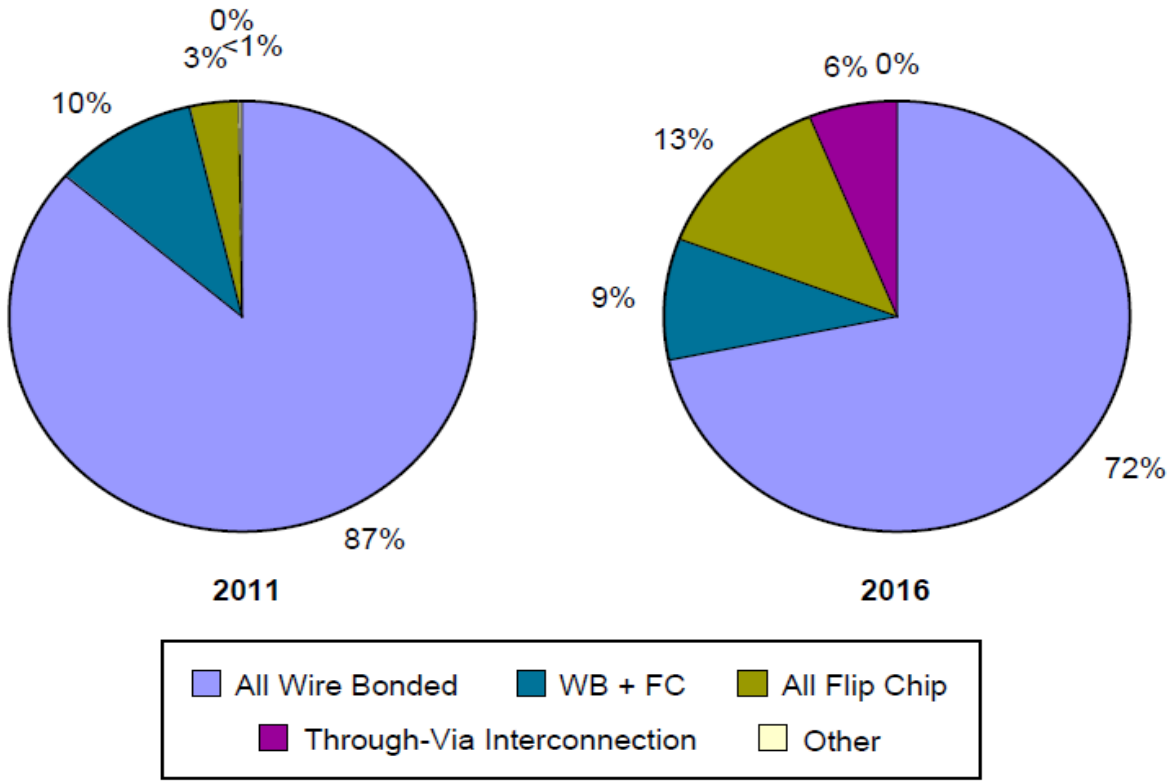
Applications Breakdown for Stacked Packages



Interconnection of Stacked Packages



System in Package (SiP)

A system in package (SiP) is a customized package with multiple elements inside, creating a functional block within a standard JEDEC footprint. This JEDEC footprint differentiates it from an MCM.

A functional block in the electronics world is a system of electronics that combines functional units together onto a single substrate to enable the shortest electrical distance between parts for superior performance. This also enables a more simplistic PCB for the final product, thus potentially reducing system costs.

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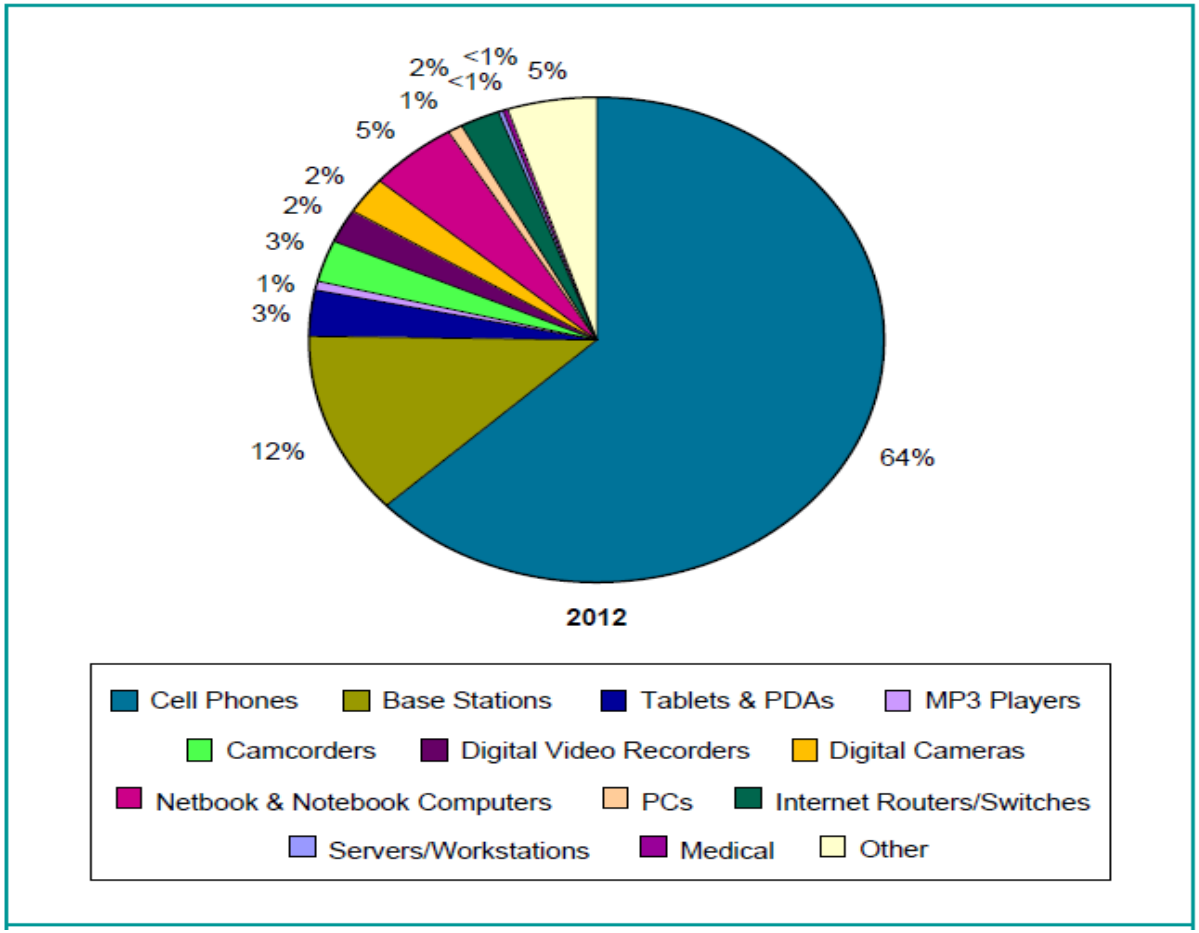
Applications Breakdown for SiPs, 2012



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TSVs, or Through Vias

- Through-silicon vias (TSVs) have been developed as an interconnection style for stacked packages or SiPs to address bandwidth issues
- 3-D and 2.5-D methods of vertical through interconnection
- Silicon, glass, and laminate interposers for 2.5-D interconnection

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3-D versus 2.5-D

- **2.5-D**: Chips are partitioned and placed side by side on an interposer with through-vias to a substrate below. The interposer and microbumps act as Redistribution Layer, or RDL.

- **3-D:** Die are stacked vertically, with through vias going through the bulk silicon to connect each one to the next.

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3-D versus 2.5-D

2.5-D

- Avoids thermal issues of stacking the die
- Less complex; through vias go through an interposer, not active silicon
- Interposer and microbumps for routing between layers
- Silicon interposers accommodate the CTE mismatch between the layers in a stack, acting as a stress reducer, thus improving reliability

3-D Interconnect

- Higher thermal issues
- More complex, vias go through active silicon
- Interposer and microbumps for routing between layers
- More potential reliability concerns
- Highest degree of bandwidth, can achieve 100 times the connectivity or bandwidth, with less power consumption, when compared to wire bonding
- Has the shortest interconnection distance, enhancing the characteristics of high speed, low power consumption, reduced parasitics, and small form factor.

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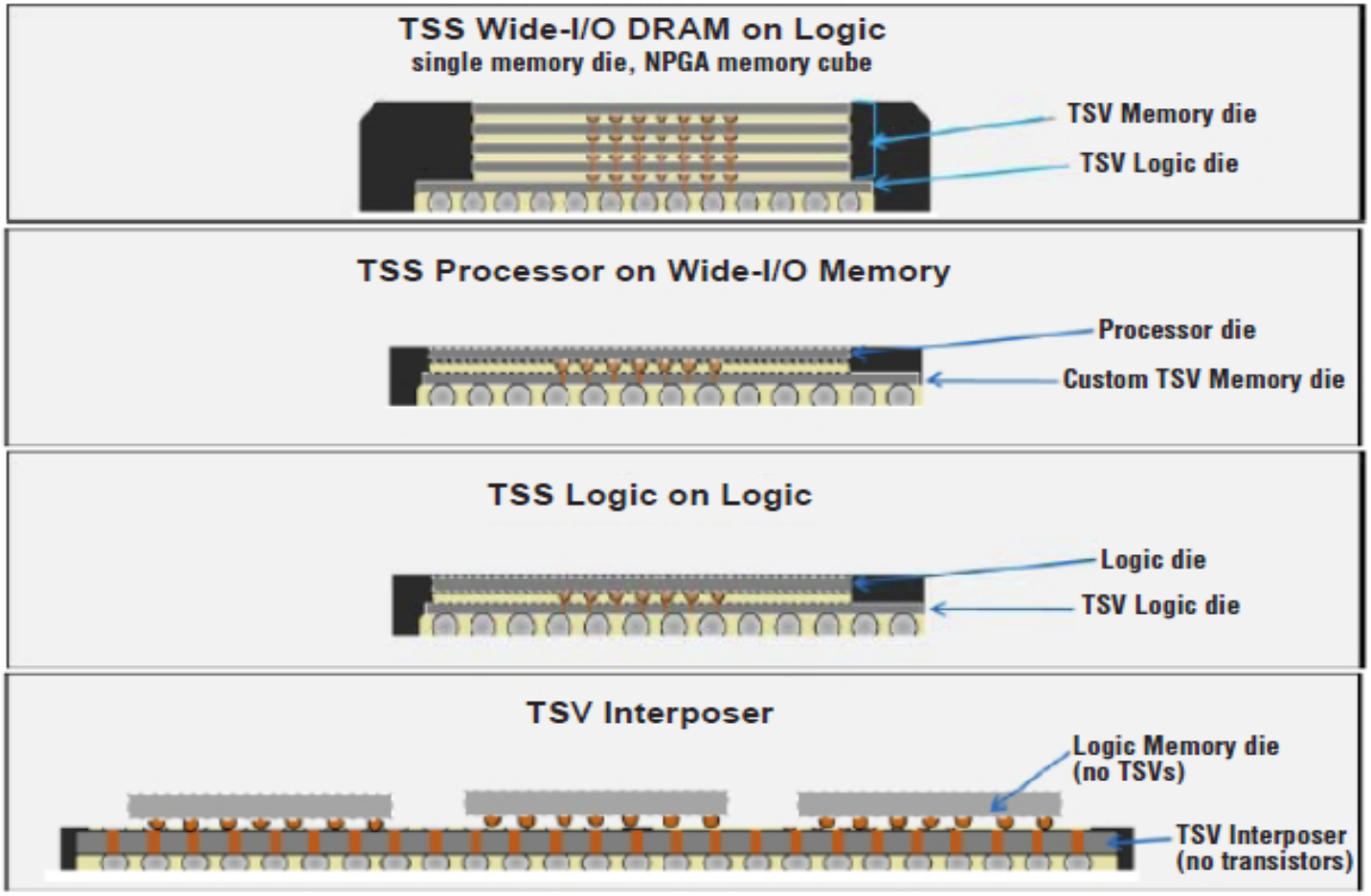
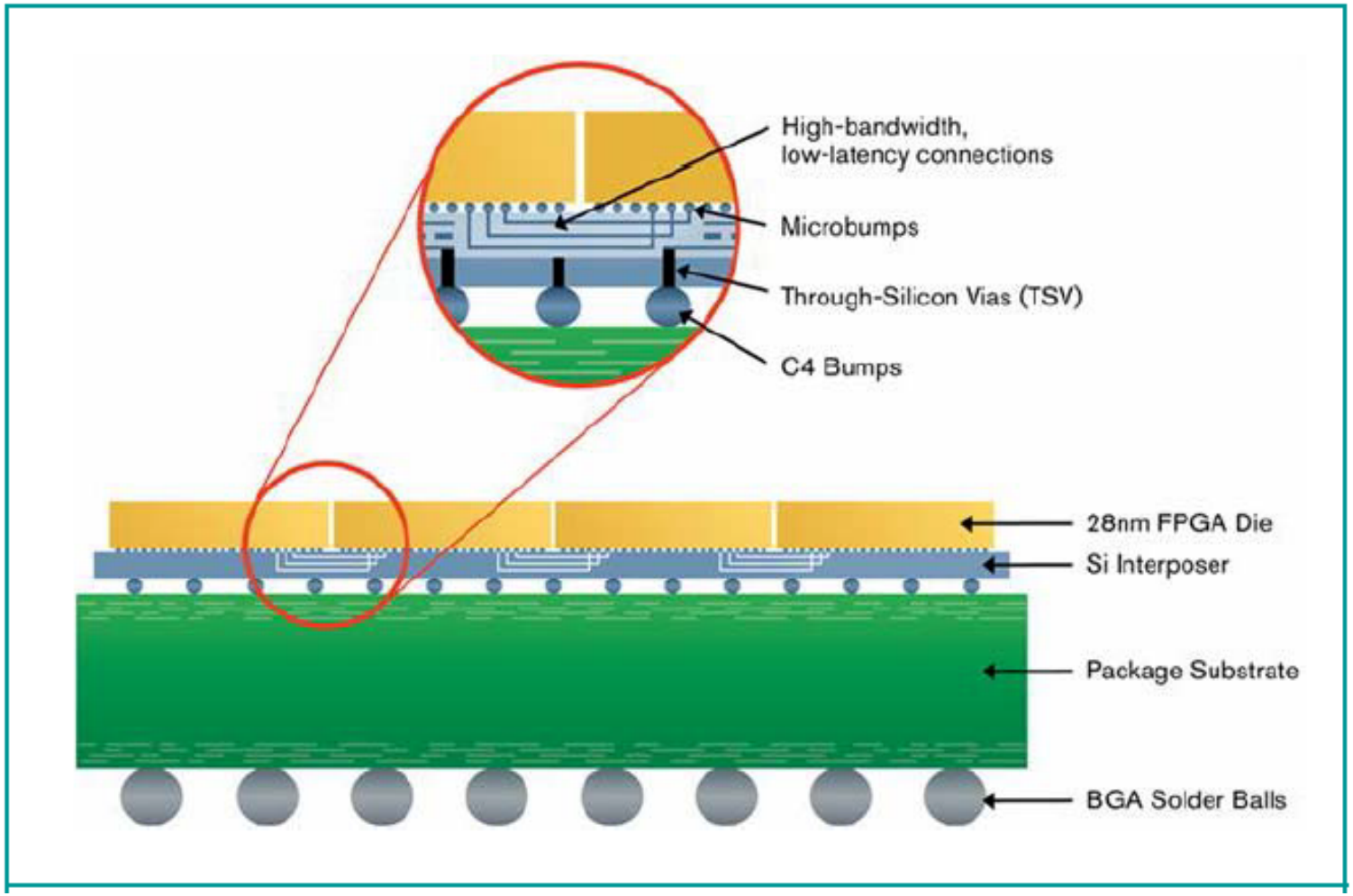
TSV Chip Partition Examples

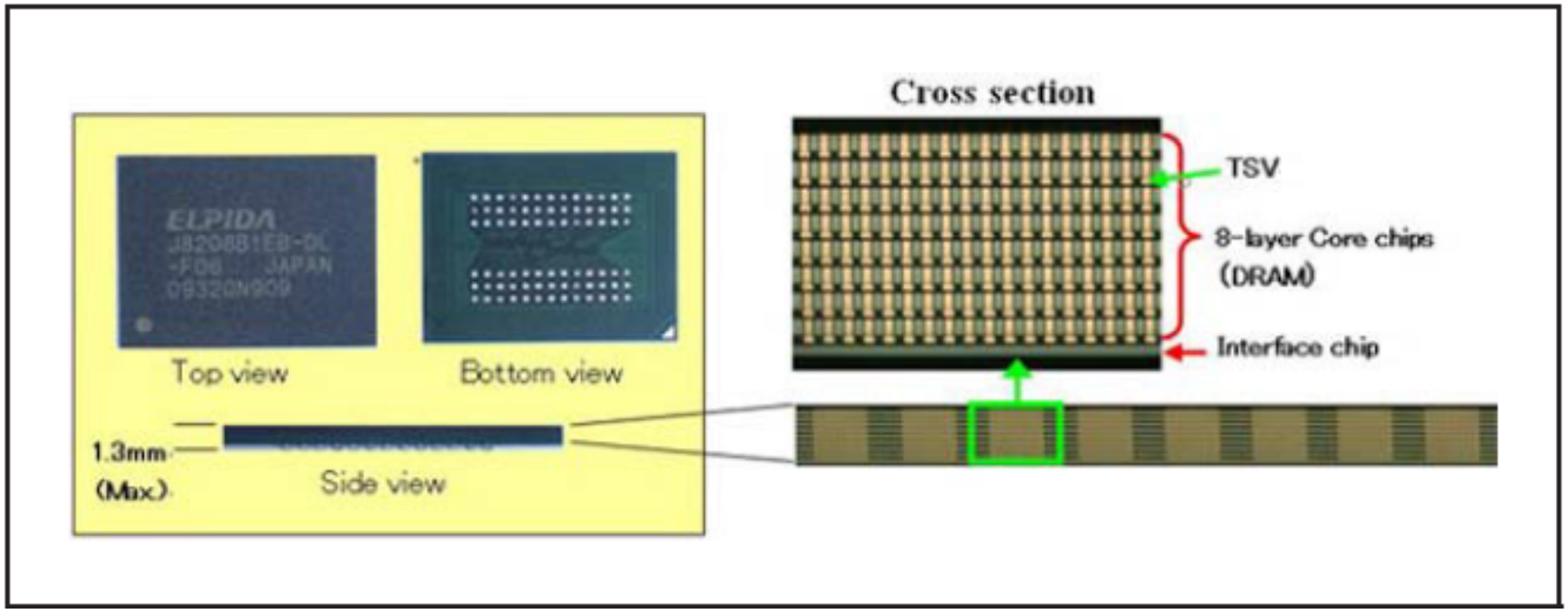
Courtesy of Qualcomm and IWLPC



Xilinx's 2.5-D Structure



Elpida's 8-Gigabit TSV DRAM Package Outline and Cross Section



Altera Corporation and TSMC chip-on-wafer-on-substrate (CoWoS)

- Altera Corporation and TSMC jointly developed the world's first heterogeneous 3-D IC
- Heterogeneous 3-D ICs include analog, logic, and memory devices
- The process flow is to attach the device silicon chips onto the silicon interposer wafer, dice the wafer, and then attach the stacked silicon onto the substrate (CoWoS)

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TSV Potential Markets, 2011–2016

	2011	2012	2013	2014	2015	2016	CAGR (%)
			Potential Units (M)				
MPUs	534	557	605	644	678	733	6.5
DRAM	16,087	16,570	18,144	19,849	21,576	23,691	8.0
Special-Purpose Logic:							
Communications	7,772	8,549	9,832	11,257	12,799	14,655	13.5
PLD and FPGA	1,662	1,883	2,209	2,538	2,898	3,336	15.0
Graphics	753	778	849	909	967	1,038	6.6
Flash	10,213	10,948	12,328	13,709	15,162	16,829	10.5
Total Potential Market	**37,021**	**39,285**	**43,966**	**48,906**	**54,080**	**60,282**	**10.2%**
TSVs as a Percentage of the Total Potential Market			0.3%	0.6%	0.7%	0.9%	—

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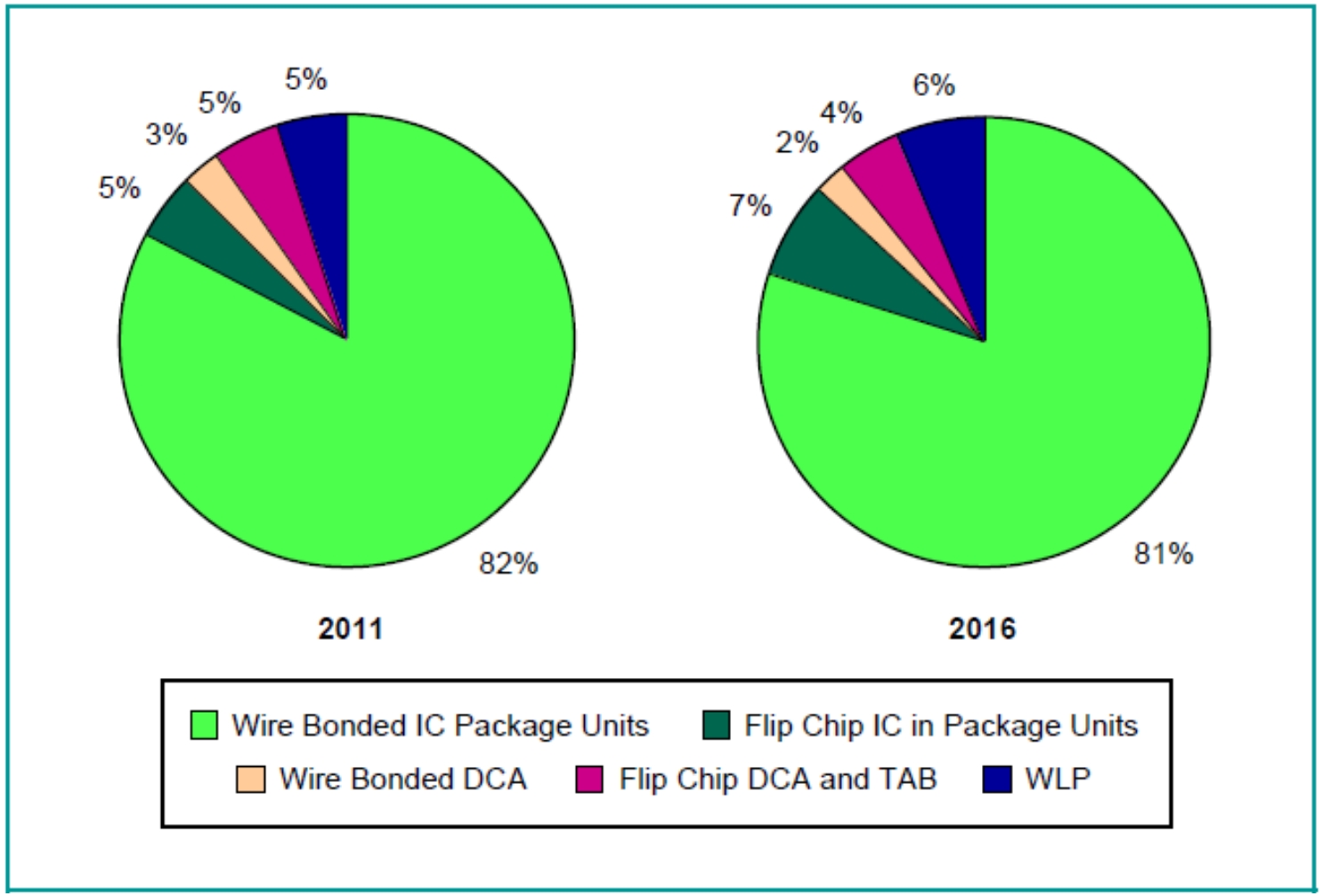
Total Interconnection for ICs, 2011 vs. 2016



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Flip Chip Interconnection

- The die is flipped face down (or active side down) so that the circuitry faces the substrate
- Bumps, not wires, create the electrical path, and is an area array covering all or part of the face of the die
- Generally for packages with substrates, although a few designs utilize leadframes
- Leadframe designs can have the die oriented upwards, and the leadframe reach over the top

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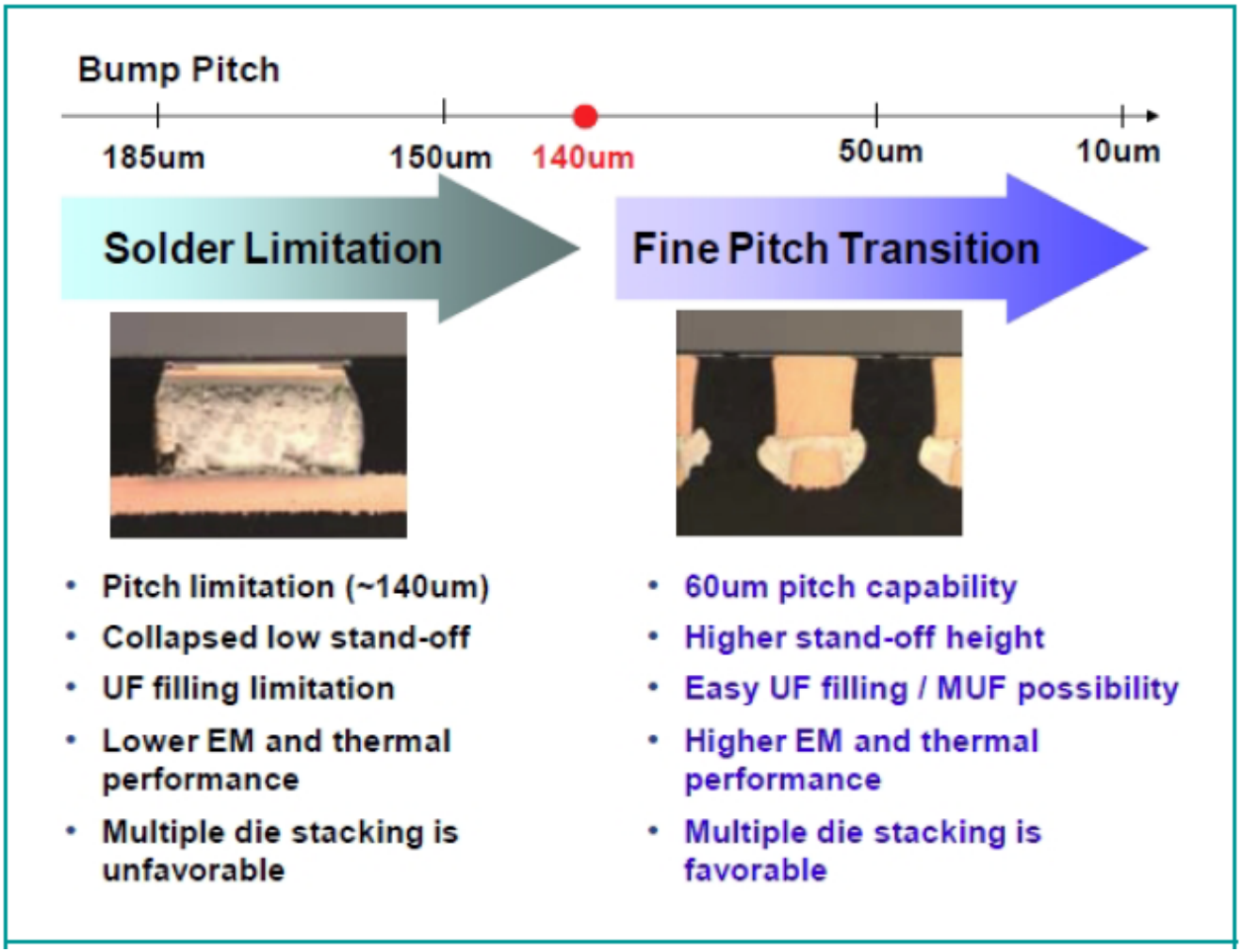
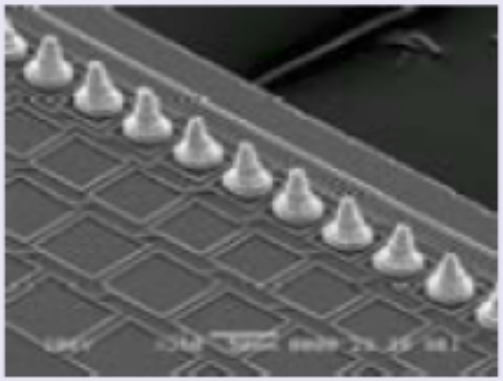
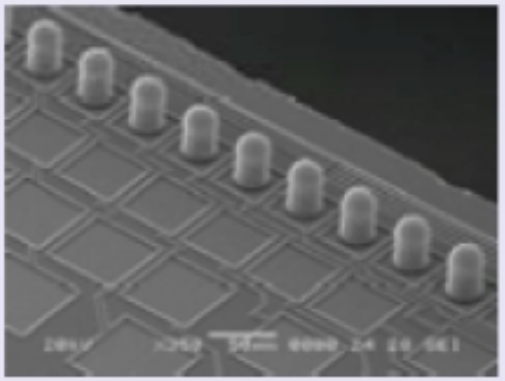
Solder Limitation to Fine-Pitch Flip Chip

Courtesy of Texas Instruments, Amkor Technology Korea, Amkor Technology, Inc., and ECTC



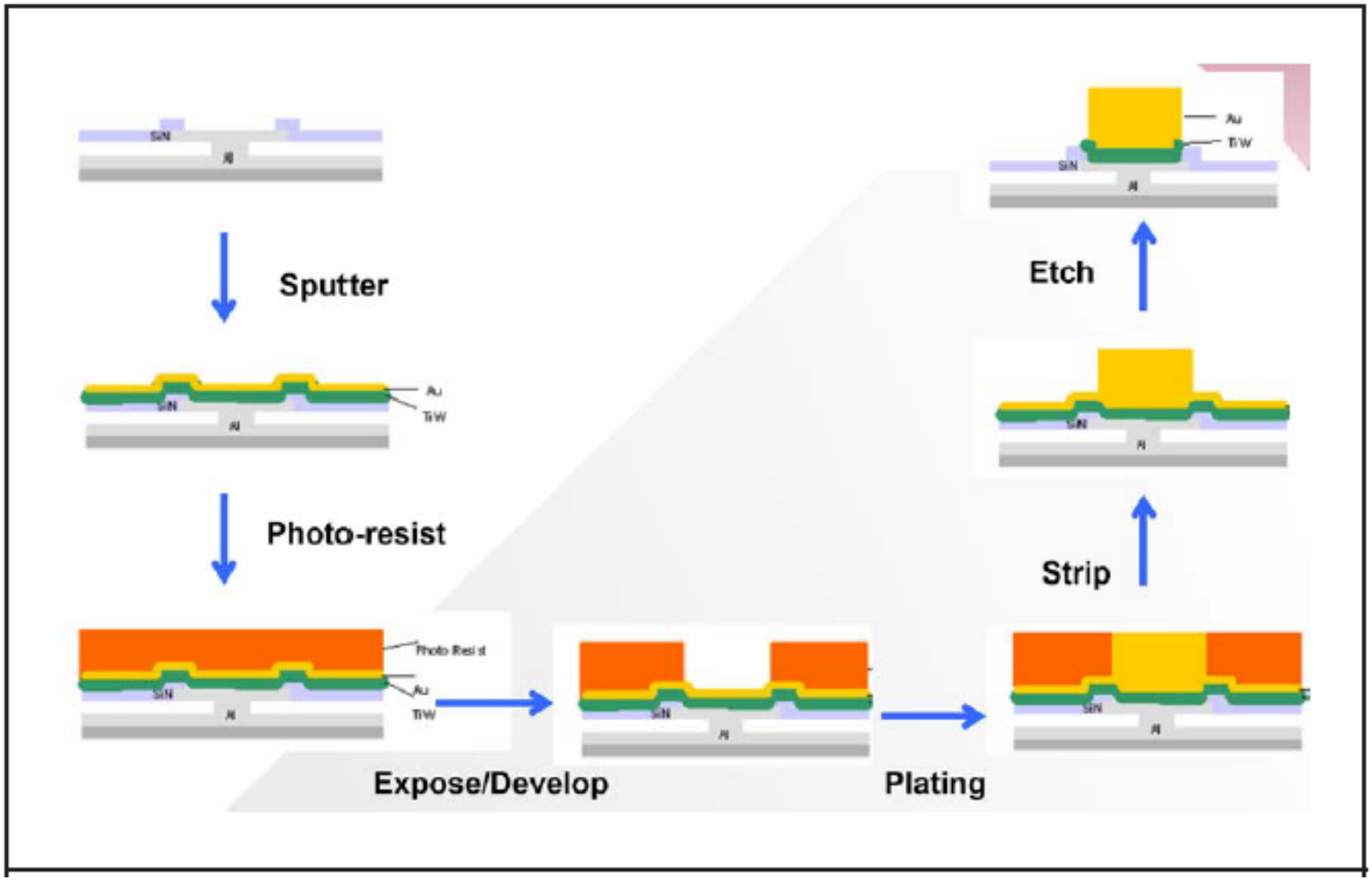
Solder Flip Chip and Fine-Pitch Flip Chip

Courtesy of Texas Instruments, Amkor Technology Korea, Amkor Technology, Inc., and ECTC

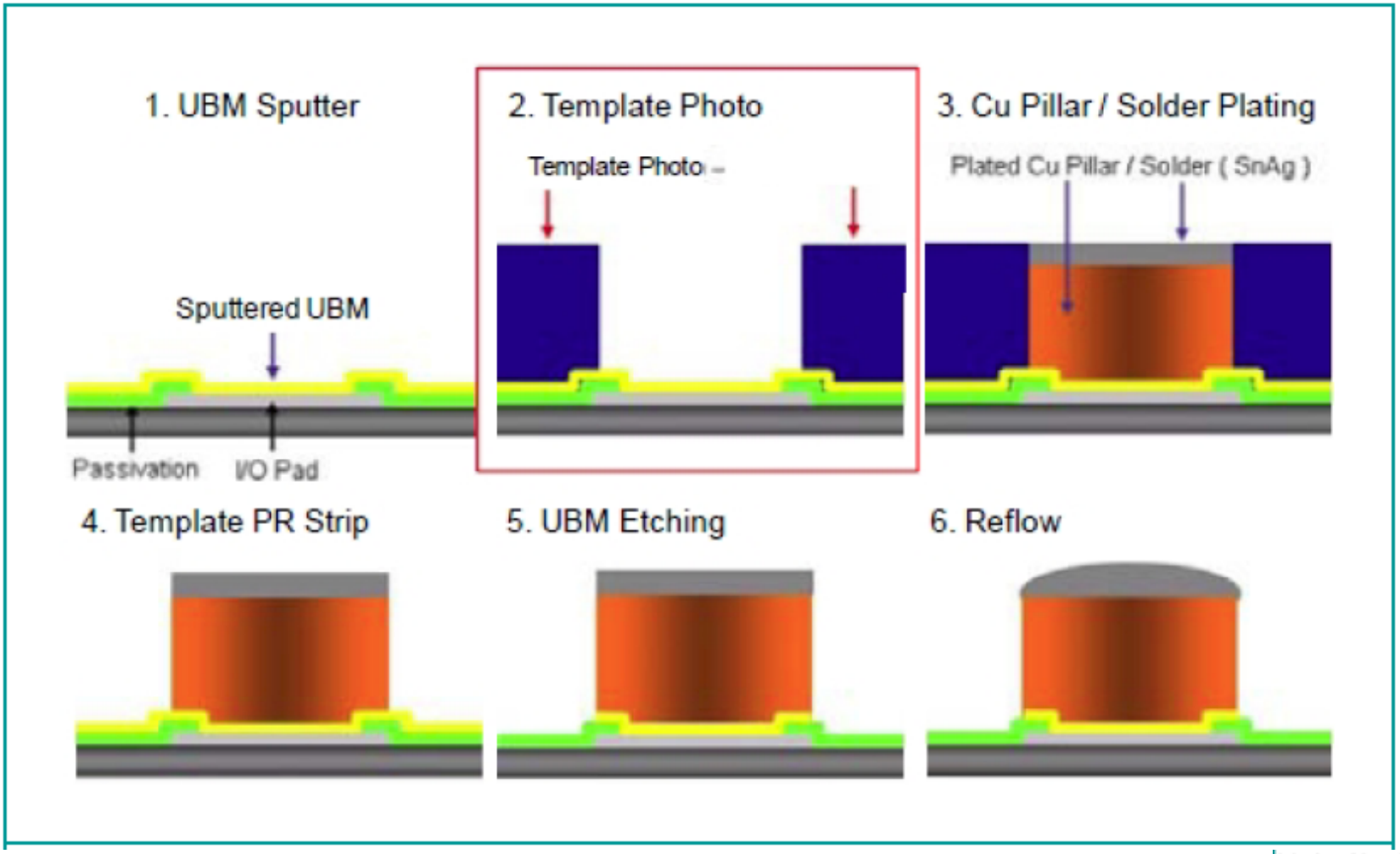
Conventional Solder Flip Chip	Fine Pitch Gold Stud Flip Chip	Fine Pitch Cu Pillar Flip Chip
		
140-180um minimum pitch	50um in-line pitch	

Gold-Bumping Process

Courtesy of NEXX Systems and IMAPS

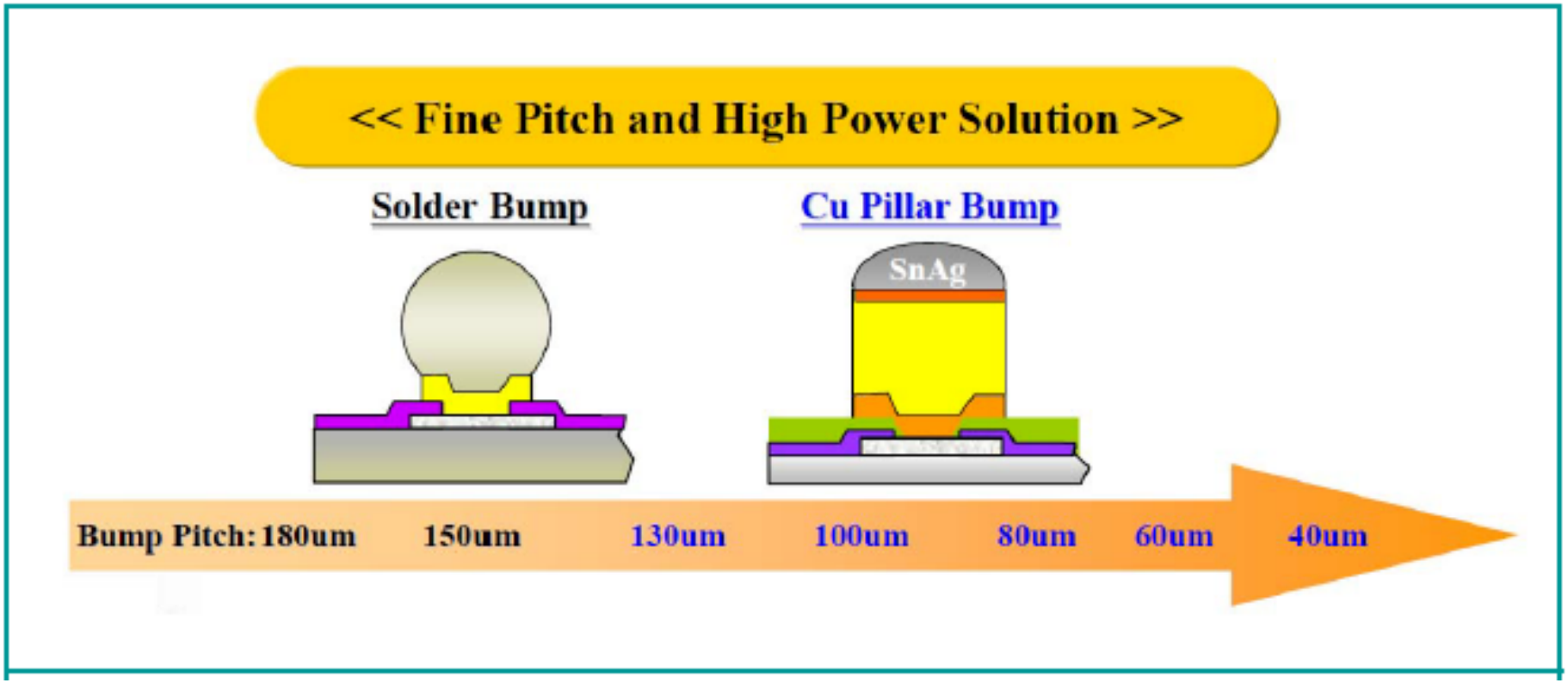


Copper Pillar Bumping Process Flow



Copper Pillar Bump

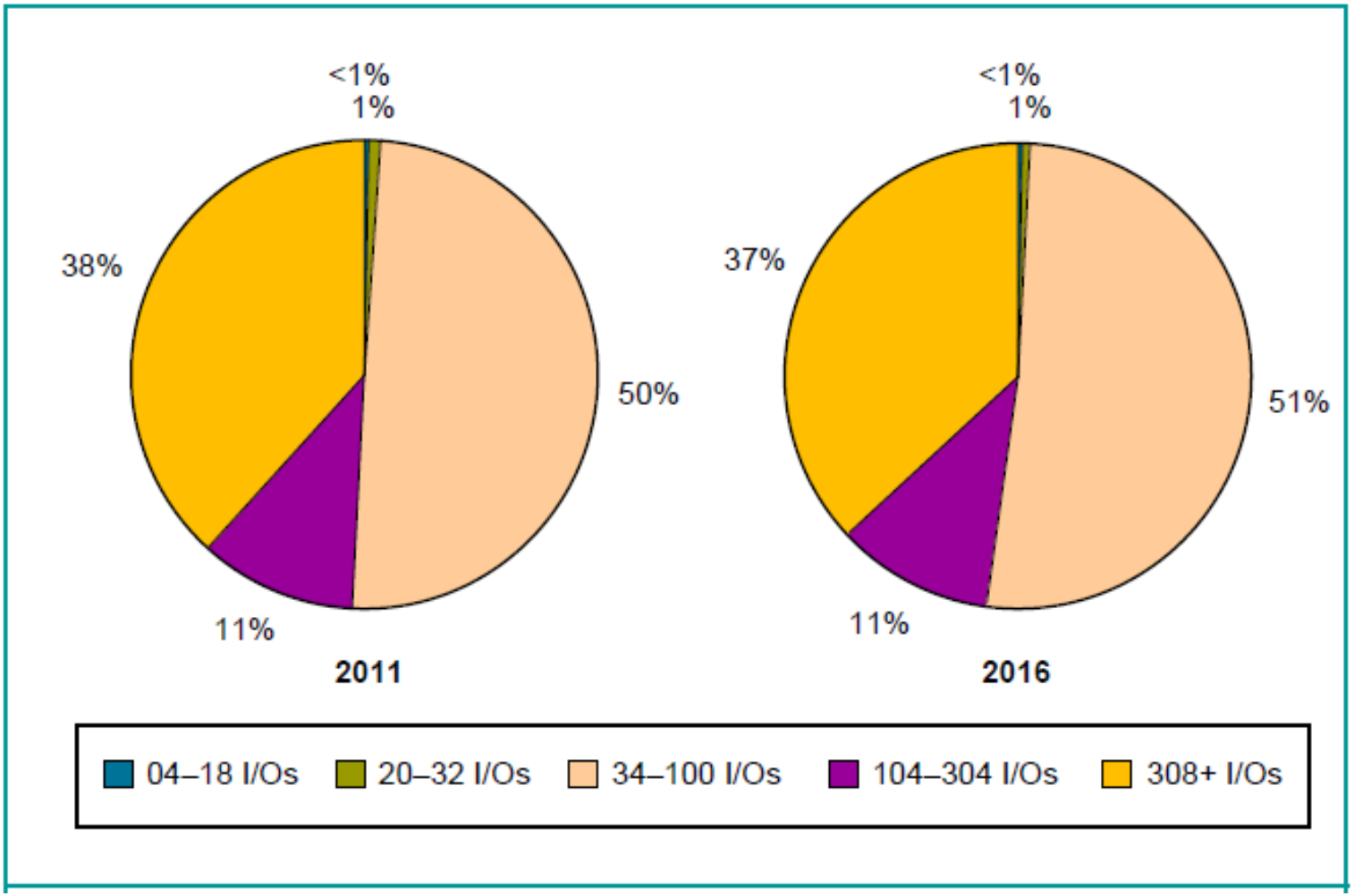
Courtesy of Siliconware Precision Industries Co., Limited and ECTC



Devices which Utilize Flip Chip

- MPU
- MCU 32-bit
- DSP
- Gate Array
- Standard Cell & PLD
- Special purpose logic: consumer, computer, communications, auto, other
- DRAM
- SRAM
- Flash
- Analog: communications, computer

Percentage of Flip Chip I/O Count Range, 2011 vs. 2016



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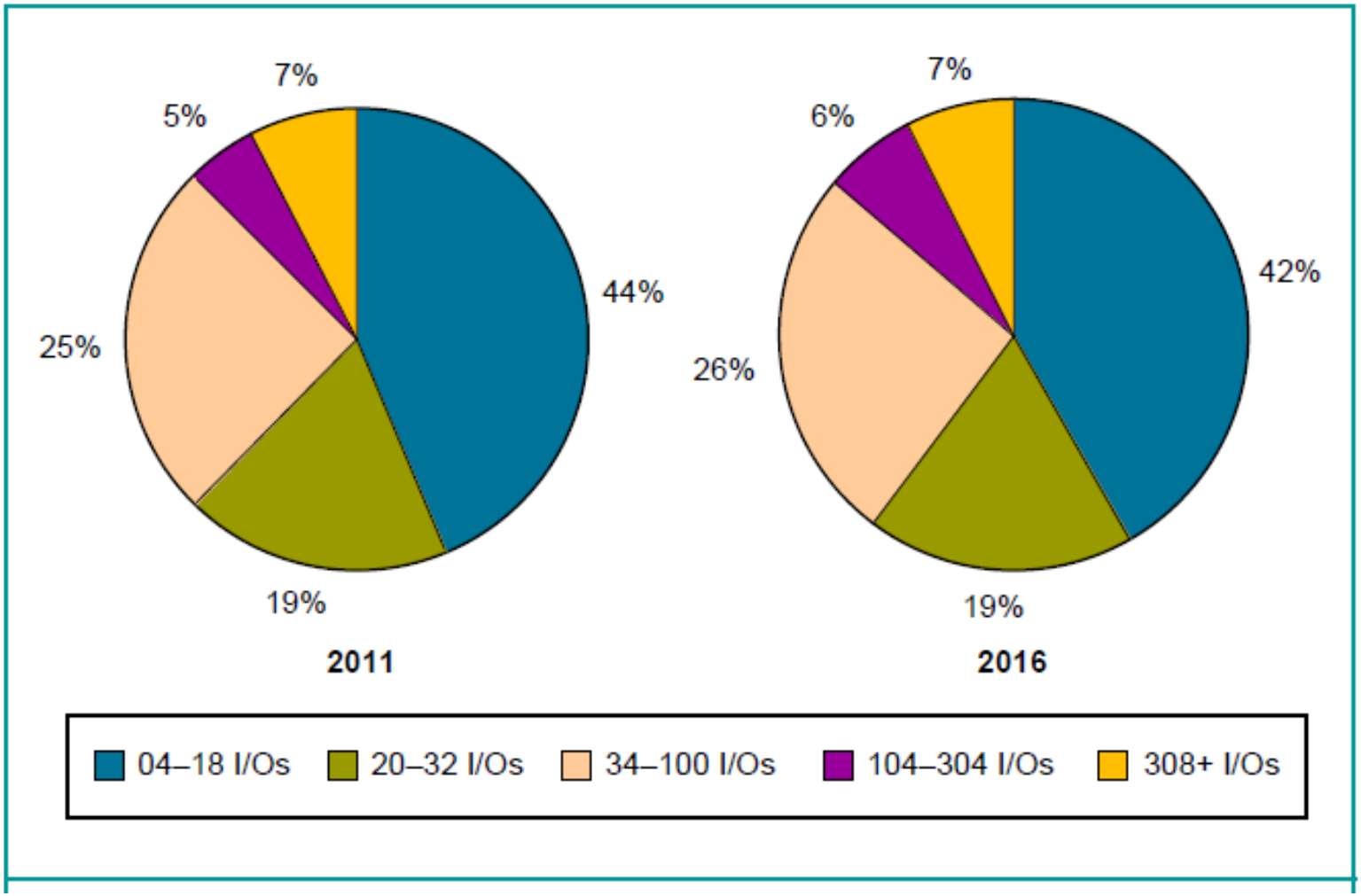
Percentage of the Total Worldwide I/O Count Range, 2011 vs. 2016



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Conclusion

- Increased bandwidth is required to meet today's and tomorrow's Internet demand
- Front end nearing the end of its ability to continue shrinking
- Backend IC packaging is now key to increasing bandwidth capabilities, by putting devices closer together, shortening the distance the electron must follow, with fewer parasitics, straightening the electron path, with fewer material changes

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