Optimizing IP for Cost-Effective
2.5D Integration
January 14, 2014
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eSilicon®

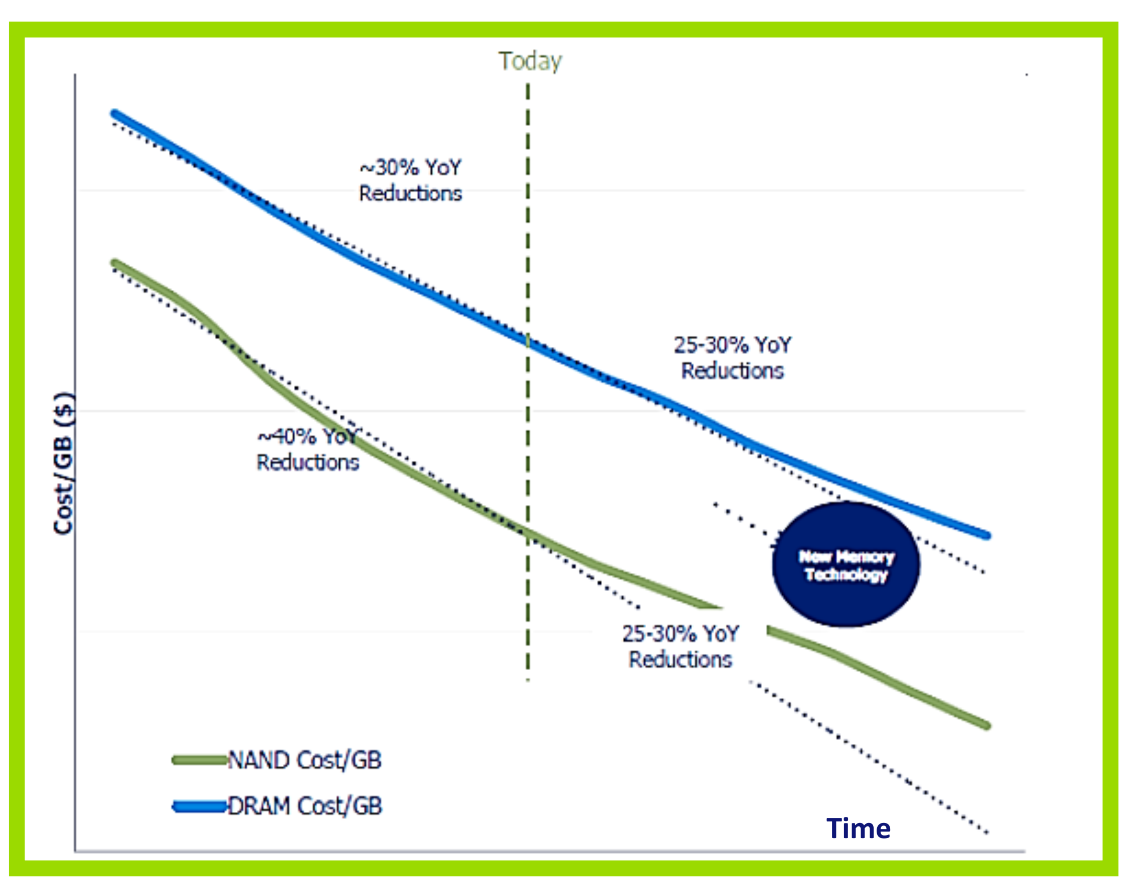
Market Dynamics

- Next generation high performance computing (HPC), graphics and networking applications require 2.5D/3D integrated memory
  - Bandwidth expansion
  - Memory enhancement
  - Product feature set expansion
  - Energy efficiency
  - Integration

Memory Cost Scaling Challenge

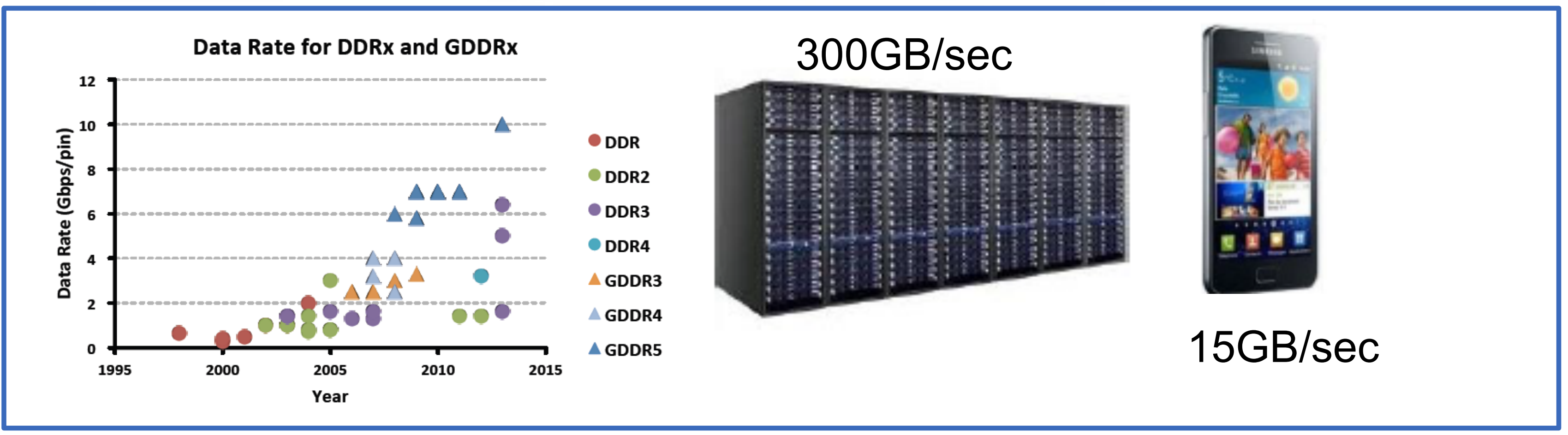
- Physical and electrical materials challenges
- Equipment capability
- Cost and complexity

Memory Cost Scaling Over Time



Source: Mike Black, Micron, EDPS 2013

Memory Bandwidth Demand

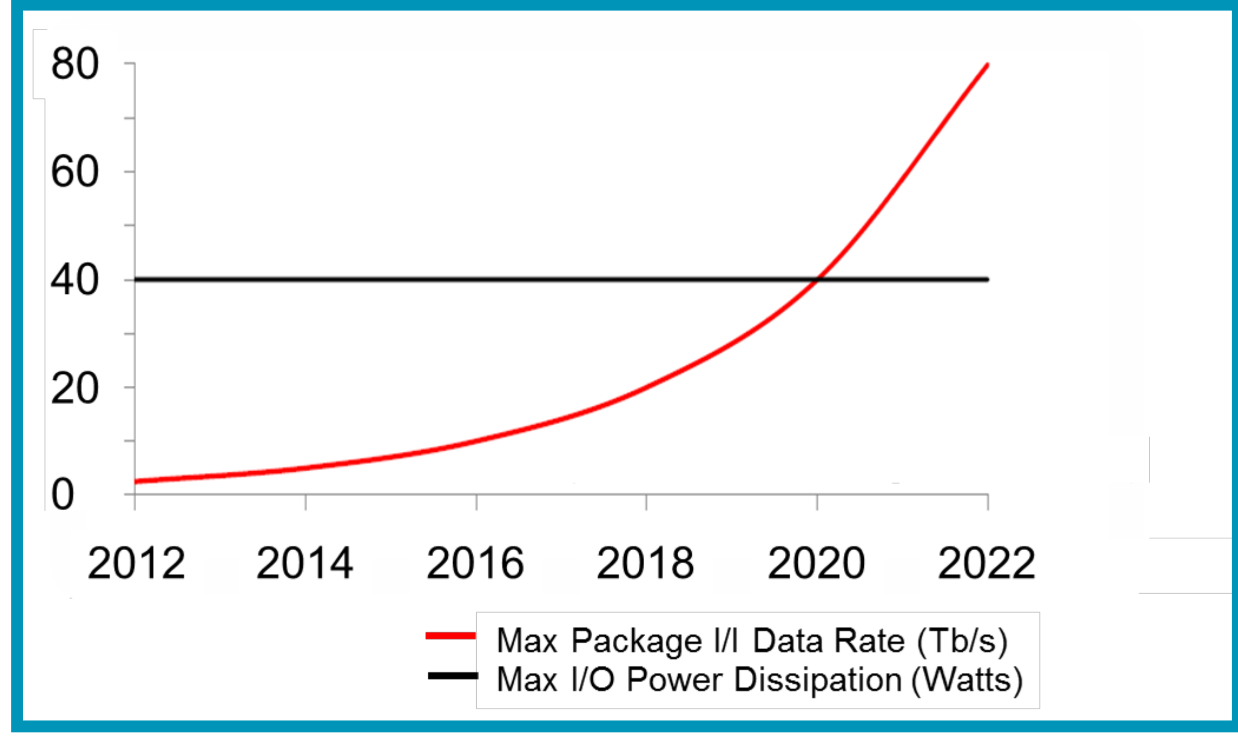


- Complex systems use ***many*** external DRAMs (DDR3/DDR4/LPDDR3/LPDDR4) for packet buffering
  - Limited bandwidth of DDRx devices now requires very high numbers of DRAM devices connected to the central ASIC
    - To buffer 1Tbps would require 40 DDR3 DRAMs all connected through separate buses
  - ASICs already at >1,500 pins and typically pin-limited. Very difficult to increase bandwidth to memory using current approach
    - DDR4 does not solve the problem – 1Tbps would still require 20 DRAMs
  - Current approach consumes a lot of power
- Traditional off-package interconnection between CPU and memory chip not going to scale
- Packaging and interconnect technology vital in defining memory sub-system performance

Source: Intel Tech Journal August 2007/ Yole Dec.2014

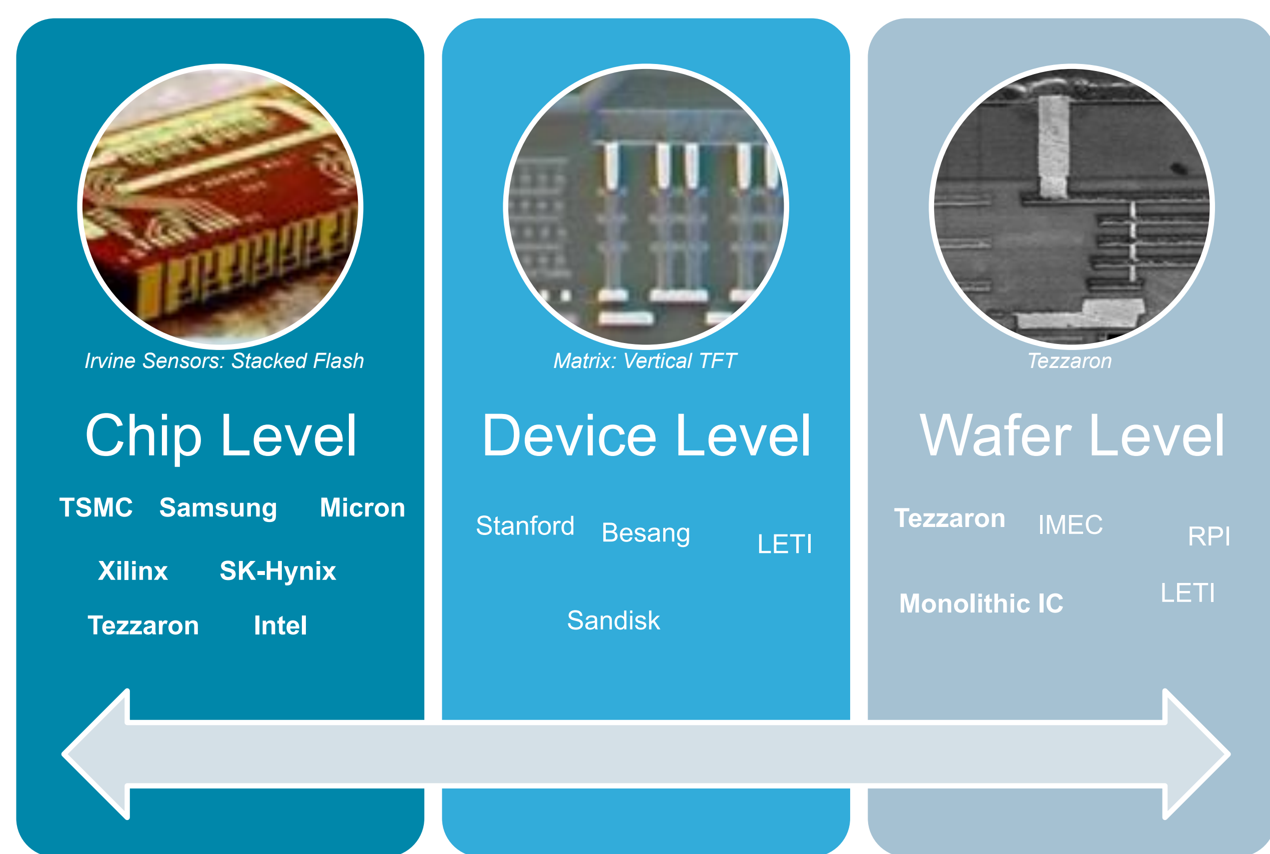
Power Efficiency Requirement

- Scaling of I/O date rate with constant I/O power dissipation
- Even more challenging for computing memory subsystem memory bandwidth (BW) scaling



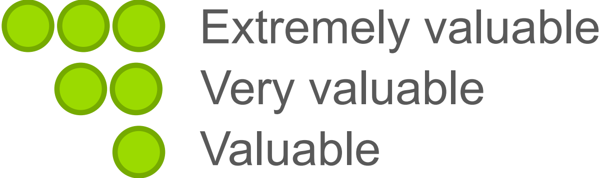
Source: ITRS 2011 Roadmap & Dr. Bill Bottoms

Approaches to 3D Integrated Circuits



Value Proposition for Higher Value Packaging

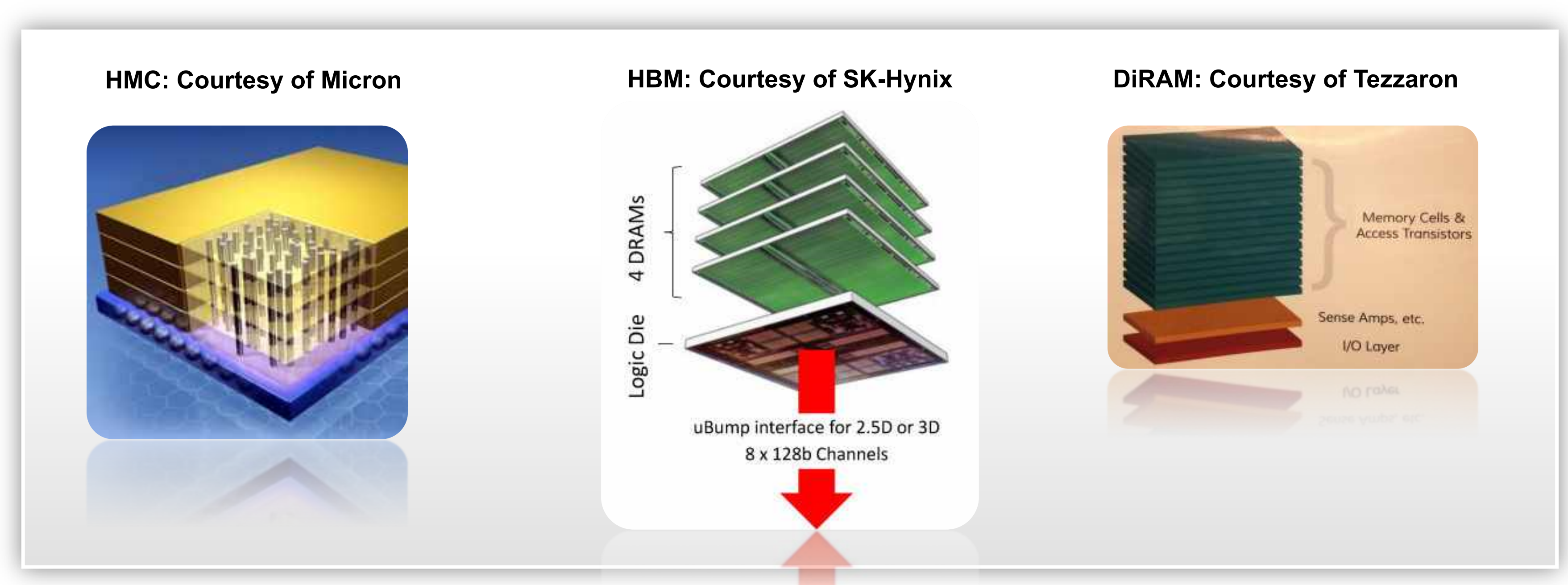
Market / Benefit	Low Power Dissipation	High Bandwidth CPU <-> DRAM	Low Latency IC <-> IC	Heterogeneous Integration	Form Factor
Cellphones and esp. Smartphones	●●●	●●	●	●●	●●●
Compute **servers**, Network routers	●●	●●●	●●●	●●	●
Tablets and other Mobile devices	●●	●●	●	●●	●
Standard PCs and Workstations	●●	●●	●	●	●
Automotive applications	●	●●	●●	●●	●



Extremely valuable
Very valuable
Valuable

Other decision factors: unit cost, system cost savings, NRE, time-to-profit, risk, etc.

Stacking Memory Technologies

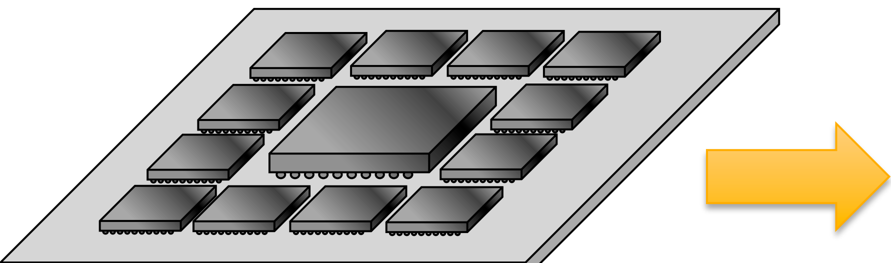


Markets for TSV- Based 3D Packaging Technologies

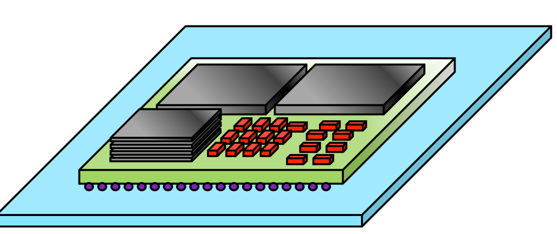
Market	Smart Phone	Tablet	Networking	Graphics
Processor	Apps. Processor	Apps. Processor	Networking Processor	Graphic Processor
Power	1 – 2W	1 – 5W	20W+	20W+
Memory Type	Wide I/Ox	Wide I/Ox or LPDDRx	HMC/HBM	HBM
Memory Size	2 –> 4 GB	4-> 8 -> 16G B	4-> 8 -> 16G B	4 -> 16GB
Interface	WideI/O2	Wide I/Ox Or DDR	SerDes or Parallel	Parallel
I/O	1000	1000 or 500	<500 or >1000	1024 (>1600 total)
Min. Bump Pitch	40x40um rows	40x50um rows or 80um rows	1mm/95x55um array	55x55um array/ staggered rows
Packaging	3D	2.5D medium L/S density or 3D with heat management	Off chip memory or 2.5D high density interposers	2.5D high density interposers

2.5D Increases Bandwidth

Current solution: ASIC plus multiple DRAMs

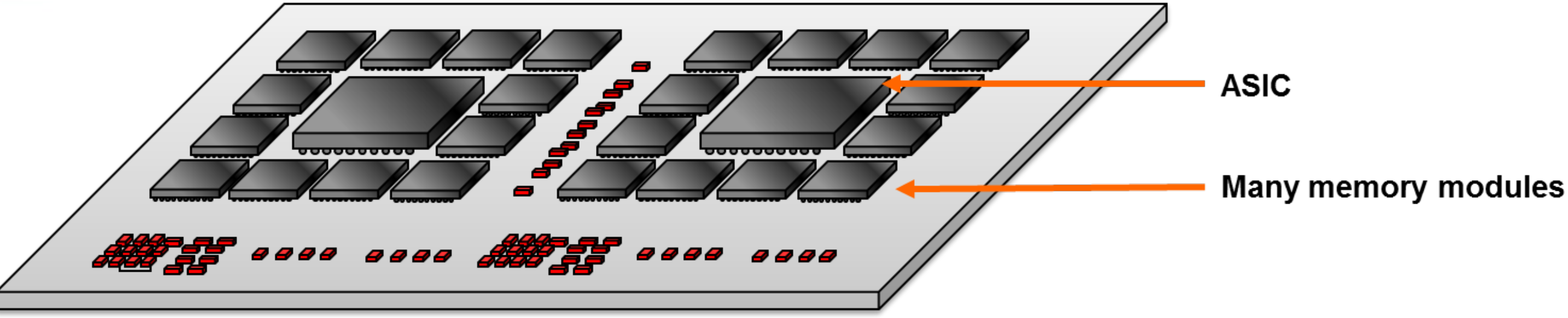


New solution: single package containing ASIC plus memory stack(s)

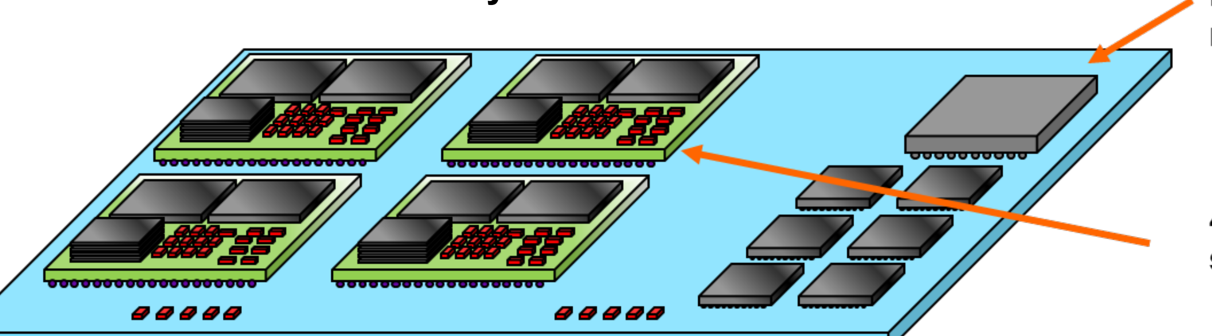


- Using an interposer allows the integration of highly parallel connections to memory stacks inside the package
- Much higher total bandwidth
- Significant reduction in power consumption
- Much smaller board footprint

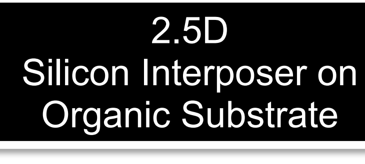
2.5D Reduces Cost

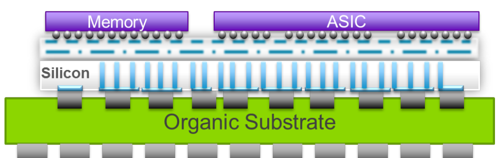


- Complex systems require multi-layer PCBs of 20+ layers – very expensive
- Typically, only a small percentage of the board requires the connection density that drives layer count
- Using an interposer removes the high density interconnect from the board
  - **Reduces the layers required and cost**
  - **Increases the manufacturability and signal integrity**
  - **Increases density**

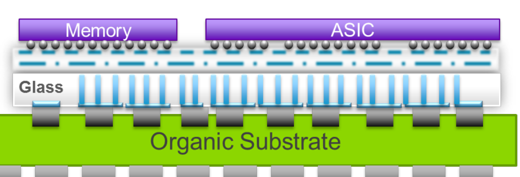


Interposer Technology Scenarios

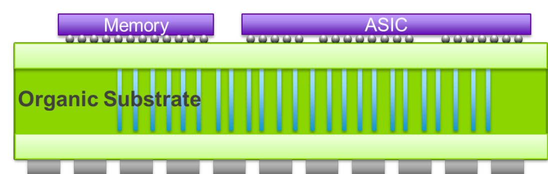




2.5D
Glass on
Organic Substrate



2.1D
Hybrid Organic
Substrate

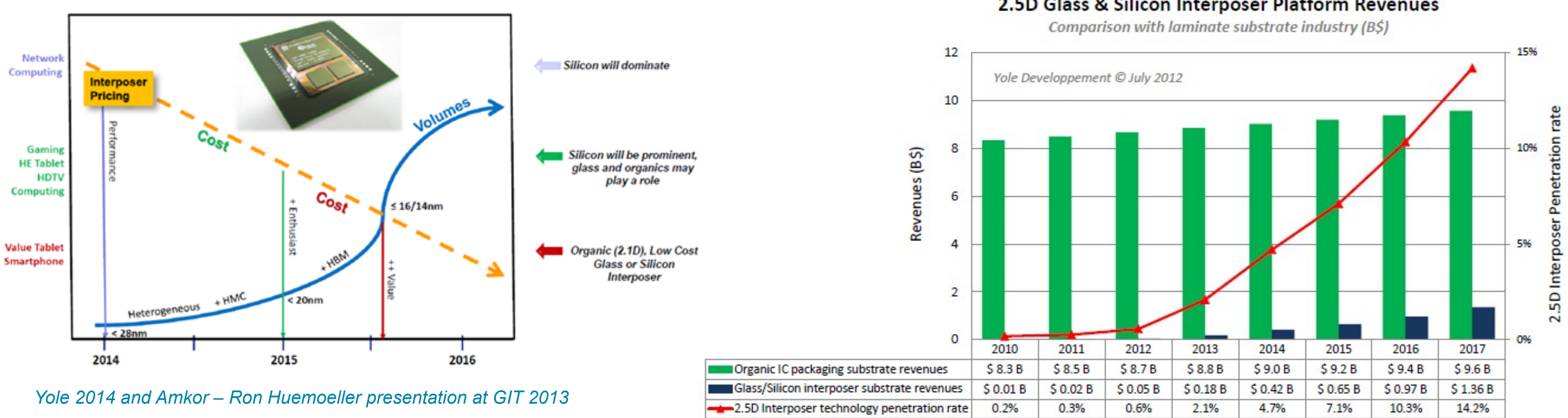


2.5D
Low Cost Silicon on
Organic Substrate

High-end Applications | Mid-range Applications | Consumer High Volume

2015 | 2016 | 2017

2.5D Market Assessment



	2010	2011	2012	2013	2014	2015	2016	2017
Organic IC packaging substrate revenues	$ 8.3 B	$ 8.5 B	$ 8.7 B	$ 8.8 B	$ 9.0 B	$ 9.2 B	$ 9.4 B	$ 9.6 B
Glass/Silicon interposer substrate revenues	$ 0.01 B	$ 0.02 B	$ 0.05 B	$ 0.18 B	$ 0.42 B	$ 0.65 B	$ 0.97 B	$ 1.36 B
2.5D Interposer technology penetration rate	0.2%	0.3%	0.6%	2.1%	4.7%	7.1%	10.3%	14.2%

Yole 2014 and Amkor – Ron Huemoeller presentation at GIT 2013

- According to Yole Développement, the market value of all the devices using TSV packaged in 3D in the 3D-IC or 3D-WLCSP platforms will grow from $2.7 billion in 2011 to $40 billion in 2017 (9 percent of the total semiconductor value)
- 2015 will be the year for the implementation of 3D TSV technology in high-volume production with silicon interposer
- Organic 2.1D will follow providing a low cost solution

2.5D/3D Technology Adoption

Three trends for customers adopting 2.5D/3D technology

Trend #1

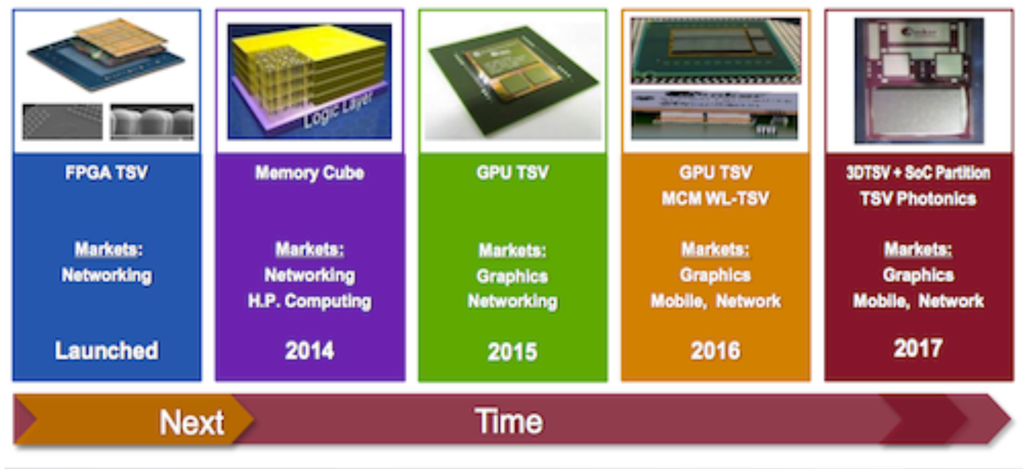
Extend the lifetime of existing packaging technologies

Trend #2

2.5D adoption for high-end markets at high price

Trend #3

2.5D/3D offered to reduce system cost



Courtesy of Amkor, Inc. and Francoise von Trapp July 1, 2014 3D by Design, Blogs, featured, Francoise in 3D 1

eSilicon – Largest Independent SDMS Provider

TIMING CLOSURE • DFT • VERIFICATION • DFM • QUALIFICATION • PACKAGING • TEST ENGINEERING • CHARACTERIZATION • YIELD ENHANCEMENT • ASSEMBLY • SUPPLY CHAIN MANAGEMENT • POWER, PERFORMANCE, AREA OPTIMIZATION •

IC Design

IC Development

IC Production

Customized IP

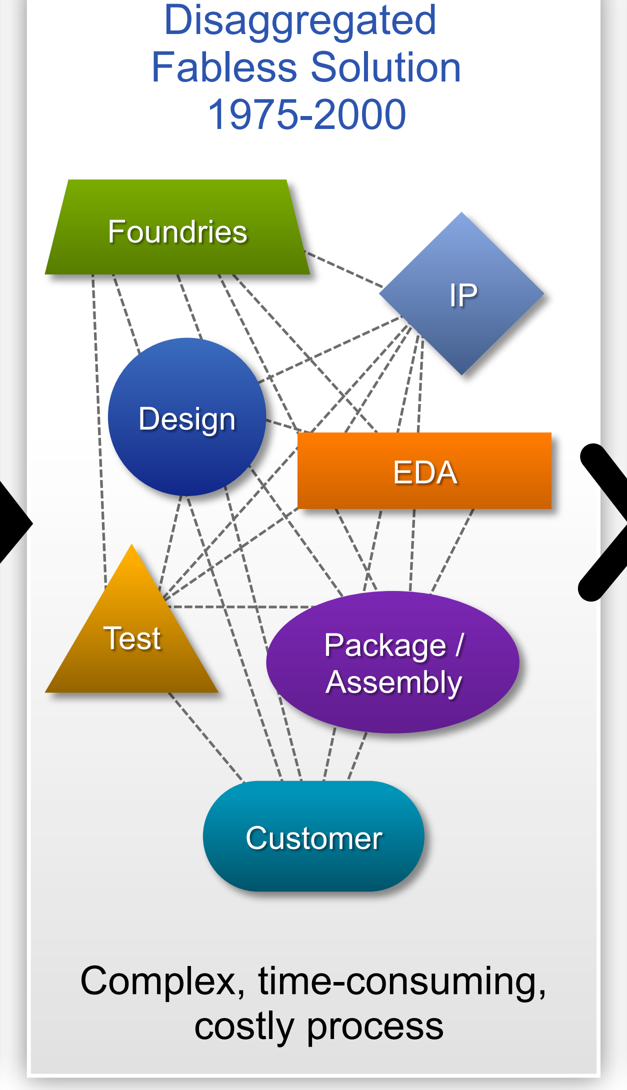
The Supply Chain Evolution

Vertically Integrated Manufacturing Solution 1958-1975

- Design
- EDA
- IP
- Foundries
- Test
- Package / Assembly

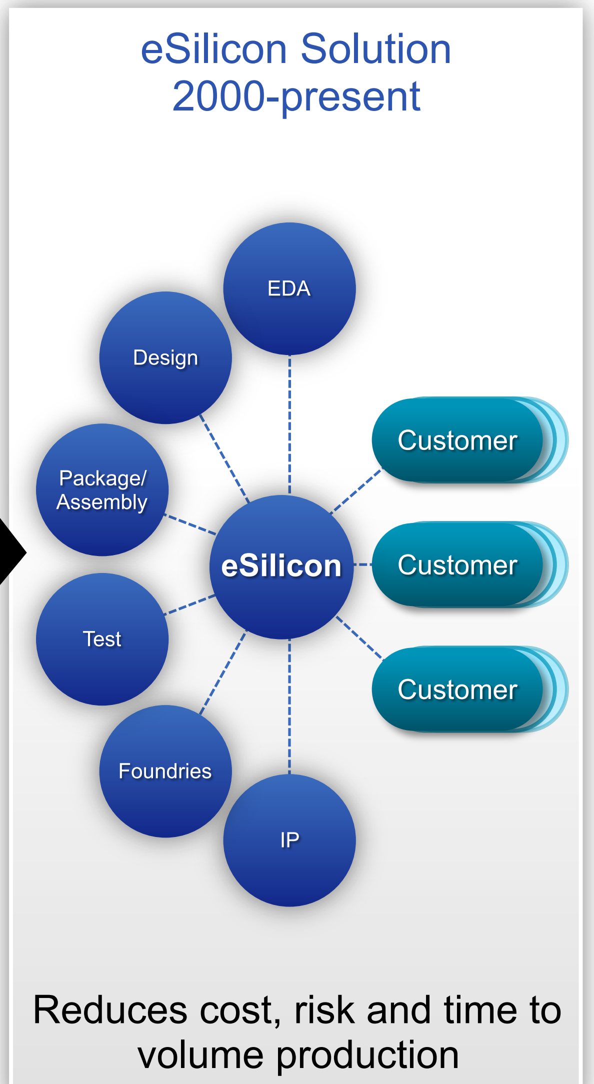
Diverts energy and resources from core competencies

Disaggregated Fabless Solution 1975-2000



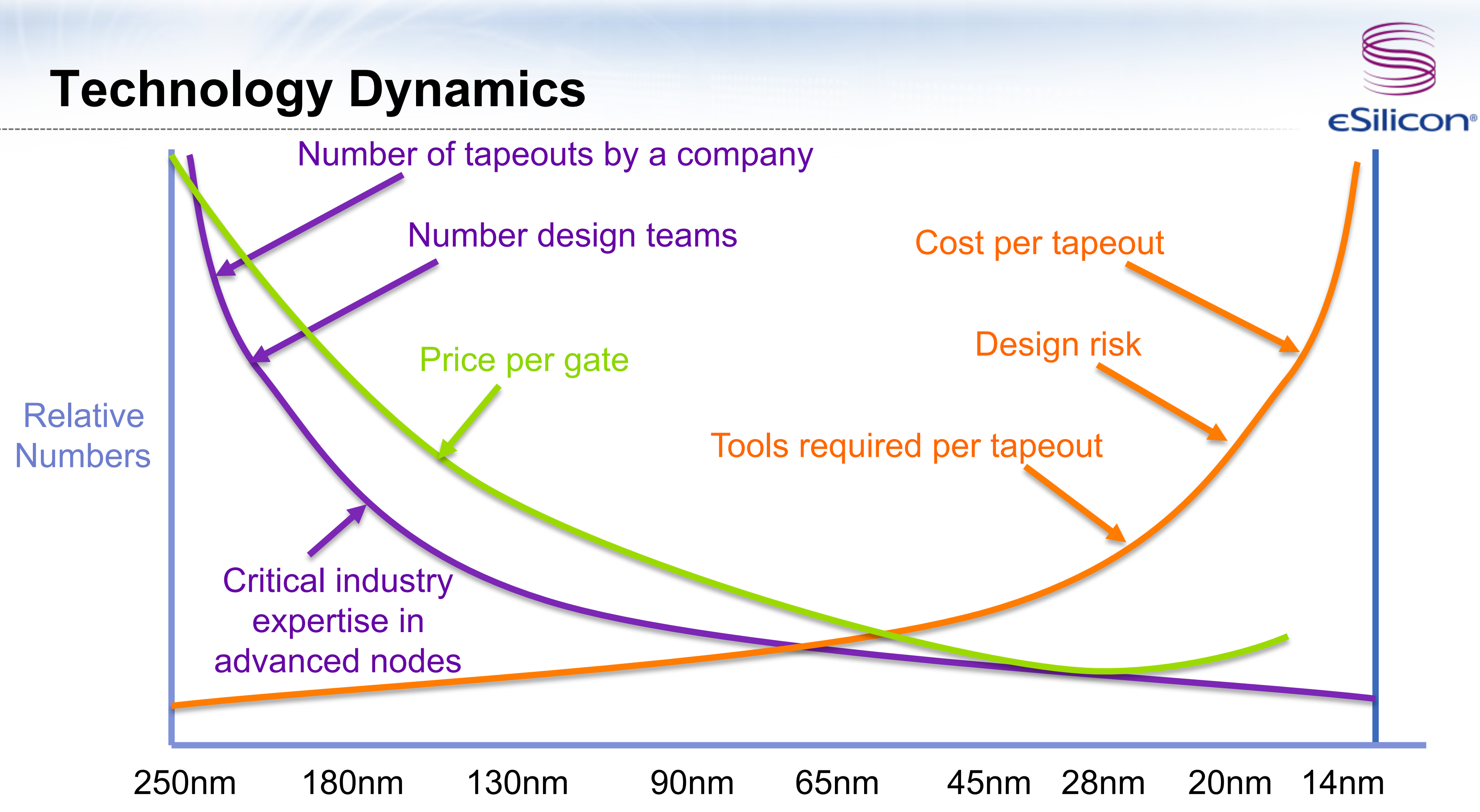
Complex, time-consuming, costly process

eSilicon Solution 2000-present



Reduces cost, risk and time to volume production

Technology Dynamics



- Increasing cost per tapeout, tooling coupled with increasing design risk
- Increased price per gate
- A new solution is necessary to keep ASICs and ASSPs moving

Effect of Landscape Change

Monolithic scaling saved for a very few due to complexity and cost

Solving the Semiconductor Problem

Complexity / Cost / Risk

$200M to Design and
Scale an IC at 20nm

SDMS with eSilicon

Adding Capability While Reducing Total Cost of Ownership, Complexity and Risk

90nm

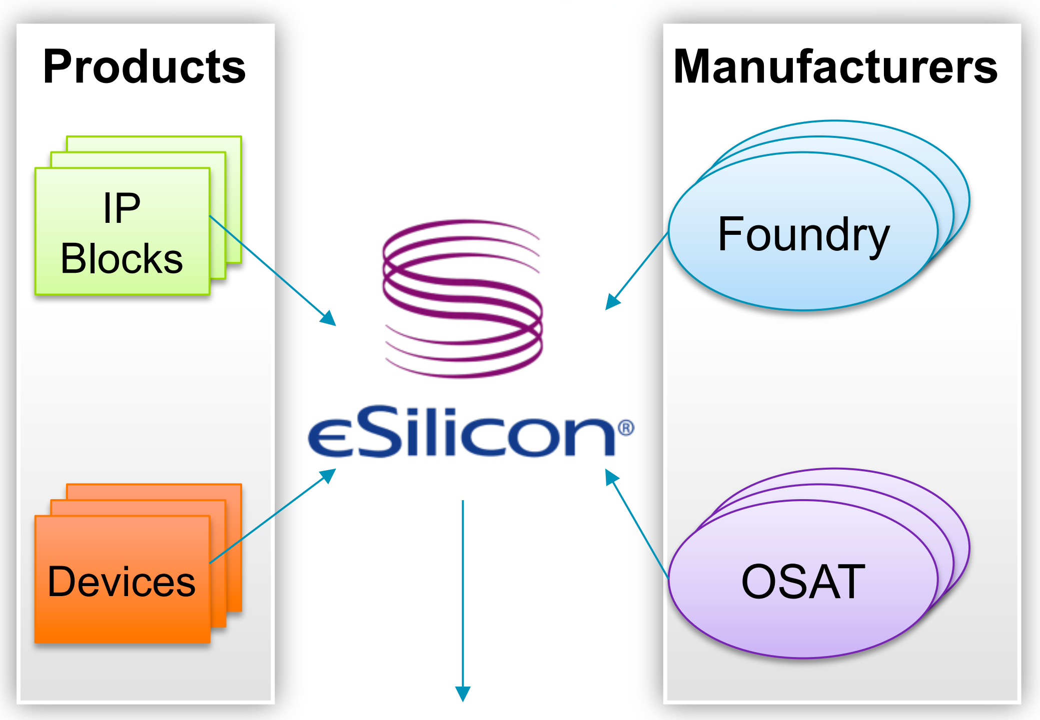
Cycles of Learning/
Design Starts

14% Drop in Design Starts
from 2011 to 2016

10nm

Source: Gartner, 2013

eSilicon – The "Integrator"



- Manufacturers
  - Foundries concerned by many alternatives on structure and interconnect
  - OSATs may have to deal with multiple incompatible interconnect methodologies
- Product companies
  - Device builders don't always want to port to new processes
  - IP companies have no way to supply as silicon
- Customers
  - Don't want to stitch together complex solutions
  - Want one supplier that will take responsibility
- eSilicon
  - Will act as the central integrator
  - Will source the best pieces of the puzzle
  - Will take responsibility for the final product

eSilicon Experience

Planning

2.5D Silicon Interposer on Organic Substrate	2.5D Low Cost Silicon on Organic Substrate	2.5D Glass on Organic Substrate	2.1D Hybrid Organic Substrate
✓		✓	Planning

Memory
ASIC
Silicon
Organic Substrate

Memory
ASIC
Glass
Organic Substrate

Memory
ASIC
Organic Substrate

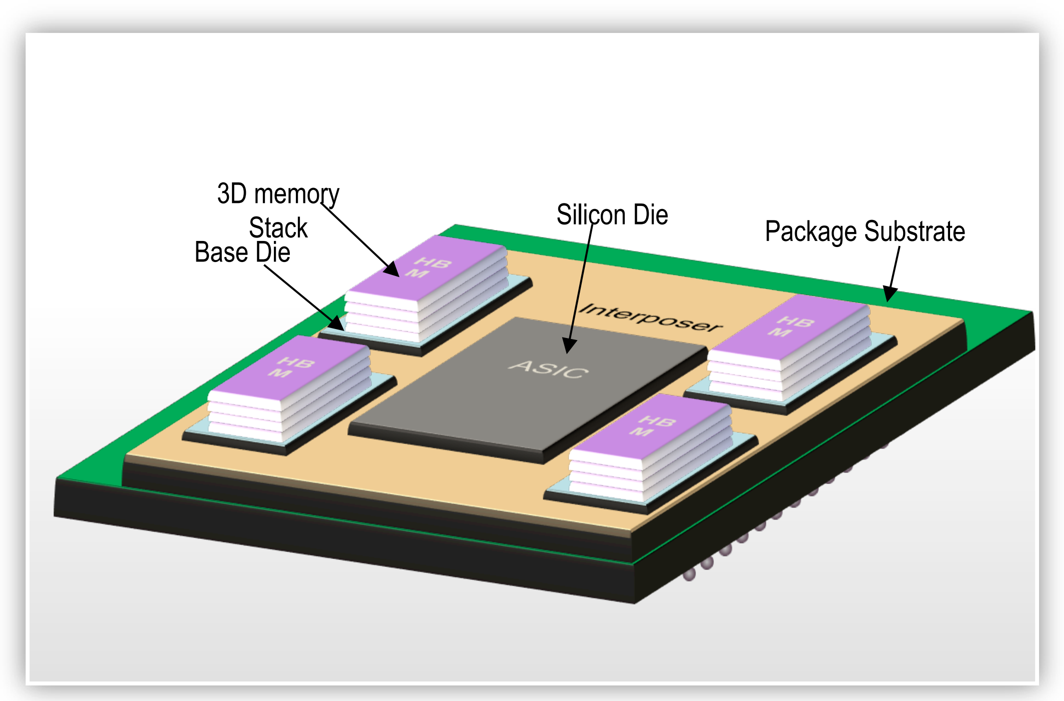
$$$$ $$$ $$ $

High-end Applications
Mid-range Applications
Consumer High Volume

2015
2016
2017

eSilicon's Mainstream 2.5D Integration Experience

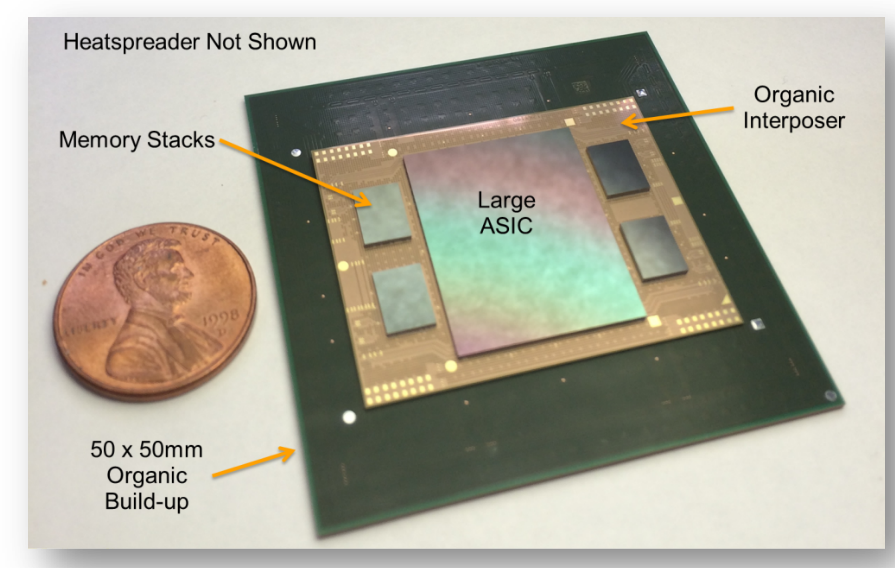
- Taped-out silicon interposer in December 2014 for large ASIC surrounded by 4 HBM1 stacks
- Graphics processing application
- Accompanying ASIC to tapeout January 2015
  - eSilicon developed PHY
  - eSilicon developed IO
  - Northwest logic controller
  - Implemented some HBM2 features including bump repair



eSilicon's Organic Interposer

Industry First Test Vehicle Targeted for Networking Applications

- 50x50mm BGA
- 38x30mm interposer
- 50% larger than largest Si interposer
- 4 HBM daisy chain memories at 5.5x7.7mm
- 1 Massive daisy chain ASIC 24x19mm
- 4 JEDEC HBM1 stacks
- All interconnect at 55um pitch



Challenges

Migrate To A New Product Release Flow

Focus needs to shift from IP, EDA, foundry and assembly

IP Sourcing
Design Tools
Architecture
Physical Design & DFT
Foundry
Wafer Sort
Assy
Final Test
Char
Yield Mgmt
Tile Sourcing & Reusability

to tile sourcing, architecture, DFT, wafer sort, final test, characterization and yield management

Architecture & Design

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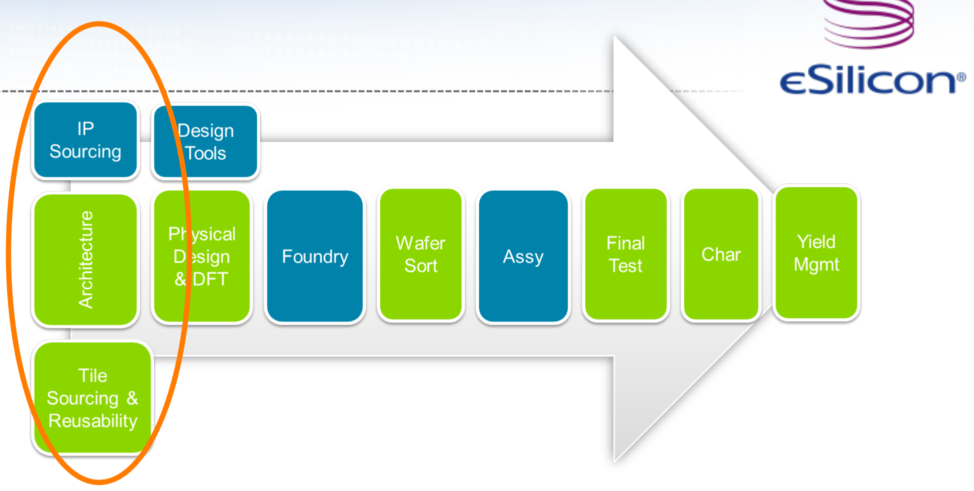
- Fine pitch for more highly parallel interfaces
- Ultra-low power to span 2mm instead of many inches
- What goes in die can be completely different
- Use nodes for what they are best for, and plan on reuse
- Performance bottlenecks removed completely



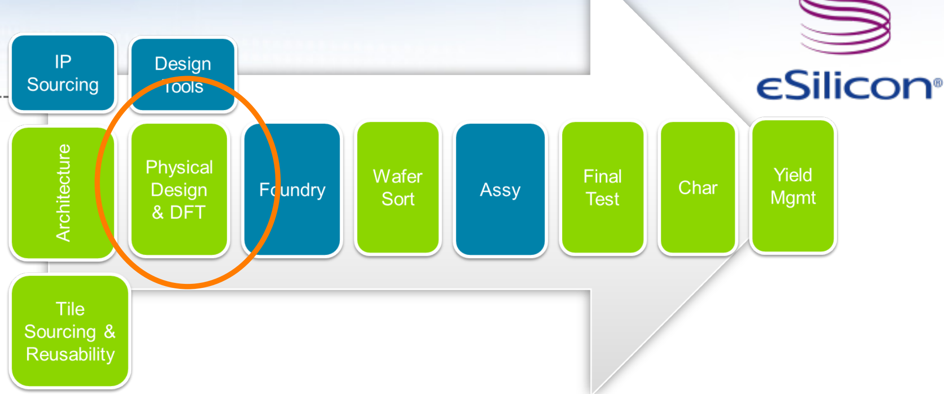
- With new architecture comes new physical design issues
- Hierarchical timing closure at tile level instead of block level
- Rectangular nature of interposers will influence die floorplan
- Unfamiliar interfaces
  - Greater capability
  - Unproven IP
- Mitigation strategies needed for design with new IP

IP Considerations

- Existing I/O solutions assume driving long distances while 2.5D solutions do not have pins leaving the package
  - ESD is 100s of volts rather than 1000's of volts
- Bump interface types not as spaced apart providing opportunity for reduced interconnect capacitive load
- Finer bump pitches enable smaller I/Os which can be combined into a large I/O macro
- Integrating new memory technologies

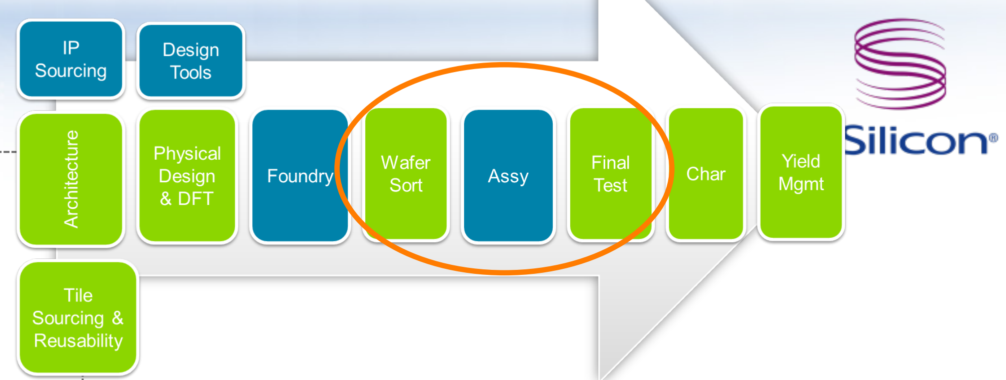
Design for Test

New set of challenges



- Test whole packaged system through a master chip
  - One chip must be custom in heterogeneous construction
  - Reduces the signal count needed at test
  - For complex networking chip, you still need about 600 pins for all of the test vectors in order to keep the test time down
  - Needs test interfaces on other tiles to be ready for test interface
- In 2.5D structure, package size is likely gated by:
  - Silicon arrangement
  - Not by ball count
  - And will have a lot of power delivery, but do not forget the test-pin requirements to keep the test time low

Test Issues/ Strategies



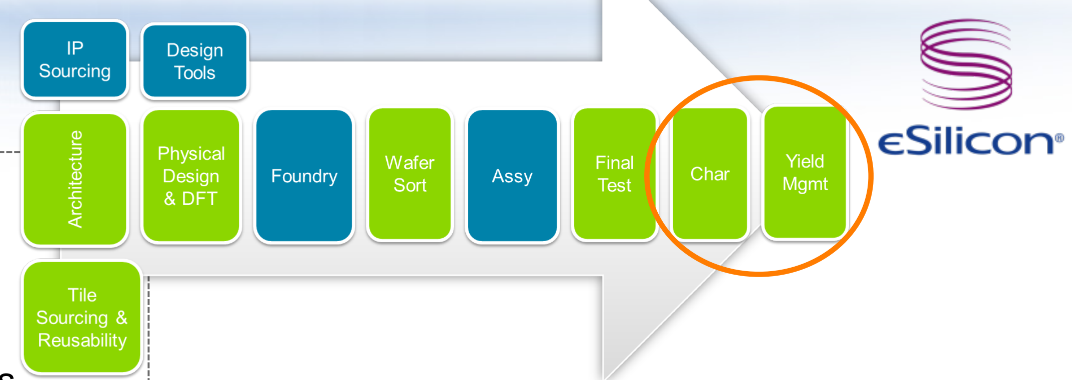
Wafer sort

- KGT (known good tiles) and KGI (known good interposers)
- Too many signals for a probe card
- Advanced use of loopback
- Can't economically access all of the microbumps
  - Depending upon pitch and wafer volume
  - Test coverage may suffer
  - Significant use of test compression
  - Many strategies may exist
    - Sparse bump areas
    - Varying bump geometries
    - Add probe pads for test

Final Test

- Small portion of signals come out to package balls
- Failure modes must include what actually failed
  - Need to know what tile failed for internal interfaces
  - Assignable failure cause instead of failure mode is critical
- Test times will be longer and there may be higher power in these system-tests at package level

Characterization & Yield Challenges



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Characterization

- Base characterization on a subset of pins
- Test coverage must be very well understood
- Requires creative DFT modes to be able to exercise and monitor critical aspects in characterization over:
  - Process corner
  - Temperature
  - Voltage
- Per-parameter characterization needs margins with Cpk>2
- Need in-depth understanding of partner tiles regarding specification margin
- System-level testing (SLT) may become more predominant

Yield

- With more integration, yield targets must drop
- Known yield is more important and realistic than perfect yield
- Define who owns what aspects:
  - OSATs
  - Tile manufacturers
  - Interposer manufacturers
  - Integrators
- Need a larger budget for failure analysis
- The board level yield management becomes much simpler, since complexity moves to package.

Complex TSV Ecosystem

eSilicon manages the ecosystem and assumes yield risk

SiP Assembly and Test

SiP Assembly and Test

Business Model for SiP

PHY and MC IP controller IP

OSAT

Memory Vendor

Set Maker

eSilicon

Foundry

IP Enabler

Where is eSilicon Going Next?

Extended HBM (EHBM) ...

Beyond the interposer

- Developing consortium
  - HBM interface that does not require interposer
  - Target markets
    - Gaming
    - Networking
    - Supercomputer
  - Dramatically drop unit cost with elimination of interposer
  - Speed the adoption of stacked memory

Enabling Your Silicon Success™