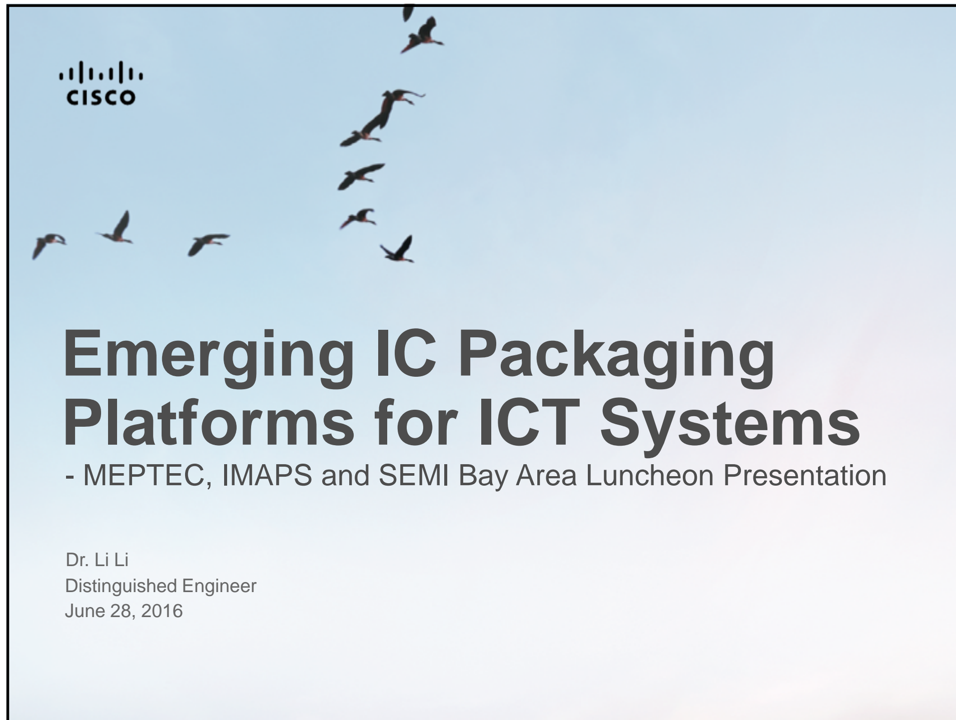


# Outline

- Evolution of Internet
- The Promise of Internet of Everything (IoE)
- Technology Challenges and Potential Solutions
  - System Requirements and Key Drivers
  - Component Technology Innovation
  - Emerging IC Packaging Technology Platforms
- Summary

# Evolution of Internet / The Promise of Internet of Everything (IoE)

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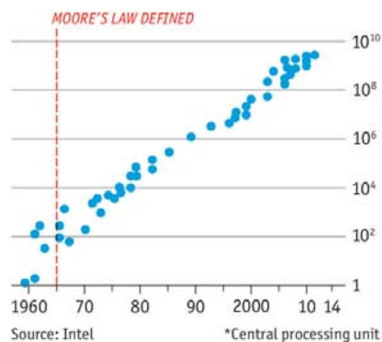
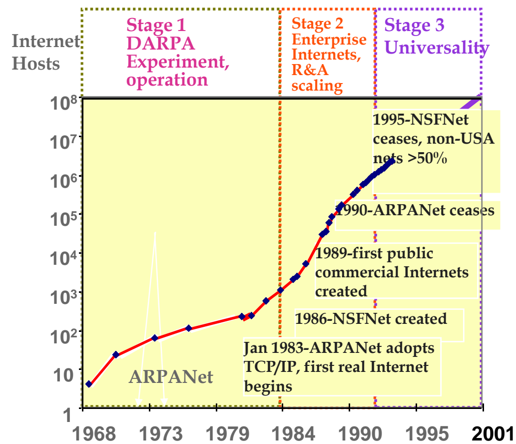
## Moore's Law & Internet: A Historical Perspective



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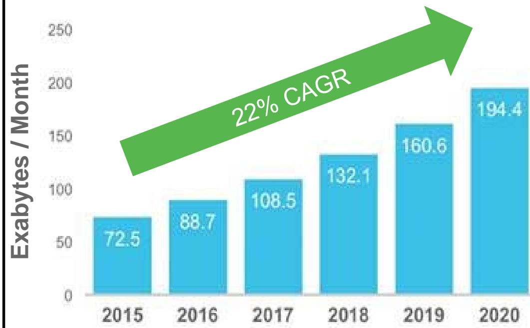
# Cisco VNI Forecast, 2015 – 2020

In June 2016, Cisco released the complete VNI Global IP Traffic Forecast, 2015-2020.




- By 2020, there will be nearly **4.1** billion global Internet users (more than 52 percent of the world's population), up from 3.0 billion in 2015.
- By 2020, there will be **26.3** billion networked devices and connections globally, up from 16.3 billion in 2015.
- Globally, the average fixed broadband connection speed will increase 1.9-fold, from 24.7 Mbps in 2015 to **47.7** Mbps by 2020.
- Globally, IP video will represent **82** percent of all traffic by 2020, up from 70 percent in 2015.

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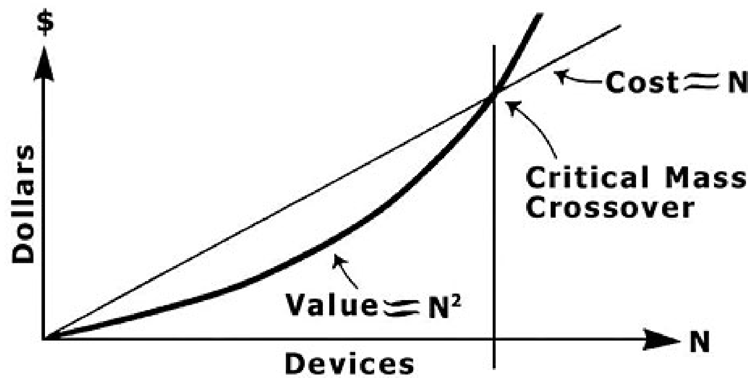
# Metcalfe's Law – The Magic of Interconnections



Bob Metcalfe

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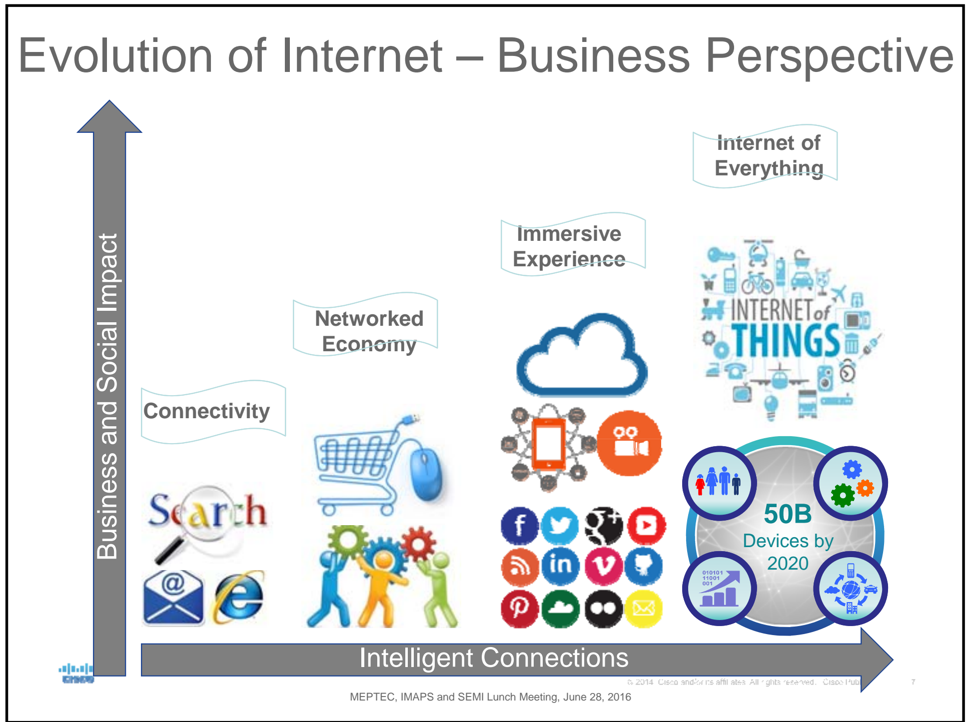


*Technology Challenges – System Requirements and Key Drivers*

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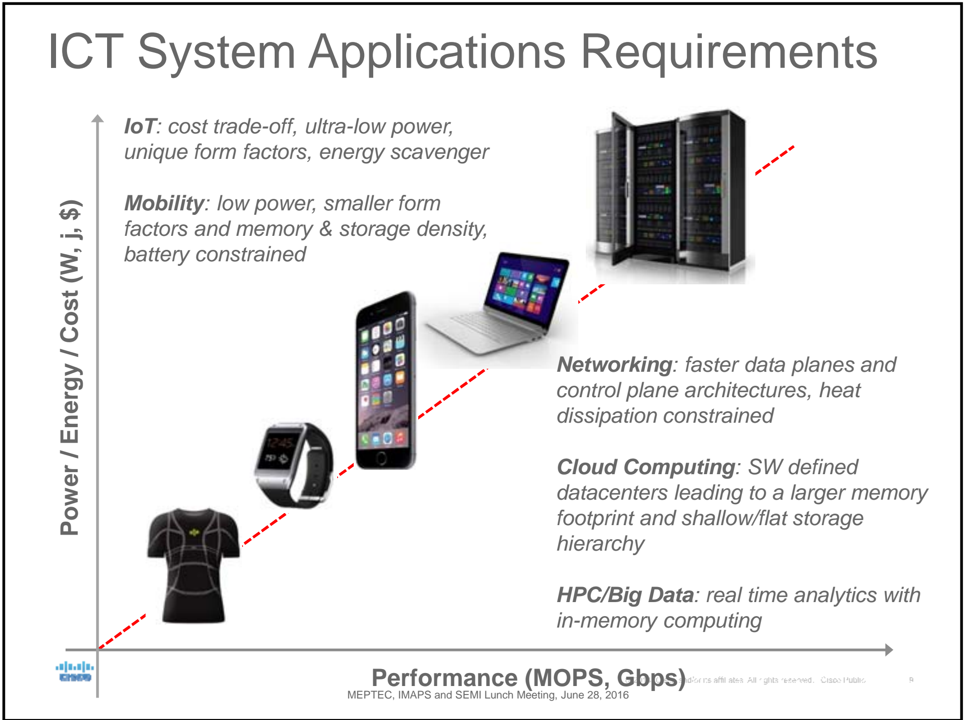
ICT System Applications Requirements
IoT: cost trade-off, ultra-low power, unique form factors, energy scavenger
Mobility: low power, smaller form factors and memory & storage density, battery constrained
Networking: faster data planes and control plane architectures, heat dissipation constrained
Cloud Computing: SW defined datacenters leading to a larger memory footprint and shallow/flat storage hierarchy
HPC/Big Data: real time analytics with in-memory computing
Power / Energy / Cost (W, j, $)
Performance (MOPS, Gbps)
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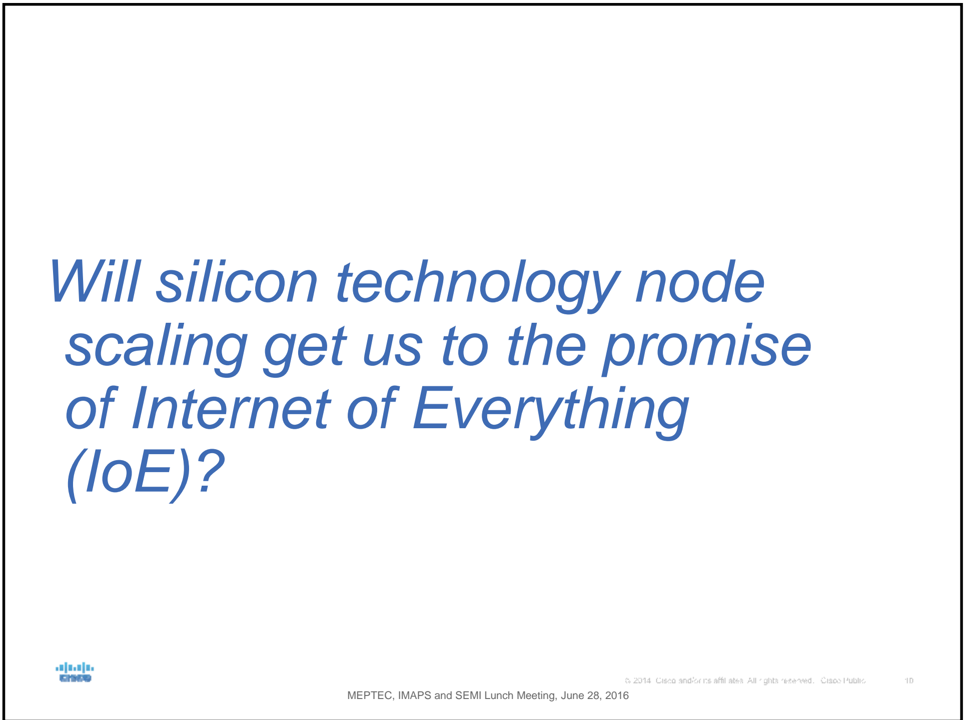
Will silicon technology node scaling get us to the promise of Internet of Everything (IoE)?
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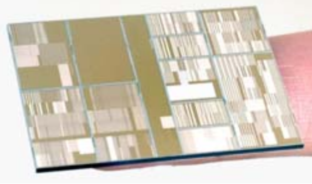
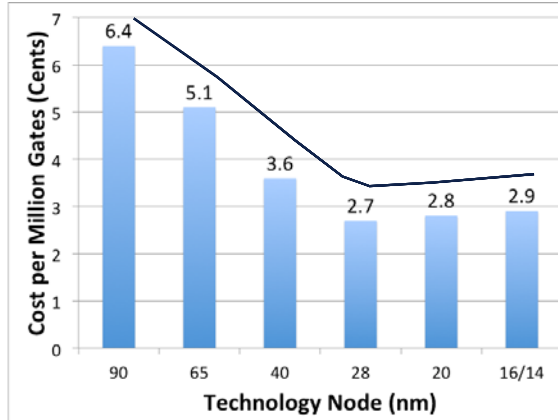
# Technology Node Scaling






Recently announced ***7nm*** test chip produced by IBM Research Alliance

However, economics will likely be the key challenges to continued technology node scaling.

Source: IBM, Broadcom

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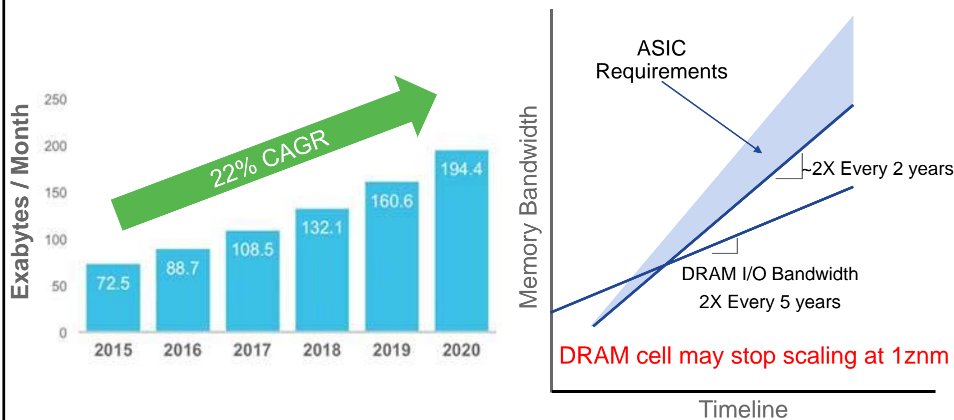
# ASIC & Memory Bandwidth Requirements & Challenges



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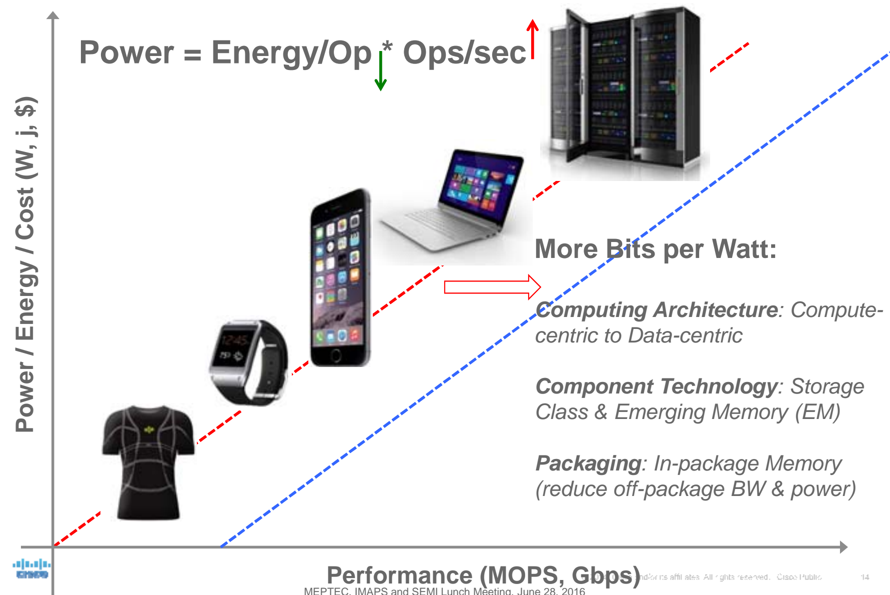
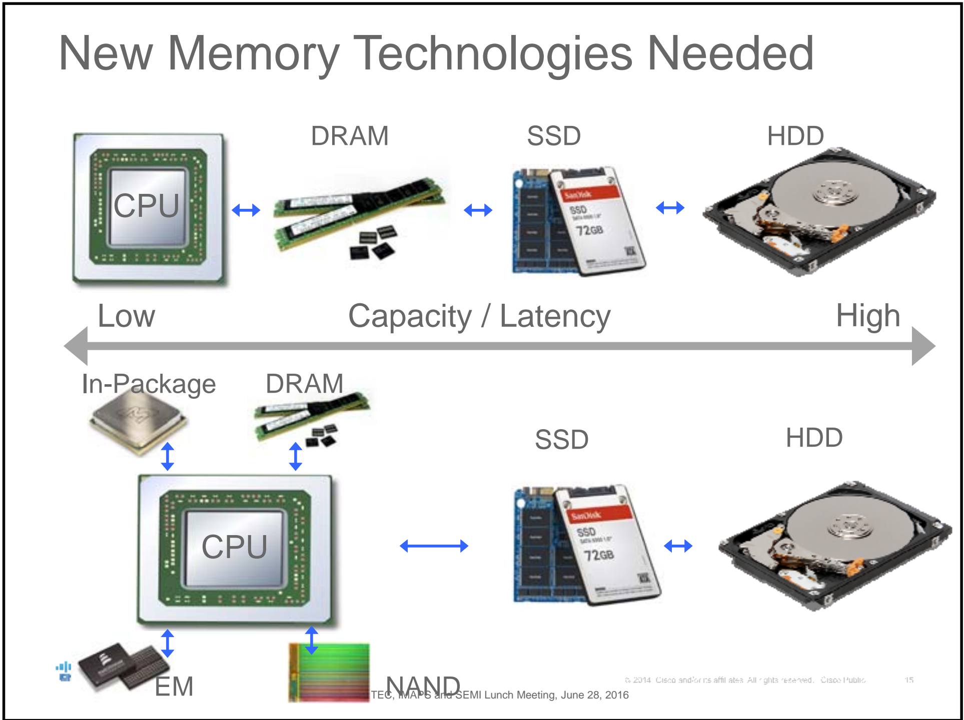
# Potential Solutions:

- Component Technology Innovation
- Emerging IC Packaging Technologies

## Drive Technology Innovation






## Emerging Memory (EM) Technologies

**Floating Gate 3D NAND (March 2015)**

- 3X high capacity than existing NAND technologies
- Enables >10TB in a standard 2.5” SSD
- Scaling for the next decade

**3D XPoint NVM (July 2015)**

- 1st new memory technology in 25+ years
- 1000X faster than NAND
- 1000X endurance of NAND
- 10X denser than conventional memory

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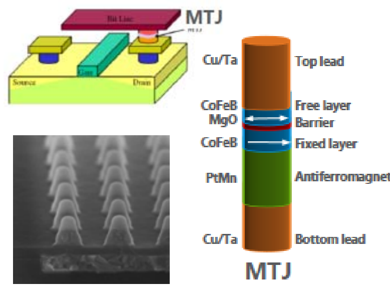
Source: Micron

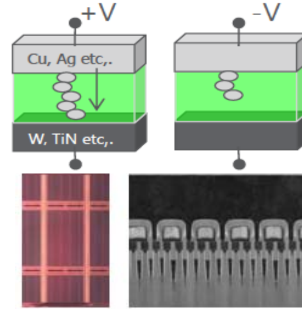
# Future Memory Technologies

## Spin Torque Memory




- Potential long-term DRAM replacement
- Early application as a high-speed cache
- Based on electron spin at atomic level

## Resistive Memory




- Flash replacement beyond 10nm
- NVM
- High-speed, low power, CMOS compatible

Source: Micron, IMEC

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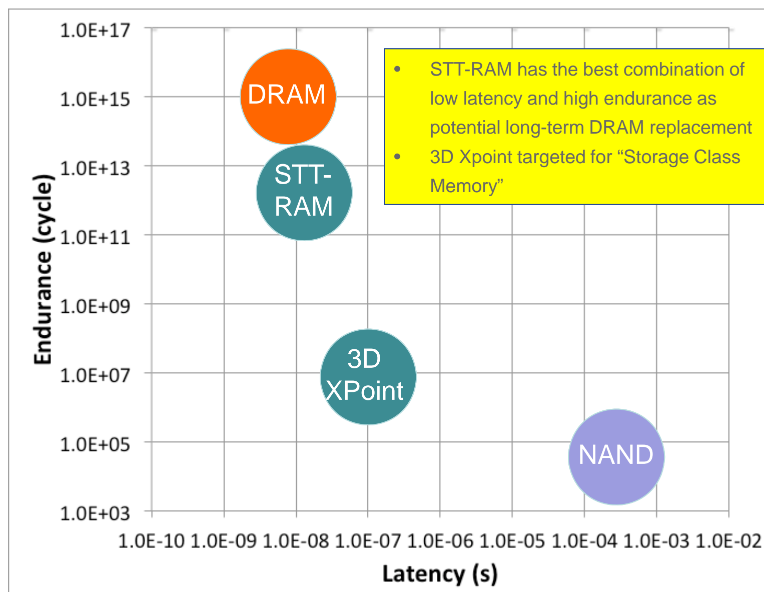
# Emerging Memory Bench Marking



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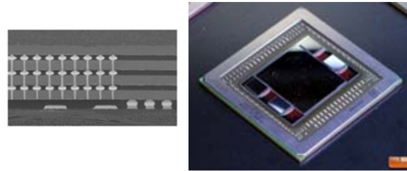
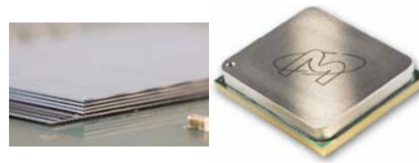
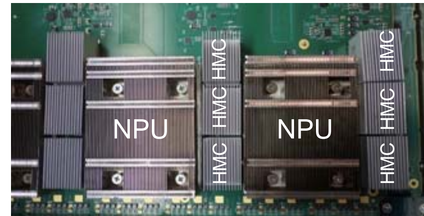
## In-Package Memory *integrating* with CPU

**High Bandwidth Memory (HBM)** | **Hybrid Memory Cube (HMC)**








Source: SK Hynix, AMD

- High BW
- Saving on energy/bit vs GDDR5
- In-Package integration with CPU
- JEDEC standard

Source: Micron, Juniper

- High BW
- Saving on energy/bit vs DDR3
- Easy of System Integration
- High-speed serial I/O

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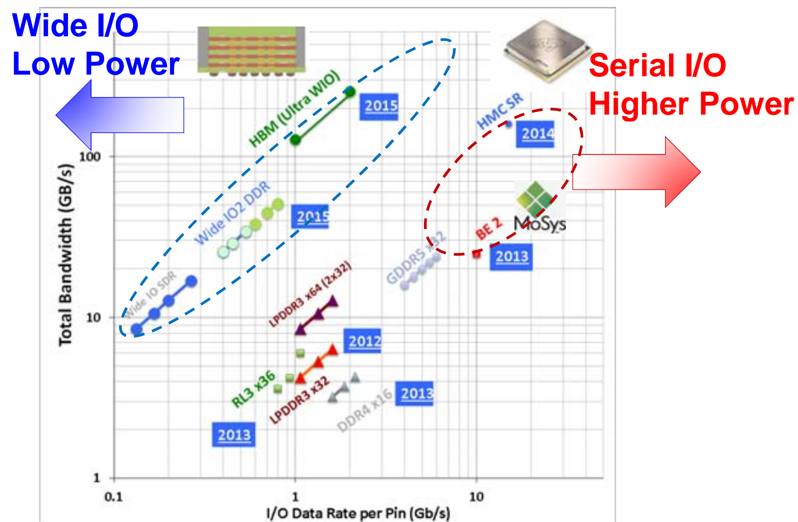
## High Performance DRAM Technology



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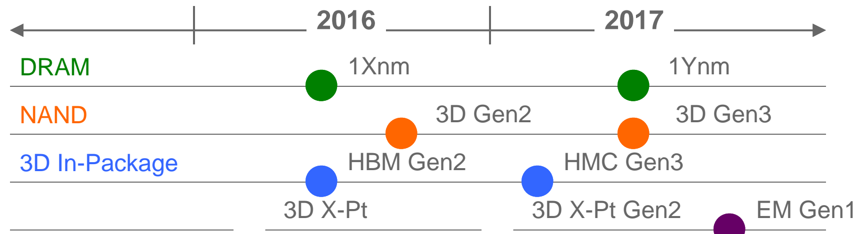
## Likely Industry Memory Roadmap




- Continued DRAM scaling to 1Ynm in 2017
- 3D NAND and 3D XPoint technology ramps in 2016
- 3D In-Package DRAM enablement for innovative system integration opportunities

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Source: Micron, kitguru.net

## Emerging Packaging Tech Platform

| | FC-MCP | Si Interposer | Embedded Si Interposer | Organic Interposer | 3D IC |
|---|---|---|---|---|---|
| **Dielectric Properties** | Good | Lossy | Lossy | Good | Lossy |
| **Feature Dimensions** | Down to ~ 10um L/S | BEOL interconnects | BEOL interconnects | Down to ~ 5um L/S | BEOL interconnects |
| **CTE Mismatch** | Mod. High | Excellent | Mod. High | Mod. High | Excellent |
| **Cost** | Moderate | Moderate | TBD | Moderate | High |
| **Availability / Supply Chain** | Available | Available | Development | Development | Development |

From Substrate Based to Wafer Level System Integration

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## Organic Interposer vs. Silicon Interposer

| Features | Organic Interposer | Silicon Interposer |
|---|---|---|
| Cu Wiring (Dielectrics) | Semi-Additive Process (Polyimide) | Damascene (Oxide) |
| Dielectric Properties | Good | Lossy |
| uBump Material | Cu/Ni/SnAg etc. | Cu/Ni/SnAg etc. |
| uBump Size / Pitch (min) | 30 / 55 um | 20 / 55 um |
| Front Side Cu wiring Line / Space / Thickness (min) | 6 / 6 / 10 um | 0.5 / 0.5 / 1.0 um |
| Via Size in Cu Wiring Layers | 20 um | 1.0 um |
| Through Interposer Via or TSV Diameter / Pitch / Thickness | 60 / 150 / 200 um | 10 / 50 /100 um |
| Bottom Side Cu wiring Line / Space / Thickness (min) | 6 / 6 / 10 um | 10 / 10 / 3um |
| Bottom Side Pad or Bump Size / Pitch (typical) | Ni/Au 100 / 150 um | Ni/Au etc. 100 / 150 um |

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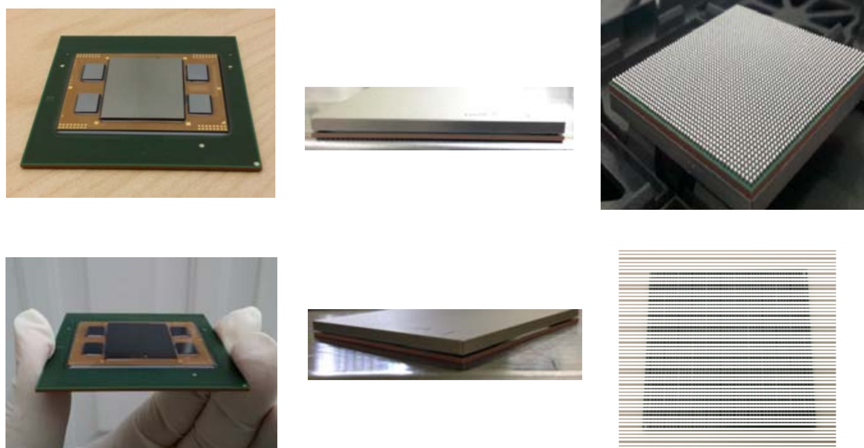
## ASIC & HBM Integration with Organic Interposer



L. Li, et al, “3D SiP with Organic Interposer for ASIC and HBM DRAM Integration”, IEEE 66th ECTC, Las Vegas, NV, June 3, 2016

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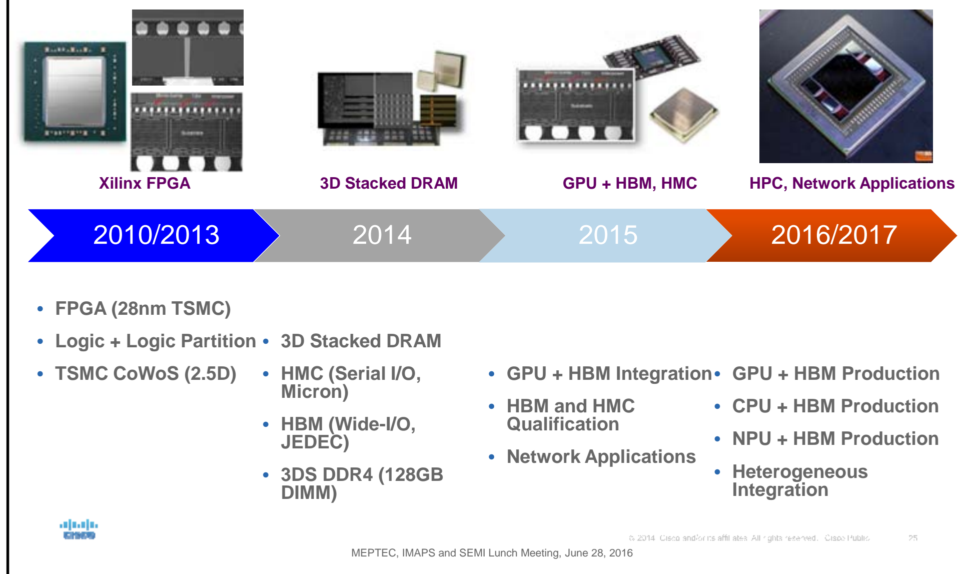
## 2.5D / 3D IC Landscape




## Summary

- Realization of the promise of Internet of Everything relies on next generations of computing, networking and storage systems.
- Silicon performance advancement alone may not get us there as (2D) technology node scaling is becoming more costly.
- New computing architectures, emerging memory components through 3D /volume scaling and 3D IC packaging technologies will be key in future system enablement.