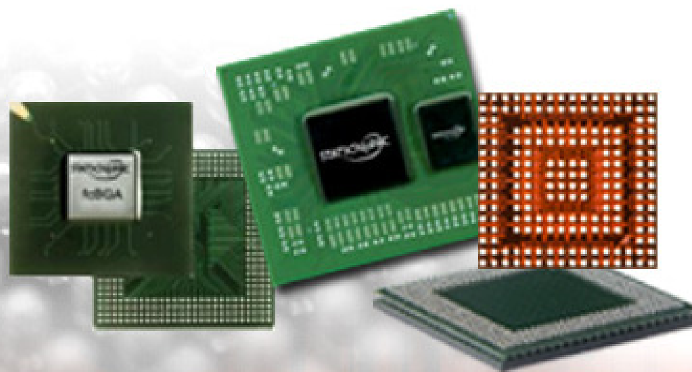
Confidential

eWLB: A Transformative Fan-out Packaging Technology for High Performance, Integration and Small Form Factors

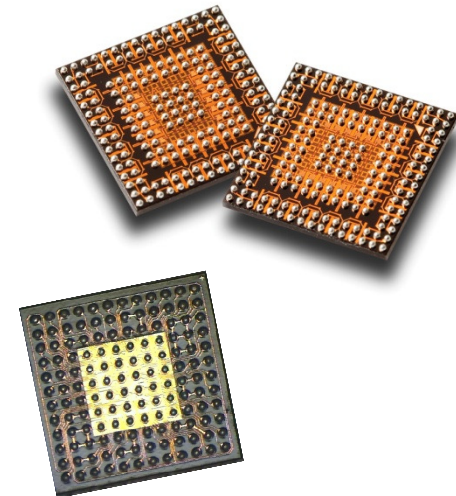
Dr. Raj Pendse
VP, Product & Technology Marketing,
STATSChipPAC



MEPTEC June 2011 Meeting

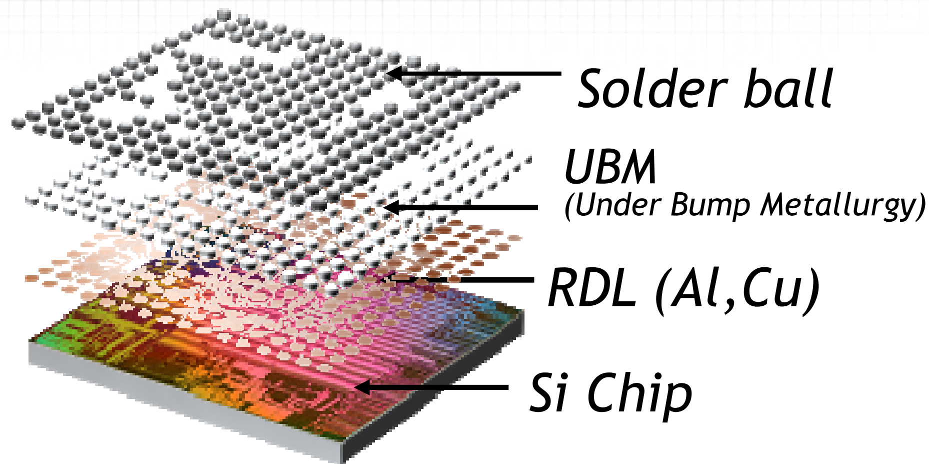
Outline

- Introduction to eWLB
- Package Performance and Reliability
- 2nd Generation eWLB Technology
  - Fine pitch and escape routing
  - Thin eWLB
  - Double sided & 3D eWLB
  - 2.5D Heterogeneous Integration
  - Extreme Small eWLB
  - Large Panel Processing
- Summary & Conclusions

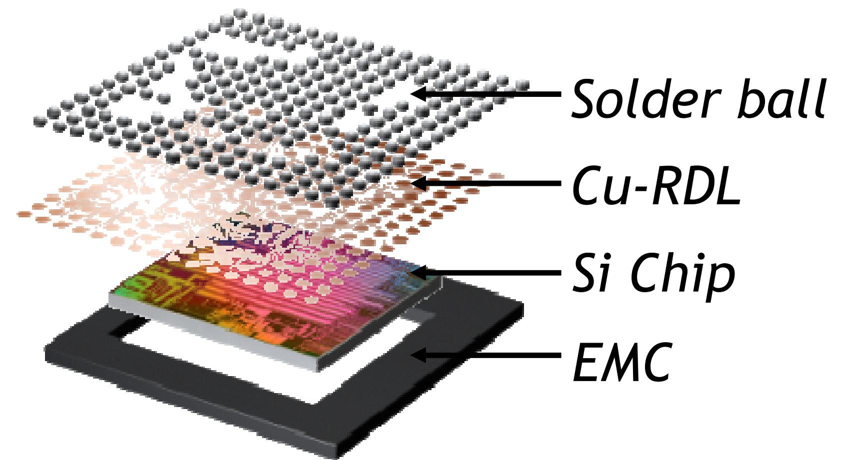


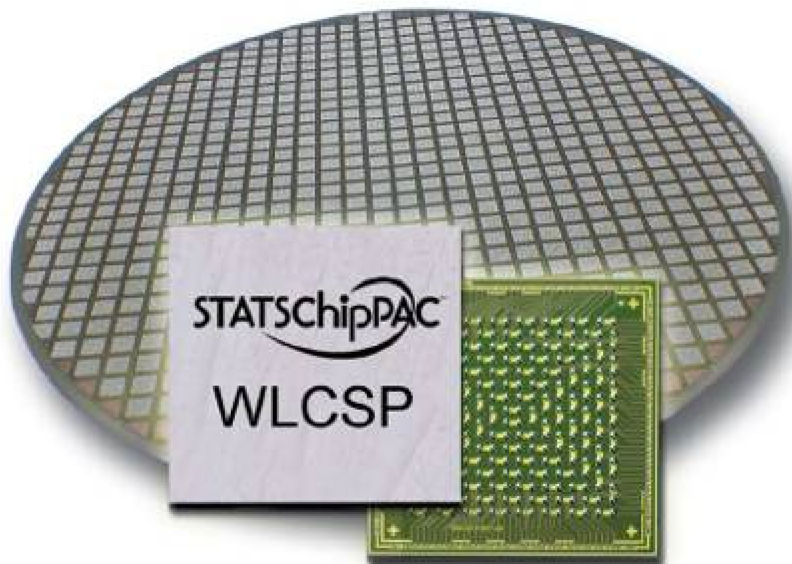
Package Structure

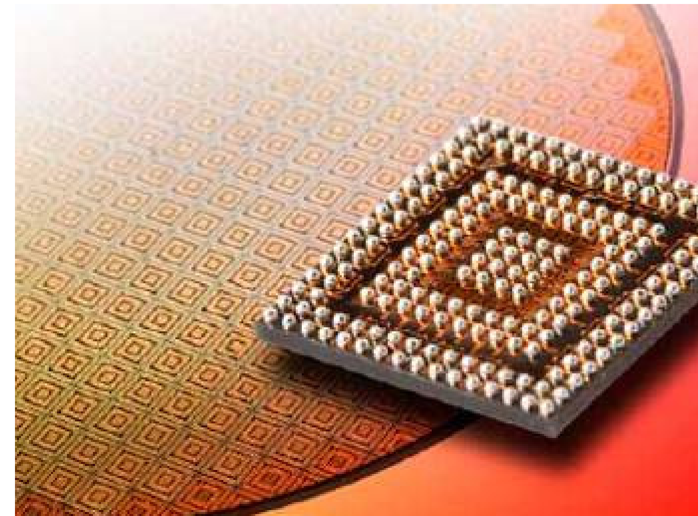
FI-WLP



FO-WLP (eWLB)

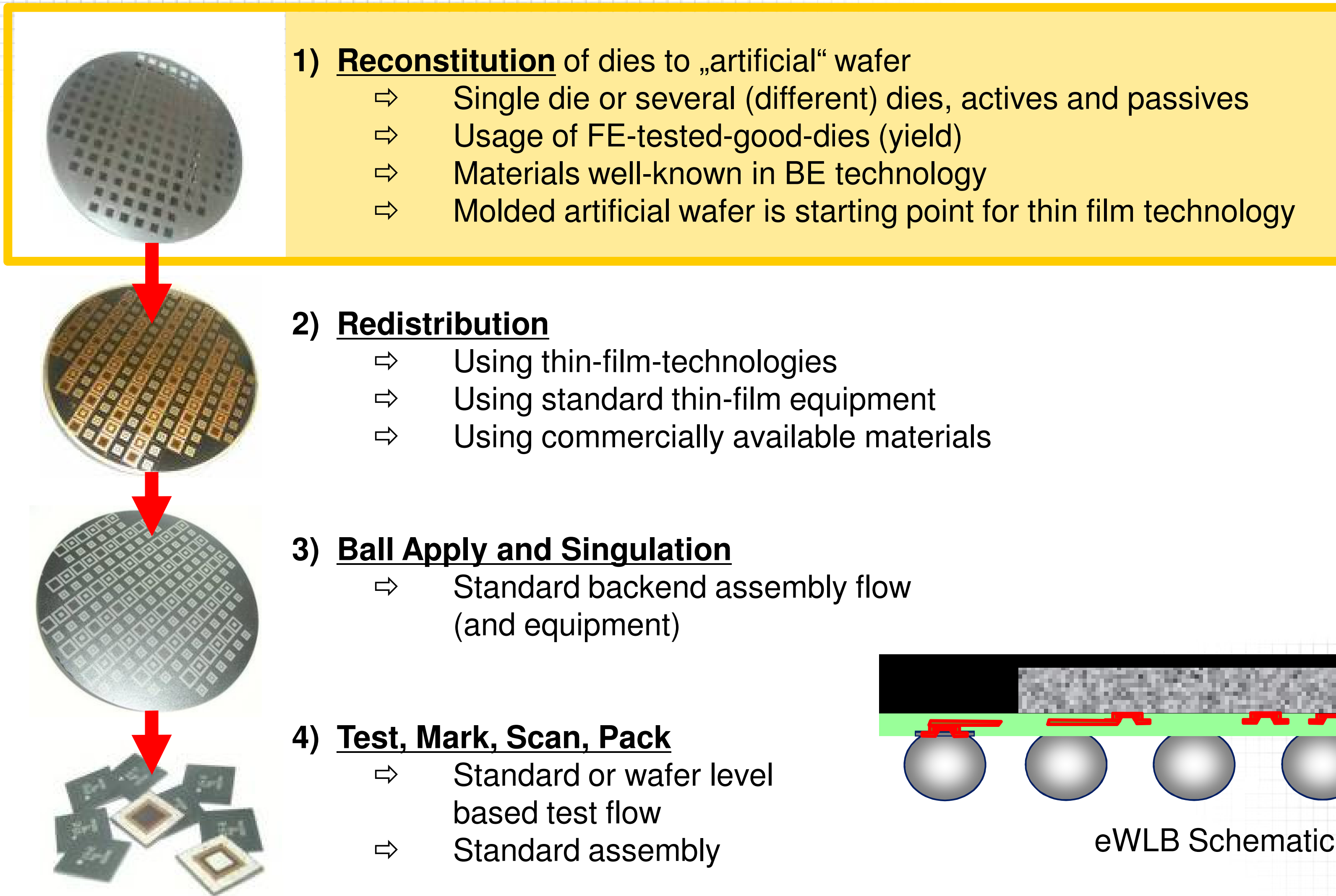






eWLB Process

Confidential



1) **Reconstitution** of dies to „artificial“ wafer
   - ⇨ Single die or several (different) dies, actives and passives
   - ⇨ Usage of FE-tested-good-dies (yield)
   - ⇨ Materials well-known in BE technology
   - ⇨ Molded artificial wafer is starting point for thin film technology

2) **Redistribution**
   - ⇨ Using thin-film-technologies
   - ⇨ Using standard thin-film equipment
   - ⇨ Using commercially available materials

3) **Ball Apply and Singulation**
   - ⇨ Standard backend assembly flow (and equipment)

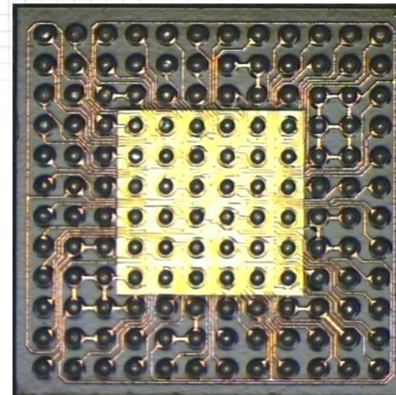
4) **Test, Mark, Scan, Pack**
   - ⇨ Standard or wafer level based test flow
   - ⇨ Standard assembly

eWLB Schematic

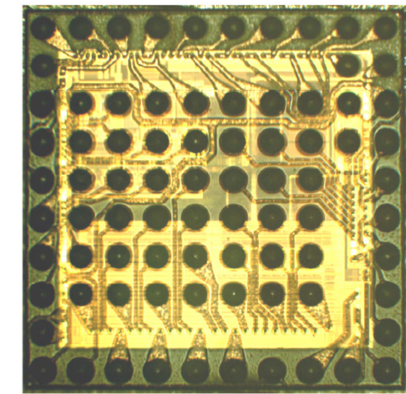
STATSChipPAC

Typical Package Structure

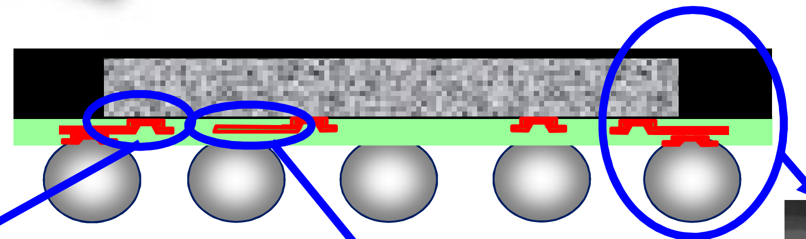
Confidential

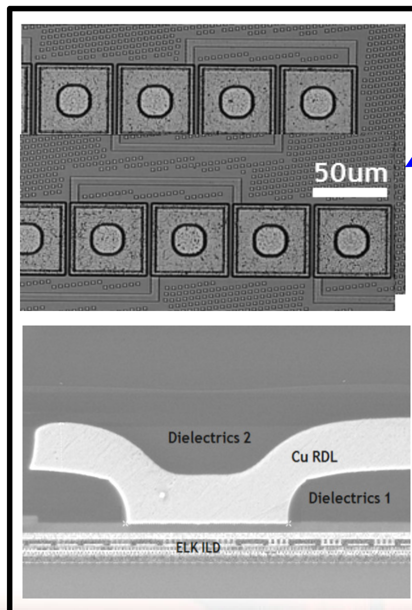


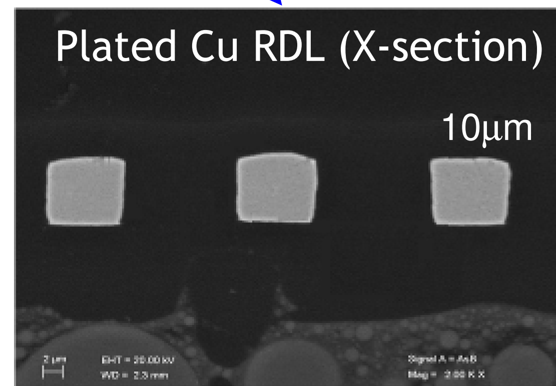
High Fan-out Ratio

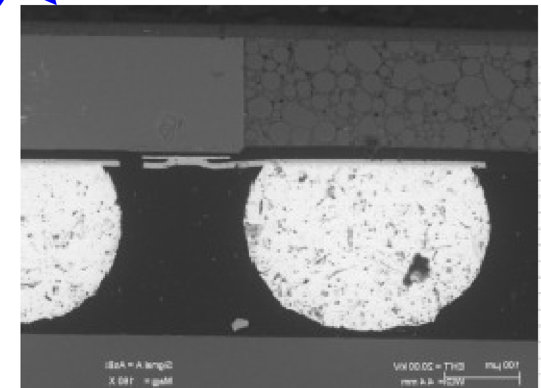


Low Fan-out Ratio





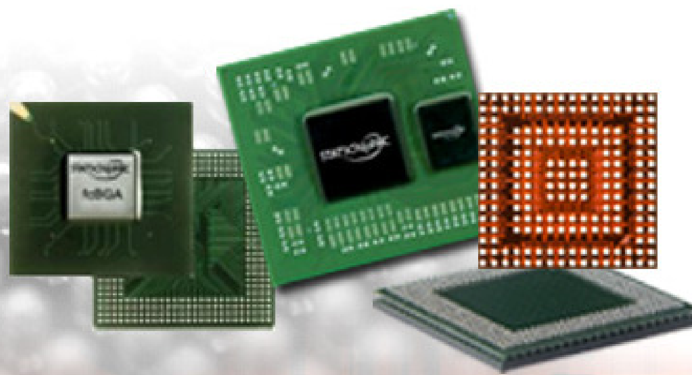




STATSChipPAC

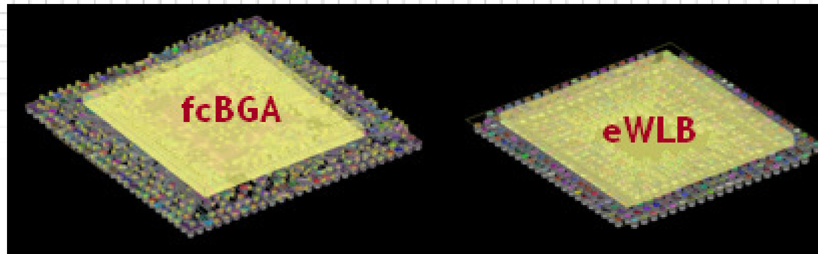
Confidential

Performance & Reliability



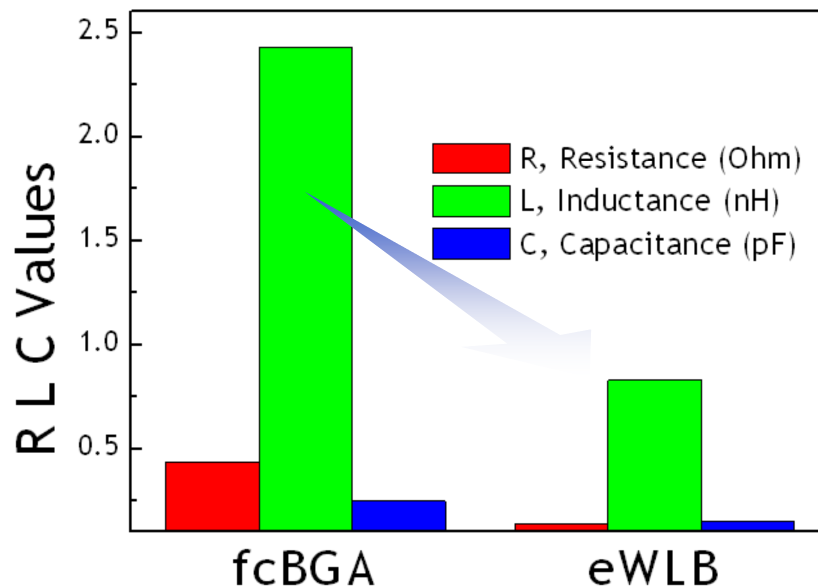
Confidential

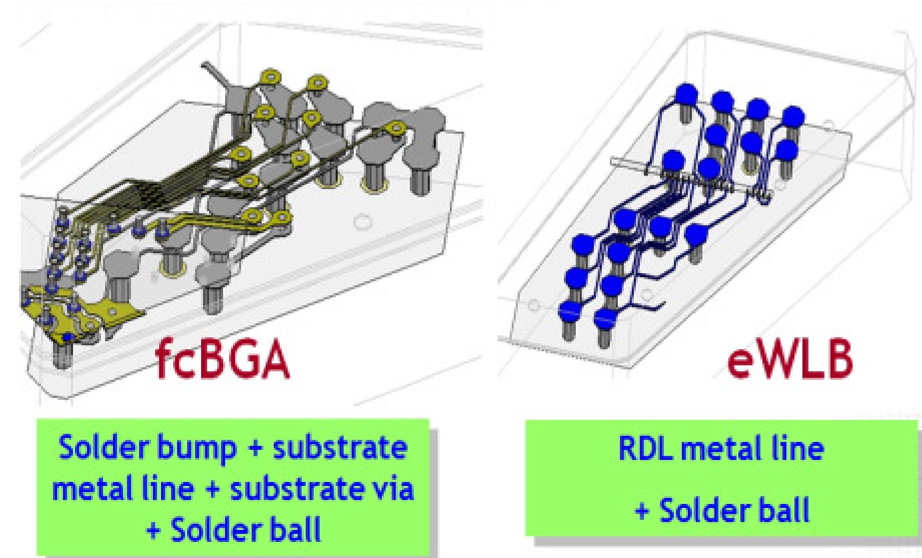
High Electrical Performance



	fcFBGA	eWLB
PKG size (mm2)	11x11	10x9
Die Size (mm2)	7.5x7.0	7.5x7.0
Substrate Thickness/Layer	0.18mm / 2-layer	1-layer RDL
Ball Count	477 I/O	508 I/O
Ball Pitch	0.50 mm	0.40 mm

Electrical Characterization





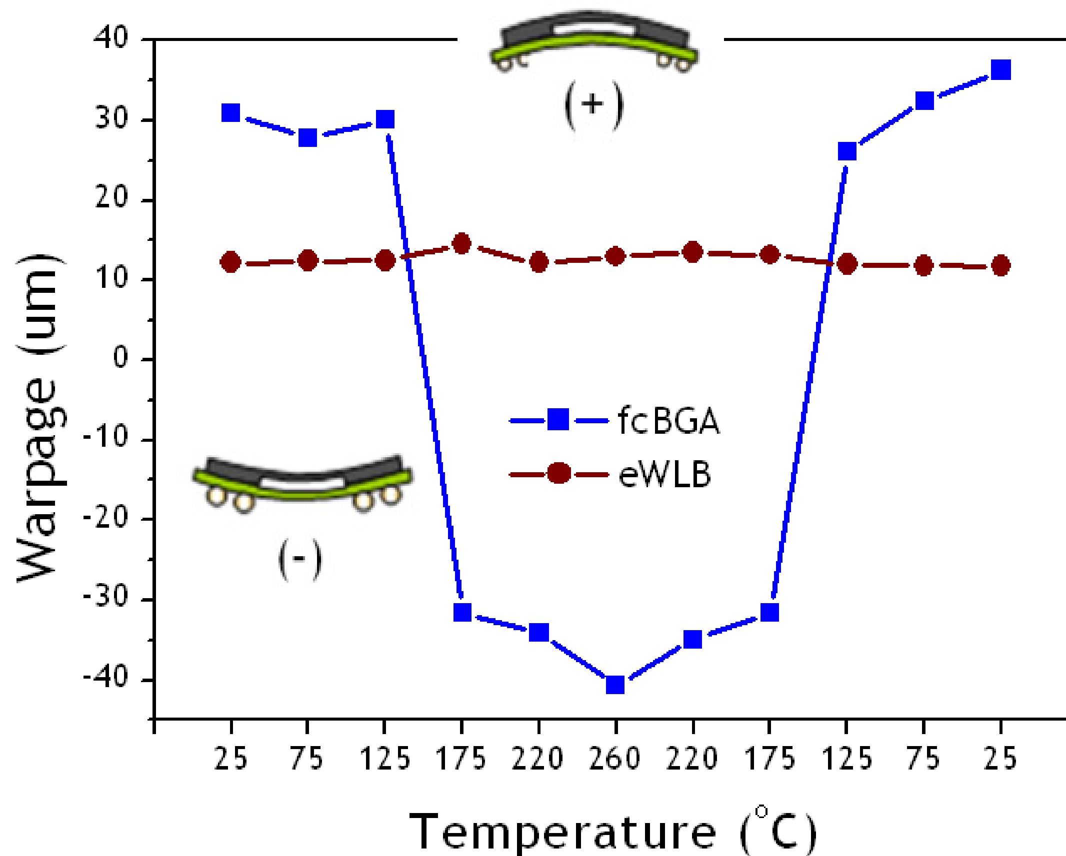
eWLB shows lower values of RLC electrical parasitics compared to fcBGA, due to short/removed interconnection.

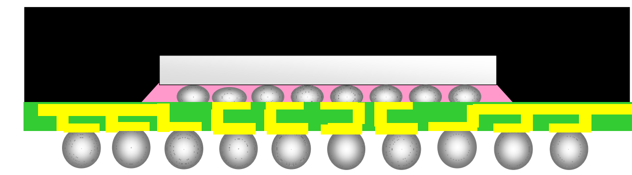
STATSChipPAC

Confidential

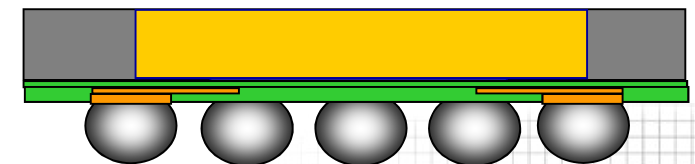
Low Warpage

- **Std single-sided (1S) eWLB**
  (Shadow Moiré data)





fcVFBGA,7x7mm, 191LD NSP
PKG height 0.95 mm
Die 4.46 x 5.65 x 0.19 mm

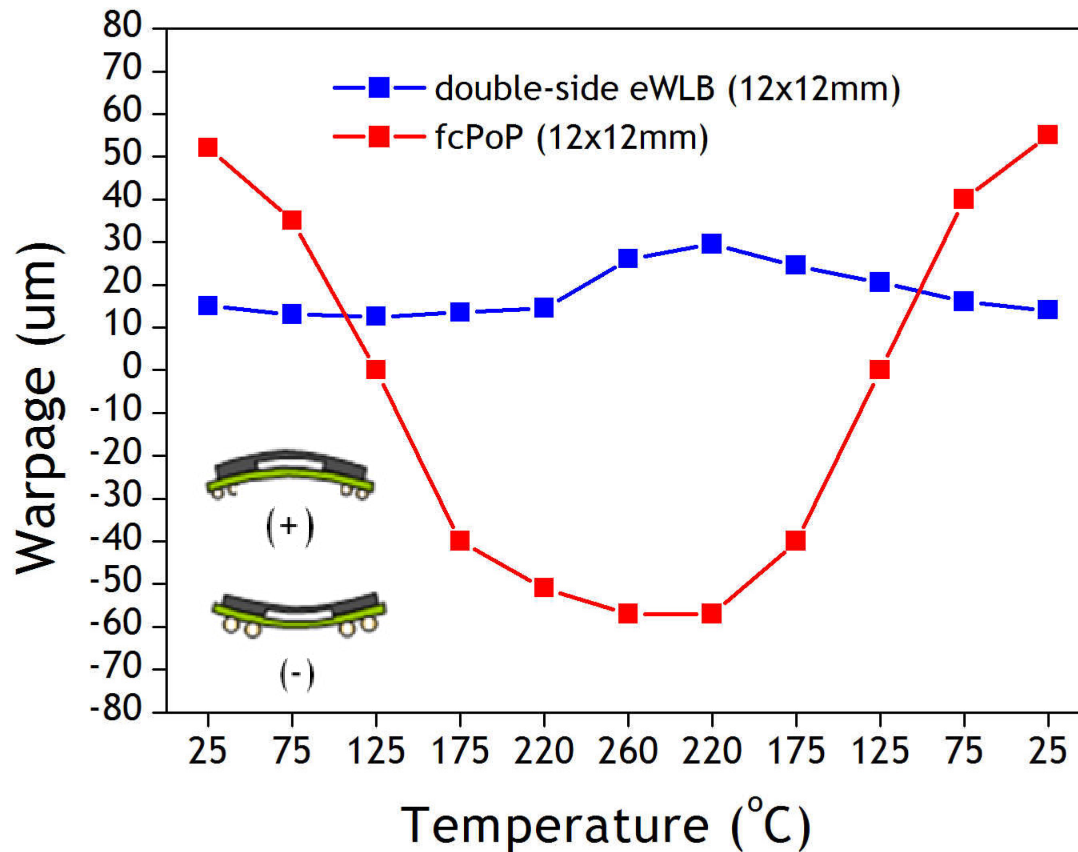


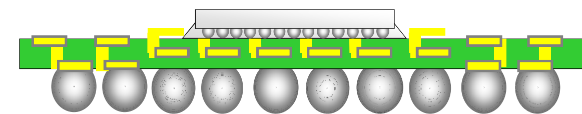
eWLB 8x8mm, 182I/O
PKG height 0.7 mm
Die 5 x 5 x 0.45 mm

Significant warpage improvement due to absence of substrate!

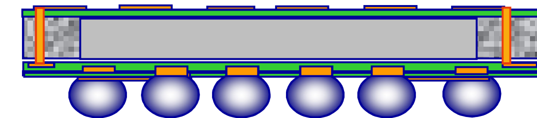
Low Warpage

- **Double-sided (2S) eWLB**





fcFBGA-PoP-b,12x12mm, 516I/O
Substrate thickness 0.43 mm
Die 9 x 9.2mm



eWLB 12x12mm,
396I/O
PKG height 0.7 mm

Dramatic improvement in warpage in 2S –eWLB lends itself to application to thin PoP solution for Mobile platforms

Confidential

Component-level Reliability

- Different package configurations
  - Std 1S 1L eWLB, 5x5 mm die, 8x8 mm body
  - Thin eWLB (250um Si thickness, 5mm x 5mm die , 8mm x 8mm body)
  - 1S 2L eWLB (5mm x 5mm die, 8mm x 8mm body)
  - Multi-Chip eWLB (two-chip, 5x2.5mm, 8mm x 8mm body)

Test		Condition		Status
Package Level*	MSL1 JEDEC-J-STD-020D	MSL1, 260C Reflow (3x)	-	**Pass**
	Temperature Cycling (TC) after Precon JESD22-A104	-40C to 125C	1000x	**Pass; some legs ongoing**
	HAST (w/o bias) after Precon JESD22-A118	130C / 85% RH	96hrs	**Pass**
	High Temperature Storage (HTS) JESD22-A103	150C	1000h	**Pass**
	BST after Multiple Reflow	260C Reflow	20x	**Pass**

** Tested for continuity (Open/Short) and mechanical integrity e.g. ball shear, package cracking etc*

Courtesy of STATS ChipPAC - ST – Infineon 3D eWLB Alliance

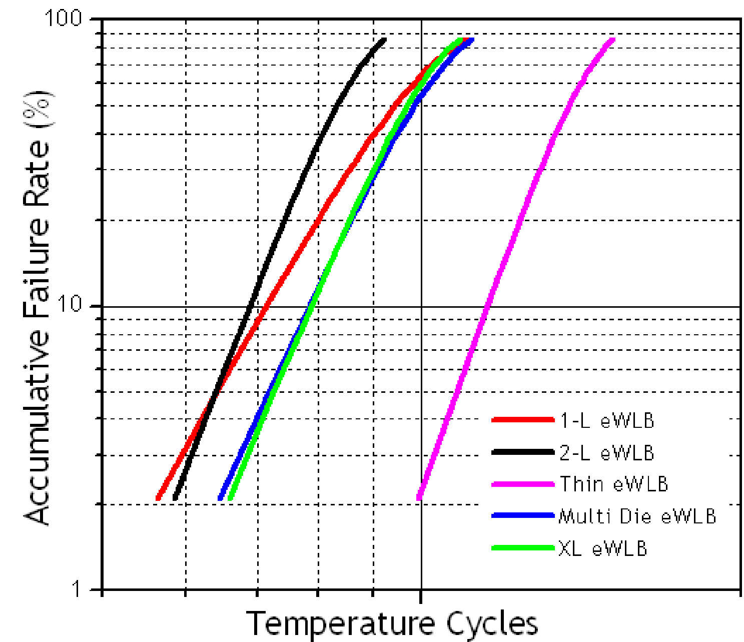
STATSChipPAC

Board-level Reliability (BLR)

Confidential

Board Level Reliability Test		
	NOKIA Spec	
	TCoB	Drop
	-40/125C,2cyc/hr, 8-layer PCB	
2-RDL	Pass	Pass
Thin eWLB	Pass	Pass
Multi Die	Pass	Pass
X-Large eWLB (12x12mm)	Pass*	Pass
X-Small eWLB (2.7x2.7mm)	Pass	Pass

** With larger ball pad size / FSP*



Courtesy of STATS ChipPAC - ST – Infineon 3D eWLB Alliance

eWLB Technology Roadmap

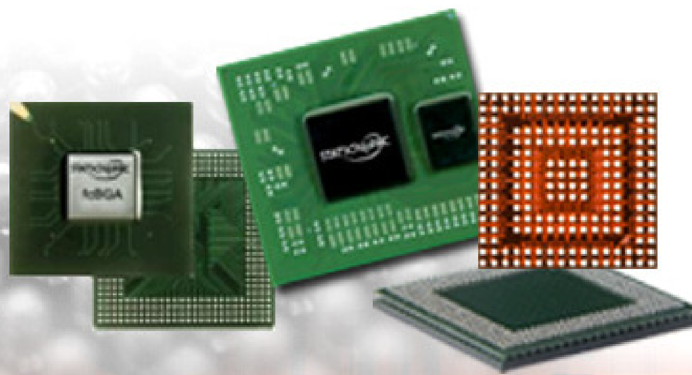
Confidential

	Item	Current	2011 1H	2011 2H	2012
eWLB Package	Max. Package size (mm)	8x8 / 10x10	12x12		>12x12
	PKG height w/ ball (mm)	0.7 / 0.5		0.4	
	Min. Ball pitch (mm)	0.5 / 0.4		0.3	
eWLB Routing	Min. RDL LW/LS (um)	15/15 / 10/10		8/8	<8/8
	Die pad pitch (um)	75um / 65um	60um	50um	<50um
	RDL layer	1	2	>2	
eWLB SiP	Die No. in Package	1 / 2	3	>3	
	3D Approach			PoP, SoW, SiP module	
eWLB Mfg	Carrier Size	8",12"			Panel

HVM !

- Std 1S 1L eWLB in HVM (high vol manufacturing).
- New technology development in fine pitch 1st level interconnect (sub-50 um), 2L/2.5D, 3D and super-thin implementations

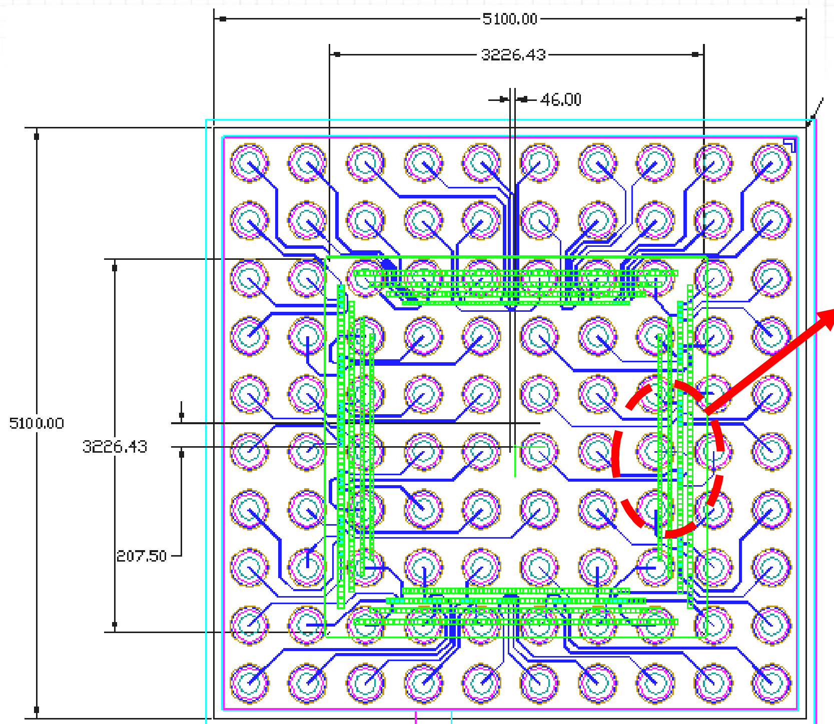
2nd Generation eWLB Technology

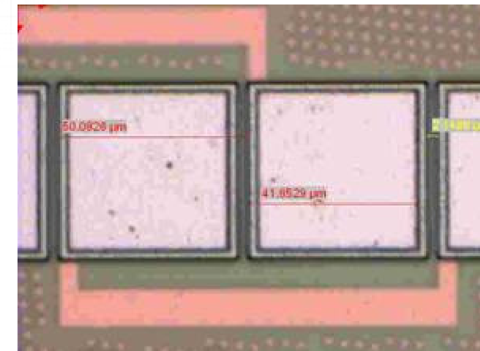


Confidential

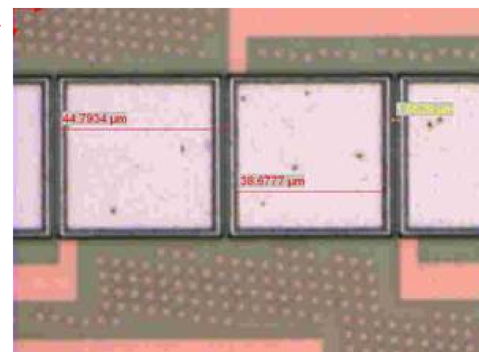
Fine Pitch: Sub 50um pitch 1st level Interconnection

- **Test Vehicle Features**

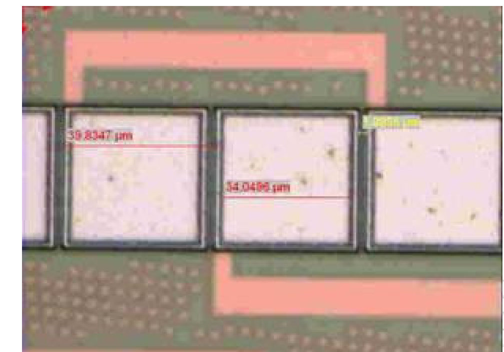




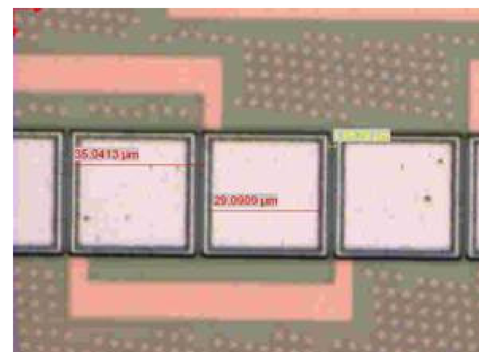
Outermost row



2nd inner row



3rd inner row



Innermost row

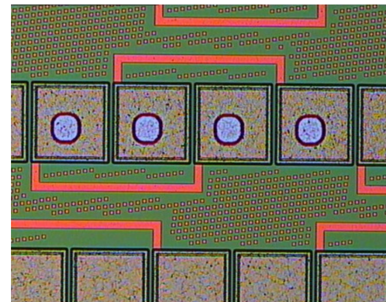
- Outermost row – pitch 50um
- 2nd inner row – pitch 45um
- 3rd inner row – pitch 40um
- Innermost row – pitch 35um

Fine Pitch: 50um pitch - 15um via

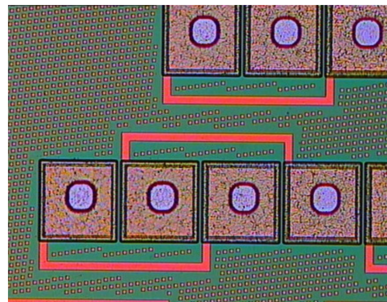
Confidential

Position on Carrier

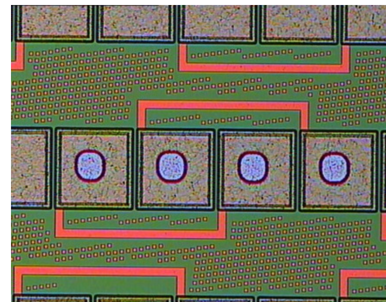
Top



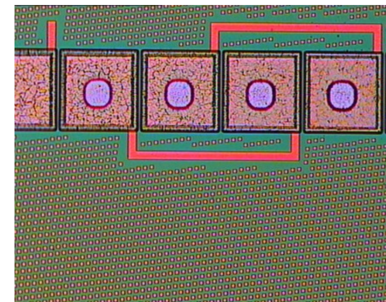
Left



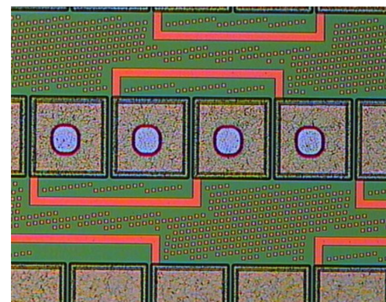
Center



Right



Bottom



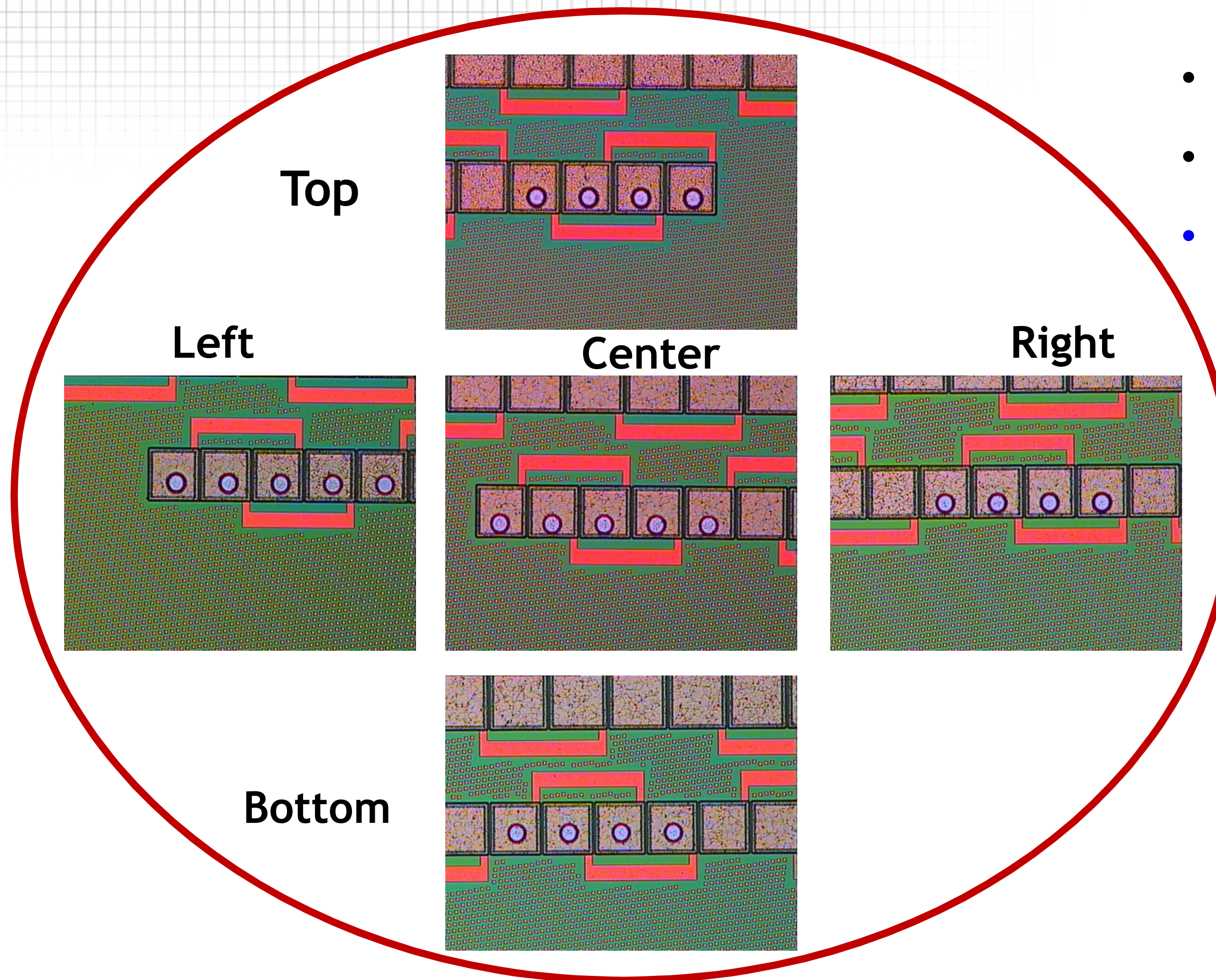
- 15um PSV via
- 43um I/O via
- **Overlap = 14um/side**

Process development and modeling used to improve registration between dielectric vias and true position of underlying pads across carrier area

STATSChipPAC

Fine Pitch: 35um pitch - 10um via

Confidential

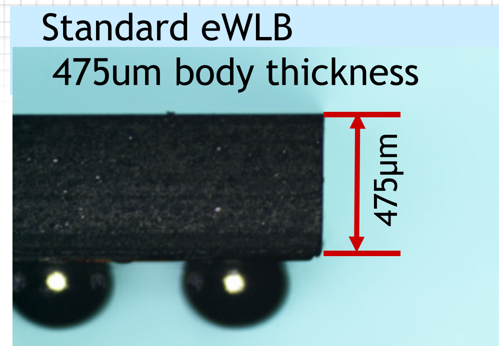


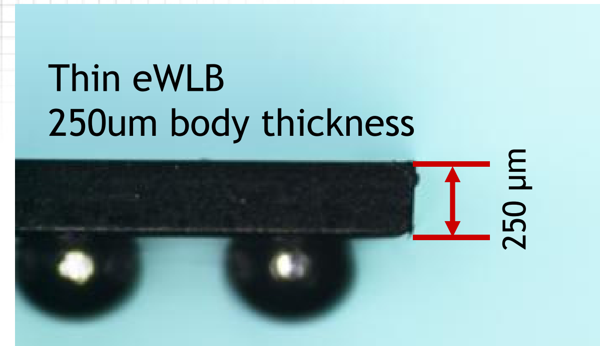
- 10 um PSV via
- 30 um I/O via
- **Overlap = 10um/side**

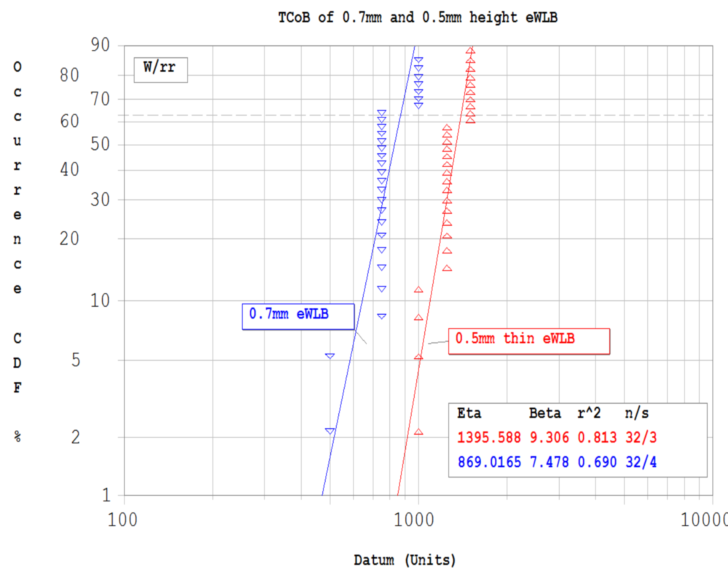
Demonstrated 10 um registration accuracy which enables 35 um linear pitch (or 25 um effective w/ 50 um pad pitch and 1 line between pads routing)

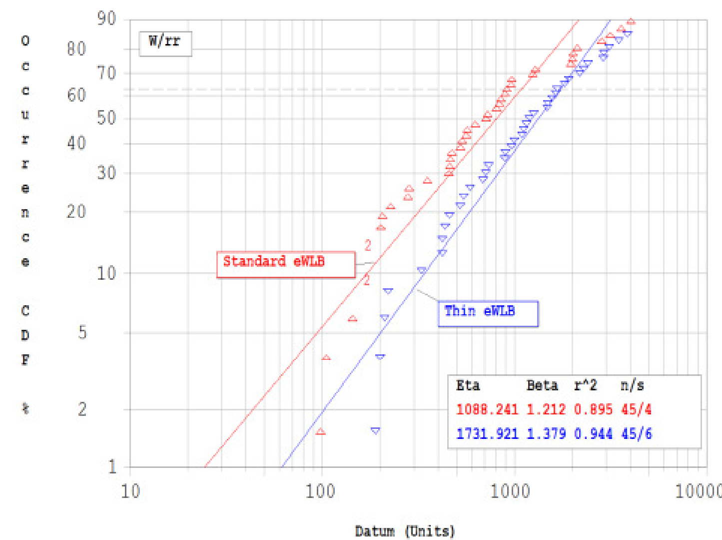
Confidential

Thin eWLB Solution





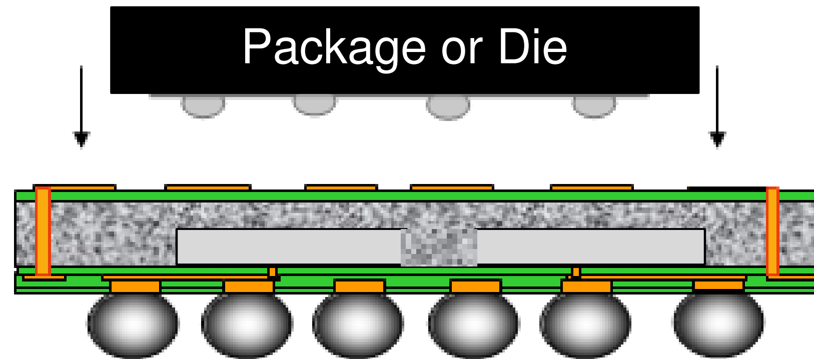




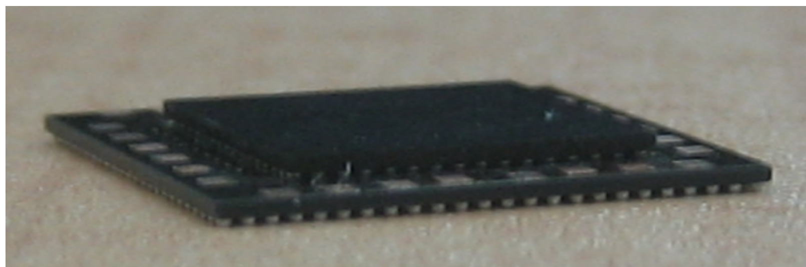
- Super thin profile eWLB package developed for mobile applications
- Superior BLR reliability by virtue of mechanical compliance of package body

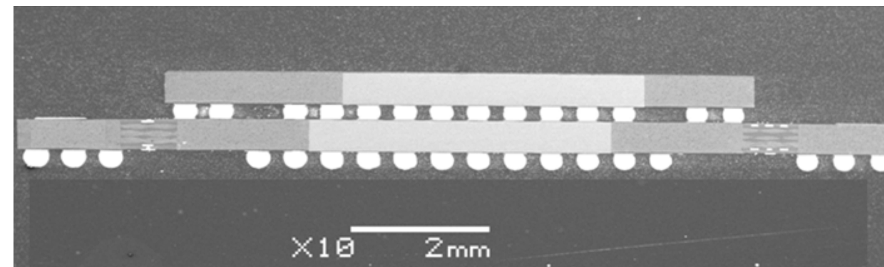
Confidential

2S - eWLB for 3D Packaging



PKG top (bare die, flipchip,eWLB)	0.3-0.5mm
eWLB bottom (thin eWLB)	0.5mm
Total	**0.8 - 1.0mm**



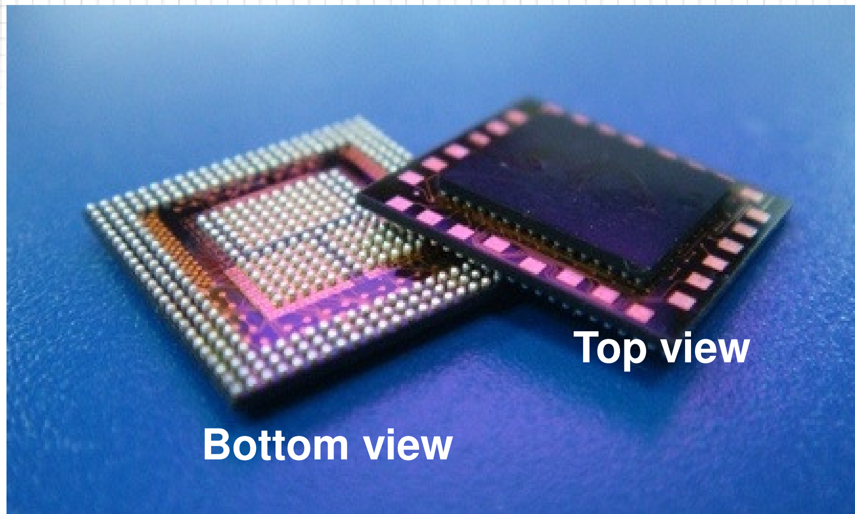


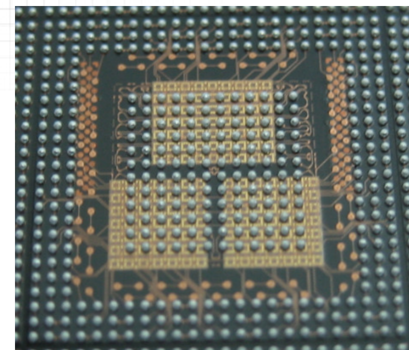
Courtesy of STATS ChipPAC - ST – Infineon 3D eWLB Alliance

- Breakthrough in density, performance and form factor !
- Provides compelling benefits for PoP packaging by virtue of sub-1.0 mm mounted height (PoPb + PoPt) and dramatic reduction in pkg warpage

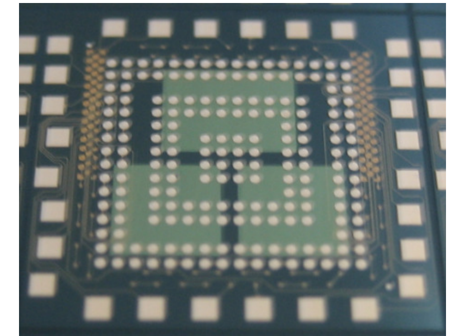
Confidential

2S eWLB for 3D Packaging

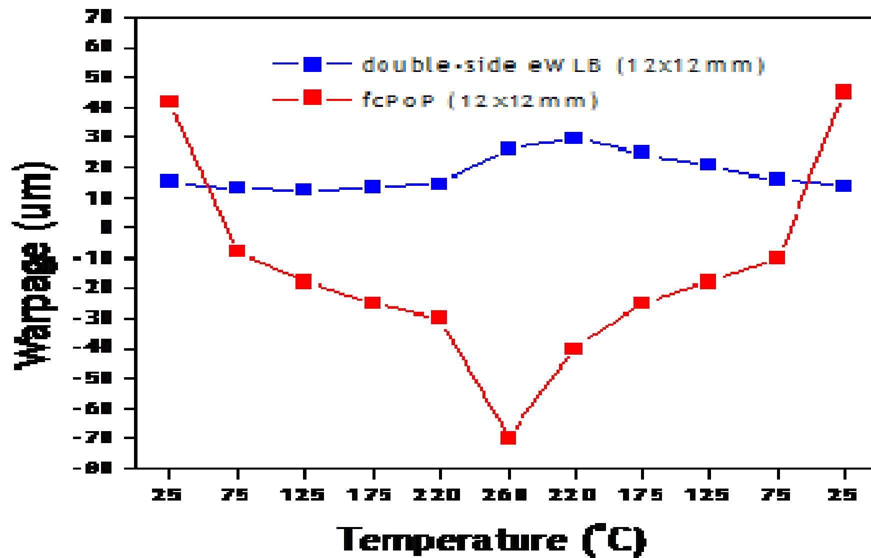


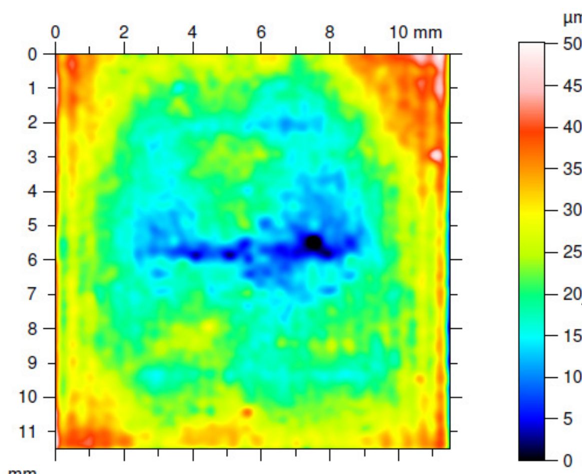


Bottom Pkg 2S eWLB
12 x 12 w/ 3 die



Top Pkg 1S eWLB
8 x 8 w/ 2 die





Thermo-Moiré Data
Max warpage 50 um

Courtesy of STATS ChipPAC - ST – Infineon 3D eWLB Alliance

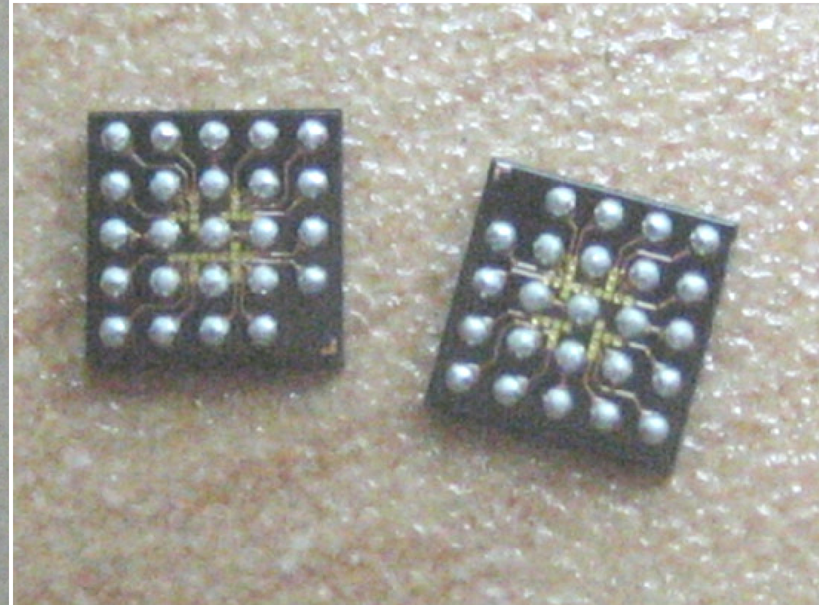
STATSChipPAC

Confidential

Extreme Small eWLB

Extreme-small,
3.2x3.2mm eWLB 0.4mm (1x1mm die)

Extreme-small,
2.7x2.7mm eWLB 0.5mm (1x1mm die)

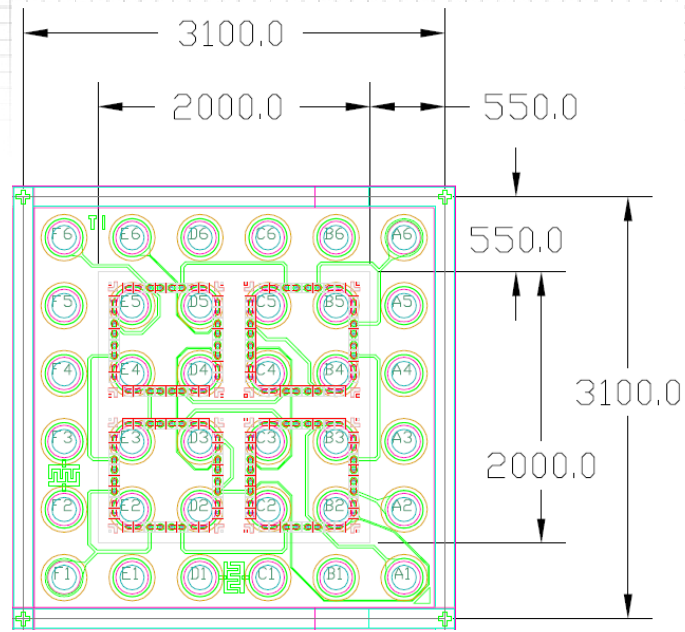


Courtesy of STATS ChipPAC - ST – Infineon 3D eWLB Alliance

- eWLB becomes progressively cost effective w/ body size reduction by virtue of economics of wafer-scale manufacturing
- “Extreme small” family competitive with FBGA, QFN of comparable pin counts and WLCSP w/ FR (fan-out ratio) of ~ 1 requiring die shrink
- Land grid versions (“eWLL”) under development for ultimate in low cost

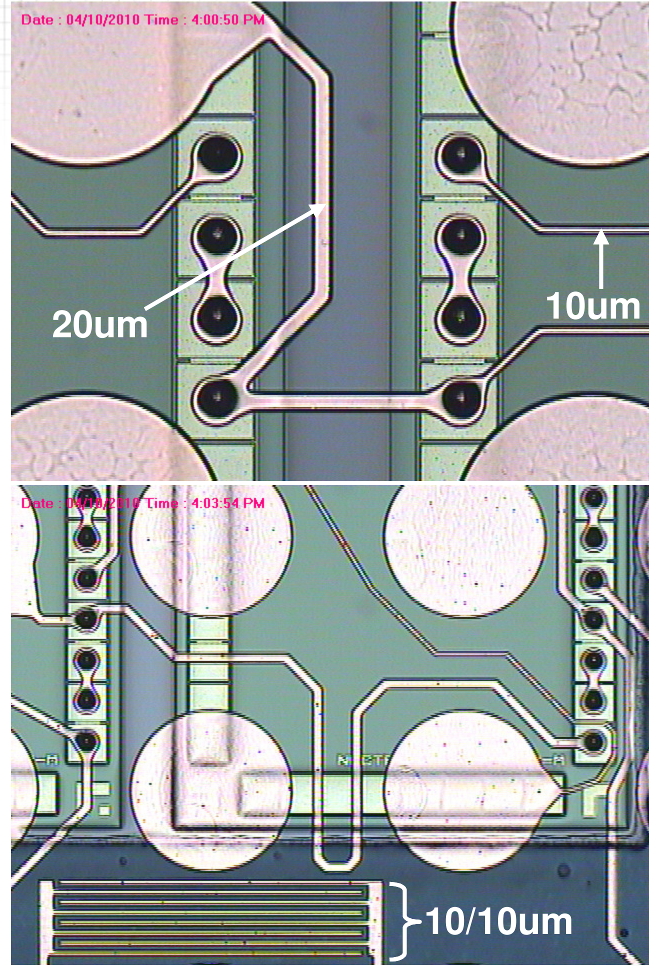
Extreme Small eWLB

Confidential



Die size – 2mm x 2mm

Package size – 3mm x 3mm

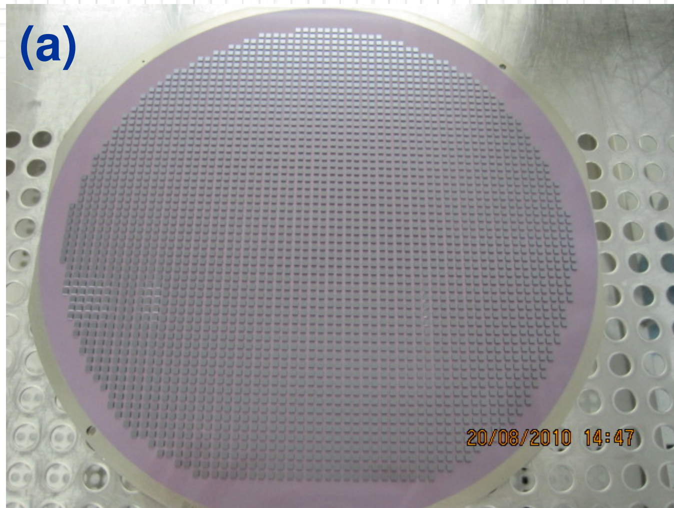


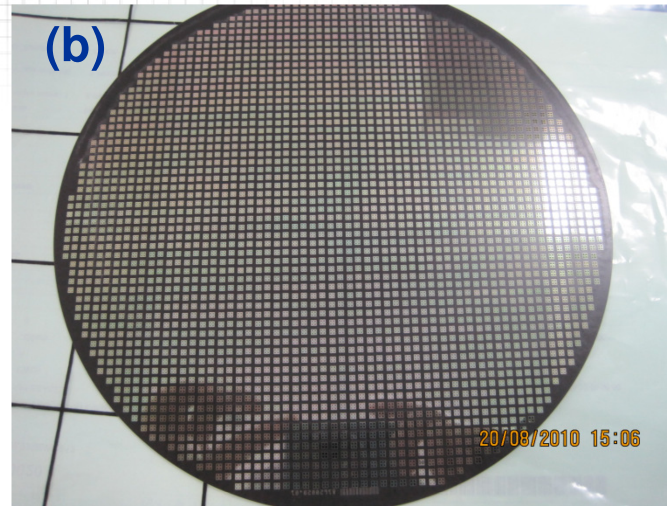
3.1 x 3.1 mm eWLB passed MSL1, TC1000X, UHAST, High temperature storage, bend, TCoB, drop reliability tests

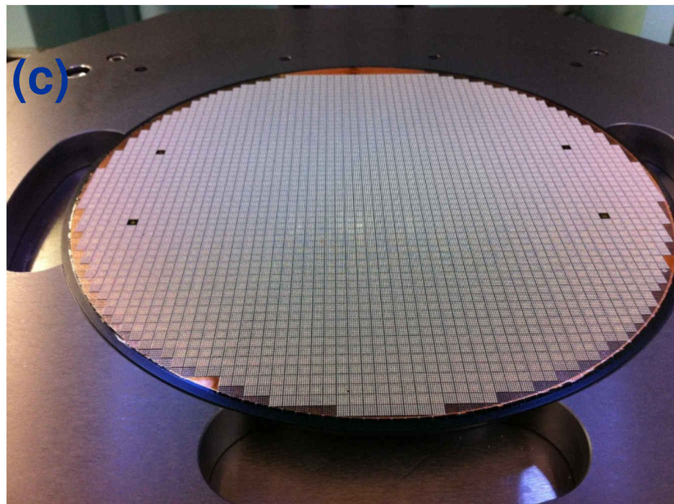
STATSChipPAC

Extreme Small eWLB

Confidential







(a) after pick & place
(b) after molding
(c) after back end

- ~ 3000 eWLB units / 200 mm carrier
- ~ 7000 eWLB units / 300 mm carrier

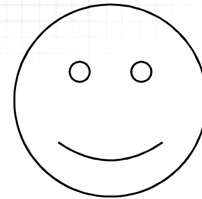
Summary

- There is an increasing trend towards Wafer level Packaging approaches over traditional substrate based solutions driven by increasing I/O densities beyond the 10-20 I/O /mm^2 range, associated with the advent of sub-40nm Si nodes; Fan-out packaging (eWLB) provides an appealing solution.
- eWLB technology is a mature, production proven packaging solution that presents a broad platform of offerings ranging from single sided, single layer structure to advanced 2.5D and 3D heterogeneous integration platforms with compelling advantages in performance and thin profile unattainable with traditional packaging
- eWLB adoption is poised to expand from the current application space of Mobile base-band and RF Transceiver products to
  i. 2.5D and 3D heterogeneous integration in mid range computing systems (Computers, Tablets) at the high end, and
  ii. Ultra-small Analog/Power packaging at the low end

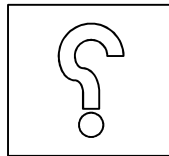
  This expansion will be further aided by new paradigms in manufacturing technology such as large panel carriers which are currently in development

Confidential

STATSChipPAC



Thanks!



Questions Welcome