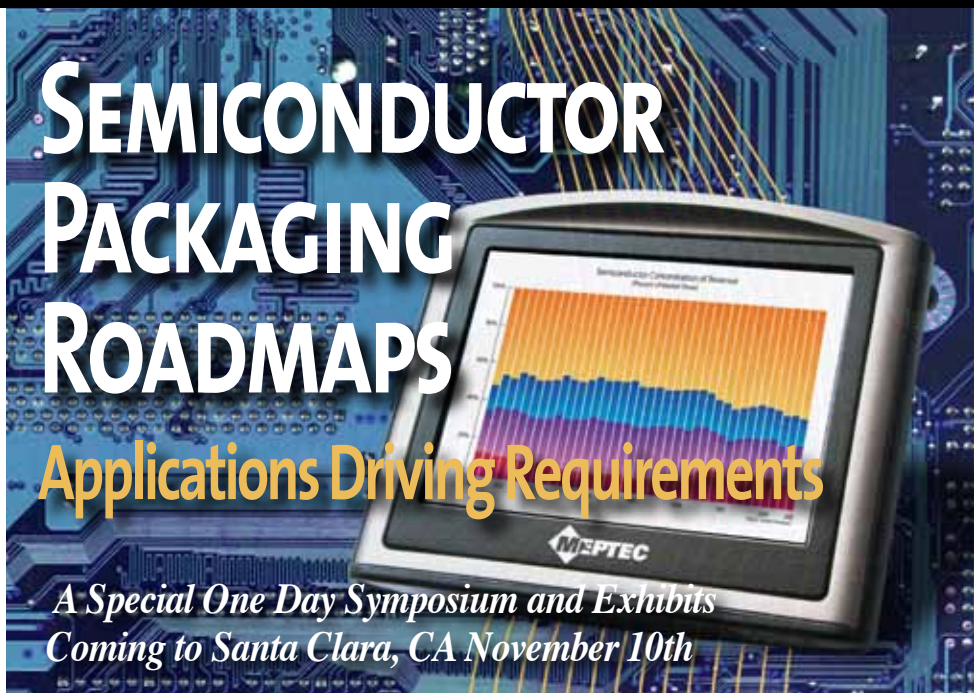
MEPTEC Report
Volume 14, Number 3
FALL 2010
A Publication of The MicroElectronics Packaging & Test Engineering Council




## INDUSTRY NEWS

**Sonoscan's** high-throughput P300 FastLine™ C-SAM® acoustic microscope was introduced at Semicon West. *page 14*

YOLE DÉVELOPPEMENT

**Yole Développement** has released the new report "3D Glass and Silicon Interposers: Technologies, Applications & Markets". *page 14*

semi™

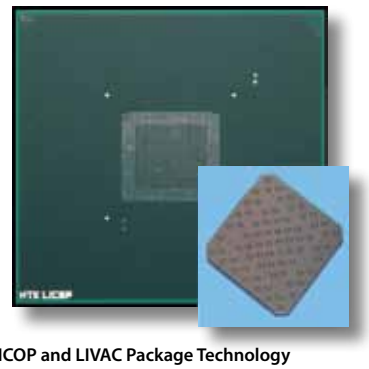
**SEMI's** World Fab Forecast indicated a 133% increase in equipment spending for Front End fabs this year and about 18% growth in 2011. *page 14*

SemiProbe™ PROBE FOR LIFE

**SemiProbe's** revolutionary Probe System for Life™ has been developed with proprietary technologies that are so unique they have been awarded a patent by the U.S. Patent and Trademark Office. *page 16*


**The MEMS Technology Summit – 25 Years in Perspective: Lessons from the Past and Vision for the Future. Don't miss this exclusive event and celebration on the occasion of the 25th anniversary of the founding of NovaSensor, a pioneering Silicon Valley MEMS company. The Summit will be held on October 19-20, 2010 at Stanford University, Stanford, CA. Visit www.memssummit.org for details.**

## MEMBER COMPANY PROFILE

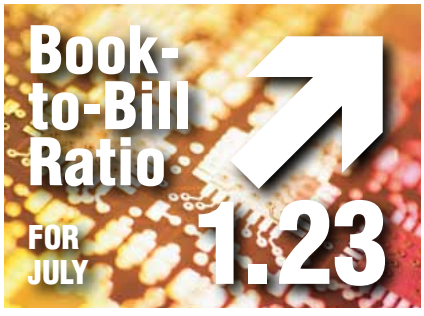


NTK's LICOP and LIVAC Package Technology

**Since their founding in 1936 as a manufacturer of spark plugs, the foundation of NTK has been one of technological innovation. The technology pioneering culture that was built around their core ceramics technology is the framework of NTK's internal culture.**

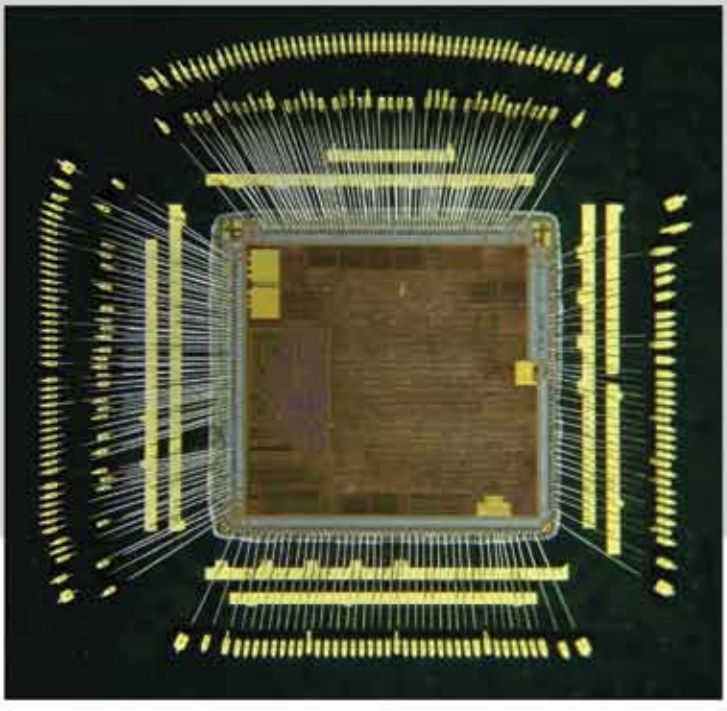
**NTK Technologies** has developed specialized technologies to provide advanced ceramic IC packaging solutions for mature and start-up semiconductor companies for nearly half a century. As one of the industries' largest packaging manufacturers, NTK's products and services have evolved to match the roadmaps of both complex ceramic and large scale organic applications. Their products are integrated in the entire array of semiconductor applications including computing, consumer, optical, wireless, medial, automotive, and space. *page 8*

Semiconductor equipment bookings increase 220.4% over July 2009 level. *page 16*



ASE GROUP

# Copper Wire



Copper Wire is a lower cost alternative to the traditional gold wire used in semiconductor packaging. Offering clear advantages, copper wire bonding is gaining popularity for products at 25 microns and below, where the majority of wire bond applications lie. ASE's copper wire bonding initiative is geared towards this group of applications. Bonding pad composition and wafer structure are major factors for copper wire evaluation, and ASE is customizing products based in specific customer needs.

**www.aseglobal.com**

MEPTEC report

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# Council Update

Welcome to the Fall issue of the MEPTEC Report! As in the last five years, our first post-summer event was our annual ***Medical Electronics Symposium*** which again was hosted by **Arizona State University** at the historic Old Main building on the Tempe campus. Last year's partnership with **SMTA** was a great success, so we decided to do it again this year. If you missed it, CDs of the proceedings are available – contact **MEPTEC** for information on ordering.

MEPTEC is pleased to be involved in the coordination and sponsorship of the ***MEMS Technology Summit*** to take place on the **Stanford University Campus** on October 19-20, 2010. The theme of the conference is *"Lessons Learned and Visions for the Future"*, and is also a celebration of 25 years of MEMS. Two of the MEPTEC MEMS symposium co-chairs, **Janusz Bryzek** and **Joseph Mallon**, are among the organizers of the conference, along with **Kurt Petersen** and **Roger Grace**. The conference will include an all-star lineup of speakers who represent the world's "who's who" of the MEMS community. In addition to the 24 technical presentations, two special multi-participant sessions and a panel discussion that will include some of the most financially-successful MEMS entrepreneurs will be held. Go to page 5 for more information, or visit www.memssummit.org.

The editorial this issue is by MEPTEC Advisory Board member **Jeff Demmin**. On page 22 Jeff writes about *"Looking into the Future at MEPTEC's Semiconductor Packaging Roadmaps Symposium"*. The event he is referring to is our Q4 event, ***Semiconductor Packaging Roadmaps: Applications Driving Requirements*** to be held on Wednesday, November 10, 2010 at the Biltmore Hotel, Santa Clara, California. As Jeff mentions we are returning to our successful past "roadmaps" topic for this event which we haven't covered since 2006.

**Mark Brillhart**, VP of Technology and Quality at **Cisco** will be our keynote speaker. In his talk, *Technology Innovation in High Performance Networking Products*, Mark will explore innovations in high-performance packaging that meet the challenges of high-speed electrical performance, signal and power integrity and enhanced thermal dissipation, as well as address the strenuous requirements of product-level reliability, high availability and long field life. In addition to a semiconductor technology roadmaps session, topics will cover technology development at the semiconductor assembly and test supplier companies; system-level implications on IC package design; and packaging roadmaps for emerging applications, including LED's, photovoltaics and medical applications. A limited number of exhibits and sponsorships are available; exhibit tables are currently half sold. See page 4 for further information.

Our Company Profile this issue is from long-time MEPTEC Corporate member **NTK Technologies, Inc.** NTK was founded in 1936 as **NGK Spark Plugs**. In 1967 the company expanded its ceramic expertise by founding NTK Technical Ceramics which eventually became NTK Technologies in 2002. Their services and products include packaging materials, semiconductor components, unique packaging technologies, and many more. See page 8 for their story.

Our Industry Analysis is from **Dan Tracy** of **SEMI** titled *Market Update for Semiconductor Equipment and Materials*. In the article on page 6 Dan addresses "the 2010 recovery in both semiconductor demand and capital investment following the dreadful period brought on by the global financial meltdown". He follows with further good news, which is the strength in the recovery. Thanks to Dan for this informative piece.

Our feature article is from **Jan Provoost**, Scientific Editor of **imec**. In *3D Chips: Stacked 2D or a Chance to Make Smarter Designs?* Jan starts his article by suggesting that by judging from the attention 3D chip manufacturing is getting, it may soon become mainstream. He further writes that "3D IC manufacturing and research as we know it today comes in three flavors". See page 12 for this informative article.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC PRESENTS

# SEMICONDUCTOR PACKAGING ROADMAPS

## Applications Driving Requirements

November 10, 2010 • Santa Clara, CA

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Gold Sponsors

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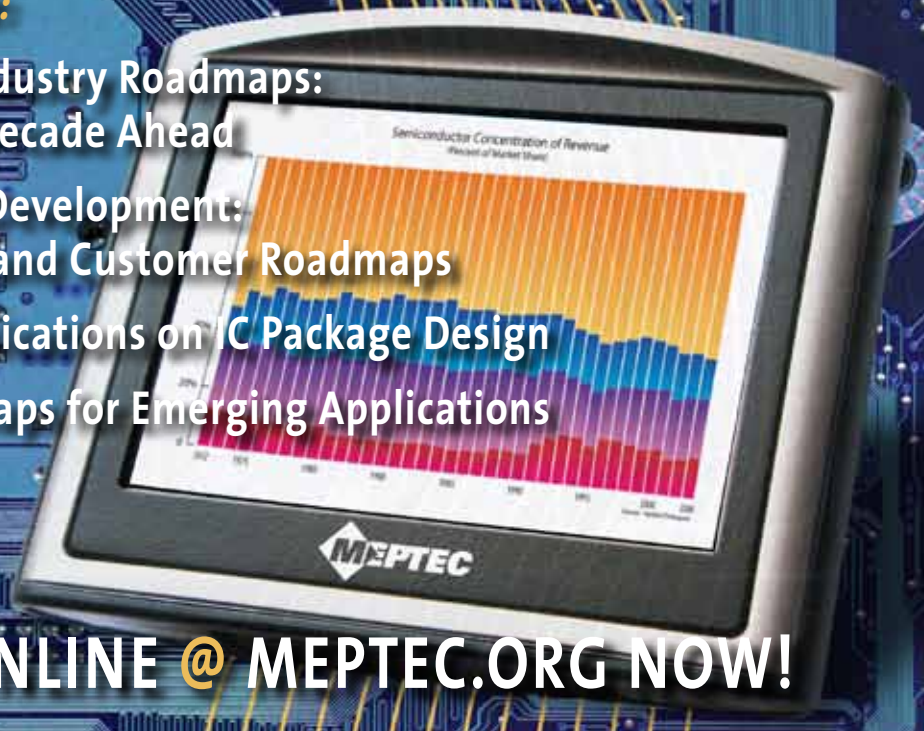
"Time Critical" Substrates

*Sessions will include:*

- Semiconductor Industry Roadmaps: Carving Out the Decade Ahead
- SATS Technology Development: Merging Internal and Customer Roadmaps
- System-Level Implications on IC Package Design
- Packaging Roadmaps for Emerging Applications

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## INDUSTRY EVENTS CALENDAR

| | | | |
|---|---|---|---|
| October 3-8, 2010 | **EOS / ESD Symposium** | USA | Sparks, Nevada |
| October 11 - 14, 2010 | **IWLPC - International Wafer Level Packaging** | USA | Santa Clara Marriott Hotel, California |
| October 13 -14, 2010 | **MD&M Medical Design & Manufacturing** | USA | Minneapolis, Minnesota |
| October 19-20, 2010 | **MEMS Technology Summit** | USA | Stanford University, Stanford, California |
| October 19-20, 2010 | **Thermal Management & Technology** | USA | Dallas, Texas |
| October 19-21, 2010 | **Semicon Europe** | Germany | Dresden |
| October 24-28, 2010 | **SMTA International** | USA | Orlando, Florida |
| October 31 - November 3, 2010 | **Milcom** | USA | San Jose, California |
| October 31 - November 4, 2010 | **IMAPS Symposium** | USA | Raleigh, North Carolina |
| November 3-4, 2010 | **Design-2-Part Show New England** | USA | Marlborough, MA |
| November 3-4, 2010 | **SoC - System on Chip Conference** | USA | Newport Beach, California |
| November 8-9, 2010 | **SVTC - Test Conference & Exhibition** | USA | San Jose, California |
| November 10, 2010 | **MEPTEC Semiconductor Packaging Roadmaps** | USA | San Jose, California |
| November 16-18, 2010 | **SMTA High Performance Cleaning** | USA | Schaumburg, Illinois |
| November 17-18, 2010 | **Design-2-Part Show - Tech Triangle** | USA | Raleigh, North Carolina |
| November 29 - December 2, 2010 | **I / ITSEC** | USA | Orlando, Florida |
| November 30, 2010 | **Counterfeit Electronic Parts Symposium** | USA | College Park, Maryland |
| November 30 - December 2, 2010 | **Printed Electronics USA** | USA | Santa Clara, California |
| December 1-2, 2010 | **Photovoltaics 2010 & Printed Electronics** | USA | Santa Clara, California |
| December 1-3, 2010 | **Semicon Japan** | Japan | Makuhari |

Calendar Listings Courtesy Topline. Visit **www.topline.tv/tradeshows.cfm** for more details.

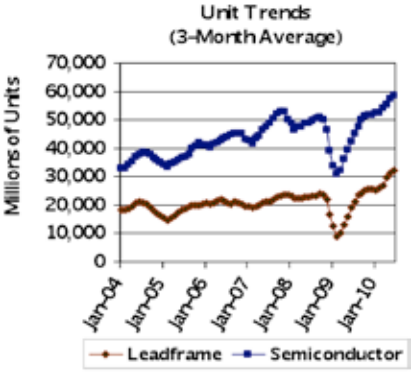
# Market Update for Semiconductor Equipment and Materials

***Daniel Tracy***
***Senior Director, Industry Research & Statistics***
***SEMI***

The 2010 recovery in both semiconductor demand and capital investment is welcomed across the industry following the dreadful period brought on by the global financial meltdown. The strength in the recovery following the market bottom in early 2009 is remarkable given that 2010 will now unfold as a record year for semiconductor revenues and unit shipments as consumers continue to spend on electronic gadgets. And looking ahead, many analysts are forecasting semiconductor revenue growth in the range of 5% to 10% for both 2011 and 2012.

Figure 1 highlights the full in the recovery in terms of unit shipments: for total semiconductor devices and for leadframe shipments. Shipments in each segment have increased sharply off the 2009 low, surpassing pre-downturn levels a number of months ago, and have set new highs beginning with the June data. Rising demand for electronics, and thus semiconductors, means fabs and assembly plants are more fully utilized, which in turn drives the growth and recovery in equipment spending and in semiconductor materials consumption.

Through the first half of 2010, semiconductor equipment revenues reached $16.6 billion, more than the total spending recorded for all of 2009 (Table 1). Improvements in spending will be significant for all the regions tracked in the SEMI/SEAJ Worldwide Semiconductor Equipment Market Statistics (WWSEMS) data program, with particularly strong year-over-year spending growth forecasted for Korea, China, Taiwan, and Rest of World. Several key companies in the industry, such as Samsung, TSMC, ASE, and Siliconware, have announced historically high capital spending plans for 2010, with investments occurring at both the fab level and for assembly and test.




Source: WSTS/SIA and SEMI

**Figure 1. Unit Shipment Trends for Semiconductor Devices and Leadframes.**

Spending in the Assembly and Test equipment segments is expected to increase by about 109 percent in 2010 compared to 2009. Spending will support added capacity for advanced packaging applications, such as wafer-level packaging and bumping and the transition to copper wire bonding. In Test, device makers and OSATS (packaging/test subcontractors) are investing in systems that provide higher throughputs and can support higher frequencies. Spending on Assembly and Test equipment in 2010 will be well below spending reported in 2006 and 2007, though a substantial improvement from the dismal levels in 2009 (Table 2).

Currently, just a modest 1.1 percent growth in Assembly and Test equipment spending is forecasted for 2011. Some spending planned for 2010 could spill over into next year in terms of reported billings (revenues) for equipment. This is due to possible constraints in the component supply chain, given the sharpness in the recovery, thus spending growth in 2010 could dampen slightly and may show up in 2011 revenues.

The total semiconductor materials market is expected to recover to almost $40.5 billion in spending this year and approach $43 billion in 2011 (Figure 2). Though the rebound in 2010 coincides well with the growth in semiconductor units, downward pricing pressure moderates the materials market year-over-year growth some.

**Table 1. Equipment Spending by Region.**
(The following results are given in terms of market size in billions of U.S. dollars)

| | 2009 Total | 2010 Year to Date through June | 2010 Total Forecast | % Growth 2010F vs. 2009 |
|---|---|---|---|---|
| **North America** | $3.39 | $2.13 | $4.57 | 35% |
| **Japan** | 2.23 | 1.88 | 4.08 | 83% |
| **Europe** | 0.97 | 0.86 | 1.92 | 98% |
| **Rest of World** | 1.44 | 1.66 | 3.01 | 109% |
| **Taiwan** | 4.35 | 4.82 | 9.18 | 111% |
| **China** | 0.94 | 1.15 | 2.24 | 138% |
| **Korea** | 2.60 | 4.07 | 7.49 | 188% |
| **TOTAL*** | **$15.92** | **$16.57** | **$32.50** | **104%** |

*Totals may not add due to rounding.

Source: SEMI and SEAJ

**Table 2. Total Spending on Assembly and Test Equipment.**
(The following results are given in terms of market size in billions of U.S. dollars)

| 2006 | 2007 | 2008 | 2009 | 2010F | 2011F |
|---|---|---|---|---|---|
| $8.80 | $7.90 | $5.49 | $2.96 | $6.18 | $6.25 |

The packaging materials market will reach an estimated $18.8 billion this year, with substrates and advanced resin materials (die attach film materials, underfill, and green mold compounds) being key growth segments. This market is forecasted to reach $19.7 billion in 2011.

Downward pricing pressures and increased competition amongst suppliers are important factors that could hamper revenue growth for packaging materials suppliers. Materials, however, have been critical in improving and developing new packaging technologies that the industry has introduced over the past decade. Material solutions and process integration will remain crucial to solving emerging challenges in packaging technologies and, as the industry moves to 32 nm and smaller device geometries, there are new material requirements that are difficult to define today.

With the downturn behind us, the semiconductor industry can focus on growth and on solving the technical hurdles that remain ahead. ◆


| | 2006 | 2007 | 2008 | 2009 | 2010F | 2011F |
|---|---|---|---|---|---|---|
| Packaging | 15.54 | 17.59 | 18.32 | 16.78 | 18.78 | 19.73 |
| Fab | 21.70 | 25.08 | 24.19 | 17.85 | 21.71 | 23.19 |

Totals may not add due to rounding. Source: SEMI Industry Research and Statistics, July 2010

**Figure 2. Total Spending on Fab and Packaging Materials.**

*The SEMI Industry Research and Statistics group provides timely market and trend information for market research, competitive analysis, and sales forecasting. We focus on the global semiconductor capital equipment, selected materials markets and fab forecasting data. Please visit www.semi.org/marketinfo for additional information.*

# NTK TECHNOLOGIES INCORPORATED

## In the Forefront of Ceramic and Organic Packaging

**NTK TECHNOLOGIES is a subsidiary of NGK Spark Plugs, Co. Ltd., (www.ngkntk.co.jp). Founded in 1936, NGK Spark Plugs is a ceramic components pioneer in the automotive industry with over 70 years of success supporting leading edge design and manufacturing of ceramics. With the inception of NTK Technical Ceramics in 1967, NGK Spark Plugs expanded its ceramic expertise by developing products and services for the semiconductor industry. NTK Technical Ceramics became NTK Technologies Inc. in 2002 as they further broadened their package offering beyond ceramics and into organic packaging.**

For nearly half a century, NTK has developed specialized technologies to provide advanced ceramic IC packaging solutions for mature and start-up semiconductor companies. As one of the industries' largest packaging manufacturers, NTK's products and services have evolved to match the roadmaps of both complex ceramic and large scale organic applications. NTK's products are integrated in the entire array of semiconductor applications including computing, consumer, optical, wireless, medial, automotive, and space.

With corporate offices in Nagoya, Japan, NTK Technologies Inc. and NGK Spark Plugs, Co. Ltd., are globally recognized as a premium brand. NTK's Sales and Design Centers and Production Facilities are positioned to facilitate close proximity to customers around the world. In the United States, there are seven Sales and Design Centers with the US headquarters located in Silicon Valley.

### NTK Technologies Expanding Markets

Since their founding in 1936 as a manufacturer of spark plugs, the foundation of NTK has been one of technological innovation. The technology pioneering culture that was built around their core ceramics technology is the framework of NTK's internal culture. NTK continues to nurture and develop new technologies that strengthen or expand product lines to offer solid customer service into the future.

Global Sales, Service & Manufacturing Sites

**A World-Wide network of design, sales, and manufacturing centers support the semiconductor industry.**

Beyond the Organic and Ceramic Packaging Businesses, NTK has been expanding their business field to areas such as semiconductor processing, medical, environment and energy products for which demands are expected to increase in the future.

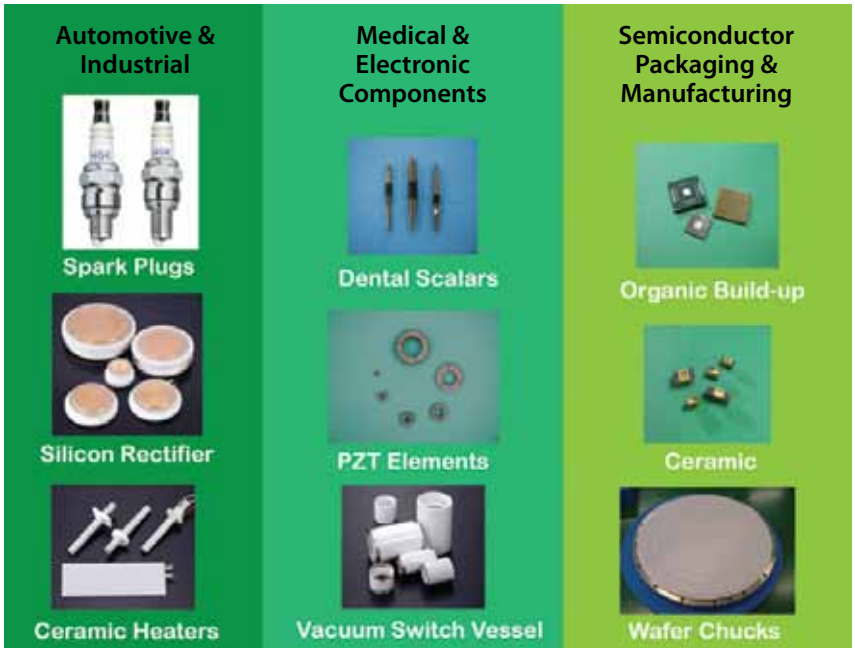
Their scope of business also extends to products used in various fields, such as transportation and information, in order to meet the changing social needs. NTK targets the cutting edge of the information and communications fields, including motorization, which will be the core industry of 21st-century society. NTK has invested in advancements in the medical field in each of its business unit segments based on the application of ceramic and organic centered technologies. Furthermore, the object of their vigorous research includes the environmental field.

### Materials for Mainstream Markets

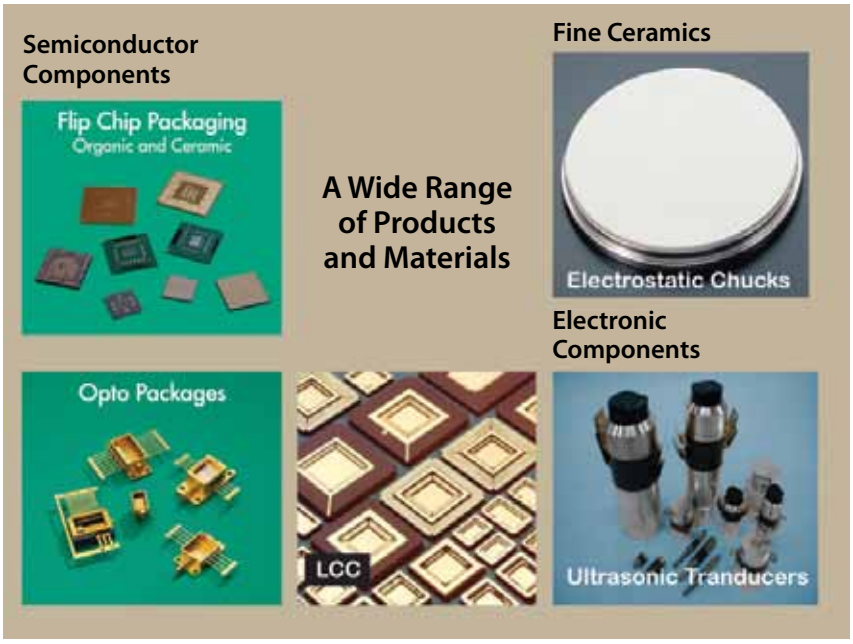
High paced markets such as CPU, Medical, RF, Power, Imaging, and Automotive demand packaging approaches that overlap ceramic and organic materials.

As a total package manufacturer responding to a diversity of needs, NTK Technologies offers a rich array of products using organic, HTCC, LTCC and other materials including: IC packages for MPUs, Arm-Based Processors, Communication, and automotive parts, dielectric filters for cellular telephones, and dielectric resonators for base stations.

In the United States, NTK Technologies' Semiconductor Components, Electronic Components, and Fine Ceramics Divisions support these growing market segments.




**NTK offers a broad range of metal and ceramic technologies for high integrity applications.**




**NTK's Semiconductor Components and Manufacturing Products.**

### Semiconductor Components – Organic and Ceramic Packaging

A diversified catalog of Ceramic and Organic Packaging products are integrated in the entire array of semiconductor applications centering around: Medical, Mobile, Computing, Consumer, Optical, Wireless, Automotive, and Satellite and Space.

In the past decade, the semiconductor industry has seen a continued shift for mobile and multi-media-based consumer applications. This consumer product trend has translated into demand for highly customized IC applications. Designs have grown in numbers while the product cycles continue to be reduced. NTK Technologies' design manufacturing services are aligned to service the fables sector by offering quick response to multiple designs and supporting short manufacturing cycle times.

### Markets and Unique Packaging Technologies

Mobile, Data communications, Networking, and Computing Products continue to evolve rapidly in three areas – compactness, high density, and ultra-high speed. In the present era of mobile, multi-media based on digital networks, the momentum of this evolution is building up at an increasing rate. The merging architectures of PCs and Mobile phones is imposing new technology development challenges for packaging.

### New Packaging Material Technology for Mobile Applications

Compact packages that can support, compact, Z-height requirements, without penalizing performance and while achieving low-price targets, are highly desired. A low loss package and streamlined manufacturing integration of embedded components can be the optimal response for these requirements. This complex application was the motivation behind NTK's new LICOP Technology

**LICOP (Low Inductance Capacitor in Organic Package)** is a new hybrid technology that enables placement of large number of embedded decoupling capacitance directly beneath the die. The LIVAC (Low Inductance Via Array Capacitor) Technology, as it is termed, offers an advanced approach for combining the electrical and thermal benefits of both packaging materials. The capacitor placement can be design-optimized for performance and manufacturability. LICOP streamlines the manufacturing flow by merging the capacitor manufacturing at the package and board level and by offering better reliability compared to traditional assembly approaches. The resulting cost, reliability, and form-factor advantages make this technology ideal for high density FPGA, ASIC, and MPU applications.

### Packaging Materials

With market trends driving demand for custom IC designs to support the expanding mobile computing and communication markets, NTK Technologies has internally developed a variety of package materials and package outlines for a wide range of applications. From RF Power packages that are Void free die attach to High-pin count Flip Chip devices with fine bump pitches. A growing number of applications are supported in the electrical side with custom dielectric materials and on the thermal side, with design-specific coefficients of expansion.

## NTK Technologies Semiconductor Products

**Semiconductor Products**

- **Organic Build-up Packages**
  - Packages for MPU/CPU/FPGA/SoC
  - Packages for Chip-set
- **Ceramic Packages**
  - Crystal Device/SAW Filter Package
  - High Frequency/Microwave Package
  - Fiber Optic Package
  - Multi-chip Module Substrate
  - Multi-layer LTCC Substrate/Module
- **Space Transformers - Multi-layer**

**Electronic Components**

- Piezo Ceramics
- Piezo Transducers
- Dielectric Resonators

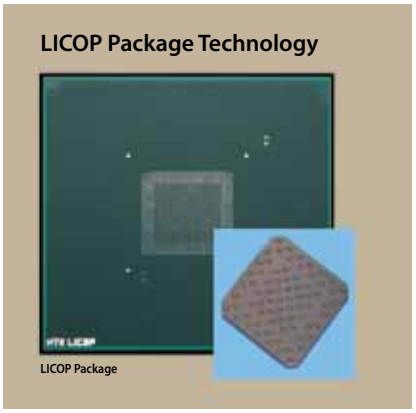
**Fine Ceramics for Semiconductor Manufacturing**

- Electrostatic Chucks
- Vacuum Chucks

**NTK Technologies Main Product Lines.**

### Supplying Leading Edge Packaging and Components

NTK has developed specialized technologies that adapt to the wide range demands of industry leaders and start-up companies. With world-class research & development and manufacturing capacity, NTK's products and services have been a proven asset in supporting the development of evolving technologies.




**LICOP and LIVAC Technologies. NTK stays in the forefront with advanced technology to support custom ASIC, FCBGA, and high pin-count at ultra-high speeds. LICOP packages with embedded LIVAC are being designed into high speed computing and complex networking applications.**

| Ceramic Materials | Electrical | | | | Thermal | | Mechanical | | Conductor Material |
|---|---|---|---|---|---|---|---|---|---|
| | Dielectric Constant | | Tan | | CTE | Thermal Conductivity | Flextural Strength | Young's Modulus of Elasticity | |
| | (1 MHz) | (2 MHz) | (1 MHz) | (2 MHz) | | | | | |
| HTCC | 9.2 | 9.2 | 0.0005 | 0.0009 | 7.6 | 17 | 350 | 280 | W, Mo |
| LTCC | 7.6 | 7.5 | 0.0030 | 0.0040 | 5.4 | 3 | 260 | 120 | |

**Ceramic material options include HTCC and LTCC.**

| Packages | Technology | Requirements |
|---|---|---|
| Flip Chip | Pb free, Green Pkg, Ceramic | Fine bump pitch, Low K, Ultra low K, High Thermal Design |
| MCM | Hirel | Void free die attach, E-testing and burn-in |
| Image Sensors | Large Die, High Density | Flatness |
| RF Products | Small die | Void free die attach, E-testing and burn-in |

**Leading edge packaging and requirements.**

### Advanced Wafer Probe Cards Integrate NTK's High Speed Space Transformers (STFs)

The IC Test of memory and high density devices continues to put significant pressure on yield and manufacturing cost reduction. As IC volumes rise, the test strategies for achieving good yields and short manufacturing cycle times have to be defined sooner in the product design phase. The consumer market, which has had the largest growth momentum in recent years, requires memory and System on a Chip (SOC) IC products to track the short lead times. To respond to the time to market manufacturing challenges of advanced IC devices, NTK developed an advanced multi-layer ceramic substrate that integrates flexible internal layout and route designs in a Space Transformer. Within this technology, critical design methods are employed in achieving trace length matching for high speed differential pairs, while maintaining tight impedance controls. Single-ended strip line structures are custom designed to meet strict low tolerance requirements. NTK's Space Transformers deliver high density, small pitch requirements in a multilayer co-fired ceramic.

NTK's Space Transformers are a central part of the hardware test strategy for devices with ground-breaking technologies. As test strategies begin to move towards parallel test or single touch-down test solutions, NTK's Space Transformers can offer high density performance with reliability.

### Electronic Components

NTK dedicates part of its development to the advancement of technologies that support optimal patient care such as minimally invasive surgeries, and dental equipment. Their partnerships with leading medical companies put them in the forefront of development.

Ceramic-based medical products continue to increase in demand due in great part to the changing medical needs of a growing and an aging population. Ever evolving medical advances drive the need for medical instruments with improved reliability and precision performance that are often best addressed with miniaturization. NTK has also long developed advanced ceramic-based industrial components including Ultrasonic Transducers, Ultrasonic Sensors, PZT Elements and Dielectric Resonators.

The market for piezoceramic elements is a diverse medical market that includes plastic surgery, medical delivery systems, and organ-related surgical procedures as well as ear, nose, and throat procedures (ENT). The electroceramic can more precisely act as a sensor in detecting the presence of air in a liquid substance.

PZT ceramics can be manufactured with traditional ceramic processes for commodity applications. Advanced applications of PZT ceramics for the medical industry, require precision tooling and manufacturing processes. Complex medical applications that benefit from the PZT material properties often run at small quantities. Less invasive but yet precision, critical applications include infusion delivery systems (Intravenous) which incorporate liquid and air sensors, dental scalars, ultrasound elements, and ultrasonic cleaners for medical applications.

The use of piezoceramics in the medical market is in its infancy for a variety of new medical applications still being explored. An expansion of its use is expected in the future in line with the medical demand from the aging population.

Also Piezo ceramics/Transducers and welders have been used for more industrial machines such as wire bonders, flip chip bonder and welding machines. NTK can provide a variety of PZT materials in different sizes and has over 40 years of history of manufacturing transducers using these PZT materials.

### Fine Ceramics

Through its established Fine Ceramics Division (FCD), NTK is also a pioneer of ceramic based technologies for semiconductor manufacturing equipment. FCD's products include advanced ceramic components, such as Electro-static Chucks, Vacuum Chucks. NTK's wafer chuck's are widely used in various stages of wafer processing and verification including ETCH, CVD, in vacuum/plasma environment, as well as Metrology (Wafer-Inspection) applications.

### NTK Technologies Supporting Advanced Packaging and Wafer Manufacturing Challenges

In the coming decade, NTK foresees a new wave of innovations challenging the supply chain to deliver products and services that support the new demands. The drive for new supply chain methods comes from the evolving high speed products from the growing markets of this decade. NTK continues its emphasis in providing new generations of ceramic, organic, and hybrid packaging. The NTK manufacturing infrastructure is on track with the package customization and short cycle times that are to come. NTK's deep involvement in development of wafer chucks and space transformers will enable the company to remain prepared to meet future IC fabrication requirements. Next generation nanometer process technologies, high density silicon stacking, power-smart device architectures, and high speed, light, and compact packaging will need to work in unison to support this new evolution in semiconductor development.

For more information on NTK Technologies Products and Services, contact NTK Technologies, Inc., 3979 Freedom Circle Drive, Suite 320, Santa Clara, CA 95050, phone: 408-727-5180, or visit www.ntktech.com. ◆


**NTK's ceramic-based medical/industrial components include Ultrasonic Transducers, Ultrasonic Sensors, PZT Elements and Communications Components. These products have been integrated into diverse medical products including but not limited to ultrasonic scalars, ultrasound systems, and a variety of hospital related equipment.**

**Technical Conference**
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Recognized as our industry's strongest technical program

**Electronics Exhibition**
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# 2010 SMTA International

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# 3D Chips: Stacked 2D, or a Chance to Make Smarter Designs?

***Jan Provoost***
***Scientific Editor***
***imec***

Judging from the attention 3D chip manufacturing is getting, it looks as if it will soon become mainstream. Nearly every chip manufacturer is working on 3D, and every week, there is a 3D conference somewhere. But at the same time, the open questions and technological options surrounding 3D abound.

Are we in for a 3D chip future? Or will 3D chips be limited to a few niche applications? And how far can we take 3D? Do we simply stack 2D designs, or can we design smarter, specific 3D architectures? Will we be able to manufacture those new 3D designs, technically and economically?

Notwithstanding these questions, the first 3D chips have already hit the market. Flash memory cards, for examples, are made of stacked memory chips, drastically increasing the number of memory cells per package. This way, 3D chips are already part of the scaling story – building ICs always smaller, faster, and cheaper. Where 2D miniaturization is faced with ever more complex challenges, it seems as though 3D can maintain Moore's momentum. And, on top of that, 3D offers a number of interesting new design possibilities.

### 3D IC Manufacturing and Research – As We Know it Today – Comes in Three Flavors

Packaging a stack of standard 2D-chips is a first possibility. This way of working does not change the chip design or the foundry processes; only the packaging process is involved. The chips are wire-bonded: the connections are made outside of the chips. An obvious example, available today, are stacks of Flash memory chips forming a memory package of, say, 16 Gbyte. But it is also possible to stack a logical chip and one or more memory chips, or a sensor, a logical chip and a memory chip.

Round, micro-sized holes etched in the silicon and filled with copper are the basis of the second technique. If the silicon wafer is then thinned until the copper nails stick out at the backside, we have chips with through-silicon contacts, or vias as they are also called. Next, the thinned wafer is placed on top of a second one, so that the copper nails on the backside of the thinned wafer contact the landing pads on top of the second wafer. This technique allows for direct contact points between the chips, making interconnect many orders of magnitude shorter and denser than those of wire-bonded packages. But this technique requires a specific chip design that distributes the components optimally over the two or more layers. And also the production process will change. The transistors, for example, have to be placed on the silicon such that there is room for the vias. And then the vias have to be etched and filled. Last, the chips have to be positioned over each other with extreme precision.

Over the next few years, research centers and chip manufacturers will perfect this technique. And following the introduction of the first 3D chips with trough-silicon vias, there will again be a lot of opportunities for further scaling. We can go on making thinner chips, smaller vias, and better designs.

Venturing into extreme 3D, we arrive at a foundry-only technique where we build the chips themselves in three dimensions. One idea is to grow extremely thin layers of silicon on a carrier, diffuse the transistors into that layer, add an interconnection layer on top, grow a new silicon layer, and so on. The interconnection layers will contact one another though nano-vias through the silicon layers. Because these vias will be so small, they can be made extremely dense, so that connections between individual transistors become possible. It would then be possible, for example, to manufacture a layer with p-transistors only, connected to a layer with n-transistors. It goes without saying that the design phase for this type of chips will be paramount. But also the production process will be totally different from what we know today.

Only time will tell if this technique will ever be viable. Today, it is still in the first stages of research. And we still don't know how much real value it will bring, and if such chips can be produced technically and economically.

Opportunities and technological options aside, there is also the question as to why we would build chips in three dimensions. Here I see some possibilities that reinforce each other. First there is the possibility to maintain Moore's momentum for a considerable time to come. Already the first 3D applications, for example Flash memories, show the promise of denser, smaller, cheaper chip stacks. And then we are just beginning to use the 3D possibilities. In other words: a new scaling landscape is opening up.

Second, if we design specifically for 3D, we can realize solutions that are very hard to achieve in 2D. In the current generation of chips, we are forced to place memories, such as an L1 cache, next to logical circuits. This is because today's fast processors can no longer efficiently work with off-chip memory alone. But it is expensive to manufacture logic and memory in one process. A 3D design could solve this dilemma, connecting a logical layer with a dedicated memory layer. By keeping interconnects extremely short, this could make an efficient design.

Thirdly, we can use 3D for heterogeneous integration, stacking dedicated layers with different technologies, such as logics, MEMS, RF, or bioactive substrates. This way, 3D designs could form autonomous embedded ICs used in clothing or healthcare applications. ◆

# IMAPS 2010

# 43rd International Symposium on Microelectronics

*Bringing Together The Entire Microelectronics Supply Chain!*

## Research Triangle

## November 2-4, 2010

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The 43rd International Symposium on Microelectronics will be held at the Raleigh Convention Center, Research Triangle, North Carolina, USA, and is being sponsored by the International Microelectronics And Packaging Society (IMAPS). The Symposium will cover four tiers of electronics: Industry, Systems & Applications, Design, and Materials & Process.

## Planned Sessions Include:

### Materials and Process

- Flip-Chip and Wafer Bumping Processes and Reliability
- Underfill/Encapsulants and Adhesives
- Pb-Free Solder Materials, RoHS, Processes, and Reliability
- Design for Reliability
- Package Reliability Testing
- Wirebonding and Stud Bumping
- Ceramic and LTCC Packaging
- Substrate Materials and Technology
- Printed Electronics
- Ultra Low-K Packaging
- Uses of Precious Metals in Microelectronics

### Design

- Electrical Modeling, Signal & Power Integrity
- High Performance Interconnects and Boards
- Embedded and Integrated Passives
- Wafer Level Packaging / CSP
- Advanced Materials

### 3D Integration and Packaging Track

- 3D System Integration
- 3D Packaging Approaches
- 3D Processing Technology
- 3D Equipment and Materials Advances
- 3D Simulation and Modeling

### Industry "Focused"

- Consumer, Portable and Wireless
- Biomedical
- Telecom
- Defense and Security
- Computing and Gaming
- Automotive, Industrial, Harsh Environment Electronics Applications
- Solar and Alternative Energy

### Systems & Applications

- Thermal Management
- Power Management
- Cost Reduction, Outsourcing and Supply Chain Management
- Electromagnetic Interference (EMI)
- Sensors and Nano Packaging
- Emerging Technologies
- System Packaging
- Microwave & RF Applications
- Electrostatic Discharge (ESD) Protection
- Photonic / Optoelectronic Packaging
- Packaging for Extreme Environments
- MEMS Packaging
- LED Packaging
- Packaging of Compound Semiconductor Devices

## Exhibit at IMAPS 2010!

IMAPS 2010 is the largest symposium related to the microelectronics packaging industry in the world. IMAPS 2010 will feature a powerful technical program, a state-of-the-art exposition, progressive professional development courses, another informative Global Business Council Marketing Forum and many other events and activities to share the latest developments in microelectronics.

The Annual IMAPS Symposium attracts approximately 2,000 attendees who represent all facets of the microelectronics and electronic packaging industries. These include: engineers, technicians, R&D, purchasing, manufacturing, management, and many more. They represent the automotive, communications, medical, aerospace, computer, defense, homeland security and consumer industries.

**www.imaps2010.org**

iMAPS

## Introducing Sonoscan's P300™ FastLine™ C-SAM® System

ELK GROVE VILLAGE, IL – The introduction at Semicon of Sonoscan's high-throughput FastLine™ C-SAM acoustic microscope has brought praise from potential users of the system, Sonoscan reports.

The most frequently discussed feature of the P300 FastLine is the SafeLoad™ carrier system, which permits one tray of parts to be scanned by the transducer while a second tray is being simultaneously loaded.

When the first tray is done, it is removed and the second tray slides into place so that scanning can begin immediately with the push of a single button.

Simultaneous scanning and loading on this manual system means that operation can be continuous to yield the highest throughput.

"This one feature will make a great deal of difference to our throughput, and is an obvious cost reducer," said Ronald Sato, Director of Backend Operations and Package Engineering at Linear Technology Corporation in Milpitas, CA. "It also helps that this new system has solid Sonoscan support behind it."

The P300 FastLine also has a minimized footprint, a new electronics platform, and Sonolytics™, a highly intuitive user interface.

Someone has already called the P300 "a super-fast process checker" for production line environments - meaning that it can very quickly scan and report on a tray of parts, looking at desired depths and giving the images and data that are needed from each depth for every part.

Is the die face firmly attached to the mold compound? Is the die attach free from flaws? Are there delaminations along the lead fingers? These and other process-related questions get answered - fast.

**Both at Once**

- What has quickly become its best-known macro feature is its "simultaneous" nature (patents pending). While one tray of parts is being scanned in the left portion of the tank, the next tray is being prepared in the isolated right portion of the tank.
- As soon as tray A has finished scanning, it is removed, and the transfer system allows tray B to slide into place. Scanning starts immediately.
- The operator can ship out tray A and prepare tray C while B is scanning. The P300's nearly continuous scanning and the ultra high speed scanner provide a much higher throughput than other systems - typically twice as fast or more.
- The transducer movement attains a peak speed of over one meter per second and their patented scanner mechanism produces the highest average speed on each area scanned.

**Very Thin Slices**

- In the micro world, the P300 uses Sonoscan's PolyGate™ technology. PolyGate lets you set many gates - depths that are simultaneously imaged acoustically - for the same component.
- For a plastic-encapsulated IC you might want to use four (4) to six (6) gates to get the most accurate image for each depth of interest.
- For a sample having a more complex structure, you can set up to 100 gates with the best images obtained within the focus of the ultrasound beam.
- PolyGate has two A-scan displays, one displaying full depth and one displaying gated depth. It also provides both amplitude and polarity data with a single image, as do all Sonoscan C-SAM systems.

**What the Results Look Like**

The results of scanning are displayed on the screen - accepts are green, rejects are red, the component currently being scanned is blue, and components not yet scanned are orange.

This is the P300 - designed to handle large quantities of components in the production environment at about twice as fast as what used to be considered normal, with new capabilities and a footprint of only 76 x 166 cm.

For further information, please contact technical marketing manager Steve Martell at 847-437-6400, Ext. 240.

## STATS ChipPAC Achieves Major Milestone of Over 35 Million eWLB Units Shipped

SINGAPORE, U.S. – STATS ChipPAC Ltd., has announced it has achieved a major industry milestone in the volume ramp of embedded Wafer-Level Ball Grid Array (eWLB) technology with more than 35 million units shipped.

eWLB is an innovative technology that offers a high performance, power efficient semiconductor solution for the wireless and consumer markets. Through a combination of traditional 'front-end' and 'back-end' semiconductor manufacturing techniques with parallel processing of all the chips on the wafer, eWLB delivers a higher integration level and greater number of contact elements at a reduced manufacturing cost as compared to other packaging technology available today.

STATS ChipPAC recently introduced 300mm eWLB wafer manufacturing capabilities which will increase the available capacity with significant cost and productivity advantages. The Company is actively developing next generation eWLB technology to enable larger package sizes, higher Input/Output (I/O) density and 3D Package on Package (PoP) solutions to address a wider application market.

Further information is available at www.statschippac.com.

## Interposers Will Play a Significant Role in Next Generation 3D Packaging Solutions

LYON, FRANCE – Yole Développement is pleased to announce the release of its new report "3D Glass and Silicon Interposers: Technologies, Applications & Markets". Their exhaustive analysis provides:

- Detailed account of all application fields: (logic, logic + memory, 3D RF/analogue integrated passive and MEMS capping interposers...)
- Drivers and expected benefits by application
- Comparison with technology alternatives and likelihood of 3D interposer penetration by application
- Market trends and figures with breakdown by application, substrate type, wafer and panel size
- Analysis of target wafer prices for key applications.
- Cost analysis of several technology and industrial cases
- Supply chain analysis: manufacturers and assemblers for 3D interposers, likely high volume players. Design, test and reliability considerations

Visit www.yole.fr to find out more about the report: detailed description, table of contents, downloadable brochure and report sample.

## Over 150 Fab Projects Lead to Strong 2010 and 2011

SAN JOSE, CA – The World Fab Forecast released at the end of August indicates a 133 percent increase in equipment spending for Front End fabs this year and about 18 percent growth in 2011. Worldwide installed fab capacity (without Discretes) is expected

to grow by 7 percent in 2010 and another 8 percent in 2011. Fab construction spending will increase by 125 percent in 2010 and an additional 22 percent in 2011. The data reveals that for both 2010 and 2011, over 150 fab projects will contribute an estimated $83 billion in spending. The projects tracked include construction projects and equipment spending for high volume, smaller capacity, MEMS, and Discrete, including LED, fabs.

Most of the current investments in construction assure additional capacity for the future. The World Fab Forecast has identified a total of 54 construction projects underway in 2010 and the result is about $4.5 billion in construction spending. About half of these projects are for LED facilities (mostly in China). In 2011, fewer but larger fabs will carry higher construction costs, about $5.5 billion. Spending on equipping fabs will increase by 133 percent in 2010 to an estimated $34 billion. This is a record growth rate, off of the historic low of 2009. Compared to 2008 spending, 2010 total equipment spending will be only 27 percent higher. Compared to 2007, 2010 spending will be 11 percent lower. The World Fab Forecast report predicts spending in 2011 to increase 18 percent, bringing total spending to $39B, finally surpassing 2007 spending levels.

SEMI's World Fab Forecast also provides details of facilities beginning operations in 2010 and 2011. By the end of 2010, about 22 facilities will begin operations. Analyzed by sector, half of these are LED, six are Foundries, three are Analog and two are Logic. No new Memory fabs will begin operation in 2010. In 2011, another 28 facilities are expected to begin operations, including four Memory fabs.

Worldwide installed fab capacity (without Discretes) is expected to grow by 7 percent by the end of 2010 to 14.4 million 200mm equivalent wafers per month (wpm), and by another 8 percent in 2011 to 15.8 million wpm. The Memory sector accounts for the largest share of worldwide installed capacity, about 41 percent in both 2010 and 2011. Foundry capacity follows having grown their market share from 24 percent in 2009 to 26 percent in 2011.

SEMI's World Fab Database reports continue to track individual fab projects very closely. Updates and more information on the reports can be found at www.semi.org/fabs.

SEMI maintains offices in Austin, Bangalore, Beijing, Berlin, Brussels, Grenoble, Hsinchu, Moscow, San Jose, Seoul, Shanghai, Singapore, Tokyo, and Washington, D.C.

For more information, visit www.semi.org.

## SemiProbe Announces Modular Probe System


WINOOSKI, VT – SemiProbe has developed proprietary technologies that are so unique they have been awarded a patent by the United States Patent and Trademark Office. The revolutionary Probe System for Life™ allows the company and users to configure test and inspection systems that meet the unique requirements customers often have creating a quality "custom" system at a price typical of a standard system.

For traditional test systems, Probe System for Life allows the user to configure the station with exactly what they need and can budget for instead of a set configuration prepared by a probe system vendor. For facilities with multiple users, the system also allows the user to reconfigure the station in minutes for another application.

In addition to wafer testing, the system has been configured to test laser bars, singulated die, packaged parts, microfluidic slides, as well as device testing in controlled environments such as vacuum, cryogenic and ultra high temperature (1,000° C). Special applications such as Double Sided Probing, Back Side Probing, Simultaneous Double Sided Probing and Visual Inspection have all been engineered and are available as standard components.

The Probe System for Life System allows users to perpetually upgrade their system as their needs change and budgets grow. Systems can be field upgraded from manual, to semi and fully automatic operation, in addition to changes in wafer size capability, environment, optics and instrument integration. Specific accessories to make probing easier for a specific application can also be added quickly and easily.

Since introducing the Probe System for Life, Semiprobe has sold systems to customers on 5 continents who recognize the value this system brings to their organization. Customers completing a field upgrade to increase wafer size capability or automation often save

# North American Semiconductor Equipment Industry Posts July 2010 Book-To-Bill Ratio of 1.23

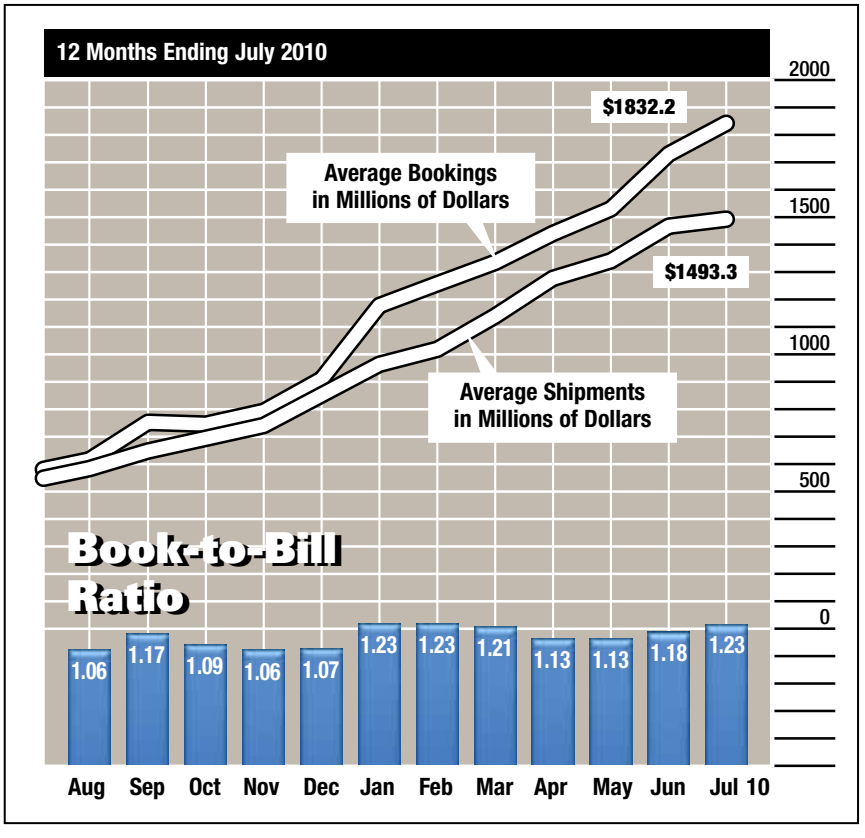
SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted $1.83 billion in orders in July 2010 (three-month average basis) and a book-to-bill ratio of 1.23, according to the July 2010 Book-to-Bill Report published by SEMI. A book-to-bill of 1.23 means that $123 worth of orders was received for every $100 of product billed for the month.

The three-month average of worldwide bookings in July 2010 was $1.83 billion. The bookings figure is up 5.9% from the final June 2010 level of $1.73 billion, and is 220.4% above the $571.8 million in orders posted in July 2009.

The three-month average of worldwide billings in July 2010 was $1.49 billion. The billings figure is up 1.8% from the final June 2010 level of $1.47 billion, and is 177.6% above the July 2009 billings level of $538.0 million.

"The July report shows continued momentum in the market for new semiconductor manufacturing equipment," said Stanley T. Myers, president and CEO of SEMI. "While there are some questions about the semiconductor industry sustaining its strong growth trends in the second half of this year, bookings for new equipment continue to increase and are at the highest levels recorded since January 2001."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



up to 70% over the traditional requirement to start with a new probe system.

More information about SemiProbe may be found at www.semiprobe.com or by calling (802) 860-7000.

## SEMI Announces Management Changes

SAN JOSE, CA – SEMI, the global industry trade organization for micro and nanomanufacturing, has announced a reorganization into three dedicated business units for IC manufacturing, photovoltaic (PV), and Emerging and Adjacent Markets. As part of the organizational changes, SEMI announces that Karen Savala will replace Jonathan Davis as president of SEMI Americas, and Davis will assume the new position, president of the Semiconductor IC Business Unit. Approximately one year ago, the SEMI Board of Directors initiated a process to review and recommend potential changes to the mission, charter, scope, operations, and organization of the global trade organization. As part of this analysis, during the recent Board of Directors meeting the Board approved a reorganization into three business units to achieve better accountability and improved member service in the primary market areas of semiconductor ICs, PV solar, and related markets such as high-brightness LEDs, MEMS/MST, and printed and flexible electronics. The three new business units will be responsible for developing and delivering member services on a global basis through SEMI regional offices based in China, Europe, India, Japan, Korea, North America, Russia, Taiwan and Singapore. Jonathan Davis, formerly president of SEMI Americas, will now serve as president of the Semiconductor IC Business Unit with global profit and loss responsibility for the business unit, including all SEMICON expositions, market research and statistics programs, and SEMI International Standards. Karen Savala, formerly vice president of Member Services, will replace Davis as president of SEMI Americas, and assume responsibility for serving member needs and delivering member services, including public policy advocacy, in the United States and pan-Americas region. Dan Martin will continue to lead the PV Group, now recognized as a dedicated SEMI business unit, assisted by Bettina Weiss who will take on new global responsibilities as executive director, PV Group. Tom Morrow will direct the activities of the Emerging and Adjacent Markets Business Unit, in addition to his duties as vice president of Global Expositions and chief marketing officer. "These changes are intended to more effectively and efficiently address the increasing complexity and diversity of member needs serving the IC, PV, LED, MEMS, and other markets," said Stanley Myers, president and CEO of SEMI. "While all these areas share a common process technology base and need for effective supply chain collaboration, these changes are intended to enable more responsive and specialized products, services and leadership in the multiple industries that SEMI members now serve."

SEMI is the global industry association serving the manufacturing supply chains for the microelectronic, display and photovoltaic industries. SEMI member companies are the engine of the future, enabling smarter, faster and more economical products that improve our lives.

Since 1970, SEMI has been committed to helping members grow more profitably, create new markets and meet common industry challenges. SEMI maintains offices in Austin, Bangalore, Beijing, Brussels, Hsinchu, Moscow, San Jose, Seoul, Shanghai, Singapore, Tokyo, and Washington, D.C.

For more information, visit www.semi.org. ◆

Henkel News
Hysol® LOCTITE Multicore
September 2010
Henkel

# New Wafer Backside Coating Innovation Stacks Up Against Film

***Jonathan Poo***
***Henkel Corporation***

Consumers continue to drive demand for smaller, thinner and more capable electronic devices which, then, require integrated packages that can cope with today's new product footprints. For packaging specialists, that means the processing of thinner wafers and stacking of much thinner die. The catch? All of this has to be achieved at an end unit cost that is palatable and marketable to tech-savvy consumers.

Without question, advances in die attach material technology have been central to the proliferation of highly miniaturized devices. And, while traditional die attach pastes and newer die attach films address many of these challenges for certain applications, the drawbacks to these options have encouraged an innovative response in the form of Wafer Backside Coatings (WBC) for stacked packages.

Widely regarded for its throughput advantages over traditional die attach pastes and lower cost as compared to film, WBC materials have been used successfully on leadframe package applications for the past several years. Conventional paste materials rely on dispensing for deposition, which is a serial process and, therefore, limits throughput. Additionally, the bondline thickness control is highly dependent on die placement force which can result in either insufficient coverage (too little force), bleed out (too much force) or die tilt (non-uniformity). For today's thinner wafers, much of the market has turned to die attach films for their handling capability, thin coverage and coating uniformity. But, like pastes, films also have some shortcomings, not the least of which is their higher cost as compared to paste mediums. The WBC materials developed for leadframe packages can be applied via screen printing, stencil printing or spin coating, which dramatically improves throughput over dispensing processes and provides a lower-cost solution to film.

Even though these materials have been successful with leadframe applications, WBCs haven't historically been perceived as a viable option for stacking of modern, thinned wafers for several reasons: High throughput deposition methods such as screen- and stencil-printing that are extremely viable for wafers thicker than 75 microns are challenged on thinner wafer dimensions.

**2 mil, 200 micron wafer with a 10 micron thickness coating of Ablestik WBC-8901UV.**

In addition, the mesh marks left from screens and the "scooping" effect often induced with squeegee traverse may lead to non-uniformity of the much thinner coatings. The other alternative, spin coating, commonly resulted in material waste of greater than 70%, which countered the material cost savings as compared to films.

Henkel's perseverance in combination with new developments in spray coating technologies, however, have led to a new WBC material, Ablestik WBC-8901UV, that overcomes many of the issues associated with films and traditional pastes for stacked die applications. The new material has been designed to address the demanding requirements of multiple die stack applications for the memory market segment, including packages such as TSOPs, MCPs and FMCs (Flash Memory Cards).

Uniquely formulated as a solution for in-line processing, Ablestik WBC-8901UV offers a robust and cost-effective alternative to current film-based solutions for die stacking techniques, reducing the total cost of ownership as compared to film by as much as 30% to 50%. Process flexibility is also enhanced with Ablestik WBC-8901UV, as packaging specialists can now adjust die attach thickness based on specific manufacturing requirements and can also select their dicing tape of choice. Film die attach materials are generally supplied in pre-determined thicknesses as a bundled product which incorporates the dicing tape.

Applied via a spray coating method following the wafer thinning process, Ablestik WBC-8901UV is precisely deposited across the back of the silicon wafer following which the material is B-staged using a UV irradiation process. After this step, dicing tape is laminated to the wafer, backgrinding tape is removed and the wafer is diced in preparation for die pick-up and placement. Henkel is currently partnering with spray technology and backgrinding equipment manufacturers to deliver an integrated, in-line process solution for this unique WBC advance.

Ablestik WBC-8901UV has successfully proven to deliver a precise wafer coating as thin as 10 microns with a total thickness variation across the wafer of +/-10% and remarkably low material waste of less than 20%. Wafers as thin as 50 microns have been processed using this method.

In keeping with Henkel's forward-looking approach, further developments to Ablestik WBC-8901UV are already underway and the company expects to achieve uniform, 5 micron coating thicknesses or better within the next year.

For more information on Ablestik WBC-8901UV or any of Henkel's WBC portfolio materials, log onto www.henkel.com/electronics or call 949.789.2500. ;◆

# Looking Into the Future at MEPTEC's Semiconductor Packaging Roadmaps Symposium

***Jeffrey C. Demmin***
***Tessera / MEPTEC Advisory Board Member***

MEPTEC's next one-day technical symposium will be **Semiconductor Packaging Roadmaps: Applications Driving Requirements**, to be held November 10 in Santa Clara, California. We have returned to the "roadmaps" topic because it's more important than ever for companies throughout the supply chain to know what each other will be trying to do over the next few years.

I have helped put together many conferences, and I've always thought that an ideal type of presentation is a potential customer telling a roomful of potential suppliers what they need. Everybody wins. Since 2003, the MEPTEC roadmap symposia have done exactly that and more. We have had notable product companies discuss upcoming features needed by their customers. Material and equipment suppliers have presented trends in their emerging product lines. Service providers have reviewed the cost impact and design considerations of new technologies.

One of the best examples of an industry roadmap is the ITRS (International Technology Roadmap for Semiconductors), which is one of the primary coordinating resources for the semiconductor industry. It is a tremendously detailed document that gets updated every year, and its authors also conscientiously point out where they have accelerated or pushed out milestones on the roadmaps based on activities since the previous update. People typically complain about roadmaps being too optimistic, not taking into account unknown factors that can delay technical progress. That can certainly happen, but there have been instances of progress happening faster than projected. For the packaging section of the ITRS, a prominent example of that related to wafer thinning. The capabilities for processing and handling thin wafers advanced faster than projected, so one ITRS update had to fess up to being overly pessimistic. I imagine that at least a few participants in the ITRS took pride in helping to accelerate this important technology that directly impacted our ability to stack semiconductor devices in thinner form factors. Look how thin AND high-functionality consumer electronics are these days, and send a thank-you note to the ITRS and others who collectively moved thin wafer processing forward quickly.

So, for this year's packaging roadmaps symposium, we are looking at the topic from four different directions. Leading off will be the semiconductor makers, since the chips are the heart and key differentiating factor of most systems. We'll get an update from an active ITRS representative, and a few key market segments – microprocessors, memory, and analog products – will be reviewed by technologists from market leaders in those fields. The upcoming technical requirements for these devices are quite different in certain areas, of course. Even pervasive technical challenges like thermal management can vary significantly depending on the device and application.

Next on the agenda will be players in the packaging and test sub-contracting business, both providers and users. The sub-cons are known for providing detailed roadmaps showing all of the packaging options that they can offer, and this session will focus on where they really see progress and opportunity. We will also look at it from the other direction, with some users of packaging sub-cons discussing how they see this business model affecting technical progress.

We will then move to the end of the supply chain with OEMs discussing what they see coming from their vantage point closer to the consumer. This is what really drives everything – what do a billion consumers want to buy next year? Getting a slice of that somewhere up the supply chain is everyone's goal.

Finally, we have a session on roadmaps for applications beyond conventional semiconductors, including photovoltaics, medical electronics, and LEDs. I drew the long straw on the committee and had the good fortune to be coordinating that session. All of us in the semiconductor industry know that our jobs in the future might be in emerging areas like those rather than more mature sectors, so this should be of great interest, even to people not currently involved with those products. It is all connected, though, and I expect that there is much to be learned from looking across conventional boundaries between different types of products. Consider, for example, the thermal challenge in LEDs, reliability requirements in medical devices, and environmental and lifetime issues for PV cells. New products and requirements force us to find new kinds of solutions, and that new thinking is likely to be helpful throughout the electronics industry.

I haven't been to very many conferences recently – my day job doesn't require much of that – but I'm very glad that I'll be at MEPTEC's latest roadmaps conference. We are trying to create the best possible use of your valuable time, and I think that the excellent collection of speakers and topics will do that for us. I hope to see you there! ◆

7TH ANNUAL

# International Wafer-Level Packaging Conference & Tabletop Exhibition

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OCTOBER 11-14, 2010

**October 11-14, 2010** ›› Santa Clara Marriott Hotel, Santa Clara, CA

SMTA Surface Mount Technology Association and ChipScale REVIEW magazine are proud to present the event of the year for buyers, specifiers and producers of chip-scale and wafer-level packaging equipment, materials and services.

For more information on the conference, or exhibit and sponsorship opportunities please contact Melissa Serres at 952-920-7682 or melissa@smta.org

## Connecting the Future of WLP, 3D, MEMS

### IWLPC EVENT SCHEDULE

| | |
|---|---|
| Oct. 11-12 | Professional Tutorials |
| Oct. 13 | Keynote Dinner |
| Oct. 13-14 | Tabletop Exhibits, Panel Discussion, Technical Presentations (three tracks), Poster Sessions |

### CUTTING EDGE TOPICS INCLUDE

- WLCSP
- 3D WLP
- Flip-Chip Bumping
- Through-Silicon Vias
- Stacking Processes
- MOEMS Integration
- SIP/SOP vs. SOC
- MEMS Processes and Materials
- Quality, Reliability, and COO

*"The IWLPC was excellent in 2008, spectacular in 2009 and I expect it to be just as good in 2010. We have already opened dialog with four major semiconductor manufacturers and three equipment manufacturers interested in partnering with us from IWLPC. We are seeing an increase in new customers for our technologies even in the first week after the show."*
– 2009 EXHIBITOR

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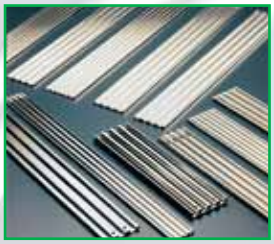
Process Carriers (Boats)

Boat Magazines



I. C. Trays - Multi-Channel

I. C. Tubes and Rails

Miscellaneous Magazines

Substrate Carrier Magazines

TO Tapes & Magazines

Wafer Carriers

***Accept Nothing Less.***

Perfection

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