MEPTEC Report

SPRING 2011

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 15, Number 1

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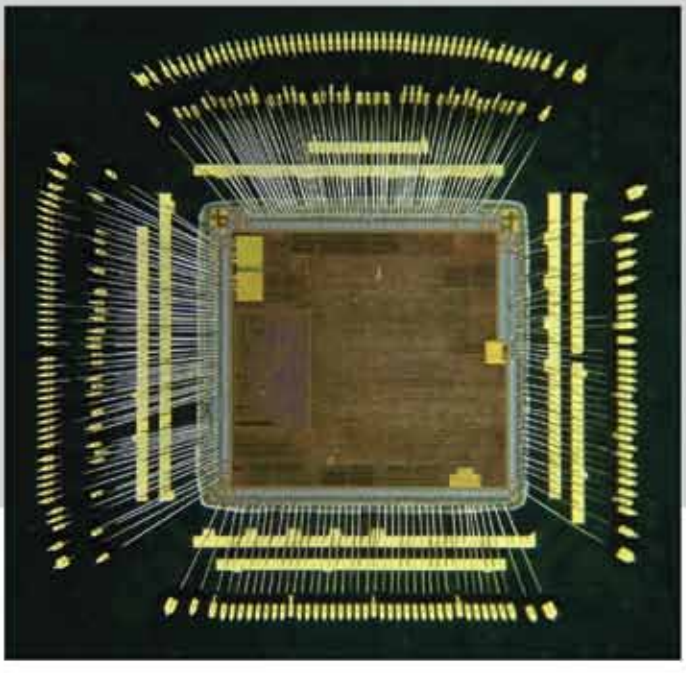
Copper Wire



Copper Wire is a lower cost alternative to the traditional gold wire used in semiconductor packaging. Offering clear advantages, copper wire bonding is gaining popularity for products at 25 microns and below, where the majority of wire bond applications lie. ASE's copper wire bonding initiative is geared towards this group of applications. Bonding pad composition and wafer structure are major factors for copper wire evaluation, and ASE is customizing products based in specific customer needs.

www.aseglobal.com

The History and Future of MEPTEC

Joel Camarda, SemiOps
MEPTEC Advisory Board Member

IN 2008, MEPTEC CELEBRATED ITS 30 year anniversary. I am proud to say that I have personally been involved with MEPTEC since approximately 1982. I guess I missed the very beginning because I was on assignment in the Philippines for National Semiconductor 1978-1981. Originally named MEPPE (MicroElectronic Packaging and Process Engineers), the organization became a close linked network of assembly and packaging engineers and our key suppliers. The "suppliers" included material vendors, equipment vendors, sales reps, machine shops, etc. This engineer-supplier relationship was critical, because we were all inventing new "stuff" together: machines, materials, processes. Most of the semiconductor companies still had moderate sized US assembly operations, although the volume operations had already been moved offshore years earlier. The US operations still served as the development platforms for materials, machines, and processes, although this was also starting to change in the early '80s. There was also a focused intimacy of this engineer-supplier relationship in MEPPE – specifically for semiconductor assembly and packaging – that was not serviced by other professional organizations, such as SEMI, IPC, JEDEC, IEEE, and NEPCON/APEX.

The business model of MEPTEC, as we now call it (MicroElectronic Packaging and Test Engineering Council) has not altered. It is still a close linked network of engineers and suppliers. The semiconductor business model has altered considerably, however, in that a lot of development is conducted offshore at the volume assembly plant. From my own experience, I can tell you that developments have to be verified in volume, in the actual manufacturing environment, so you might as well start there. Further, the "high volume assembly plant" and the source of new development is more likely to be a contract SATS (semiconductor assembly test supplier) firm, or "sub-con" as we used to call them, vs. an IDM (integrated device manufacturer) plant. The material and capital equipment suppliers are global, not just US based. There is nothing to relent here. This is the reality of the business, and it has made our business stronger and more cost effective, and it has made semiconductor products more pervasive in our culture. So far, I am not telling you anything you do not already know. Still in this new reality, MEPTEC has survived and thrived. The SATS firms have joined the MEPTEC suppliers, as well as suppliers of design software, reliability testing products and services, ATE and test support products, etc. The engineers may be hands-on, or people managers or project managers. Many in engineering have "evolved" into executive management or the supply side (the "dark side"?... just kidding). We are a resilient group and we are in a resilient business.

When MEPPE was founded, there were probably dozens of semiconductor companies. Today, there are hundreds of companies, each with at least one packaging person, and a few test engineers...

On the other hand, even though USA based IDM packaging departments may have shrunk, there are many more semiconductor companies in the Bay Area, thanks to the fabless business model. When MEPPE was founded, there were probably dozens of semiconductor companies. Today, there are hundreds of companies, each with at least one packaging person, and a few product/test engineers. So the relevance of MEPTEC still exists and may even be greater, for the close interaction and mutual education of engineers and suppliers.

Allow me to recap some of the MEPPE/MEPTEC milestones.

The organization was founded by W.D. Smith in 1978. I believe W.D. was an early employee at Intel, before he moved on into his own business enterprises. Many years later, around 2000, I ran into him again when I was President of K&S Flip Chip Technology, in Phoenix. My staff evaluated an alternate bump forming process that his firm was developing. In 1985, MEPPE was acquired by Duane Wadsworth and Shirley Heim. Duane was a great sales rep and I did a lot of business with him at a few companies. He always had the right products. In 1991, MEPPE was acquired by Harry Rozakis and Dean Strausl. Harry and Dean were industry guys, and still are. Dean had assignments in various parts of the globe. He has a hilarious story about his interview process in Guatemala, at a time when it was politically very unstable. He declined that job. Harry later became VP/GM of ChipPAC, and is currently a CEO of a photovoltaics firm in Canada. Harry and Dean had big plans for MEPPE, and they really elevated the organization beyond the monthly luncheons. They initiated multi-day technical symposiums and attracted speakers beyond the MEPPE membership and the Bay Area. In 1996. MEPPE became MEPTEC, a partnership of Rozakis and Bette Cooper. Bette had joined the organization a few years earlier and was running most of the logistics, as she still does today. Changing the name to MEPTEC reflected our intent in expanding beyond assembly-packaging and getting the local test industry involved and included. Bette became President of MEPTEC in 1999 in a partnership with Gary Brown, who is a graphic designer and media wiz. Bette remains almost totally behind the scenes of MEPTEC, but is really the glue (and sometimes the whip!), to keep things together and moving along.

Bette initiated the Advisory Board in the mid '90s, which I am proud to be a member for several years. The job of the AB is essentially to provide the technical content of MEPTEC. The AB membership has historically been impressive, and this compliment is directed purely at my colleagues. The quality and relevance of our luncheon presentations and full day symposiums is the AB's raison d'etre.

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MEPTEC Report

SPRING 2011

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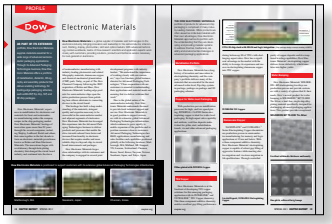
Volume 15, Number 1

ON THE COVER

14 MEMS - DRIVING INNOVATION – The Ninth Annual MEPTEC MEMS Symposium returns to San Jose on May 19th. This year's event will focus on new directions for the applications of MEMS technology and the challenges encountered to move forward, and the existing semiconductor technologies that can help enable them.

16 ANALYSIS – In the long term, Fan-out WLP and Embedded Die Technology could seriously compete in the fast growing 3D packaging market space as they will both enable the construction of ever more complex, larger SIP modules.

BY JÉRÔME BARON & JEAN-MARC YANNOU
YOLE DÉVELOPPEMENT

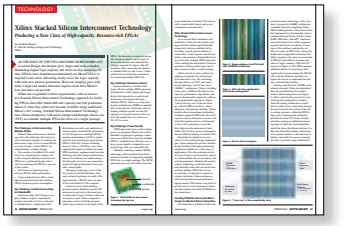


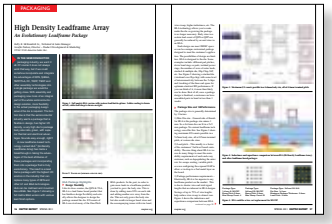
18 PROFILE – Through its Advanced Packaging Technologies business, Dow Electronic Materials offers a portfolio of metallization, dielectric, lithography and assembly products that deliver enabling technology for leading-edge packaging systems.

DOW ELECTRONIC MATERIALS
MEMBER COMPANY PROFILE

22 TECHNOLOGY – As the role of the FPGA becomes more dominant in system design, the designs grow larger and more complex, demanding higher logic capacity and more on-chip resources. Xilinx has responded to these requirements with an innovative Stacked Silicon Interconnect Technology.

BY SURESH RAMALINGAM
XILINX





26 PACKAGING – In the packaging industry we want it all. Of course it does not always work that way, but if we could somehow incorporate and integrate the advantages of QFN, fpBGA, TAPP/TLA, FC, TQFP, TSOP and other assembly technologies into a single package we would be getting close.

BY KELLY R. MCKENDRICK SR & SERAFIN PEDRON
UTAC

DEPARTMENTS

MEPTEC

THE NEXT GENERATION

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MEPTEC
THE NEXT GENERATION

YOU'VE PROBABLY noticed by now that MEPTEC has taken on a new look and feel with a new logo, publication redesign and a new look to our website that is now "*MEPTEC – The Next Generation*". We've had a great run over the last 30+ years, but we began to notice the "graying" of MEPTEC; many of our long time supporters and members are creeping towards (or have taken the full leap) into retirement or moving on to the next phase of their careers and life. Joel Camarda addresses these issues in his Board Letter (page 3) and we've decided to tackle them head on.

One of our first tasks moving forward was to take a look at our existing Advisory Board. All of our Advisory Board members agreed it is time to restructure and bring in "new blood", both on the Board and in the membership by starting to reach out to our younger professionals who will be the future of our industry. These moves are just the beginning of an effort to drive MEPTEC into the "Next Generation".

Restructured Advisory Board

In the front of each issue of this publication is the listing of the MEPTEC Advisory Board members. You may have noticed over the years that for most of them their companies have changed (sometimes twice, three times or more). Some of them have moved from the day-to-day corporate life to "semi-retirement" and started their own firm or consult part-time; some have fully retired. Many of the names on the list will no doubt be familiar to you since they have been in the industry for many years. As part of the "Next Generation" of MEPTEC we are restructuring the board, forming a core Advisory Board, and adding a couple new categories: *Special Advisors* (someone who is an expert in a segment or area of the semiconductor or other industry that is relevant to the MEPTEC audience) and *Honorary Advisors* (someone who has been a long-time supporter of MEPTEC and still helps with event program development, assists with other activities, etc.) As the years passed many of our members moved away from the main categories of our membership, which include:

- Subcontract assemblers
- Merchant semiconductor manufacturers
- Fabless/design only semiconductor manufacturers
- Material suppliers
- Equipment manufacturers
- OEMs
- Semiconductor support services

We think a rejuvenated board will go a long way to a re-energized MEPTEC. In future issues we'll introduce you to all of our board members. We would like to thank all of our past, current and new Advisory Board members who have offered their great support over the years. ◆

Wafer Shipments Reach Record Levels in 2010

SAN JOSE, CA – Worldwide silicon wafer area shipments increased by 40 percent in 2010 when compared to 2009 area shipments, according to the SEMI Silicon Manufacturers Group (SMG) in its year-end analysis of the silicon wafer industry. Revenues also improved by 45 percent in 2010 compared to 2009. Silicon wafer area shipments in 2010 totaled 9,370 million square inches (MSI), up from the 6,707 million square inches shipped during 2009. Revenues reached $9.7 billion up from $6.7 billion posted in 2009. "2010 was clearly a very strong recovery year for the semiconductor industry, resulting in a 40 percent area growth in wafer demand." said Dr. Volker Braetsch, chairman of SEMI SMG and corporate vice president of Siltronic AG. "Given current market forecasts, we are expecting solid demand for silicon wafers in 2011, although at a much more modest post-recovery rate." For more information, visit www.semi.org. ◆

Annual Silicon* Industry Trends

Worldwide Silicon Data	2005	2006	2007	2008	2009	2010
Area Shipments (MSI)	6,645	7,996	8,661	8,137	6,707	9,370
Revenues ($B)	7.9	10.0	12.1	11.4	6.7	9.7

*Shipments are for semiconductor applications only and do not include solar applications.

MEMBER NEWS

M-QFN OPEN CAVITY PACKAGE

Mirror Semiconductor started shipping new M-QFN series open cavity (air cavity) QFN packages. M-QFN is constructed with a pre-molded cavity wall. The cavity can be filled with glob top, or attach a flat lid to seal the cavity. Copper leadframe is pre-plated Ni-Pd-Au. Applications include prototyping, and product levels for fabless IC makers, MEMS, RF/Microwave and sensors. Preferred assembly partner Promex offers full range of assembly services. *www.MirrorSemi.com*

HENKEL FOCUS

Henkel has focused much of their development efforts on products that deliver sustainable alternatives to current offerings. These include halogen-free formulations, RoHS-compliant green mold compounds and materials that offer improved process efficiency. For the semiconductor packaging market, significant developments in die attach films, wafer backside coating (WBC) materials for stacked packages and novel NCPs have been achieved by Henkel. *www.henkel.com/electronics*

16 YEARS STRONG

N-Able Group International is beginning its 16th year with a continued focus on recruiting and consulting services for the semiconductor industry. After what seems to be an eternity, things are heating up. If you're looking for a full time position or project consulting work, please ▸▸

contact N-Able. If you've never sent them a resume or have updated information, please send a current resume and let them know your interests and preferences. Email ron.jones@n-ablegroup.com or call 408-872-1301.
www.n-ablegroup.com

MARKET REPORT

MEMS Investor Journal has published a comprehensive market research report on wafer level packaging (WLP) technologies and applications. The report provides detailed information on the five distinct WLP process platforms: wafer-level chip scale packaging (WLCSP), also known as fan-in wafer level packaging (FI-WLP); fan-out wafer level packaging (FO-WLP); embedded wafer level packaging (Embedded WLP); three-dimensional wafer level packaging (3D WLP); and MEMS wafer level packaging (MEMS WLP). The report also provides a detailed list of WLP applications including current trends and emerging developments. For further information or to request a free report sample, please contact Steve Awtrey at sawtrey@memsinvestorjournal.com.
www.memsinvestorjournal.com

PAST LUNCHEON PRESENTATIONS NOW AVAILABLE FOR MEPTEC MEMBERS

Presentations from past MEPTEC luncheons are now available for download at the MEPTEC website for Members Only. Contact Bette Cooper for access.
bcooper@meptec.org ◆

STATS ChipPAC Launches Enhanced Flip Chip Packaging with fcCuBE™ Technology

Innovative fcCuBE™ delivers a high density, low cost solution with superior reliability for advanced silicon nodes

STATS CHIPPAC LTD. HAS LAUNCHED the innovative fcCuBE™ technology, an advanced flip chip packaging technology that features copper (Cu) column bumps, Bond-on-Lead (BOL) interconnection and Enhanced assembly processes. fcCuBE technology delivers high input/output (I/O) density, high performance and superior reliability in advanced silicon nodes. The fcCuBE technology offers enhanced flip chip packaging with a 20-40% lower cost over standard flip chip packaging, a compelling value with price points comparable to mainstream semiconductor packaging solutions.

As semiconductor devices are scaled to advanced wafer technology nodes of 45/40nm and below, innovations in package structure, design and assembly process are key to achieving high performance, cost-effective product solutions. fcCuBE technology addresses a complex set of packaging challenges and delivers important benefits including:

- Ultra high I/O escape routing density
- Scalability to very fine bump pitches of 80 micron and below with finer effective pitches
- Significant reduction of stress on Ultra low-k (ELK/ULK) structures that has been proven down to 45/40 nanometer (nm) and 28nm silicon structures
- Broad fab node compatibility
- Higher resistance to electromigration
- Lead-free alternative to conventional lead-free bumps and solder-based bumps
- A 20-40% lower cost over standard flip chip packages for most designs

fcCuBE technology is based on STATS ChipPAC's patented BOL interconnect structure which has been combined with Cu column bump to deliver an ultra high I/O escape routing density with a finer bump pitch compared to standard solder bumps. The advancement enables more relaxed substrate design rules than standard flip chip packaging and provides scalability to very fine bump pitches of 80 micron and below.

For more information about STATS ChipPAC innovative fcCuBE™ technology visit www.statschippac.com. ◆

*i*MEMS Gyros Deliver Higher Performance Under Harsh Vibration

ANALOG DEVICES, INC. is introducing three new high-performance, low-power iMEMS® gyroscopes with analog output specifically for angular rate (rotational) sensing in harsh environments. The ADXRS642, ADXRS646, and ADXRS649 incorporate ADI's advanced, differential quad-sensor technology, which rejects the influence of linear acceleration and vibration to enable these new MEMS gyros to offer exceptionally accurate and reliable rate sensing even where severe shock and vibration are present.

"These new MEMS gyros have linear acceleration sensitivities as low as 0.015°/sec/g as compared to 0.1°/sec/g offered by the leading alternative MEMS gyros," said Wayne Meyer, MEMS/Sensors Technology Group, Analog Devices, Inc. "The ADXRS64x series also offers much faster start-up times, as fast as 3 milliseconds, and 10 times lower power consumption at 3.5 mA compared to other MEMS gyros that consume as much as 60 mA."

For applications where ultra-wide measurement ranges are needed, the ADXRS649 also offers the highest rate of rotation sensing available with ±20,000°/sec and fast 3 millisecond (ms) start-up time for quick power cycling. This measurement range is extendable to ±50,000°/sec with the addition of an external resistor. The ADXRS646 gyro offers a measurement range of ±250°/s, 1 kHz bandwidth, and 8°/hr drift with low broadband noise. Coupled with its exceptionally low-g sensitivity of 0.015°/s/g and vibration rectification of 0.0001°/s/g2, the ADXRS646 is ideally suited for high-performance heading measurement and platform stabilization. For more information visit www.analog.com/gyro. ◆

LETTER continued from page 3

So now that I have bored you with the history, let me get to the point of this essay. MEPTEC is taking some clear actions for the continued success and growth of the organization. Like a semiconductor company, reinvention and continuous improvement are required for survival as well as success. We need you, our stalwart members, supporters, sponsors, and event attendees, to assist in this process. MEPTEC serves for your benefit. We are making some adjustments to the Advisory Board for better balance and reflection of the membership: fabless semi companies, IDMs, material suppliers, equipment suppliers, SATS, sales professionals and independent industry experts. This will allow us to continue putting together quality programs. The AB members decide on the programs' contents and recruit the excellent speaker and presenters.

We also look to you to help our recruitment efforts, particularly for the engineers, since they are spread out among so many more companies. Membership is nice, but not critical. Attendance and participation is the key. In my executive management positions, I encouraged my staff to attend the lunches and symposiums, for their benefit, as my participation has benefited my career along the years. Those of you in senior management now should do the same. The costs are very reasonable, even in hard times. Especially in hard times, one does not discourage self-improvement, which usually translates into better performance for the company. For the suppliers and vendors, continue to take your customers to MEPTEC lunches. In fact, that is how I started. If I recall, Don Eads, a machine shop vendor, took me to my first MEPPE lunch. He is happily retired in Maui now. As a number of stalwarts approach retirement in the not too distant future, it is important that we invigorate MEPTEC with the next generations of professionals so those professionals can also reap the same benefits. For the supply side you already know that MEPTEC is a successful venue for you to connect to customers in a relevant-to-the-technology setting.

There may be some cultural differences these days vs. the early industry days. At NS, after a long trying day, several engineers would typically "unwind" at a local pub. This post-work camaraderie doesn't seem to exist to the same extent now, and, of course, we are also more socially responsible when it comes time to drive home. Our communication media are more electronic now, vs. face to face. Email, tweets, Facebook. Personally, I have been attending a few "webinars" lately. The webinar works OK, but is by no means a substitute for live participation, Q&A, and attendee interaction. We on the AB are certainly open to suggestions. For those of you in sales, I believe you still depend on the human interaction to find and service your customers. Maybe we can hold a focus group with a few of you. Please feel free to pull me, or any AB member, aside at any MEPTEC event or send me an email. OK, that's electronic, but that is reality. ◆

JOEL CAMARDA is a veteran in the international packaging community with 30 years of experience in the USA and Asia. He began his career in packaging at National Semiconductor and was responsible for packaging and assembly at Cypress Semiconductor. He can be reached at jcamarda@semiops.com.

TEST INTERFACES

By Nick Langston

Still a Bottleneck

AS THE BIT RATES OF MOST OF today's network centric devices have moved to 15-28GB/s and communication interface standards have moved quickly from several hundred Mb/s to 6-8Gb/s, Signal Integrity of the test interface has become a dominant issue for characterization and full production test of these devices. Big ASICs and FPGA's can have dozens of 10Gb/s Serdes differential pairs plus another couple of 25Gb/s Serdes differential pairs and pull power on the order of 40A or more. So, in addition to Signal Integrity issues, the performance of the Power Distribution Network cannot be overlooked. This remarkable advancement in I/O speeds and technology is driven by the requirements for networks to process and transfer more information and faster.

This development probably doesn't have a huge impact on the core architecture of the current generation of ATE, but it does have an impact on testing techniques of the DUT I/O. ATE vendors have developed new application specific modules to work in concert with the BIST/DFT capability that is built into most Serdes devices. Given that multi Gb/s come in matching I/O pairs a common BIST/DFT capability for loopback testing has been incorporated into many devices. This approach eliminates the need for the full ATE test support, including test-program protocol handling, and opens the way for various loopback models using loadboard support.

A comprehensive way to test the I/O is to use waveform analysis or eye diagram masks to quickly measure jitter, noise and calculate BER. Jitter is always the comparison of a data edge to a reference clock and the extent that they don't overlay exactly is Jitter. Total Jitter has 2 primary contributors, Deterministic jitter and Random jitter. Deterministic jitter may be due to PDN variation, data pattern dependent or interconnect dependent and is contributed mainly by the Test Interface Hardware. The Random Jitter is produced by the PE cards, reference clocks, the device itself as well as thermal causes. BER is the only way to relate device performance to measure jitter and depending on the application the target BER is 1x1012 or one failed bit per trillion bits. Unfortunately, the I/O speeds are increasing faster than the ability of the ATE vendor to include the tools for test. A Digital Sampling Oscilloscope or Telecom standard stressed eye signal generator are standard tools for characterizing the Tx and Rx in the lab, but it is a challenge for an ATE vendor to quickly and inexpensively implement their functions in the Test Head.

A lot of effort is being made to integrate 3rd party tools, DSO's SSG's, onto the load boards to provide solutions to at least 15Gb/s. For higher bit rates the DCA's or BERTs from Agilent, Tek or LeCroy must be used. These edge rates and power demands make it imperative for the test engineer to view the test interface not as a combination of unrelated components but as an integrated system. Deterministic jitter of 5-6ps can squint an eye for a 5Gbit transmitter. The Test Interface Hardware design is critical for optimum performance. The Loadboard is the largest contributor to the unintentional impairment of loop backs and the design has to minimize losses due to dielectrics and impedance discontinuities. Perhaps it is time for Load board vendors to implement passive equalization techniques to reduce ISI and jitter on the data signal transmitted through the test socket and the board. Test interconnects like probes and especially pogo pins are sources of jitter. I think it is best to use Time Domain simulation for the board and interconnects of the Test Hardware to enable you to get an Eye Diagram to review before you fab the board.

As the measurement and characterization of jitter in high speed devices becomes more challenging, Semiconductor manufacturers have been coming to terms with developing test strategies for stacked die, referred to as 3-D packages. For a test engineer the problem is; how do you get at the different devices so that they can be tested. Testing of each device before it becomes part of the 3-D stack is of course part of the solution. But the assembly process will invariably introduce additional defects that will need to be found. Boundary Scan pattern testing is the most popular for functional test and verification. The IEEE has generated a standard 1149.7 which is specific and squarely aimed at the testing of stacked die. The stacking technology is still evolving so the test solutions will continue to be updated and standardized. ◆

NICK LANGSTON is president of Liberty Research Company. Email Nick at nick@liberty-research.com.

MEMS MAKERS

By Dr. Alissa Fitzgerald

Machinists Who Work in Silicon

THE VERSATILE AND AMAZING silicon devices that are microelectromechanical systems (MEMS), such as microphones and inertial, light and pressure sensors, have already found their way into a multitude of consumer electronics devices and automobiles, among other products. As exemplified by the proliferation of iPhone apps that utilize motion sensing, there seems to be no end to what one can do with MEMS devices, from the sublime (lifesaving automotive stability control systems) to the ridiculous (the iBeer app).

MEMS technology was pioneered nearly 40 years ago by mechanical engineers who wanted to make tiny 3-D structures out of silicon—not transistors. They used the tools at hand, borrowed from integrated circuit (IC) manufacturers, and shaped silicon with light, chemicals and plasmas in the cleanroom facilities known as "fabs." Once regarded as exotic, crazy stuff, MEMS has become a mainstream technology with annual global sales of $8 billion.

Now that bigger markets are at stake, particularly in consumer electronics, attention is focused on how to make MEMS cheaper, faster and better. The drumbeat for standardization has started. The loudest call is coming from those who believe that MEMS, being made from silicon wafers, ought to conform to the successful IC industry model: process standardization. In the IC industry, wafers are manufactured using set process flows with rigid design rules controlled by the foundries.

There is a good reason for the IC system. Standardized, highly controlled processes allow foundries to run a few processes very well and provide their customers with low-cost, high-yielding chips through economies of scale.

Those with an IC perspective often lament that MEMS manufacturing is stuck in the trap of "one product, one process" and is therefore doomed to high production costs until it can conform to the IC model. This commonly held belief, however, is borne from the flawed assumption that MEMS devices are just like ICs. They are not.

MEMS devices are mechanical: They are freestanding bridges, diaphragms, hinges and trusses, shrunk down to microscopic size. Like any mechanical structure, their features are intentionally selected to serve a particular mechanical function, whether deflecting under certain loads or resonating at a specified frequency. The height, or Z-axis, of these features is created by the process steps of etching (sometimes deeply into the silicon wafer) or by material deposition. Different MEMS designs must use different process flows because it is not possible to create two different Z-axis features with the same process.

ICs, on the other hand, are planar devices. A cross-sectional slice of an IC chip reveals a Z-axis structure that forms transistors, the common building block of all integrated circuitry. An IC designer creates new designs by linking transistors on the wafer's X-Y plane into different circuits. Many IC designs can be manufactured using the same process, as long as they share the same basic transistor architecture.

The planar nature of ICs facilitates process standardization. The IC manufacturing model consists of the foundries that own the Z-axis design—and therefore the process flow—and the chip companies that own the X-Y axes design, such as the circuit. Only with a common Z-axis building block, similar to the transistor, could MEMS ever conform to a standardized process flow.

So what now?

Just because MEMS cannot conform to the IC model does not mean we should abandon the quest for standardization. MEMS devices do need to be made cheaper and faster in order to enter additional markets. But we need to look elsewhere for a transformative manufacturing business model.

As a mechanical engineer who once shepherded parts through a machine shop and now does custom MEMS development for dozens of different applications, I believe the MEMS industry—despite its use of silicon wafers—has far more in common with producers of custom-machined parts. A machine shop, like a MEMS fab, uses a suite of machines, such as mills, lathes, saws and benders, to perform specific functions. The same shop might make products as diverse as door hinges or engine blocks. No two mechanical products will move through the shop the same way because their widely varying features—the very features that make them door hinges or engine blocks—demand different manufacturing steps. Sound familiar?

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MEMS MAKERS continued from page 9

MEMS manufacturing is micromachining. We use plasma and silicon like a shop uses drill bits and workpiece materials. To reduce manufacturing costs and product development time, we should be looking to machine shops for ideas and emulating their manufacturing models.

In a shop, one finds standardization not in the process flow, but in the tools and methods that accompany each machine tool, such as drill bits, saw blades, cutting speeds, sheet metal gages and fastener sizes. Mechanical engineers have learned to work within these machine-specific standards when designing products. They specify 3.0mm holes, for example, instead of 3.023mm holes because the former can be drilled with a standard tool, which makes the part cheaper to produce.

To improve our manufacturing efficiency and lower costs, the MEMS industry must start thinking about how to standardize at the tool and/or recipe level, similar to how a standardized set of drill bits accompanies the drill press. Standardization of MEMS silicon wafer specifications such as for layer thicknesses of silicon-on-insulator devices, silicon-etch recipes to achieve specific depths or aspect ratios, and commonly used film deposition thicknesses are all within easy reach.

The potential benefits are many:

- standard material specs would enable material suppliers to plan production and inventory more effectively;
- standardized tool recipes would allow foundries to avoid costly process development and operate more efficiently; and
- MEMS designers could select from known process modules to ensure design success and repeatability.

Customization would still be available—but, like a machine shop, the supplied product would be priced accordingly. ◆

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MEDICAL ELECTRONICS

By Guna Selvaduray

Industry Collaborations

IT IS WHEN INDIVIDUALS AND organizations work together that great things can be accomplished. MEPTEC is one such organization that has always collaborated with other organizations in order to deliver the best possible information and knowledge to its members and meeting/conference participants. And, they continue to do so.

Living in Silicon Valley, it is easy to fall into the misconception that the microelectronics industry serves only the consumer industries such as cell phones and lap tops. There is a very large, though not very visible, medical device industry in Silicon Valley. Many medical devices are completely dependent on the performance of the electronics to deliver appropriate care for their users. Open up any blood glucose monitor or, for that matter a simple thermometer, and the insides will contain a significant number of microelectronic components. These are the visible ones. There is also a growth of implantable devices that depend on microelectronics for their functioning. Pace makers were probably the first such medical devices where the contents of a pace maker are primarily microelectronics and a battery pack.

The medical device industry has also benefited from, and taken advantage of, the constant miniaturization of microelectronics – driven by the demand for "smaller, faster, cheaper". This trend has enabled the development of devices that were not conceivable 10 to 15 years ago. We can now swallow a tiny camera that is slightly larger than an aspirin tablet instead of undergoing the uncomfortable procedure of an endoscopy.

While the actual assembly and interconnection technologies for medical devices do not vary significantly from consumer electronics, all medical devices must be approved by the Food and Drug Administration, the mission of which is to ensure the "safety and efficacy" of all medical devices. This calls for a level of record keeping that the microelectronics industry has probably not faced thus far. In addition, clean rooms need be not just particle free, but also germ and bacteria free. The term "clean room" takes on a slightly different meaning.

MEPTEC's Symposium on Medical Electronics is the only forum in the world, as far as I know, that is devoted solely to this important issue. The Biomedical Engineering Society San Jose State University is very pleased to join MEPTEC as a sponsor of this important symposium series. The next one will be the sixth annual to be held September 27-28 at Arizona State University. We hope you can join us there. ◆

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INDUSTRY INSIGHTS

By Ron Jones

TSMC Moves on 450mm

ON FEBRUARY 11, TSMC MADE an announcement that will have far reaching consequences to the semiconductor industry for the next decade and beyond. They officially announced their plan to bring 450mm production capacity on at the 22 nm node in 2015. In December, Intel made an announcement that their new Hillsboro fab would be 450mm compatible, but could run 300mm, a bit of a hedge. Now there is nothing sacred about the TSMC announcement and they could certainly extend 300mm if necessary. This is, however, a company stepping out and boldly declaring that they are moving on with 450mm. This will be an evolving saga as there many things to be worked out with equipment suppliers and myriad hurdles to clear on process technology.

I think that TSMC and Intel will be the leaders in the move to 450mm. The both have deep pockets and excellent technology portfolios. Other than themselves, they don't have to depend on anybody but the tool vendors for success. As they are both leaders in their respective spaces, this is an opportunity to pull further away from their competitors. If things don't go as planned, they won't be severely damaged if 450mm is delayed.

I think that Samsung will be a fast follower in order to maintain their leadership in memories and widen the gap with their competitors. They can focus their 450mm effort narrowly on memories, which simplifies the task a bit. Once they get memories under their belt, they could move on to the foundry segment. Samsung is also much more than just a semiconductor company.

The most interesting one to watch, in my opinion, will be Global Foundries. They are neither a technology leader, nor do they have deep pockets, themselves. They must depend almost entirely on Abu Dhabi's government funded Advanced Technology Investment Co., at least until they go public. This puts their future out of their direct control. The ATIC website says "The company has a clear and single purpose: to deliver superior financial returns to our shareholder by responsibly and sustainably investing in, and building, leading technology companies around the world". So what is the impact on continued funding if Global Foundries is not able to deliver superior financial returns?

The investments for all stakeholders in 450mm will be tremendous. For 450 to be a success overall, it must be a success for the tool vendors and for the tool purchasers. I think the tooling vendors will be very careful and probably do their conservative estimates on ROI based on purchases by Intel, TSMC and maybe Samsung, at least early on. ◆

RON JONES is CEO and Founder of N-Able Group International. Visit www.n-ablegroup.com or email Ron at ron.jones@n-ablegroup.com for more information.

Henkel News
Hysol® LOCTITE® Multicore®
Spring 2011
Henkel

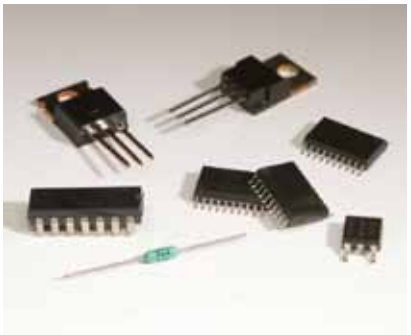
Improved Thermal Performance for Power Devices

Paul Gleeson
Henkel Corporation

MUCH HAS BEEN WRITTEN about the challenges associated with production of today's smaller, high functionality semiconductor devices. Indeed, manufacturing these highly miniaturized devices while maintaining superior performance has been a major paradigm shift for the packaging industry. While there are many design and production changes that must be implemented to ensure robust performance, one of the greatest challenges facing semiconductor specialists today is thermal management, particularly as it relates to semiconductor power devices. Greater functionality in a smaller footprint means more heat generation and, consequently, the need for enhanced thermal control strategies.

Today, high-lead soft solders are the most widely used die attach materials for power semiconductor packages. For high power passive and discrete components, such as TO 220s and the like, solder's ability to manage the thermal load is undisputed. But with the 2014 deadline for RoHS compliance around the corner, packaging specialists must have a plan in place for alternatives to solder. To address this reality, Henkel has developed a new conductive adhesive that provides a viable alternative to solder in an organic material. Historically, organic adhesives have not been able to compete with solder in terms of electrical or thermal conductivity. Based on decades of expertise and growing materials development sophistication, however, Henkel's materials scientists have formulated organic materials that can offer electrical and thermal performance that, for some applications, rivals solder.

Specifically, Henkel has commercialized a brand new organic conductive adhesive for small die (4 x 4 mm and below) power devices. The material, Ablestik ABP-8000, has been designed for high reliability, high power leadframe applications. With good adhesion capability, excellent reliability, outstanding dispense performance and strong electrical and thermal conductivity, Ablestik ABP-8000 provides today's power package specialist with a robust adhesive for modern small die power applications. Using formulation techniques honed in developing the market-leading Hysol



QMI529HT and Hysol QMI529HT-LV materials, Ablestik ABP-8000 extends the thermal resistance capability even further, moving from 0.8 K/W to 0.6 K/W and rivaling that of solder, which sits at approximately 0.4 K/W.

Though certainly not a one-size-fits all solution for all small die power packages, Ablestik ABP-8000 has shown particularly good performance on leadframe devices with PPF or AgCu finishes. The material also has excellent dispense capability and a long open time, offering significant process flexibility and ease-of-use.

One of the most important notes regarding Ablestik ABP-8000 – or any of Henkel's advanced materials, for that matter – is that its performance has been proven in-package. With data on how the material responds when it is bonded between different surfaces, wire bonded and overmolded, Henkel can provide critical information on a material's true capability. All of these factors impact a material's performance – particularly when speaking about thermal competence. While other suppliers offer data on a material's bulk thermal conductivity, these values are, quite frankly, fairly meaningless when you put the material into a package. The difference in thermal performance in-package versus a bulk conductivity measurement is really like comparing apples and oranges. And, let's face it; what's most important is how the product will perform within the package it was intended to enable. When a material is bonded to two different surfaces, there is interfacial thermal resistance, which is the biggest contributor to in-package thermal performance efficiency. With only a bulk thermal conductivity measure to go on, performance is just a guess. When Henkel tests and confirms a material's in-package thermal performance, customers then have a high level of confidence that the material will perform as intended – because it's already been proven to do so. And that's just what Ablestik ABP-8000 provides – a proven, in-package material with a thermal resistance of 0.6 K/W.

For power semiconductor device manufacturers looking for an organic solution to solder, Ablestik ABP-8000 may be the perfect solution.

For more information on this material or any of Henkel's advanced die attach products, call the company headquarters at 714-368-8000 or log onto www.henkel.com/electronics. ◆

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9th Annual MEMS Symposium

Thursday, May 19, 2011
Wyndham Hotel San Jose, San Jose, California

FOR THE LAST 70 YEARS American companies have been unrivaled innovators. We take great pride in our ability to create the means to change our nation and the world for the better. This makes recent revelations on the state of innovation in the US quite concerning. According to a Boston Consulting Group report the US now ranks 8th in the world for innovation. There is hope – our culture of embracing risk, ability to attract talent from around the world, top universities, and existing capabilities give us a leg up. Companies are increasingly realizing that a focus on innovation is a critical strategic imperative.

MEMS innovations are having an ever-increasing impact on American industry. MEMS and other groundbreaking technologies is the path for continued innovation across all industrial sectors and a means for helping companies maintain the technology leadership needed to propel them into the next decade. Technology intensive sectors of our economy are benefiting from microfabricated devices. Some of those sectors include biotechnology, communications, energy saving technologies, information technology, advanced materials, transportation, alternative energy and more. Even those sectors that do not currently use MEMS are beginning to realize the promise of MEMS concepts. In addition many of these technologies are going to need to rely on microfabrication, advanced packaging (both MEMS and IC), and other semiconductor professionals to help forward them.

This symposium will focus on new directions for the applications of MEMS technology and the challenges encountered to move forward, and the existing semiconductor technologies that can help enable them. If you interested in finding out how you and your company can impact these nascent and emerging applications of MEMS you should not miss this event. ◆

Topics will include:

- **Biotechnology**
- **Communications/ New Generation IT/ Security**
- **Environmental/ Remediation Technology**
- **High-End Manufacturing Equipment and Techniques**
- **Advanced Materials**
- **Energy Saving and Environmentally Friendly Technologies**
- **Emerging MEMS Markets**

Symposium Co-Chairs

Janusz Bryzek, Ph.D., Vice President, *Fairchild Semiconductor*

Sean Cahill, VP of Research and Development, *BridgeWave*

John Heck, Ph.D., Research Scientist, MEMS Packaging, *Intel*

Joseph R. Mallon, Jr., CTO, *axept/Stanford University researcher*

Special Advisors

Kevin Chau, Vice President, *MEMStaff, Inc.*

Raj K. Gupta, Ph.D., Managing Director, *Volant Technologies*

Mike Pinelis, CEO and Editor, *MEMS Investor Journal*

Jim Walker, Vice President of Research, *Gartner-Dataquest*

The Wyndham Hotel is conveniently located at 1350 North First Street in San Jose, CA in close proximity to the San Jose Airport.

Dr. Janusz Bryzek

Joseph Mallon

Dr. Kurt Petersen

We are pleased to have **Dr. Janusz Bryzek**, **Joseph Mallon** and **Dr. Kurt Petersen** as our keynote speakers. In 1985 collectively they founded *NovaSensor*, considered by many to be pivotal in early MEMS technology and market development. Between them they have created and mentored a number MEMS companies and startups. Employees of founders' companies started multiple other companies, and they have created products that have sold in the billions with significant economic impact. They were also the organizers for the *2010 MEMS Technology Summit* held at *Stanford University*. The subject of their keynotes will be *"From the MEMS Technology Summit: Visions of Opportunities – Through the Eyes of Three MEMS Entrepreneurs"*. ◆

Fan-Out WLP/Embedded Die Packages

Be ready for next generation IC Packaging & Substrate Assembly waves!

Jérôme Baron, Market/Technology Analyst
Jean-Marc Yannou, Project Manager
Yole Développement

HISTORICALLY, EMBEDDED IC package technology is not new at all: several players such as Freescale with its RCP, Infineon with its eWLB and Ibiden for die embedded into PCB laminated substrates have developed dedicated technologies and process IP in this area for years. Benefits of embedded package integration include miniaturization, improvement of electrical and thermal performance, cost reduction and simplification of logistic for OEMs.

Things are moving really fast at the moment as this year, we see both Fan-out wafer level packaging and chip embedded into PCB laminate infrastructures emerging at the same time, ramping to high volume production.

Fan-Out WLP Technology is Emerging on Both 200mm/300mm Infrastructures

Infineon is having a great success with its proprietary eWLB technology: the first FO-WLP wafers are mass produced on 200mm both at Infineon and ASE since 2009. Indeed, Fan-Out WLP is extending the general concept of Wafer Scale Packaging to new application categories, especially the ones with higher pin-counts and larger chip size such as wireless communication ICs. First embedded package products based on eWLB have been identified within LGE and Nokia handsets. This year, a few additional players are even more aggressive in putting further capacity for eWLB manufacturing as both STATs ChipPAC and NANIUM are at the moment ramping-up their facilities for manufacturing the first generation eWLB on 300mm reconfigured wafers. Other packaging houses such as SPIL, Amkor, UTAC, ACE and others are also on the point to announce the start of their own Fan-out wafer level packaging operations.

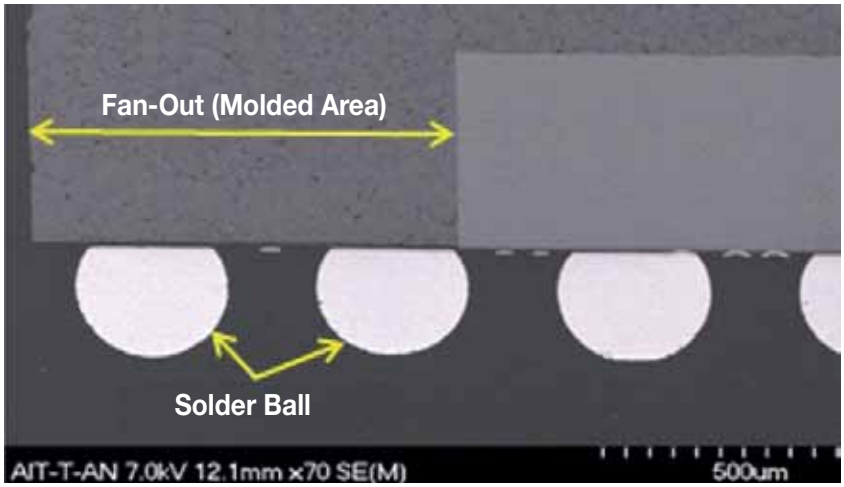


Figure 1. 1st generation eWLB cross-section. *(Courtesy of Infineon)*

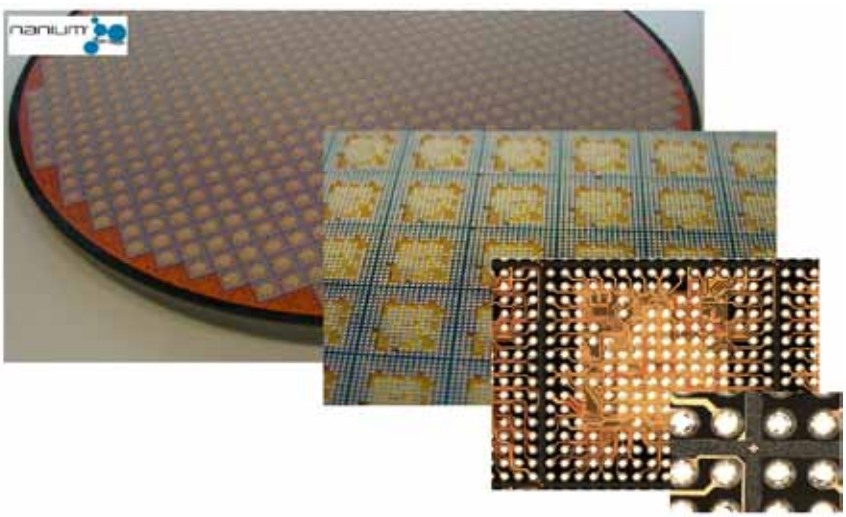


Figure 2. 300mm Fan-out WLP molded and reconfigured wafer. *(Courtesy of NANIUM)*

Embedded Die Package Technology to Expand Fast from Niche to High Volume Markets

At the same time, embedded die package technology has made a lot of progress on its side. Based on PCB laminate infrastructure, chip embedding technology is actually on the way to catch a relatively important portion of the actual WLCSP packaging business as it does leverage the existing WLP/RDL infrastructure already established worldwide: indeed, most of WLCSP die applications are "embedded ready", so to realize the full benefits of this "WLCSP to Embedded die" conversion, only a few extra manufacturing steps are missing like the realization of thin copper plating

Figure 3. iBGA embedded die package WLP cross-section. *(Courtesy of Imbera/Daeduck)*

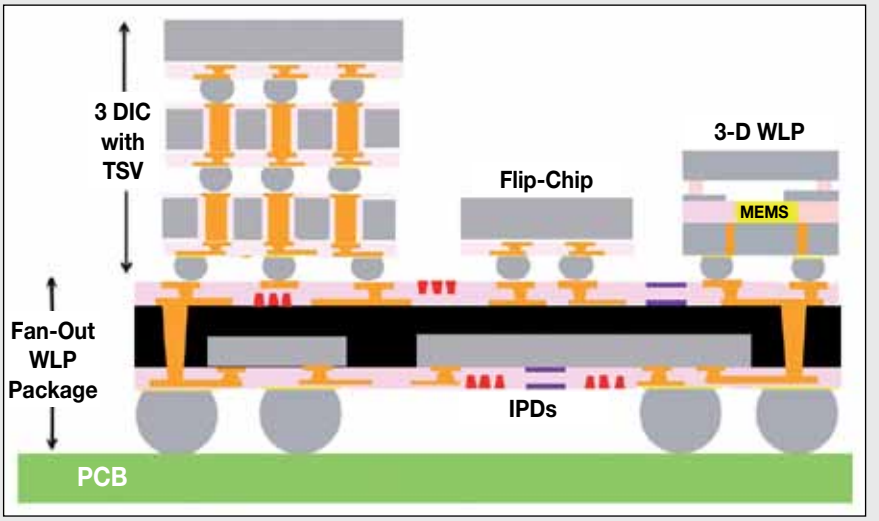


Figure 4. Overall tool-box solutions for 3D Packaging. *(Source Yole Developpement)*

process, extreme wafer thinning down to 50μm, thin dies handling and dicing.

Electrical performance, testing and manufacturing yields are still major issues and showstoppers for chip embedding technology to move forward. Therefore, initial volume markets for embedded packages will be rather small, low pin-counts analog type of applications such as integrated passive devices (IPD), RFID and power MOSFET components that are at the moment under qualification for mass production before the end of this year already. Generally speaking, we believe that the winning situation for embedded die packages can be met for company partnerships able to cross-over the traditional packaging, assembly and test supply chain. A good example would be to put together a leading analog IC player (such as TI, Maxim IC, NXP or ST) with a WLP/RDL partner (such as FCI, Casio Micronics, NEPES, etc…) together with a PCB integrator player (such as Imbera / Daeduck, Ibiden, AT&S, Taiyo Yuden or SEMCO). This type of emerging partnerships are absolutely necessary in order to standardize the embedded package technology and to leverage an entire new packaging infrastructure based on low-cost, panel size PCB manufacturing techniques.

FOWLP Versus Chip Embedding: Competing Technologies and Infrastructures?

Today, embedded die and Fan-Out WLP technologies are not competing at all. Indeed, these two emerging semiconductor packaging techniques are targeting very different applications initially: the chip embedding technology is looking for replacement of low cost, low pin-counts WLCSP / SOT / QFN / LGA family package applications while FOWLP technology is rather targeting the direct replacement of higher I/Os (> 200 pins) BGA package applications. However, in the long term, with standardization and through further technology improvements towards higher yield, better electrical performance, lower profile, better testability and smaller pitch features, Fan-out WLP and Embedded die technology could seriously compete in the fast growing 3D Packaging market space as they will both enable the construction of ever more complex, larger SiP modules with different active and passive functions, all connected on both sides of the active substrate… So Fan-out WLP and chip embedded into PCB laminates are just two additional key pieces of the widening tool-box for 3D Packaging! ◆

Electronic Materials

AS PART OF ITS EXTENSIVE portfolio, Dow Electronic Materials supplies materials essential for a wide range of advanced semiconductor packaging applications. Through its Advanced Packaging Technologies business, Dow Electronic Materials offers a portfolio of metallization, dielectric, lithography and assembly products that deliver enabling technology for leading-edge packaging schemes, such as WLCSP, flip chip, SiP, and 3D chip packages.

Dow Electronic Materials is a global supplier of materials and technologies to the electronics industry, bringing innovation and leadership to the semiconductor, interconnect, finishing, display, photovoltaic, LED and optics markets. With advanced technology centers worldwide, teams of Dow research scientists and application experts work closely with customers, providing solutions, products and technical service necessary for next-generation electronics.

Dow Electronic Materials' experience in metallization for electronics and materials for front-end semiconductor manufacturing makes the company unique in the chip packaging market. Dow Electronic Materials' heritage of innovation spans more than 50 years through the several companies, including Shipley, LeaRonal, Rodel and others, that came together in the last decade to form an electronic materials powerhouse known as Rohm and Haas Electronic Materials. The innovations began with revolutionary through-hole plating chemistry that changed the circuit board industry and continued into the dawn of semiconductor manufacturing with industry-leading photoresists and related lithography materials, damascene copper, and chemical-mechanical planarization (CMP) pads. Today, as part of The Dow Chemical Company following the 2009 acquisition of Rohm and Haas, Dow Electronic Materials' leading-edge products for semiconductor chips span the entire production process from polishing bare silicon substrates to connecting devices to the circuit board.

This heritage has built a deep understanding of the materials, stringent quality and expertise necessary to be successful in the semiconductor market and adjacent segments of electronics. Dow Electronic Materials has leveraged this experience into the Advanced Packaging Technologies business to deliver products and processes that enable the drive towards reduced form factor and increased functionality in electronic devices that require smaller and more reliable chip-to-chip and chip-to-circuit board interconnects and packages.

Dow Electronic Materials forges close relationships with its customers and the company is engaged in several joint development programs with industry leaders. "We understand the importance of working closely with our customers," says Leo Linehan, global business director for Advanced Packaging Technologies. "Close cooperation with our customers is essential to understanding their applications and material needs and ensuring that we deliver solutions that work."

Due to the global nature of the semiconductor industry, Dow Electronic Materials understands the need to provide local technical support and service. Dow Electronic Materials is in good position to support customers with its extensive global Advanced Packaging Technologies infrastructure, which continues to grow rapidly to enable expansion of the portfolio and to position resources close to customers. Advanced Packaging Technologies has R&D, applications, manufacturing and sales facilities and capabilities positioned globally at the following locations: Marlborough, MA; Midland, MI; Freeport, TX; Lucerne, Switzerland; Cheonan, Korea; Seoul, Korea; Taoyuan, Taiwan; Sasakami, Japan; and Tokyo, Japan.

Dow Electronics Materials is positioned to support customers with its extensive global Advanced Packaging Technologies infrastructure.

Marlborough, MA

Sasakami, Japan

Cheonan, Korea

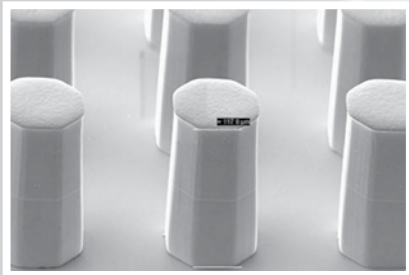
THE DOW ELECTRONIC MATERIALS portfolio of products for advanced chip packaging is comprised of many industry-leading materials. While products are often viewed as individual materials with their own advantages, Dow Electronic Materials approaches its portfolio with the understanding that they are developing and providing material systems to address thermal, mechanical, reliability and environmental challenges in advanced packaging applications.

Metallization Portfolio

Dow Electronic Materials has a long history of invention and innovation in electroplating chemistry, and the company's portfolio delivers many of the materials that are essential for the most advanced wafer-level, flip chip, system-in-package, package-on-package and 3D packaging schemes.

Copper for Wafer-level Packaging

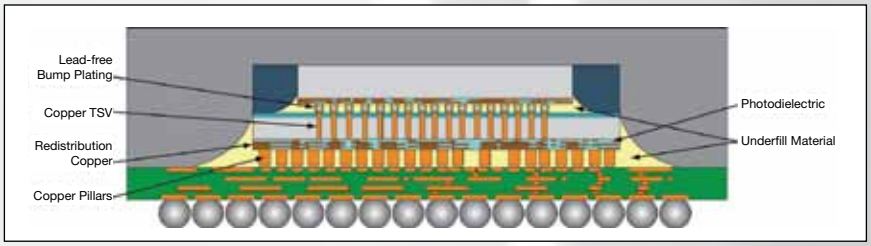
With production-proven metallization processes for high- and low-speed plating, INTERVIA™ Cu 8500 Series electroplating copper is ideal for wafer-level packaging. Its high aspect ratio capability and uniform, void-free deposits make it ideal for pillar, stud, redistribution, trench, via and other advanced packaging applications.



Pillars plated with INTERVIA Copper.

TSV Copper

Dow Electronic Materials is at the forefront of developing TSV copper solutions for this emerging packaging application with its INTERLINK™ and ULTRALINK™ TSV Copper chemistry. This three-component additive chemistry enables excellent gap-filling performance during bottom-up fill of TSVs with challenging aspect ratios. Dow has a significant advantage in the market with the ability to leverage its experience and success in electroplating damascene copper into TSV copper.

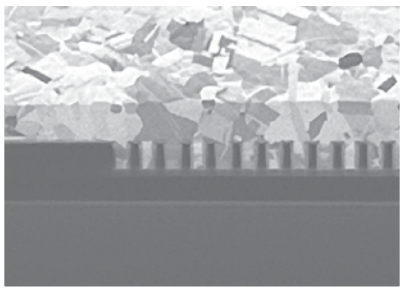


ETNA 3D chip stack with DRAM and Logic integration. (Chip package design concept courtesy of IMEC)

INTERLINK TSV Copper.

Damascene Copper

NANOPLATE™ and ULTRAFILL™ Series Electroplating Copper chemistries are production-proven in semiconductor manufacturing for memory and logic applications at 32 nm and below. With a three-component additive chemistry, Dow Electronic Materials' electroplating copper is capable of robust gap filling of aggressive features while meeting electro-migration and via stress migration in fab qualifications. Through controlled purity of copper deposits and its exceptional leveling capabilities, Dow Electronic Materials' electroplating copper delivers lower defectivity which translates into higher yields.

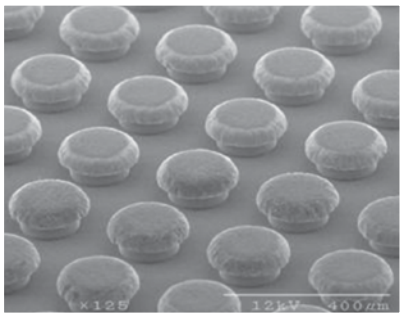


Leveled Deposit, ULTRAFILL Electroplating Copper.

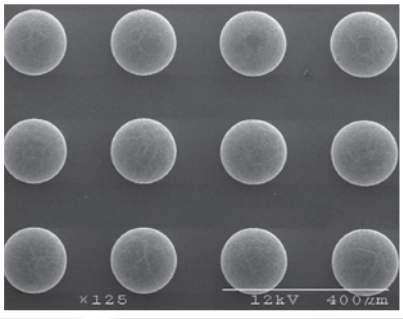
Wafer Bumping

Dow Electronic Materials' SOLDERON™ BP electroplating tin alloys are production-proven and provide customers with a variety of options that fit their needs. Dow's newest product for wafer bumping is SOLDERON™ BP TS 4000 Tin-Silver, a lead-free, single-step alloy plating material specifically designed for challenging advanced packaging applications. This product provides exceptional

SOLDERON BP TS 4000 Tin-Silver



Excellent within-die thickness uniformity.



Fine-pitch, reflowed SnAg bumps

processing flexibility for wafer bumping because it can be processed in a wide operating window at either high or low speed using a single formulation, while consistently producing uniform, void-free, smooth fine-grained deposits at fine pitches. With its excellent performance characteristics and industry-leading cost of ownership, SOLDERON BP TS 4000 Tin-Silver plating chemistry is ideal for in-via bumps, mushroom bumps and cap plating.

The tin portfolio also includes tin-lead, which is available in multiple alloy compositions, for applications that still require lead content in bumping applications. SOLDERON BP tin-lead deposits possess excellent solderability and are easily reflowed to form solder bumps. Dow Electronic Materials also leads the way with low-alpha materials by offering both tin and lead with low alpha particle emitting versions of their products, which are ideal for packaging applications sensitive to the effects of these emissions.

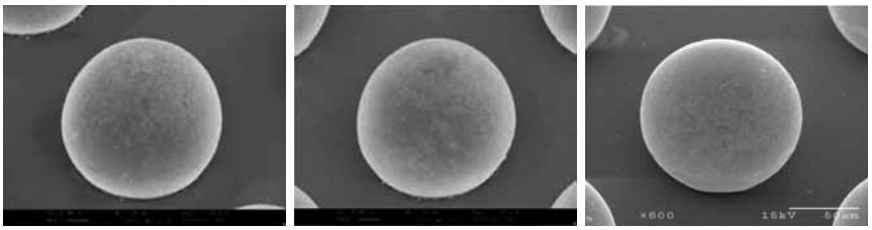
Electrolytic Wafer Plating Processes

To fill a variety of other metallization needs in advanced packaging, Dow Electronic materials offers both gold and nickel electroplating solutions. The electrolytic gold, AUROFAB™ BP II, is provided in a ready to use formulation that is suitable for semiconductor applications, and it delivers uniform deposits, excellent solderability and high cathode efficiency. Dow's NIKAL™ BP nickel provides a low-porosity electroplating bath with deposits that have high ductility and serve as an excellent barrier to copper diffusion.

Under Bump Metallization

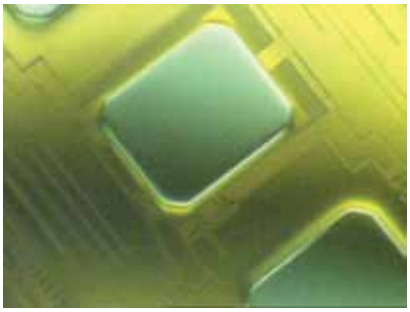
Dow Electronic Materials offers a range of electroless plating chemistries, including nickel, zincate, immersion gold and palladium, that are ideal for under bump metallization. These products are formulated to produce the varying customer needs for uniform deposits, high wear resistance, high hardness, porosity control, solderability and other characteristics that are essential for consistent wafer fabrication.

SOLDERON BP TS 4000 Tin-Silver



6 ASD | 8 ASD | 12 ASD

Wide Operating Window

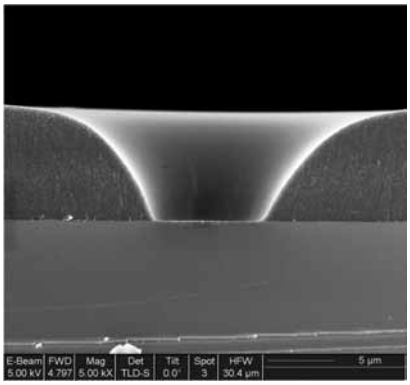


ENIG (electroless nickel/immersion gold) for wafer plating processes, after electroless nickel process.

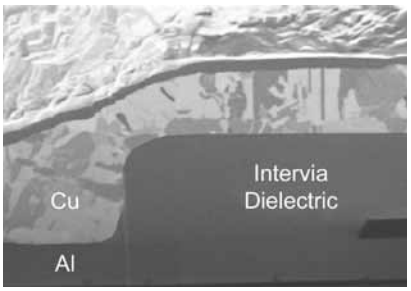
Dielectric Portfolio

Dow Electronic Materials offers two lines of dielectric materials specifically designed for advanced packaging applications.

CYCLOTENE™ Advanced Electronics Resins from Dow Electronic Materials are high-purity polymer solutions that have been developed for microelectronic applications. The resins are formulated as high-solids, low-viscosity solutions, which, along with exceptional performance characteristics, make them ideal as dielectrics in wafer-level packaging applications. The hallmark of CYCLOTENE dielectric materials is its excellent electrical properties and superior chemical resistance. Customers can choose from the 3000 series, which is a dry-etch grade spin-on dielectrics, or the 4000 series, which is a negative-tone, photosensitive, spin-on dielectric. CYCLOTENE dielectrics a low dielectric constant along with good planarization properties and compatibility with copper. The material is used for dielectric redistribution, bumping, passivation and wafer bonding applications, among others.



10 µm via in 10 µm thick film, CYCLOTENE positive-tone dielectric.

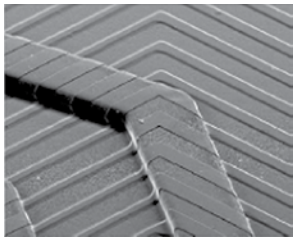


INTERVIA Photodielectric in WLCSP Fan Out Package (courtesy: NXP Semiconductor)

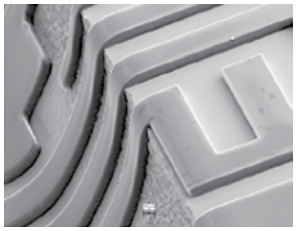
INTERVIA™ Photodielectrics are epoxy-based, negative-tone permanent dielectric materials designed for use on wafers and organic/inorganic substrates. The spin-on material has a low dielectric constant, low moisture absorbance, low temperature cure, low stress, and excellent adhesive characteristics for bonding applications. INTERVIA photodielectrics can be used for passivation stress buffer, die topcoat, redistribution, permanent polymer adhesive and TSV polymer fill/metal insulator.

Packaging Photoresist

Available as positive- and negative-tone resists, INTERVIA™ 3D Photoresists are aqueous-based emulsions that can be electrodeposited onto a wide variety of electrically-conductive substrates. The conformal properties of these resists make them ideal for substrates with complex geometries. The resists have exceptional chemical resistance to plating and etching solutions. They are designed for wafer, MEMs, lead frames and three-dimensional photolithography applications.



INTERVIA 3D Photoresist, 25 µm lines over 45 µm high features. (courtesy: IZM Fraunhofer)



INTERVIA 3D Photoresist over topography
(courtesy: IZM Fraunhofer)

Assembly Materials

As the semiconductor industry approaches the limitations of Moore's law, Dow Electronic Materials recognizes the industry need for innovative material solutions capable of meeting challenges of achieving reliability for large die with low-k and ultra-low-k layers. For that reason, Dow Electronic Materials is developing underfill material solutions for flipchip and 3D packaging in collaboration with leading industry partners. The new materials are aimed at addressing many of the thermal and mechanical challenges inherent in increased die size and 3D packaging.

According to Dr. Jeff Calvert, director of R&D for Advanced Packaging Technologies, progress on these underfill development programs has been enhanced by the combination of the legacy Rohm and Haas Electronic Materials with The Dow Chemical Company. "Our Advanced Packaging Technologies business now has access to much deeper analytical and R&D capabilities as well as to a wider range of material technology options." says Calvert. "Combining the strengths of Rohm and Haas with Dow together with close customer partnerships has been powerful."

As semiconductor technology for front end and back end packaging and assembly converges, materials and material interactions become more complex. According to Bhavesh Muni, global marketing manager for Assembly Materials, "Dow is uniquely positioned to offer complete integrated packaging material solutions for the next-generation of semiconductor packages with our in-depth understanding and product offerings in the semiconductor front-end, our growing portfolio of back-end products, and our focus on innovation in material science."

For more information about Dow Electronic Materials and the advanced packaging portfolio, visit www.dow.com or contact Bhavesh Muni at bmuni@dow.com. ◆

Xilinx Stacked Silicon Interconnect Technology

Producing a New Class of High-capacity, Resource-rich FPGAs

Suresh Ramalingam
Sr. Director Package Design and Technology
Xilinx

AS THE ROLE OF THE FPGA BECOMES MORE DOMINANT in system Design, the designs grow larger and more complex, demanding higher logic capacity and more on-chip resources. To date, FPGAs have depended predominantly on Moore's Law to respond to this need, delivering nearly twice the logic capacity with each new process generation. However, keeping pace with today's high-end market demands requires more than Moore's Law increases can provide.

Xilinx has responded to these requirements with an innovative Stacked Silicon Interconnect Technology approach for building FPGAs that offer bandwidth and capacity one full generation ahead of when they otherwise become available using traditional Moore's law scaling. Stacked Silicon Interconnect Technology uses silicon interposers with micro-bumps and through silicon vias (TSV) to combine multiple FPGA die slices in a single package.

The Challenges of Interconnecting Multiple FPGAs

Stacked Silicon Interconnect Technology solves the challenges that had previously obstructed attempts to combine the interconnect logic of two or more FPGAs to create a larger, "virtual FPGA" for implementing a complex design:

- The amount of available I/O is insufficient for connecting the complex networks of signals that must pass between FPGAs in a partitioned design and as well as connecting the FPGAs to the rest of the system.
- The latency of signals passing between FPGAs limits performance.
- Using standard device I/O to create logical connections between multiple FPGAs increases power consumption.

Key Challenge: Limited Connectivity and Bandwidth

System-on-chip (SoC) designs comprise millions of gates connected by complex networks of wires in the form of multiple buses, complicated clock distribution networks, and multitudes of control signals. Successfully partitioning an SoC design across multiple FPGAs requires an abundance of I/Os to implement the nets spanning the gap between FPGAs. With SoC designs including buses as wide as 1,024 bits, even when targeting the highest available pin count FPGA packages, engineers must use data buffering and other design optimizations that are less efficient for implementing the thousands of one-to-one connections needed for high-performance buses and other critical paths.

Packaging technology is one of the key factors to this I/O limitation. The most advanced packages currently offer approximately 1,200 I/O pins, far short of the total number of I/Os required.

At the die level, I/O technology presents another limitation because I/O resources do not scale at the same pace as interconnect logic resources with each new process node. When compared to transistors used to build the programmable logic resources in the heart of the FPGA, the transistors comprising device I/O structures must be much larger to deliver the currents and withstand the voltages required for chip-to-chip I/O standards. Thus, increasing the number of standard I/Os on a die is not a viable solution for providing the connections for combining multiple FPGA die.

Key Challenge: Excessive Latency

Increased latency is another challenge with the multiple FPGA approach. Standard device I/Os impose pin-to-pin delays that degrade the overall circuit performance for designs that span multiple FPGAs. Moreover, using time-domain multiplexing (TDM) on standard I/Os to increase the virtual pin count by running multiple signals on each I/O imposes even greater latencies that can slow I/O speeds down by a factor of 4X–32X or more.

Key Challenge: Power Penalty

TDM approaches also result in higher power consumption. When used to drive hundreds of package-to-package connections across PCB traces between multiple FPGAs, standard device I/O pins carry a heavy power penalty compared to connecting logic nets on a monolithic die.

Similarly, multichip module (MCM) technology offers potential form-factor reduction benefits for integrating multiple FPGA die in a single package. The MCM approach, however, still suffers from the

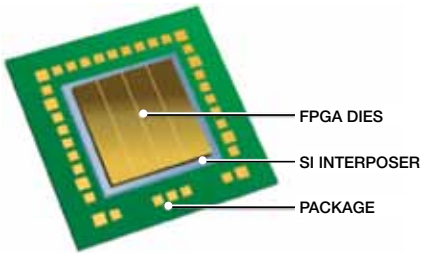


Figure 1. Stacked Silicon Interconnect Technology die top view

same restrictions of limited I/O count as well as undesirable latency and power consumption characteristics.

Xilinx Stacked Silicon Interconnect Technology

To overcome these limitations and roadblocks, Xilinx has developed a new approach that enables high-bandwidth connectivity between multiple die by providing a much greater number of connections. It also imposes much lower latency and consumes dramatically lower power than the multiple FPGA approach, while enabling the integration of massive quantities of interconnect logic and on-chip resources within a single package.

Xilinx arrived at such a solution by applying several proven technologies in an innovative way. By combining through-silicon via (TSV) and micro-bump technology with its innovative ASMBL™ architecture, Xilinx is building a new class of FPGAs that delivers the capacity, performance, capabilities, and power characteristics required to address the programmable imperative. Figure 1 shows the top view of the die stack-up with four FPGA die slices, silicon interposer, and package substrate. Xilinx stacked silicon interconnect technology combines enhanced FPGA die slices and a passive silicon interposer to create a die stack that implements tens of thousands of die-to-die connections to provide ultra-high inter-die interconnect bandwidth with far lower power consumption and one fifth the latency of standard I/Os.

Originally developed for use in a variety of die-stacking design methodologies, silicon interposers provide modular design flexibility and high-performance integration suitable for a wide range of applications. The silicon interposer acts as a sort of micro-circuit board in silicon on which multiple die are set side by side and interconnected. Stacked silicon interconnect technology avoids the power and reliability issues that can result from stacking multiple FPGA dies on top of each other. Compared to organic or ceramic substrates, silicon interposers offer far finer interconnect geometries (approximately 20X denser wire pitch) to provide device-scale interconnect hierarchy that enables more than 10,000 die-to-die connections.

Creating FPGA Die Slices with Micro-bumps for Stacked Silicon Integration

The foundation of Xilinx stacked silicon interconnect technology is the company's proprietary ASMBL architecture, a modular structure comprising Xilinx FPGA building blocks in the form of tiles that implement key functionality such as configurable logic blocks (CLBs), block RAM, DSP slices, SelectIO™ interfaces, and serial transceivers. Xilinx engineers organize the blocks in columns of each type of tile and then combine the columns to create an FPGA. By varying the height and arrangement of columns, the Xilinx engineers can create an assortment of FPGAs with different amounts and mixes of logic, memory, DSP, and I/O resources (Figure 2). The FPGA contains additional blocks for generating clock signals and for programming the SRAM cells with the bitstream data that configures the device to implement the end user's desired functionality.

Starting with the basic ASMBL architectural construct, Xilinx has introduced three key modifications that enable stacked silicon integration (see Figure 3). First, each die slice receives its own clocking and configuration circuitry. Then the routing architecture is modified to enable direct connections through the passivation on the surface of the die to routing resources within the FPGA's logic array, bypassing the traditional parallel and serial I/O circuits. Finally, each slice undergoes additional processing steps to fabricate microbumps that attach the die to the silicon substrate. It is this innovation that enables connections in far greater numbers, with much lower latency, and much less power consumption than is possible using traditional I/Os

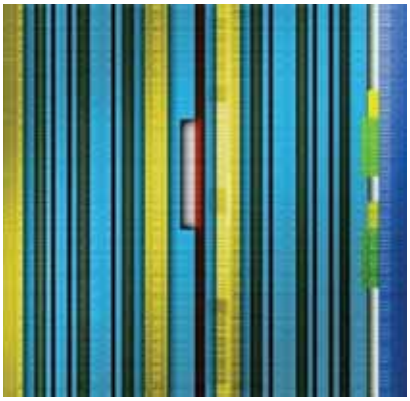


Figure 2. Representation of an FPGA built with ASMBLTM architecture

Figure 3. FPGA die slice optimized for stacked silicon integration

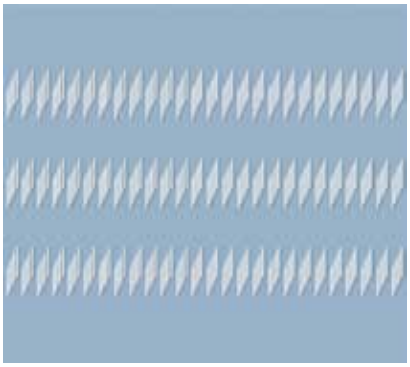


Figure 4. Passive silicon interposer

Figure 5. "X-ray view" of the assembled die stack

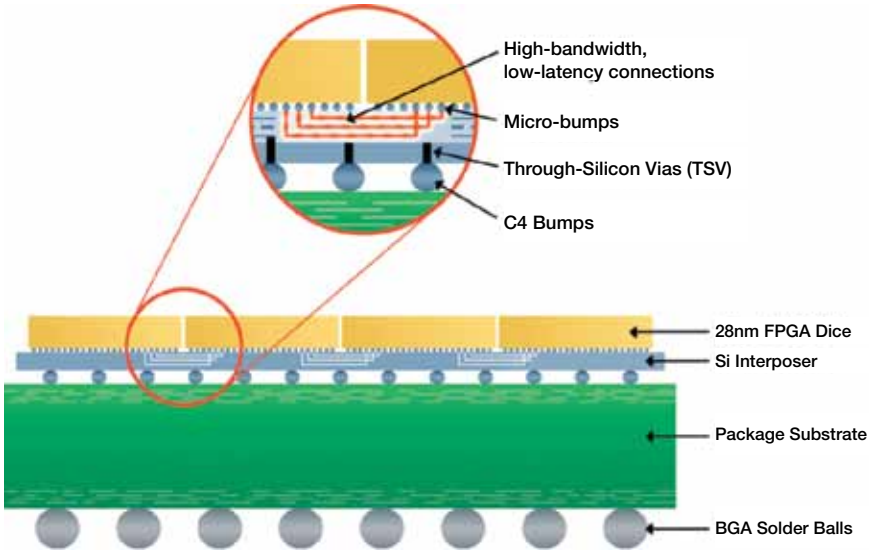


Figure 6. FPGA-Silicon interposer integration on a package substrate

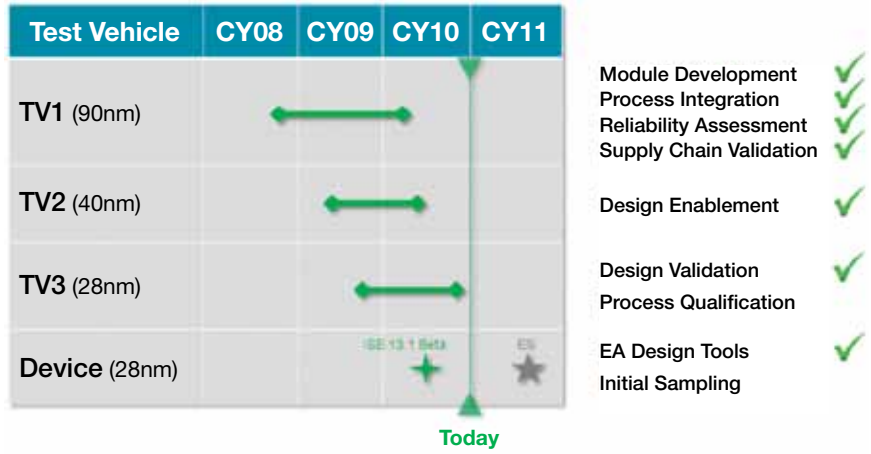


Figure 7. Top die test vehicle (technology node) assessment with silicon interposer and package

(100X the die-to-die connectivity bandwidth per watt versus standard I/Os).

Silicon Interposer with TSV

The passive silicon interposer interconnects the FPGA die. It is built on a low-risk, high-yield 65 nm process and provides four layers of metallization for building the tens of thousands of traces that connect the logic regions of multiple FPGA die (Figure 4).

Figure 5 illustrates the concept of an "X-ray view" of the assembled die stack. It contains a stack-up of four FPGA die mounted side by side on a passive silicon interposer (bottom view). The interposer is shown as transparent to enable a view of the FPGA die slices connected by traces on the silicon interposer (not to scale).

The TSVs combined with controlled-collapse chip connection (C4) solder bumps enable Xilinx to mount the FPGA/interposer stack-up on a high-performance package substrate using flip-chip assembly techniques (Figure 6). The coarse-pitch TSVs provide the connections between the package and the FPGA for the parallel and serial I/O, power/ground, clocking, configuration signals, etc.

Comprising numerous patent-pending innovations, this stacked silicon interconnect technology provides multi-Terabit-per-second die-to-die bandwidth through more than 10,000 device-scale connections – enough for the most complex multi-die designs. Xilinx is using this new technology to create the Virtex®-7 FPGA family, which offers unprecedented capabilities including up to: two million logic cells; 65 Mb of block RAM; 2,375 GMACS of DSP performance (4,750 GMACS for symmetric filters); 1,200 SelectIO pins supporting 1.6 Gb/s LVDS parallel interfaces; and 72 serial transceivers delivering 1,886 Gb/s aggregate bidirectional bandwidth.

Bringing Stacked Silicon Interconnect Technology to Production

The development strategy Xilinx has employed in the creation of the FPGA with stacked silicon interconnect technology begins with extensive modeling and the creation of a series of test devices, or test vehicles, used for design enablement and for manufacturability and reliability validation.

Stress simulation models show an additional advantage of stacked silicon technology. The silicon interposer functions as a buffer that reduces low-K dielectric stress and improves C4 bump reliability, compared to monolithic solutions.

Extensive simulations investigating the thermal impact of the die stack show that thermal performance of devices with stacked silicon interconnect technology is comparable to that of monolithic devices.

Xilinx is well on the way to volume production of the first FPGAs with stacked silicon interconnect technology, having completed over five years of research and development with industry-leading suppliers and extensive testing on series of multiple test vehicles (Figure 7). These test vehicles address process module development and integration, reliability assessment, supply-chain validation, design enablement, interposer known-good-die (KGD) methodology, and microbump electromigration (EM) rules.

Test vehicle-based reliability tests successfully completed to date include:

- 1,000 cycles of package and wafer level Temperature Cycle B evaluation of TSV, C4 balls, and interposer interconnects
- 1,000 hour high temperature storage evaluation of micro-bump joints

• 0.1% cumulative density function (CDF) for electromigration at the microbump Joint

Xilinx already has a robust supply chain in place for the technologies required to build the industry's first FPGAs with stacked silicon interconnect technology. TSMC, Amkor, and Ibiden contribute their combined resources and expertise for fabricating 28 nm FPGAs and 65 nm silicon interposers, interconnect layers, microbumps, C4 balls, and package substrates as well as performing wafer thinning, die separation, chip-on-chip (CoC) attach, and package assembly.

Summary

As the only FPGA manufacturer to use stacked silicon interconnect technology to create super high capacity FPGAs with unmatched die-to-die bandwidth, Xilinx is breaking important new ground in the system-level integration arena. Stacked silicon interconnect technology will enable Xilinx to deliver the highest logic density, bandwidth, and on-chip resources with the fastest ramp to volume production at every process node.

Customers will find these FPGAs with stacked silicon interconnect technology significantly easier to design with than multiple FPGAs, with flexible tool flows that provide complete design tools for ease of use, yet allow designer interaction for achieving even higher performance. ◆

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High Density Leadframe Array

An Evolutionary Leadframe Package

Kelly R. McKendrick Sr., Technical & Sales Manager
Serafin Pedron, Director – Product Development & Marketing
UTAC UGS America Sales Inc.

IN THE SEMICONDUCTOR packaging industry, we want it all. Of course it does not always work that way, but if we could somehow incorporate and integrate the advantages of QFN, fpBGA, TAPP/TLA, FC, TQFP, TSOP and other assembly technologies into a single package we would be getting close. With assembly and packaging now more of an integral part of the whole semiconductor design solution, more flexibility in the actual packaging design around the die is required. The bottom line is that the semiconductor industry wants a package that is flexible in design, has higher I/O density, a very high die to package body size ratio, green, with superior thermal and electrical advantages. Sounds easy enough, right?

A new leadframe-based technology named HLA™ (Hi-Density Leadframe Array) has made a breakthrough in taking the advantages of the best attributes of these packages and incorporating them into a package that is truly evolutionary. The result is a lead frame package with the highest I/O solution in the industry that can replace many types of QFN and other LF and BGA technologies. HLA can be matrixed and mounted like a BGA. See Figure 1 showing a full matrix BGA version with various lead finish options.

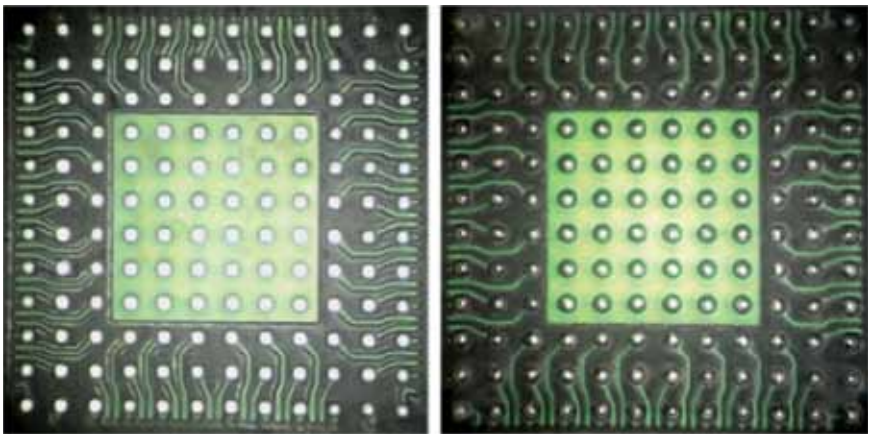

Figure 1. Full matrix BGA version with various lead finish options. Solder coating is shown on left, solder ball drop is shown on right.

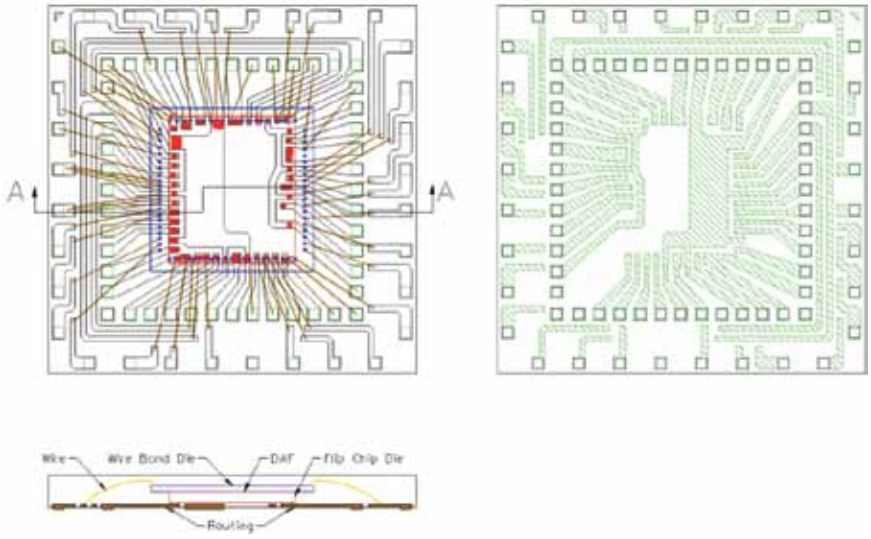

Figure 2. Stacked die (wirebond over flip chip).

HLA Package Highlights

Design Flexibility

Like its close cousins, the QFN & TLA, HLA is a lead frame based product that has limitless design flexibility and actually allows the designer to design the package around the die. I/O counts of HLA can rival many of the Fine Pitch BGA products. In the past, in order to gain more leads in a leadframe product, you had to grow the body size. This is done by adding more I/O's on each side and adding another row away from the die. This not only grows the body size but also results in longer bond wires and the accompanying issues with wire bond,

wire sweep, higher inductance, etc. The HLA technology allows you to route under the die so growing the package is no longer necessary. Body sizes in a certain lead count of QFN or QFP can generally be reduced by several sizes in an HLA.

Each design can meet JEDEC specs or can be a unique customized package designed to meet the customer's application. The possibilities of design are limitless. HLA is designed to the die. Some examples include: different pad pitches, down bond rings or pads, isolated power rings, the number of rows of outer leads, stacked & multiple die, Flip Chip, SiP, etc. See Figure 2 showing a stacked die (wirebond over flip chip) with some level of interconnectivity between the 2 chips and tweaking of the lines and space for optimum electrical RF performance. If you can think of it, it more than likely can be done. Best of all, once a package design is finalized, a customer can have assembled parts in hand in less than 3 weeks.

Package Size and Performance

The package size is generally determined by 3 factors.

1) Max Die size - General rule of thumb for HLA is the package size minus 1 mm. So a 4x4 mm die can fit in a 5x5 mm package. No current leadframe technology can offer this. See Figure 3 showing maximum I/O counts possible in a 5x5mm body size, all at 0.5mm terminal pitch, at various die sizes.

2) Lead pitch – This usually is a factor of the customers' 2nd level board routeability. The nice thing about HLA is we can do many things to meet the routeability requirements of each and every customer, such as depopulating the outer row for escape routing, variable pitch or even configuring the exposed DAP to allow a via drop to a 2nd metal layer on the board.

3) Package performance requirements – Electrically, HLA is far superior to any leadframe product on the market. This is due to shorter wire and total signal lengths that are inherent in HLA designs. Savings of up to 75% of wire lengths help reduce wire sweep to almost zero. Figure 4 shows the inductance and capacitance comparison between HLA

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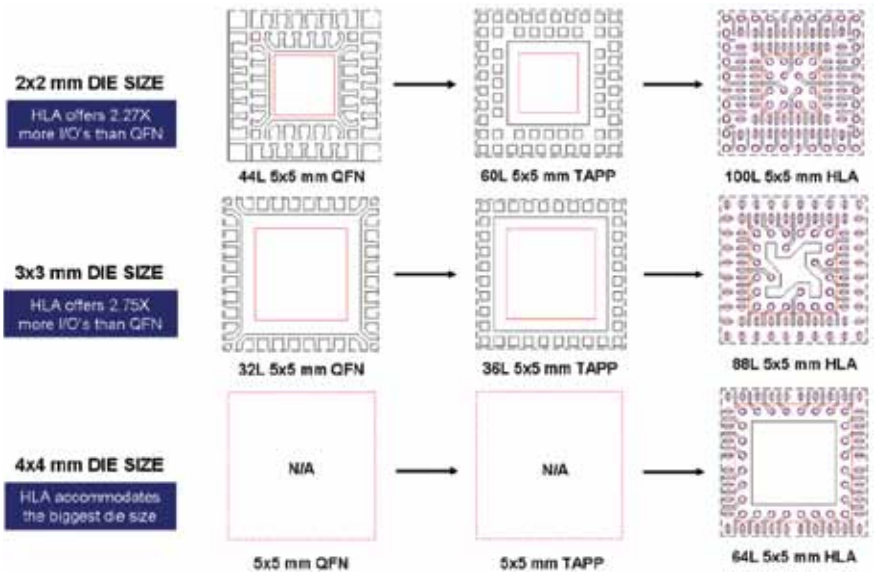


Figure 3. Maximum I/O counts possible in a 5x5mm body size, all at 0.5mm terminal pitch.

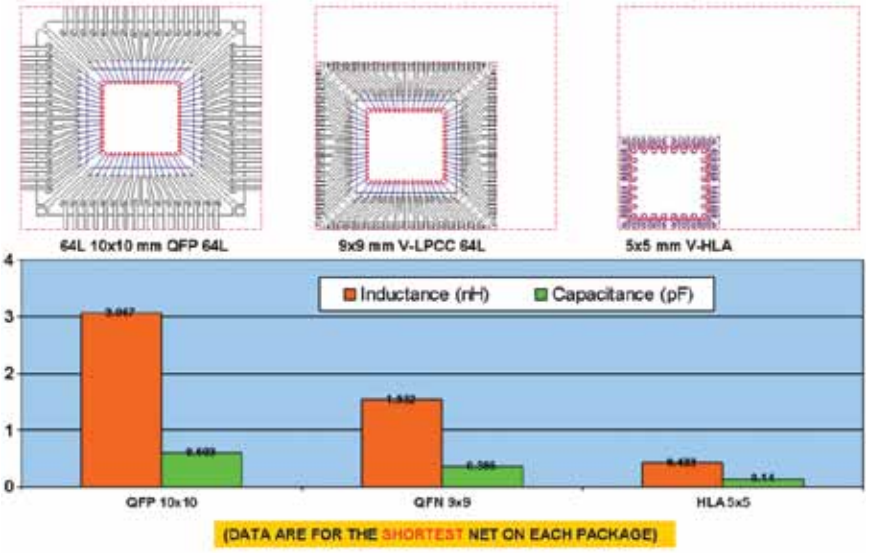
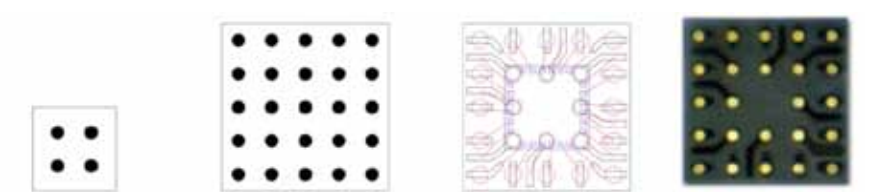


Figure 4. Inductance and capacitance comparison between HLA (Hi-Density Leadframe Array) and other leadframe-based packages.



Package Type:
1x1mm 4L WLCSP
Bump Pitch: 0.4mm
Max. Bump Count: 4

Package Type:
2x2mm 25L WLCSP
Bump Pitch: 0.4mm
Max. Bump Count: 25

Package Type: 2x2mm 24L HLA
Die Size: 1x1mm
Maximum Package Thickness: 0.4mm
Lead Pitch: 0.4mm

Figure 5. HLA could be a low cost replacement for WLCSP.

PACKAGING continued from page 27

and other leadframe-based packages. Thermally, HLA is superior as the large die size capability results to a lower thermal density; i.e., more silicon area for dissipating the heat generated by the chip, as well as options for an exposed DAP that can be soldered to a thermal land on the PCB.

Lead Finish

Unlike the leads on a QFN, the leads on an HLA have a 1-2 mil standoff. The standard plating is solder coat. If you would prefer to have solder balls, you can have this as well. Many people like solder balls as they are used on a BGA type package. See Figure 1. Either of these options are similar to the self-aligning characteristics of a BGA product and also facilitates PCB rework.

Other Applications and Advantages

Besides the possible replacement of many larger packages HLA can also be advantageous in other areas. For example: HLA could be a low-cost replacement for WLCSP. Let's look at a 1x1mm die. The maximum number of bumps recommended by JEDEC at 0.4mm pitch is 4 bumps. In order to increase the I/O count, the silicon size would need to be increased to 2x2mm in order to achieve 25 bumps. On the other hand, a 2x2mm HLA with a 1x1mm die size configured for wirebond has 24 bumps, possibly 25. No additional die size is needed and no redistribution layers are required. See Figure 5.

Another application or advantage is that of strip test. Once the final etch is complete, the leads are not tied electrically, thus it is ready for strip test. No additional mechanical or chemical process is required to isolate the leads for strip test. In addition, with no metal in the streets, most all saw singulation issues, especially those dealing with copper, are now eliminated. Like saw singulated QFN's, one mold is all that is needed for every design. Materials are green and can meet all of the current lead free standards.

Board Routeability and Reliability

Frequently asked questions center around routeability and reliability. Design as well as routeability rules are in place. HLA is customized for the customer's die and package needs as well as their board application. These are all taken into consideration when the HLA is designed.

The OEM manufacturers can also benefit from HLA. They can either reduce board space or integrate more functionality into the same amount of real estate.

Reliability is also a key question for all customers. HLA is an MSL level 1 package. All current data as well as data from a very similar technology, the TLA package, shows that HLA will perform as well or even better than any other leadframe product.

Conclusion

So what is the ultimate package? I guess it depends on what you need or want. There are many good choices out there and one size does not fit all. But with the packaging world going more and more toward inclusion of the overall final product design, definitely more and more flexibility is needed. We see a change in the way the industry will think about how to design and manufacture packages. There will be a shift in the assembly world and the HLA type products are going to lead the way. ◆

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OPINION continued from page 30

The US is still the world's leader in science and technology, accounting for 40% of the global spending on R&D and a proportional share of enabling patents according to a recent RAND Corporation analysis. Despite our economic and innovation strengths, a new Gallup Poll taken in early February found that the majority of Americans believe that China is the world's largest economy. The facts are that the US economy is $14.66T in size and will average growth of 2.2% over the next several years – the largest rate of any mature economy. China's economy is $5.88T and is projected to grow at a rate of 8.3%. China's gross domestic product could surpass that of the US by 2020, but even then, the average Chinese citizen will earn far less than the average American on a per capita basis.

The world's fastest supercomputer as of November 2010 is the Tianhe-1A system at the National Supercomputer Center in Tianjin, China, achieving a performance of 2.57 petaflops and taking the title from the Cray XT5 "Jaguar" system (rated at 1.759 petaflops) residing at the US DOE's Oak Ridge National Laboratory. One interesting thing to note is that the system does not use chips designed in China; it is powered by more than 7000 GPU's from US-based Nvidia. Rumors in the supercomputing community are that IBM and Fujitsu will unveil powerful systems designed to perform at more than 10 petaflops in the next year. Bottom line, competition is a good motivator for continued innovation.

Secondary education in the US is a concern, but the countries that outperformed the US on the PISA test are typically small or homogeneous or both. America's public school system works well for non-poor non-immigrant students who performed comparably to their leading-country counterparts around the world. Rather than bashing our K-12 education system, we need to combat the sources of poverty directly by means of job creation – something that continuing to innovate can help address. As an example, innovation in the solar power industry has implications for fabricators, distributors, sellers, contractors, installers, maintainers – folks all throughout the economic spectrum.

Technology development is the primary source of prosperity in the US, the cornerstone of our competitiveness, and fundamental to our view of ourselves as a nation of bold and pioneering problem solvers. We have a culture of embracing risk, the ability to attract talent from around the world, top universities, and a willingness to invest in ourselves. We must play to our strengths, face up to our shortcomings, continue to innovate, and worry – but not too much. ◆

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The Innovation Edge – Do We Still Have It?

Sean S. Cahill
BridgeWave Communications, Inc.

THERE IS LIKELY NO MORE fundamental aspect of the American mythos than our belief in ourselves as pioneers, risk takers, embracers of new ideas – innovators. Economic models of productivity have shown that, from 1909 – 1949, 80% of economic growth in the US was driven by technological progress, and technology innovation continues to be our most powerful engine of prosperity. For the last 70 years American companies have been unrivaled innovators. We take great pride in our ability to create the means to change our nation and the world for the better.

Yet, we increasingly hear that justifications for our technological exceptionalism may be diminishing. According to a recent Boston Consulting Group (BCG) report, the US now ranks 8th in the world for innovation. In the World Economic Forum (WEF) report on Global Competitiveness, the US has dropped from 2nd to 4th, behind Switzerland, Sweden, and Singapore. The fastest supercomputer in the world no longer resides here, but in China. According to the Program for International Student Assessment (PISA), the U.S. ranks 12th in reading, 17th in science and 25th in mathematics. In recent polls, 63% of Americans said they believe they will be unable to maintain their current standard of living. With all this bad news, should we be worried, and how worried should we be?

The answers here are not simple. We must confront some unsettling truths, yet there are reasons to be hopeful that the US will continue to lead in many important ways. First, lets talk about what we mean by innovation. In their report, BCG and Business Week magazine asked survey respondents to identify the importance of innovation leading to five different types of output:

- "New to the world" products/services to create entirely new markets
- New offerings allowing expansion into new customer groups
- New offerings for existing customers
- Incremental changes to existing offerings
- Lower production costs for existing offerings (eg. cheaper materials)

Their report concludes that most companies (92%) are increasing their innovation investments, but concentrating mostly at the more conservative end of the spectrum – fewer new offerings, more incremental changes and lowering of costs. Companies are emphasizing safe bets, and preparing for a range of options. Much of their investment is being placed in the rapidly developing economies of Brazil, India, and China (BIC). 84% of the survey respondents said their company considers innovation as very important in their positioning for an economic recovery, and three-quarters of companies are calling innovation a top priority – up nearly 15%. The report also shows that the most innovative companies outperformed their peers by a 12.4% margin over a three-year period. Of the 20 most innovative companies in the world, 11 are American. Big movers on the list: Intel moved to 12th place from 33rd, Ford moved to 13th from 31st, and the first-time entry of Oracle at 40th Most Innovative.

So where is the bad news? The BCG report summarizes the results of surveys – how people feel. Survey respondents from the BIC nations are attaching greater importance to innovation and are more confident than their counterparts in mature economies like the US. The presence of BIC companies on the Most Innovative list is expanding, while the presence of US companies is diminishing. Of the seven first-time entrants to the Most Innovative list, only two were from non-BIC countries. Only 49% of respondents thought the US would "…maintain its acknowledged leadership role in innovation over the next five years." Don't miss that last point – the US is the current acknowledged leader in innovation.

The WEF report defines competitiveness as, "…the set of institutions, policies, and factors that determine the level of productivity of a country." They list 12 pillars of economic competitiveness for which the US was ranked along with 138 other countries: Institutions (40th), Infrastructure (15th), Macroeconomic environment (87th), Health and primary education (42nd), Higher education and training (9th), Goods market efficiency (26th), Labor market efficiency (4th), Financial market development (31st), Technological readiness (17th), Market size (1st), Business sophistication (8th), and Innovation (1st). That's right – number one in Innovation. The WEF report concludes that US companies are innovative, supported by an excellent university system that collaborates strongly with business in R&D. The US still has the largest domestic economy in the world by far, and the second largest foreign economy. US labor markets allow ease of hiring and significant wage flexibility.

So what are our biggest issues? In the category of Institutions, US respondents felt that the business costs of crime, organized crime, and dealing with terrorism were onerous. They also felt that government was generally wasteful in its spending. On the Macroeconomic front, they were concerned with a poor national savings rate and government debt/spending. On the Health/Primary Education category, they were very concerned with the prevalence and impact of HIV/AIDS and with our poor primary education enrollment rate, where we rank an unbelievable 79th in the world according to UNESCO. The number one issue identified by US corporate executives for this year given their litany of worries – poor access to financing.

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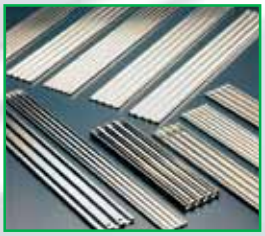
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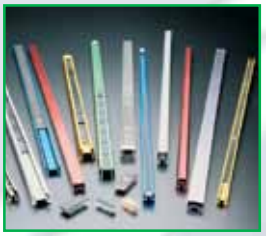
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