MEPTEC Report

FALL 2011

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 15, Number 3

KGD 2011

KNOWN GOOD DIE

In an Era of Multi-Die Packaging and 3D Integration

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2.5D, 3D and Beyond

Bringing 3D Integration to the Packaging Mainstream

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STATS ChipPAC –
The 2004 merger of STATS and ChipPAC created the fourth largest OSAT company in the world.

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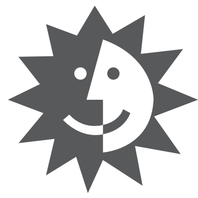

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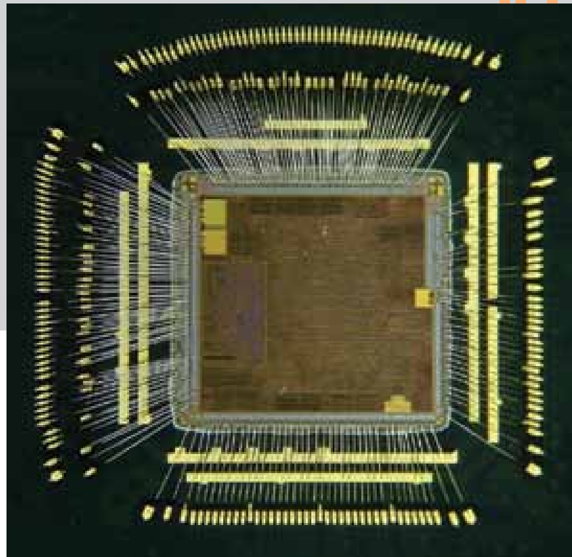
Copper Wire



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Rising Silver Costs, Looming RoHS Deadlines and Leadframe Package Scalability... Is There a Die Attach for That?

Doug Dixon, Henkel Electronic Materials LLC
MEPTEC Advisory Board Member

TALK ABOUT A LITTLE PRESSURE! The last few years have seen dramatic changes in the semiconductor packaging segment largely driven by unrelenting device miniaturization in combination with increased functionality demands. Given these market dynamics, semiconductor packaging materials have also had to adapt, with new formulations delivering far greater performance while addressing ever decreasing device dimensions. When you add to the mix the meteoric rise in silver cost (a key metal for the packaging sector), the impending move to lead-free materials in the power device segment and the need for leadframe package manufacturers to achieve better workability and scalability, the pressures on die attach materials developers are immense.

These new challenges are the types of issues that MEPTEC is focused on addressing and are also precisely the things that our company has been working to overcome and has been able to achieve. Breakthrough die attach formulation techniques have yielded some novel material systems that address many of these perceived obstacles and, in my view, will move the industry forward faster by enabling new package designs and more cost-efficient production processes. Let's start by addressing the most well-known and critical raw material in the packaging sector: silver. Over the last year, silver has more than doubled in cost. As one of the key components of modern die attach formulations, this has made materials development and, therefore, package production a more pricey proposition. To help stem the price volatility and offer some long-term cost stability, a die attach that uses significantly less silver than that of traditional formulations has been developed. The technology – silver plated copper (SPC) – is not a new concept, but one which has been perfected to ensure rheology control and system stability. With the SPC technique, tiny particles of copper are coated with silver, producing SPC filler that has been proven to deliver similar thermal and electrical performance to that of traditional silver flake. The coating process itself is tricky, as is the incorporation of the particles into a robust die attach formula, but both have been achieved and new SPC die attach pastes are now commercially available.

If you're a power device specialist, you may have avoided the silver conundrum as the dominant die attach materials used in this segment are lead-rich soft solders. But, the 2014 RoHS deadline for the elimination of lead in power packages is just a few short years away and alternatives to high lead soft solders must be decided sooner rather than later. Some high power applications have relied on silver (Ag) sintering technology to address certain thermal requirements and reliability needs, but traditional Ag sintering techniques have limitations. Specifically, because conventional Ag sintering processes need both heat and pressure to form the metal joint, unit volume has been severely limited. In some cases, throughput can be as low as 30 units per hour (UPH). Unique formulation techniques, however, have yielded an Ag sintering technology that does not require pressure and, therefore, can be cured in a standard batch oven process. With this ground-breaking technology, UPH as high as 6,000 can be achieved – a 200x improvement on traditional Ag sintering methodologies. What's more, new Ag sintering materials have thermal resistance and reliability performance that is impressive. Power cycling testing has revealed an improvement over solder by a factor of 10 and thermal conductivity and resistance are also superior to solder – plus, it's a lead-free formulation, so addresses the upcoming 2014 RoHs deadline. This is all welcome news for manufacturers of high power devices such as IGBTs, newer-generation LEDs and, frankly, any application that requires high thermal capability in high volume.

But, it's not just high power package developers that have seen die attach advances as of late. Those in the low- to medium-power space are also capitalizing on innovations in die attach materials. Historically limited to laminate-based, non-conductive processes, die attach films for leadframe applications are now market-ready. Similar to trends in the laminate device market, leadframe manufacturers are also dealing with thinner, smaller die and processing them using traditional paste-based die attach materials is often quite challenging. But, newly developed conductive die attach films are lending improved levels of process control to low- and medium-power devices. Not only do film-based formats add stability for today's ultra-thin wafers, but also provide for the elimination of die tilt, reduction in fillet width and better bondline control. With the fillet width reduction and a lower die to paddle clearance, designers now have far greater latitude and can develop more scalable designs, lending to more cost-efficient manufacturing. In fact, some of today's top device manufacturers have already proven these materials in-process and are benefiting from their performance.

So, to answer the question posed in the headline: Yes, there is a die attach for that…and that….and that! ◆

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ON THE COVER

15 & 17 MEPTEC will present two symposiums in November in association with SEMI. "2.5D, 3D Symposium – Bringing 3D Integration to the Packaging Mainstream" will be held on Wednesday, November 9, 2011. "Known Good Die – In an Era of Multi-Die Packaging and 3D Integration" will be held the following day, on Thursday, November 10, 2011. Both events will be held at the Biltmore Hotel in Santa Clara, California.

20 ANALYSIS – Using 3-D interconnection with TSVs creates a die stack with the shortest interconnection distance, enhances speed, lowers power consumption, and has a small form factor... all important features in the high demand world of small mobile devices connected to the Internet.

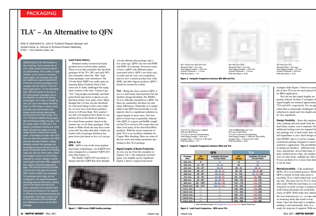
BY SANDRA WINKLER
NEW VENTURE RESEARCH

22 PROFILE – The true success behind STATS ChipPAC has been the Company's ability to transform itself into an industry leader with a competitive business model that is focused on technology differentiation, full turnkey assembly and test solutions, and operational excellence.

STATS CHIPPAC
MEMBER COMPANY PROFILE

26 PACKAGING – The TLA™ (Thermal Leadless Array) is a close cousin to QFN, yet a TLA design is extremely flexible and more often will meet the needs of a chip design and/or a board level requirement. Advantages include more I/O's, reduced package footprint, and design flexibility.

KELLY R. MCKENDRICK, SR. AND SERAFIN PEDRON, JR.
UTAC – UGS AMERICA SALES, INC.



29 TECHNOLOGY – Semiconductor process technology scaling has been the key driving force for component and system performance evolution in the modern high tech industry. Moore's Law has been the golden rule until recently.

BY JOHN Y. XIE, PH.D.
ALTERA CORPORATION

DEPARTMENTS

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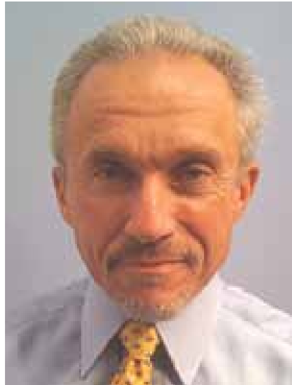
Meet the MEPTEC Advisory Board



Joel Camarda
SemiOps

IN THIS ISSUE WE CONTINUE introducing our fourteen Advisory Board Members. All Board members are listed at the left.

JOEL CAMARDA is an industry consultant, concentrating on manufacturing operations management and is also a Sr. Member Technical Staff for Amonix, a leading CPV system supplier. Joel is well known in the international packaging community via his work history of 30+ years in the USA and Asia. He has been active in IMAPS and is an advisor for MEPTEC. Joel has held several executive management positions: VP Operations at Sipex/Exar, President of K&S Flip Chip Technology, and Director of Worldwide Assembly and Packaging at Cypress Semiconductor. Joel started his career at National Semiconductor.

Phil Marcoux
PPM Associates

PHIL MARCOUX is one of many SMT and IC Packaging Pioneers. In 2007 he was named “The Father of US SMT” by the IPC. In 1981 he founded, AWI, the first US Company devoted exclusively to SMT which was later acquired by SCI Systems. In 1992 he founded, ChipScale, one of the first Wafer Level Packaging companies which developed a portfolio of over 36 patents. The patents are now the cornerstone of the camera modules commonly found in the current cell phones, computers, and games. Today, Phil is an active Business Development consultant in the area of 2.5D and 3D IC packaging infrastructure, design, and assembly. He is also an avid sea kayaker.

Bhavesh Muni
Dow Electronic Materials

BHAVESH MUNI is currently Global Marketing Manager for Dow Electronic Materials’ Advanced Packaging Technologies business and is responsible for the strategic marketing of the semiconductor packaging materials segment. Mr. Muni brings more than 23 years of experience in electronic materials covering all aspects from concept to commercialization of innovative materials for electronics assembly and semiconductor packaging. Prior to joining Dow, Mr. Muni worked with leading electronic material suppliers, such as Henkel Electronic Materials, Lord Corp., Emersion & Cuming and Olin Hunt Conductive Materials, and has held various positions covering global business development. Mr. Muni has presented & published several papers on the importance of the semiconductor packaging industry.

Fab Equipment Spending up 23% in 2011 – Still Highest on Record

The SEMI World Fab Forecast indicates that capital expenditure will increase to $41.1 billion in 2011, the highest on record. This new prediction is revised downwards to a 23% increase (from 31% increase predicted in May 2011), as some companies have adjusted plans due to broader economic conditions. Although 2012 spending will decline, the total for 2012 may still be the second highest on record. In 2011, SEMI counts 223 facilities spending on equipment. Of these, 77 projects are for LED dedicated facilities. Next year, 190 facilities will start or continue equipping, with 72 LED projects. Over the last few months, some companies announced cuts in capex for 2011, but for a number of companies, capex plans remain unchanged. Some announced even slight increases, though caution is becoming more apparent in the market. Visit SEMI at www.semi.org. ◆

MEMBER NEWS

2011 ELECTRONIC DESIGN’S SURVEY RANKS INTERSIL AS ONE OF THE TOP EMPLOYERS

Intersil Corporation has been ranked 14th in the Electronic Design annual top 50 electronic design companies survey. From a total of 97 U.S. technology firms, Intersil moved forward by 37 positions from the publication’s 2009 survey. Electronic Design annually assesses the top companies in the electronics industry to measure overall economic conditions and identify the specific strategies that lead to success. The publication selected the top 50 companies based on criteria ranging from sales growth and operating profit growth to the number of patents issued to a company and its total long term debt. *www.intersil.com*

NEW PLEXUS MANUFACTURING FACILITY ON SCHEDULE

The construction of **Plexus**’ fourth manufacturing facility in Penang, Malaysia is on schedule for completion in Q1F12. The 37,000 square foot facility will bring Plexus’ total Asia Pacific footprint to 1.3 million square feet. The new facility will feature a two-story manufacturing area and a three-story office area. Production is expected to begin on the first floor in August 2011, with the remaining manufacturing and office space to be completed and occupied by November 2011. *www.plexus.com*

CARSEM RECEIVES BEST SUPPLIER OF THE YEAR AWARD

Carsem announced that, for the second year in a row, it has received Microsemi Corporation's Best Supplier of The Year Award for assembly and test services that were provided by the Carsem factory located in Suzhou, China. The award is based on Microsemi's supplier program that measures key metrics such as, on-time delivery, yield, customer service, quality, competitiveness, responsiveness and technology.
www.carsem.com

ISOCYANATE-FREE ADHESIVE SETS BENCHMARK IN THE FLEXIBLE PACKAGING INDUSTRY

Flexibility – not only with regard to packaging, but also along the value chain – is one of the key benefits offered by the latest **Henkel** innovation Liofol Fast One. The new one-component laminating adhesive features an extremely fast cure, combined with high initial bond strength. At the 7th ICE Europe in Munich, Henkel presented the first-ever laminating adhesive that contains no free isocyanates: Liofol Fast One LA 1640-21.
www.henkel.com

$325 MILLION CREDIT AGREEMENT

Intersil Corporation announced that it has executed a new five year $325 million revolving credit agreement, which replaces the current long-term debt. The after-tax interest rate will be approximately two

▶▶

Amkor Announces Availability of First Ever QFN Package Design Kit for Agilent Technologies' Advanced Design System Software

AMKOR TECHNOLOGY, Inc. has announced the availability of its Quad Flat No-Lead (QFN) package design kit for Agilent Technologies' Advanced Design System (ADS) electronic design automation software. This innovative package design kit is the first ever available for ADS.

Based on Amkor's popular MicroLeadFrame® (MLF®) packages, the package design kit enables mutual Amkor and Agilent customers to significantly improve their RFIC/MMIC design quality and time-to-market. It allows designers to quickly explore various design specifications with accurate package information and implement optimized RFIC/MMIC designs, providing a greater range of choices and more flexibility when designing QFN packages.

"Our customers demand ever-increasing design effectiveness and efficiency to achieve their business objectives with today's sophisticated QFN packages," said ChoonHeung Lee, Amkor Technology Korea's corporate vice president and chief technology officer. "As Agilent is the RF and microwave CAD leader and many of our customers already use ADS for circuit design and characterization, we are excited to offer this first ever package design kit to our mutual customers."

"Our customers are looking for easy ways to accurately characterize vendor-supplied packages, both alone and with ICs and laminates mounted," said Todd Cutler, planning and marketing senior manager with Agilent's EEsof EDA organization. "Amkor is one of the world's leading outsourced assembly and test services providers, and we are extremely pleased with this package design kit. This collaboration between Amkor and Agilent delivers significant benefits for our mutual customers, and illustrates our aligned focus on meeting customer needs."

The Amkor package design kit contains models for 3x3, 4x4, 5x5, and 6x6 MLF® QFNs. All die are scalable, and their material properties can easily be modified. The Amkor package design kit also includes scalable models for bond pad arrays and board via arrays. The Amkor package design kit was developed for use with ADS 2009 Update 1 and ADS 2011.01.

Customers can request the QFN Package Design Kit from the Amkor website at www.amkor.com/go/ads. ◆

Unisem Chooses LTX-Credence's PAx RF Test System for WLAN, WiMAX, Bluetooth and Other Front End RF Devices

KUALA LUMPUR, MALAYSIA – UNISEM has announced the addition of LTX-Credence's PAx RF Test System to its U.S-based test development center located in Sunnyvale, CA. This system is a "super set", fully loaded with all the features the PAx test platform has to offer for cost effective test development and production test of the latest generation of front end RF devices.

LTX-Credence's new test system has been specifically developed to address the high volume manufacturing test challenges of suppliers of advanced front end RF devices such as Multiband RF Power Amplifiers, RF Front End Modules, RF Analog System in Package and RF discrete devices. Leveraging the X-Series XRF test instrumentation, the PAx enables cost effective, high-volume performance testing of advanced front end RF devices used in applications utilizing WLAN, WiMAX, GSM, Edge CDMA, WCDMA, LTE, Bluetooth or other RF signaling standards.

"The RF front end device market is being driven by three key dynamics: higher levels of functionality, high unit volume growth and constant pricing pressures. The PAx has been developed to meet the challenges caused by these dynamics," commented John Shelley, product director, LTX-Credence. "We are excited that Unisem's Sunnyvale test development center has chosen the PAx platform to serve as the tester of choice for this market segment."

LTX-Credence is a global provider of ATE solutions designed to deliver value through innovation enabling customers to implement best-in-class test strategies to maximize their profitability. Additional information can be found at www.ltxc.com.

For more information about Unisem visit its website at www.unisemgroup.com. ◆

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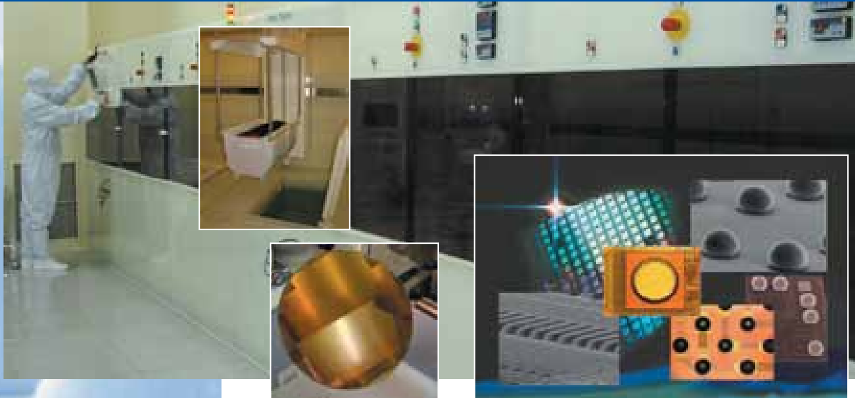

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SEMI Names Dennis P. McGuirk President and CEO

SEMI has announced the appointment of Dennis "Denny" P. McGuirk as president and CEO, effective November 14, 2011. McGuirk succeeds Stanley T. Myers, who led SEMI for the past 15 years and has served on its board of directors since 1986. Myers announced his plans to retire in April and the SEMI International Board of Directors subsequently initiated a globally comprehensive search process which identified several highly qualified individuals. McGuirk served for 12 years as the president and CEO of IPC – Association Connecting Electronics Industries®. IPC is a global trade association serving 3,000 member companies involved in printed board design and manufacture, electronics assembly and test. ◆

percent.

"Our business model and history of strong free cash flow allowed us to obtain very favorable terms," said Jonathan Kennedy, Senior Vice President and Chief Financial Officer. "The new facility will reduce our cost of capital while providing flexibility to pursue our business objectives."

www.intersil.com

NEW HIGH-END LAB ACOUSTIC MICROSCOPE SYSTEM

Sonoscan, Inc. announced the availability of the Gen6™ C-SAM® acoustic micro imaging system at Semicon West in San Francisco on July 11. The Gen6 incorporates new and upgraded capabilities building on its well-known predecessor, the Gen5™. While the Gen6 maintains the highly-praised look of the Gen5™, the electronics and operating system are on a completely redesigned platform.

www.sonoscan.com

INVENSAS UNVEILS MULTI-DIE FACE-DOWN PACKAGING TECHNOLOGY

Invensas Corporation, a wholly-owned subsidiary of Tessera Technologies, Inc., announced that it will demonstrate the dual-face down (DFD) implementation of its new multi-die face-down (xFD) packaging technology at the Intel Developer's Forum (IDF) in San Francisco September 13-15, 2011. xFD is a novel multi-die, wirebond-based packaging technology that

mounts integrated circuits (ICs) upside down and staggers them in a shingle-like configuration, incorporating short wirebonds in a structure similar to that of a window-BGA package.
www.invensas.com

XILINX SPARTAN-6 FPGAS USED IN NEWEST LINE OF SIGMA DIGITAL CAMERAS

Xilinx, Inc. has announced that longtime customer, SIGMA Corp., has designed Spartan®-6 FPGAs into its flagship digital single lens reflex (DSLR) camera, the SIGMA SD1, for professional and enthusiast photographers. Shipping since June, the new 46-megapixel camera delivers robustness in a splash-proof and dust-proof body, providing high-definition and high resolution images.
www.xilinx.com

ASE RISES TO THE TOP OF THE LIST

Advanced Semiconductor Engineering Incorporated (ASE) was honored by Business Next Magazine in the publication's special edition of the "Asia Info Tech100". In this year's judging for Taiwan's Top 100 Tech Enterprises and Asia's Top 100 Tech Enterprises, ASE was ranked number 3 and number 6 respectively. In the category of Taiwan's Top 100 Tech Enterprises over 700 publicly listed Taiwanese tech companies were evaluated. In the category of Asia's Top 100 Tech Enterprises, over 2000 publicly listed companies from 9 countries in the Asia region were evaluated.
www.aseglobal.com ◆

Altera Ships World's First 28-Gbps-Enabled FPGA for Next-Generation 100G Systems and Beyond

Industry's Highest Performance FPGA Featuring 28-Gbps Transceivers Enables Higher Throughput, Increased Performance and Reduced Power in High-End Applications

ALTERA CORPORATION HAS ANNOUNCED it has started shipping the world's first FPGA featuring 28-Gbps transceivers. Stratix® V GT devices are the industry's highest bandwidth and highest performance FPGAs available today. The industry-leading technological innovations in Stratix V GT FPGAs are tailored to enable designers of leading-edge communications systems to quickly bring to market solutions that support the ever-growing demand for network bandwidth.

Stratix V GT FPGAs support the rapid growth in network traffic being driven by Internet and Internet Protocol (IP)-based services and applications. Innovative companies like JDSU leverage Altera's solutions to get early access to the most advanced technologies for use in their next-generation test and measurement solutions.

Stratix V GT FPGAs integrate over a decade of internally developed transceiver technology innovations into the industry's highest performance 28-nm process technology (28HP). The devices support backplane, optical module and chip-to-chip applications through four 28-Gbps transceivers, 32 full-duplex, 12.5-Gbps transceivers, and up to 4x72-bit DIMM DDR3 memory interfaces supporting 2133 Mbps. The 28-Gbps transceivers featured in Stratix V GT FPGAs meet the CEI-28G specification while consuming only 200 mW per channel, dramatically reducing a system's power-per-bandwidth profile. A video showing the transceiver performance of Stratix V GT FPGAs titled "*Sneak Peek: Industry's First 28-Gbps FPGA*" is available for viewing on Altera's website.

Engineering samples of Altera's Stratix V GT FPGAs are available today. For additional information visit www.altera.com/stratix5 or contact your local Altera® sales representative. ◆

SEMI Co-Sponsors Conferences Addressing Known Good Die (KGD) and 3D Packaging Challenges

INDUSTRY EXPERTS WILL gather at the annual Known Good Die (KDG) conference to address the mounting challenges in semiconductor die product test, assembly, manufacturing and business. The conference – organized by MEPTEC and co-sponsored by SEMI – focuses on "KGD in an Era of Multi-Die Packaging and 3D Integration." The event will be held on November 10, 2011 at the Biltmore Hotel in Santa Clara, California, and is co-located with another MEPTEC conference, "2.5D, 3D and Beyond: Bringing 3D Integration to the Packaging Mainstream," set for November 9.

"Mobile consumer products including tablets and smart phones are driving adoption of multi-function 3D, vertically stacked or multichip packages to meet demanding performance and form factor requirements," states Jonathan Davis, president of the Semiconductor Business Unit at SEMI. "The increasingly complex configurations and packages require high-quality known good die to ensure product functionality and cost performance. We are pleased to support MEPTEC in presenting this important event as the industry addresses the challenges of 3D integration."

For 18 years, the KDG conference has marshaled technical experts, managers and business development professionals from around the world for an interactive exchange on the latest developments in the die product industry.

The KGD conference sessions will cover such topics as KGD test, handling, delivery, standards, current methods, options and infrastructure.

For more information on both conferences visit www.meptec.org. ◆

GLOBALFOUNDRIES

GLOBALFOUNDRIES and Amkor to Collaborate on Advanced Assembly and Test Solutions

GLOBALFOUNDRIES AND Amkor Technology, Inc. have announced that they have entered into a strategic partnership to develop integrated assembly and test solutions for advanced silicon nodes. The companies plan to collaborate to co-develop and commercialize integrated fab-bump-probe-assembly-test solutions aimed at multiple customers and end-market applications and expand their lead-free bump licensing relationship. Through the partnership, Amkor would become a founding member of GLOBALFOUNDRIES' new Global Alliance for Advanced Assembly Solutions, which is designed to accelerate innovation in semiconductor interconnect, assembly and packaging technologies. By joining forces, GLOBALFOUNDRIES and Amkor plan to extend the ecosystem to address growing market needs, while bolstering their ability to deliver end-to-end solutions for customers at advanced technology nodes.

Amkor and GLOBALFOUNDRIES have also recently expanded their prior lead-free wafer bump licensing relationship by amending their existing lead-free bumping technology license agreement.

As the industry moves aggressively to more advanced technology nodes, innovation in interconnect, assembly and packaging solutions is becoming increasingly important. Supply chain management has become a critical topic, as the ability to enable innovative packaging techniques can lead to improvements in performance and power-efficiency as well as reduced costs for chip designers. At leading-edge nodes, the adoption of three-dimensional (3D) stacking of integrated circuits is increasingly being viewed as an alternative to traditional technology node scaling at the transistor level. As new technologies such as this are introduced, the complexity of chip-package interaction is going up significantly and it is increasingly difficult for foundries and OSATs to be able to deliver end-to-end solutions that meet the requirements of the broad range of leading-edge designs.

The partnership between GLOBALFOUNDRIES and Amkor will enable the supply chain to better meet these diverse requirements and deliver robust and reliable solutions to mutual customers.

Launched in March 2009 through a partnership between AMD and the Advanced Technology Investment Company (ATIC), GLOBALFOUNDRIES provides a unique combination of advanced technology, manufacturing excellence and global operations. With the integration of Chartered in January 2010, GLOBALFOUNDRIES significantly expanded its capacity and ability to provide best-in-class foundry services from mainstream to the leading edge.

GLOBALFOUNDRIES is headquartered in Silicon Valley with manufacturing operations in Singapore, Germany, and a new fab under construction in Saratoga County, New York. Visit www.globalfoundries.com for more info. ◆

OPTOSEM Technologies
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OPTOSEM TECHNOLOGIES SDN BHD was established in Johor, Malaysia in 2002. The company specializes in the design and molding of Open Cavity IC Packages. Development in Injection Molding of QFN packages open up the market for MEMS and other Open Cavity products and application, and creating new opportunities and solution for its customers..
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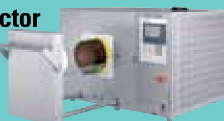

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MEMS TECHNOLOGY

By Mårten Vrånes

MEMS Testing Strategies: 3D Stacked Devices

RAPID ADOPTION OF MEMS devices in high growth consumer markets, fuelled by innovative application developers and consumers' constant hunt for the next "cool thing" in handheld electronics, is challenging MEMS companies to produce the next generation products' form factor, functionality, and unit price. Competition in the marketplace is further tightening up as new start-ups with disruptive technology are entering the market. Further, established semiconductor companies also have intentions to leverage their prior semiconductor knowledge and take advantage of their existing customer base to provide a wider product portfolio and value-added chipset offerings. Market-driven product requirements and expectations include an increased focus on quality, lower unit price, lower power consumption, smaller form factor, and added functionality. Three-axis accelerometers are currently being offered at below $0.5 per unit for high volumes, magnetometers are following suit and so will other MEMS devices on their path to commoditization.

In their answer to the aggressive market forces, MEMS companies are striving to integrate multiple sensor modules, and provide fully tested and calibrated system-in-a-package (SiP) solutions. Market leaders are already integrating several sensor modules in combo products, such as motion sensor combos, or motion and magnetometer combos, with a total of 6 or 9 degrees-of-freedom (DOFs). With an addition of an altimeter, one has a 10 degree-of-freedom dead reckoning system for navigation applications. With so many DOFs and increasingly stringent form factor requirements, the integration into smaller footprint devices is a key to success. Whether it is wafer stacking using intricate wafer bonding technologies, or die stacking using flipchipping or wirebonding, 3D stacking of MEMS is definitively of the major trends in the MEMS industry.

Adding multiple sensor functions into a single package excites the marketing executives, as it also poses tough challenges to test engineers. Given that each individual sensor combo system needs to be tested by applying physical stimuli during production testing, different sensor combos will require different sets of test criteria and often entirely different test systems. It is often not practical to integrate several different test stimuli in one test system, such as pressure and motion stimuli. Further, it can be highly uneconomical to purchase separate test systems for each product variant. Established companies are at an advantage here as their wide product offerings and deep pockets allow them to establish entire test floors in anticipation of high production volumes. If done right, test systems can be used across different product ranges – for example, testing the motion sensors in one system and the pressure sensor (altimeter) in a separate system. This allows accelerometer-pressure sensor combos and gyro-pressure sensor combos to share test systems, should these products be developed and sold separately. Finally, the use of identical packages for different sensor combos, such as a 3x3x1mm QFN, can allow companies to avoid frequent and potentially time consuming test system changeovers.

Monolithic MEMS and ASIC die solutions, either by 3D wafer stacking or single-wafer processing, enables the ability of doing a one-pass electrical probe covering both the analog and digital circuitry. This is an advantage over discrete components that are separately probed. The advantage is a shorter overall test time, one type of probe card and one probe setup. Further cost savings include lower overhead and single die assembly. The flipside of the one-pass probe approach is the effect of value-added yield loss where a failed die will result in rejecting the entire chip with all of its functionality. This effect propagates with systemic wafer processing defects, often seen with micromachined sensors, as these processes are not always as mature as standard semiconductor processes. Discrete components that are probed separately allow discretionary rejection of MEMS and CMOS die without the compounding value of one or the other. A similar effect can be observed at final test where added complexity through added functionality can increase the occurrence of failures. This effect is not typical for monolithic

continued on page 12

INDUSTRY INSIGHTS

By Ron Jones

Japan ... Six Months After

SEPTEMBER 11, 2011, MARKS NOT only the 10 year anniversary of the terrorist attacks on the US but also the 6 month anniversary of the Tohoku Earthquake and Tsunami which has had a disastrous effect on the Japanese people and a major impact to business worldwide.

It's hard to comprehend the scale of the event. The earthquake had a magnitude of 9.0 Mw with duration of 6 minutes. It is the 4th largest world quake since recording began in 1900. To get a sense of the relative magnitude, the Loma Prieta (World Series) Quake was a 6.9 and lasted for 15 seconds. The Tohoku quake was 125x stronger and lasted 25 times longer. The quake must have seemed like the imminent end of the world to many, being so strong and lasting so long. Many probably heaved a sigh of relief when the quake stopped, only to have the horrific waves come, some as high as 130 feet.

The government has reported 15,741 deaths with another 10,000 either injured or missing. Hundreds of thousands were evacuated and scores of thousands of people remain displaced. There was widespread flooding, landslides, fires, damage to buildings and infrastructure, and impacts to nuclear and conventional power.

The human drama of the impact to the people and the unfolding chronicle of nuclear reactor damage captured the attention of the news media for weeks. On the business side, every company whose supply chain intersected with Japan began looking at potential implications. Several key commodities that are basic to semiconductor devices such as BT Resin and Si wafers were all the talk, as a high percentage come from the impacted region.

EE Times publishes their "Week in Review" newsletter each Friday, listing the top ten articles from the week. On the first three Fridays after the quake, over half the articles were related to the Japanese disasters. By week four, it had dropped to two. Then the number in the top ten dropped to zero, where it has remained for months.

Most disruptions did not occur in a cataclysmic (read newsworthy) fashion; rather things slowed down, forecast continually changed, lead times extended, allocations were put in place, etc. It was very difficult to get any public info on anything. We issued a newsletter to this effect titled "The Silence is Deafening." Most companies, fearing impact to stock prices, allocations, etc. just stopped talking. It was harder to get a public announcement on the impact than a copy of Obama's transcript from Columbia.

Though outwardly things were quiet, on the inside, there was a feverish pitch up and down the supply chain. Take the BT resin shortage. It impacts, in order, the substrate manufacturer, the BGA package manufacturer, the OSAT that assembles and tests, the fabless company, the EMS that assembles the end device, the end device company and the consumer. Laminates that previously had lead times of 6 weeks were now running 12-14 weeks. People were on long hours, 7 days a week. Every customer wanted to know what, when, how much and answers weren't forthcoming. Things were changing hourly as a shortage on another component could ripple through demand. The fact that not much was being reported did not mean that everything was OK. No news was not good news, it was no news.

It has now been six months since the events of March 11. The lingering effects seem to very dependent on where you are in the supply chain and factors such as which markets you serve. There never seemed to be a big impact on wafer fabs and die supply other than ones that were actually hit by the quake. Fabless companies that employ simple packages seem to be OK while some that use complex BGA's may still be on allocation. Companies are still being impacted by the total supply of all components to their customers with their demand fluctuating because of supply issues with other parts.

I think the conventional wisdom is that things should improve daily, which generally it is. Because the power infrastructure has not been fully recovered, however, the hot summer season in Japan could cause some unexpected disruptions even now. Like the past, I wouldn't expect them to be cataclysmic, but could have an impact.

As those of you that subscribe to my newsletter know, I thought the impact to our industry and the world economy would be much greater than it was. I am very glad to say that I was wrong. I think this is a testament to the level of planning and control we in the high-tech sector employ. Those that know me well know that I am a huge proponent of using systems to help manage our complex environment. I think having those systems in place has allowed us to react more quickly and accurately than we would have even a few years ago.

The open question is what, if any, changes will be made to inventory and supply chain policies going forward. The natural sequence is initial overreaction, which dissipates over time, finally leading to practices that are too weak. The way we have made it through this calamity gives hope for the future. Upgrades to the current policies and procedures could well give us an even more robust environment that is both cost effective and sustainable over time.

The wild card is that the next event could have a totally different profile. Something that negatively impacted all the wafer fabs in Hsin-chu, for instance, would be quite a different animal. Let's hope for the best . . . but plan for something a bit less. ◆

RON JONES is CEO and Founder of N-Able Group International. Visit www.n-ablegroup.com or email Ron at ron.jones@n-ablegroup.com for more information.

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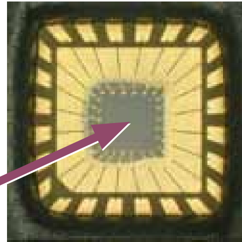

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MEMS TECHNOLOGY continued from page 10

devices, but encompasses all complex system-in-a-package (SiP) devices.

Low throughput attributed to slow physical test stimuli can be compensated by faster handling, higher parallelism, and more aggressive and innovative methods of applying physical stimuli, such as electrically excited MEMS motion sensors or dynamically changed magnetic fields for magnetometers to test functionality without the need to physically move the device. In addition, fewer test points and reliance on statistical data to predict calibration coefficients, by look-up tables or otherwise, can be used to shorten test times while maintaining product specifications and quality. MEMS test engineers and system manufacturers will need to use every trick in the book to keep up with the aggressive test cost targets. At the same time, the more comprehensive test systems developed in support of combo MEMS products will likely cost more, not less. This trend is quickly becoming the biggest hurdle for MEMS test cost optimization. ◆

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MÅRTEN VRÅNES is the Director of MEMS Testing and Reliability at MEMS Investor Journal's Consulting Services Group. Mr. Vrånes has a long track record in the area of MEMS testing at SensoNor, LV Sensors and Consensic. For further questions about MEMS Investor Journal's consulting services, please contact us at mvraanes@memsinvestorjournal.com.

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May 15–16, 2012	SEMICON Russia	Moscow, Russia
July 10–12, 2012	SEMICON West	San Francisco, California
September 5–7, 2012	SEMICON Taiwan	Taipei, Taiwan
October 9–11, 2012	SEMICON Europa	Dresden, Germany

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November 9–11, 2011	SOLARCON India	Hyderabad, India
December 5–7, 2011	PVJapan	Chiba, Japan
March 20–22, 2012	SOLARCON China	Shanghai, China
May 15–16, 2012	SOLARCON Russia Conference and Pavilion	Moscow, Russia
June 13–15, 2012	Intersolar Europe	Munich, Germany
July 10–12, 2012	Intersolar North America	San Francisco, California
October 3–5, 2012	PV Taiwan	Taipei, Taiwan

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2.5D, 3D Symposium

Bringing 3D Integration to the Packaging Mainstream

Wednesday, November 9, 2011
Biltmore Hotel, Santa Clara, California

This event will be co-located with the MEPTEC KGD Symposium to be held on November 10. Discounts are available for attending or exhibiting at both events.

INTERCONNECTING DIE with Through Silicon Vias (TSV) in a 3D format or through a silicon interposer in a side-by-side "2.5D" format is rapidly moving from the roadmap to the factory floor. Larger, vertically integrated and volume driven companies are already productizing "Killer Apps", notably stacked memory. A broad swath of ASIC, ASSP, FPGA and standard product manufacturers and consumers are beginning to imagine new products which leverage these technologies to address opportunities in their markets. These opportunities include solving latency and bandwidth issues in high end systems, the combination of different silicon processes or the combination of disparate functions such as MEMS, image sensors and optics.

This symposium will discuss these new products, emerging standards and will address the issues of Design, Modeling, Supply Chain and Manufacturing that face new entrants to 3D integration and what it will take to bring this technology to the Packaging Mainstream.

Of course, once the Design, Modeling, Supply Chain, Sourcing and Manufacturing issues are addressed there remains a rather large elephant in the room – the issues of testing thousands of miniaturized interconnects on combinations of internal AND 3rd party silicon such that the electrical yield of the assembled system is close to 100%. These issues are collectively referred to as Known Good Die (KGD). ◆

The Biltmore Hotel is conveniently located at 2151 Laurelwood Road in Santa Clara, CA in close proximity to the San Jose Airport.

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Symposium Chair

Ivor Barber, Director, Package Design and Characterization
LSI Corporation

Session Chairs

Sai Ankireddi, Package and Assembly Engineering
Intersil Corporation

Yeong Lee, Director, Wafer Scale Products
STATS ChipPAC

David Towne, Director, Advanced ASIC Value Chain Technologies
Cisco Systems, Inc.

John Xie, Sr. Manager, Packaging Technology Dept.
Altera Corporation

Technical Sessions:

- **Session 1:** 2.5/3D Packaging: Why Do We Need It? – Drivers and Solutions
  Chair: David Towne, Cisco Systems, Inc.

- **Session 2:** Advanced 2.5D/3D Assembly Process Technologies
  Chair: Yeong Lee, STATS ChipPAC

- **Session 3:** Thermal, Power Distribution and Reliability Interactions in 2.5/3D Packaging – Modeling & Simulation
  Chair: Sai Ankireddi, Intersil Corporation

- **Session 4:** Standards and Supply Chain Development
  Chair: John Xie, Altera Corporation

KEYNOTE

ChoonHeung Lee

Emerging Approaches to 3D Integration

ChoonHeung Lee, Head of Corporate Technology HQ, Amkor Korea Technology Inc.

3D-TSV integration is attracting attention as a vehicle for high performance, versatile functionality and lower power consumption with lower foot-print. There are many collaborating activities for 3D-TSV integration technologies across the semiconductor industry including mobile, memory, and networking segments. But it is not too early to say it is coming for various reasons of maturity of basic platform, balanced cost-performance, etc. Silicon Interposers are currently being introduced (2.5D approach), both as a system level solution or as an intermediary step before going to full 3D-TSV integration. The silicon interposer uses bare silicon substrate with TSV technology to enable higher density interconnections. The silicon interposer is mounted with different devices using conventional mass reflow or TCNCP technology. Another aspect to be considered is the supply chain of the 2.5D business. The complexities and the ownership of liabilities due to different reasons will be discussed.

ChoonHeung Lee joined Amkor in 1996 as the team manager of Simulation Team and Advanced Product Development Team. In 2010 he became the Head of Corporate Technology HQ, Amkor Korea Technology Inc. ◆

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- Current and Future Bare Die Issues
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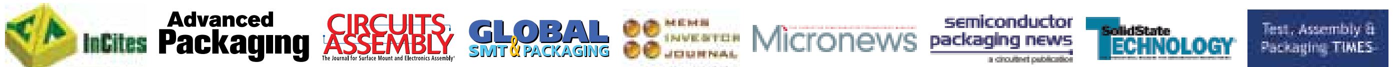

Known Good Die Symposium

Thursday, November 10, 2011
Biltmore Hotel, Santa Clara, California

This event will be co-located with the MEPTEC 2.5D, 3D Symposium to be held on November 9. Discounts are available for attending or exhibiting at both events.

THE ANNUAL KNOWN Good Die (KGD) event is the leading source for information on semiconductor die products test, assembly, manufacturing, and business issues at the forefront of the microelectronics industry. Formerly known as the KGD Workshop, this year's conference, run by MEPTEC and co-sponsored by SEMI, will be co-located with another MEPTEC event 2.5D, 3D and Beyond - Bringing 3D Integration to the Packaging Mainstream on November 9.

Today's applications in portable consumer electronics and mobile phones require small form-factors by combining multiple functions into single, vertically stacked or multi-chip packages. Despite the benefit at the end applications, these complex package techniques are challenging and require high quality known good die to insure the success of SIP, PoP and MCP design and manufacturing.

The conference will bring together technical experts, managers and business development professionals from around the world for an interactive exchange of information on the latest developments in the die product industry. Over the years of the KGD Workshop participants helped to shape the evolution of KGD packaging from an early focus on specialized high performance systems to the successful low-cost solutions enabling the portable world. This year's conference will have a special focus on the challenging issues for KGD as the industry moves toward 3D packaging technologies. Sessions will cover such topics as KGD test, handling, delivery, standards, current methods, options and infrastructure. ◆

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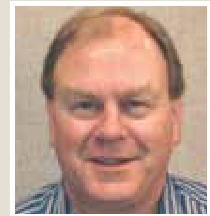
KEYNOTE



Ivor Barber

KGD is Cool Again

Ivor Barber, Director, Package Design and Characterization LSI Corporation

The surging industry interest in 2.5/3.5D packaging with its promise of "Much More than Moore" silicon integration through the stacking of heterogeneous silicon products in a single package has made KGD a critical discipline for established and new players in the semiconductor industry. Familiar themes of supply chain, testability, fault coverage, IP protection and failure analysis vie with newer concepts of wide I/O testing, very high density microbumps, wear out mechanisms and even the recognition that everything cannot be tested leading to system level concepts of redundancy, fault tolerance and error correction. In the era of 2.5D/3D the goals of a robust KGD strategy must move beyond the "how to test" and the "what to test" to include mitigation of what cannot be tested.

Ivor Barber graduated from Napier University in Edinburgh, Scotland in 1981 with a Bachelors degree in Technology. He has worked in package assembly and design at National Semiconductor, Fairchild Semiconductor and VLSI Technology. Ivor has spent the last 21 years at LSI Corporation in Milpitas in various Engineering and Management positions in Assembly, Package Characterization and Package Design. Ivor is currently Director of Package Design and Characterization at LSI Corporation. Ivor holds 12 US patents related to package design. ◆

Throughput: The Driving Force in the Development of Improved Metallization Materials

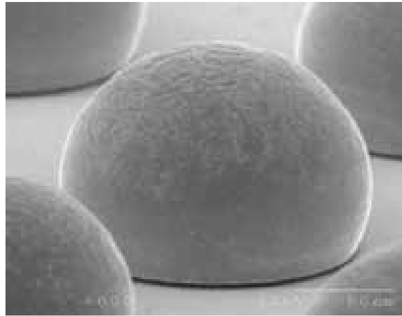
Mike Rousseau
Dow Electronic Materials

FROM THE BEGINNING OF THE industry, metallization has been a cornerstone of electronics. As the conduit through which data flows, the importance of metallization in electronic devices still holds today. Whether it is for the transistors or copper interconnect in semiconductors, package-on-package, system-on-chip, or chip-to-board packaging, or across the circuit boards and into I/Os, metallization is at the center of the processing necessary to manufacture electronic devices.

Metals, which are seemingly basic elements, have been continually adapted through the evolution of electronics, which has required continual innovation. We are currently in an era in which chip packaging is increasingly responsible for better performance and more functionality in consumer electronics. This drive towards better performance is predicated in large part on innovation in metallization that directly enables substantial performance improvements in chip packaging, which includes higher I/O speeds, easier, more efficient stacking, more compact designs with smaller form factors, and, of course, 3D packaging.

The requirements for increased feature density and reduction in feature size to achieve improved package performance are putting demands on materials and processes that are challenging. Additionally, there is intense pressure to improve the cost position of materials for advanced packaging to challenge traditional wiring bonding processes' hold on the position as the low-cost option, and this challenge is largely being addressed by pushing improvements in throughput.

Two of the metallization applications that are focus areas for advanced packaging improvements, wafer bumping and copper pillars, have already had enormous impact on package performance. While wafer bumping has been in use for quite some time, the push for lead-free options along with the capability to form structures with more demanding size and density requirements has been an industry-wide challenge. In 2009 Dow Electronic Materials introduced a solution, SOLDERON™ BP TS 4000 Tin Silver, which can be applied to a wide current density range – as high as an industry-leading 12 ASD (6 μm/min. plating rate) – and capable of 30 μm features at a 1:2 pitch with void-free deposits and excellent morphology.



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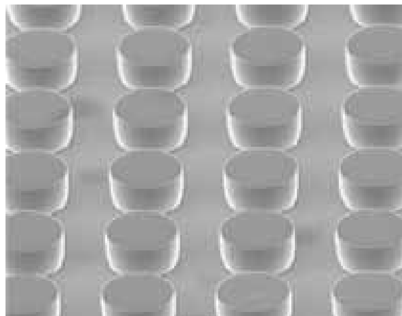


30 μm Micro Pillars

Impressive performance for a lead-free material, however, wider adoption requires addressing continuing challenges. Delivering a material capable of higher current density is a must to maximize tool utilization and offset the cost of the requisite low-alpha emitting tin. The speed cannot come at the cost of quality – smooth, fine-grain and void-free deposits at a variety of pitches for applications such as in-via bumps, mushroom bumps and cap plating must be maintained.

Within wafer (WIW) and within die (WID) variations need to be controlled, hitting ≤10% WIW and ≤5% WID targets. To manage in-process material and maintain throughput, improved industry metrology and analytical techniques are being developed, thus enabling analysis of all bath components either off-line or in-situ to maintain precise control.

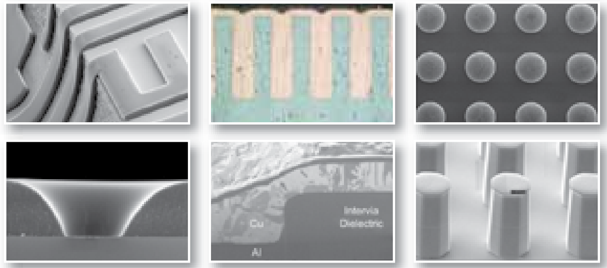
Dow Electronic Materials was also an early supplier for electroplating copper for pillars with INTERVIA™ 8540 Copper for applications that require higher interconnect densities than is possible through bumping. Next-generation materials are under development to meet the future industry throughput targets as high as 20 ASD (5 μm/min. plating rate) with flexibility for plating a large variety of pillar, bump and redistribution layer (RDL) sizes, pitches and thicknesses. Feature sizes will vary from 20-150 μm pitch for 20-70 μm pillars at a height of 15-75 μm to accommodate everything from conventional pillar structures to micro pillars.

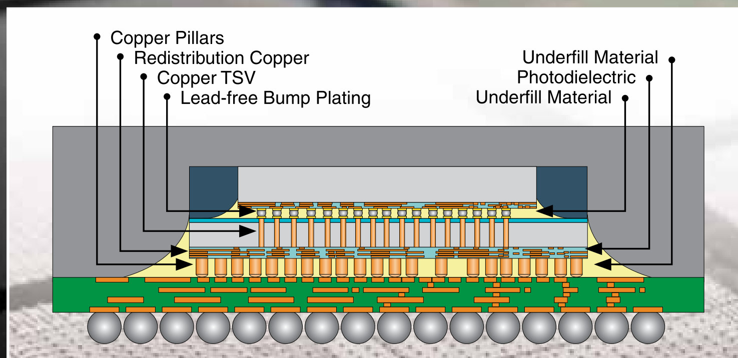
An important aspect to control with pillar structures is doming to achieve flat, dished or slightly domed features, depending on the design specifications. Dow's next-generation INTERVIA copper product is targeting improved total indicated runout (TIR) with even tighter control of doming characteristics. TIR ranges of 0-5% will satisfy many of the most-demanding specifications while maintaining 5-10% WIW and 1-5% WID requirements. Our sulfuric-acid based materials are also compatible with other capping materials, such as Sn alloys, with good adhesion.

Dow Electronic Materials is driving development of the metallization materials needed at the next advanced packaging technology horizon, addressing the increasingly demanding specifications calling for fine pitch features with tighter control. The driving force along the way, however, is increased throughput to maximize yields and tool utilization. ◆

With Innovation Comes Revolution

Leading-edge packaging schemes are spurring a revolution in electronics. Dow Electronic Materials is there with a wide range of innovative metallization, dielectric, lithography and assembly materials – all delivered with global support from technical labs positioned close to customers. These are the innovations that drive the revolution.





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Through the Silicon

Sandra Winkler
New Venture Research

3-D PACKAGES

In today's electronics, smaller, faster, lighter, and less energy consumption are desirable characteristics. Moving to stacked packages and SiPs puts devices in closer proximity, thus helping to realize these characteristics.

Stacked packages are multichip packages in which the die are placed vertically. They can be electrically interconnected in several ways, one of which is with through-silicon vias (TSVs). This interconnection style utilizes vias that go through the silicon to electrically connect one die to the next in a vertical stack, in place of wire bonds or other forms of connection.

Use of TSVs is known as a 3-D interconnect. This differs from 3-D packages, in which devices are stacked up vertically, without going through the silicon. The interconnect method in that case would be wire bond or some other method of electrical connection.

Using 3-D interconnection with TSVs creates a die stack with the shortest interconnection distance, enhancing the characteristics of high speed, low power consumption, reduced parasitics, and small form factor. In a world in which small mobile devices connected to the Internet are in high demand, these are important features. By moving to 3-D interconnection, the device can achieve 100 times the connectivity or bandwidth, with less power consumption. With lines and traces on the silicon die moving to 45-, 32-, and 22-nm lithographies, utilizing TSVs is a way for the back-end interconnection to keep pace with the front-end manufacturing.

Figure 1 provides the package outline and cross section of Elpida's 8-Gbit TSV DRAM package.

An alternative is 2.5-D interconnection, where chips are generally placed side by side on an interposer with through-vias to a substrate below. This packaging scheme avoids the thermal issues of high-powered die stacked on top of one another that 3-D interconnect has.

Wide I/O Interposers and Microbumps, AKA 2.5-D

The notion of 2.5-D was born in early 2010, as a variation of 3-D integration. 3-D integration stacks devices vertically using TSVs for electrical connection, and possibly an RDL (redistribution layer) created with a dielectric material as a layer to reroute the electrical connections between chips to allow the vias to travel to the lower substrate.

2.5-D replaces the RDL with a silicon (or glass) wide I/O interposer as the routing layer, so that the through-vias run through the interposer or substrate rather than through the active die. This interposer can be used to fan out or reroute the electrical traces of a device while routing the traces to another vehicle in a vertical dimension, such as the package substrate. These layers utilize microbumps on the interface to electrically connect to the next layer in the stack. Silicon interposers accommodate the CTE mismatch between the layers in a stack, thus improving reliability. 2.5-D simplifies the structure in a way that allows the OSAT (outsourced assembly and test) community to participate, providing a handoff point for OSAT companies to get involved in the final packaging operation. 2.5-D integration provides a smooth process transition from 40 nm to 28 nm. Figures 2 and 3 display a 2.5-D package from STATS ChipPAC.

A silicon interposer can be introduced between devices and a package substrate, or between devices in the stack. Devices can include a number of passive devices, a CMOS image sensor (CIS), or ICs (integrated circuits).

If used between an IC and the package substrate, the silicon interposer absorbs some of the fan-out to the substrate, reducing the complexity of the package substrate. Multiple devices then sit side by side on the interposer, and thermal issues associated with 3-D interconnect recede.

Using a silicon interposer between ICs, such as a memory and logic chip, provides a layer on which to reroute the circuitry to accommodate the differing positions of the bond pads.

When used for passive devices, a number of these devices would fit on top of, or within, the interposer, thus eliminating the need to put these directly on a PCB with individual traces.

The TSV can be modified to manage the jitter, equalize the channel power delivery, and embed decoupling capacitance between the layers. Multiple capacitors can

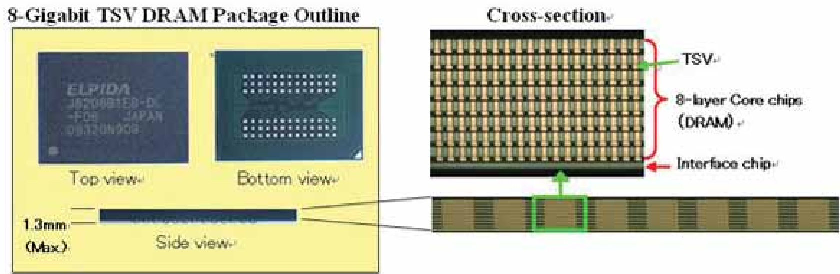

Figure 1 Elpida's 8-Gigabit TSV DRAM Package Outline and Cross Section

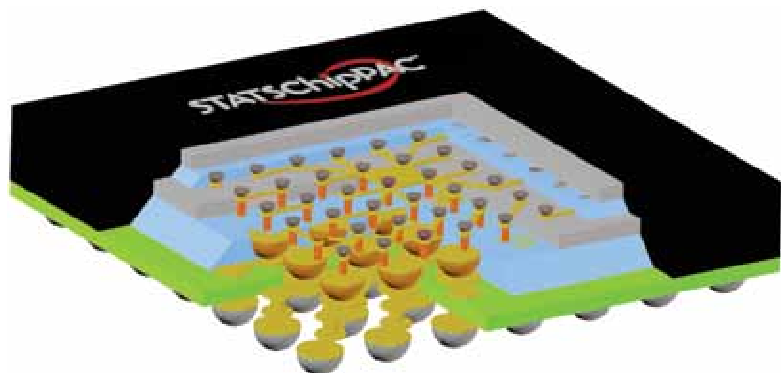

Figure 2. STATS ChipPAC's fcBGA with TSV structure.

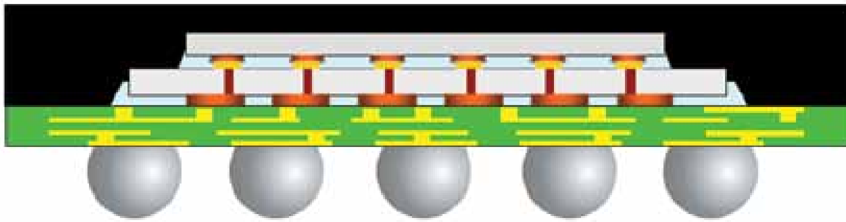

Figure 3. STATS ChipPAC's fcBGA with TSV cross section.

be embedded, and if they are of different sizes, this then controls the resonance in the package. If the routing layers are in a vertical plane, this increases the capacitance. Lowering the capacitance for signal TSVs involves alternating thin high-k and thick low-k materials in the series of layers. Columns can be added between layers if a greater separation is desired between layers.

2.5-D integration is expected to begin in 2012, and develop alongside 3 D integration. 2.5D integration is well suited for tablets, which have a phenomenal growth rate. 3D integration, which is more complex, if better for smart cell phone technology which requires high bandwidth.

Market Potential

Prior to the 2009 meltdown, IBM, Intel, Samsung, Micron, and others had announced their intent to introduce TSV products in production volumes in the 2011 to 2012 time frame. To maintain their leadership in this area, they have continued to invest in bringing this promising technology to production, although at a slower pace. Many other companies, such as Kyocera, Xilinx, Altera, and others, have also indicated their interest in utilizing this technology. Memory maker Elpida was the first to introduce a product on the market involving ICs. Whereas its product was expected on the market in late 2009, it actually took until 2011 to produce sample products, with production expected later this year.

TSVs will someday be found in stacked packages, CMOS image sensors (CISs), and medical devices such as hearing aids. CIS appears to be the market that offers the most promise, as putting a cover over the sensor increases the yield. Once covered, however, wire bonding is not possible. Thus TSVs make sense.

Potential TSV Market	CAGR 2010-2015
MPU	7.8%
DRAM	11.0%
SPL - Communications	11.1%
Standard Cell/PLD	17.7%
Flash	2.3%
Total Potential TSV Market CAGR	9.2%

Table 1. CAGR for potential TSV markets.

Given the high cost of creating the vias, they will not be produced in significant volumes for a few more years.

The following markets are those in which TSVs will be found initially: MPU, DRAM, Special-purpose logic - communications, PLD and FPGA, Flash.

These are markets that have relatively high ASPs and demand high performance. The compound annual growth rate for each of these markets is presented in Table 1. ◆

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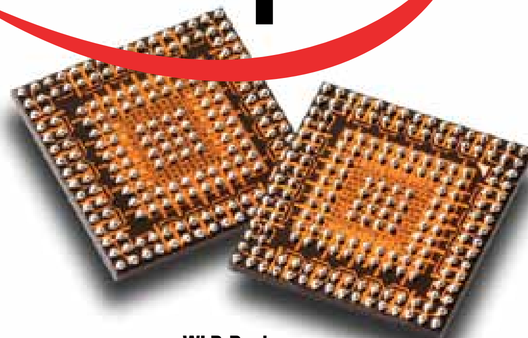
TRANSFORMATION INTO AN INDUSTRY LEADER

STATS ChipPAC is a relatively young company formed in 2004 as a result of the merger between STATS and ChipPAC, two mid-tier Outsourced Semiconductor Assembly and Test (OSAT) companies. ST Assembly Test Services (STATS) was established in 1995 as a test operation in Singapore. ChipPAC was spun off from Hyundai Electronics' Assembly and Test Division in 1997. The merger of these two companies formed STATS ChipPAC, the fourth largest OSAT company in the world.

The merger provided a number of clear benefits: increased scale and technology offering, complementary assembly and test capabilities, and a broader geographic footprint. Yet, the true success behind STATS ChipPAC has been the Company's ability to transform itself into an industry leader with a competitive business model that is focused on technology differentiation, full turnkey assembly and test solutions, and operational excellence.

STATSChipPAC®



eWLB Package

Focus on Device Convergence

The driving theme in the electronics world today is convergence as the traditional markets of computing, communications and consumer are converging to create new markets in smart devices such as smart phones, smart books and tablets. Consumers are looking for mobile devices that have multiple functions such as data processing, imaging and Radio Frequency (RF) capabilities in smaller and smaller sizes. The digitization of information and on-demand entertainment requires, more than ever, semiconductor devices that are smaller, thinner, faster, cheaper and capable of performing more functions.

In order to satisfy this demand for increased functionality, semiconductor companies need to rapidly develop new models and ramp products quickly to meet aggressive time-to-market goals. With the convergence of voice, video and data functions into a single platform, semiconductor companies are relying on OSAT providers to enhance their ability to achieve these new levels of functionality by pushing integration technology to new levels.

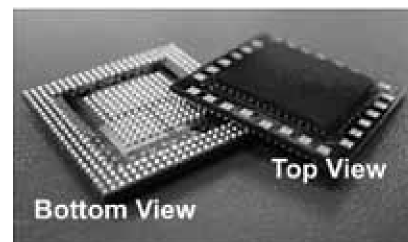
STATS ChipPAC's business model is focused on the rapid advancement to device convergence and a comprehensive service offering that is tailored around the requirements of the communications, computing and consumer markets. By strategically investing in next generation integration technology and full turnkey assembly and test services which address this trend, STATS ChipPAC offers the experience and technology that positions its customers for success in the markets they serve.

Differentiation Through Technology Innovation

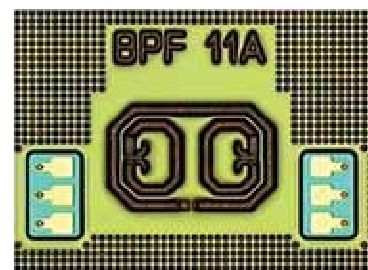
Consumer demand for low cost, innovative mobile devices poses an ongoing challenge for the semiconductor industry. As die sizes and lithography nodes continue to shrink, manufacturers must find the most efficient way to integrate more functionality and performance into a final solution.

With the industry movement to finer and finer geometries, packaging technology is undergoing a significant change and becoming an important differentiator. STATS ChipPAC believes technology is one of the most important ways to differentiate itself. The Company offers a broad technology portfolio ranging from leadframe to laminate packages, flip chip, wafer level and advanced three dimensional (3D) packaging solutions.

STATS ChipPAC differentiates itself through advanced technology such as



eWLB Package-on-Package (PoP)



IPD with TSV

wafer level packaging (WLP), flip chip interconnect and 3D solutions which integrate multiple devices into a single, integrated solution. The Company maintains a strong investment in R&D, equipment and engineering resources to establish a powerful platform of integration technology and solutions at the silicon and system levels.

Wafer Level Technology for High Performance, Highly Integrated Packaging Solutions

As a small, lightweight, high performance semiconductor solution, wafer-level technology is a compelling, cost effective solution for space constrained mobile and consumer applications. STATS ChipPAC has been focusing on expanding its wafer-level technology offering, which today encompasses wafer bump, fan-in Wafer Level Chip Scale Package (WLCSP), fan-out Wafer Level Packaging (FOWLP), Integrated Passive Device (IPD) and Through Silicon Via (TSV).

Fan-out Wafer Level Packaging is one clear example of how STATS ChipPAC differentiates its technology offering. FOWLP offers the ability to provide a higher number of interconnects than is possible with fan-in wafer level technology. The cornerstone of STATS ChipPAC's fan-out wafer level technology platform is embedded Wafer-Level Ball Grid Array (eWLB). eWLB is a powerful wafer level technology that has the design flexibility to accommodate an unlimited number of interconnects, is unconstrained by die size and offers one of thinnest package profiles in the industry today. eWLB provides significant performance, size and cost benefits compared to current packaging technologies and can enable the next generation of convergence devices.

STATS ChipPAC's significant focus and investment in the evolution of this technology has resulted in an expanded range of eWLB package architectures, including single die, multi-die, ultra thin, System-in-Package (SiP) and 3D packaging. In terms of time-to-market, the Company can deliver advanced eWLB solutions with cycle times that are competitive with flip chip packages. The development of next-generation eWLB is continuing at a rapid pace at STATS ChipPAC with a number of new advanced package architectures which integrate eWLB with Through Silicon Via (TSV) and Integrated Passive Devices (IPD) to achieve new levels of heterogeneous functional integration.

TSV utilizes short vertical interconnections through a silicon wafer to achieve greater space efficiencies and higher interconnect densities. It also enables the integration of semiconductor die fabricated in different technology nodes with diverse testing requirements into a single solution. STATS ChipPAC was one of the first OSAT providers to invest in TSV technology and has complete front to back-end manufacturing capabilities for 200mm wafers with current capabilities to handle both chip-to-chip (C2C) and chip-to-wafer (C2W) assembly. The Company recently added a 300mm "mid-end" process flow that occurs between the wafer fabrication and back-end assembly process. Mid-end processes support the advanced manufacturing requirements of 2.5D and 3D TSV as well as wafer level packaging, flip chip and embedded die technologies.

With over 10 years of development experience, STATS ChipPAC has an extensive background in IPD technology. IPDs such as resistors, capacitors, inductors, filters and baluns can consume 60% to 70% of available space in a system, subsystem or SiP package. Integrating IPD and TSV technology in an eWLB design delivers advantages such as reduced form factor and better overall system performance. STATS ChipPAC's vast knowledge and experience in eWLB, TSV and IPD has enabled the Company to differentiate its technology offering and deliver new levels of heterogeneous integration in a wide range of design configurations for its customers.

Flip Chip Technology Innovation

Flip chip technology is another key area where STATS ChipPAC has chosen to differentiate its product portfolio. Flip chip technology offers superior electrical performance, smaller form factors and high I/O capabilities which are very attractive to a growing number of applications. However, traditionally higher costs and mechanical stress issues on extra low-k and ultra low-k (ELK/ULK) interlayer dielectric layers in finer silicon nodes have slowed or even prevented adoption of flip chip in certain applications. STATS ChipPAC has taken a comprehensive approach to reengineering the package structure and has enhanced key processes to achieve an innovative flip chip technology that delivers high input/output (I/O) density, high performance and superior reliability in advanced silicon nodes.

STATS ChipPAC's innovative flip chip packaging technology, fcCuBE™,

300mm eWLB Wafer

WLCSP Assembly

Wire Bond Assembly

Wafer Level Test

Final Test

combines copper (Cu) column bumps, Bond-on-Lead (BOL) interconnection and enhanced assembly processes to deliver a higher performance, higher density and low cost flip chip solution for advanced technology nodes down to 45/40nm. The innovative fcCuBE package structure and cost-effective manufacturing process delivers the performance benefits of flip chip interconnect with a 20-40% lower cost than standard flip chip packaging. With increased performance, superior reliability, miniaturization and lower costs, fcCuBE technology is a compelling solution for a wide cross section of end products in the mobile/handheld, computing and high-end network/telecom markets.

Cost Innovation

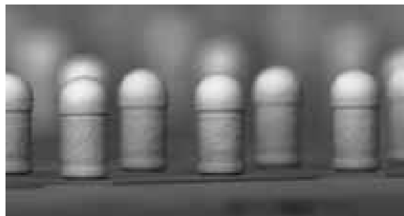
While most companies recognize that technology is important in driving innovation in functionality and performance, STATS ChipPAC is using technological advancements to achieve lower cost solutions for its customers. Throughout the Company and across every product line, STATS ChipPAC looks for ways to increase manufacturing efficiencies and reduce costs through technology and process innovations. fcCuBE technology is a prime example of STATS ChipPAC's success in delivering both technology and cost innovation in an advanced solution.

Another important cost focus for STATS ChipPAC is the transition from gold to copper wire package interconnect. This offers a significant saving in material costs while delivering electrical and thermal performance with quality and reliability levels that are comparable to gold wire. STATS ChipPAC has copper wirebond capabilities in all five of its manufacturing facilities in Asia, and is rapidly increasing production volumes in both leadframe and laminate packages.

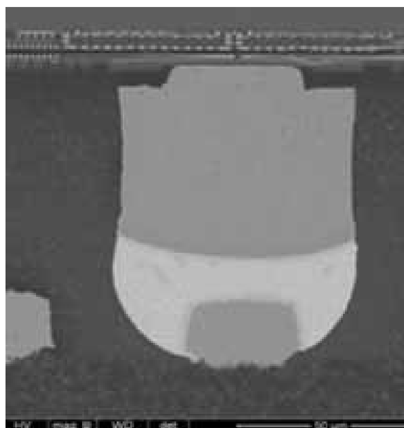
STATS ChipPAC is actively investing in technology, equipment and engineering resources to utilize copper wire in advanced wafer nodes down to 45/40 nm with low-k and extra low-k (ELK) dielectric materials. Development is focused on areas such as finer bond pad pitches, thinner wire diameters, stacked die packaging and die-to-die bonding, and STATS ChipPAC is successfully addressing many of the technical challenges that are associated with using copper wire interconnect in more complex package structures.

Investment in Intellectual Property

Technology innovations and manufacturing process improvements have been critical to STATS ChipPAC's success and ability to offer customers differentiating solutions. STATS ChipPAC has made significant investments in research and development, and has been aggressively expanding its Intellectual Properties (IP) portfolio. In 2011, the Company achieved a milestone of over 2,000 patents filed and over 650 patents issued. Since 2005, over half of STATS ChipPAC's IP portfolio is in advanced technologies such as fan-out wafer-level packaging (FOWLP), wafer bump, TSV, IPD, 2D/3D wafer level packaging and System-in-Package (SiP).



40um Copper Column Bump for fcCuBE



fcCuBE Copper Column Bump

Copper Wirebond

Integrated Turnkey Solutions

The strength of STATS ChipPAC's packaging technology is complemented with a comprehensive service offering in wafer bump, wafer sort and final test capabilities. With extensive knowledge and experience in test, STATS ChipPAC offers customers a full suite of solutions and test platforms to address and support their requirements for highly integrated devices that are powering the next generation of mobile, consumer and other advanced electronics devices. A full turnkey offering is a compelling value proposition as it provides customers with faster time-to-market solutions, improves product quality and reduces overall costs for customers. This strategy has been an important factor in the Company's growth and success.

Operational Excellence

STATS ChipPAC's technologies and services are supported by an extensive global manufacturing footprint, with facilities in Singapore, South Korea, China, Malaysia, Thailand and Taiwan. These manufacturing facilities are strategically located in close proximity to the major hubs of semiconductor wafer fabrication, and work together to support customers around the world with full turnkey packaging and testing solutions. The Company has built a strong record of operational excellence and unrelenting drive to improve quality, reliability and cycle time.

STATS ChipPAC's operational excellence is built around Lean Six Sigma methodology. This has led to the achievement of significant milestones year over year that reduce costs and increase efficiencies through breakthrough methodologies and process improvements. STATS ChipPAC's deep commitment to operational excellence and best-in-class customer support have earned the Company numerous customer awards and recognition over the years.

Summary

In today's highly competitive markets, choosing the right OSAT partner to support a company's business requirements is critical. Technology innovations and manufacturing capabilities can have a significant impact on the success of a product. STATS ChipPAC offers customers technology differentiation, full turnkey assembly and test solutions, operational excellence and a commitment to making sure its customers have a competitive edge in the market.

For more information about STATS ChipPAC visit www.statschippac.com. ◆

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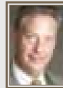
PROGRAM

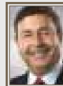
8:30 a.m. Registration and Networking Breakfast Sponsored by Samsung

9:15 a.m. Keynote: State of the Industry
Len Jelinek, Director & Principal Analyst, Semiconductor Manufacturing, IHS iSuppli



Session I: Collaborative Supply Chain

9:45 a.m. Keynote: Flash Memory: The Importance of Fostering Collaboration in Today's Mobile Ecosystem
Sanjay Mehrotra, President & CEO, SanDisk Corporation



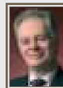
10:15 a.m. Networking Break

10:45 a.m. Roundtable Session: Best Supply Chain Practices for a Successful Partnership

11:45 a.m. Networking Lunch sponsored by GLOBALFOUNDRIES

Session II: Advanced Technology Development

1:15 p.m. Keynote: Security & the Smart Technology Evolution
Tudor Brown, President, ARM



1:45 p.m. Panel: Improving Device Performance - Simplifying Software/Hardware Integration

2:45 p.m. Networking Break

Session III: Financial Trends

3:15 p.m. Keynote: Macro-Economic & Social Trends - The Future of Semiconductor Growth in Emerging Markets
Dan Niles, CEO, Alpha One Capital Partners LLC

3:45 p.m. Panel: Semiconductor Investment - Redefining the Funding Model

Session IV: Evolving Semiconductor Ecosystem

4:45 p.m. VIP Reception sponsored by GLOBALFOUNDRIES

5:30 p.m. Conversational Interview

- **Dr. Aart de Geus,** Chairman & CEO, Synopsys, Inc.

- **Scott McGregor,** President & CEO, Broadcom

6:45 p.m. Closing Remarks

7:00 p.m. VIP Dinner sponsored by eSilicon

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TLA™ – An Alternative to QFN

Kelly R. McKendrick Sr., Sales & Technical Program Manager and
Serafin Pedron, Jr., Director of Technical Product Marketing
UTAC – UGS America Sales, Inc

SEMICONDUCTOR PACKAGING is still morphing. Some require many I/O's, others better thermal & electrical performance. Thin is often a major criterion, yet to some it is all about board space. All will agree that cost and quality are a given requirement. There are numerous packaging technologies that are used for these different applications. On the leadframe side, QFN still seems to be one of the more popular packages due to its simplicity, as well as its pricing advantages, but it often is limited by size, pin count and design flexibility. Dual row QFN helps in certain areas but adds cost and process challenges while laminate alternatives are not timely and often pricey. The TLA™ (Thermal Leadless Array) package technology bridges this gap. TLA is a close cousin to QFN yet a TLA design is extremely flexible and more often will meet the needs of a chip design and/or a board level requirement. Advantages include more I/O's than are otherwise possible with QFN, reduced package footprint, design flexibility wherein the package can be designed around the die and can easily incorporate options like floating rings and split die attach pads. Other advantages include no hard tooling required for custom designs, shorter wire lengths and better MSL capability than organic laminate based packages. The terminal standoff provides some level of self-alignment during SMT, similar to BGA type packages. TLA package technology can be configured in the same thicknesses and body sizes as QFN and it utilizes most of the same manufacturing flows, equipment and materials sets. Electrical performance is far superior to QFN and the thermal properties are comparable. Let's take a closer look at TLA and some of the similarities and differences it has with the QFN package.

Lead Frame History

Standard surface mount lead frame products have evolved rather quickly. Those of you that remember the big thick packages of the 70's, 80's and early 90's also remember when the "thin" lead frame packages were introduced. The 1.0 mm thick TQFP was really quite an amazing thing to behold when it first came out. It really challenged the equipment vendors at the time. Trying to get "low" loop height consistently and backgrind (back lap) down to places no one had been before were quite a feat. Many thought that 1.0 mm was the threshold. As with most things in this crazy industry, we now have lead frame products down to 0.20 mm thick. Now maybe I am still a bit skeptical but I think we are getting close to the limits of thinness for a lead frame product, based on the current way we do these packages. Chip Scale or Wafer Scale die may have some room still, but other than that, I think our Limbo stick of package thickness has gone down just about as low as it can go.

QFN & TLA

QFN – QFN is one of the more popular lead frame technologies. An X2QFN (0.4 mm) compared to a standard VQFN (0.9 mm) (See Figure 1).

The thicker VQFN (0.9 mm thick) is thinner than the TQFP that most thought was the ultimate thin package only a few years ago. QFN's are now the PDIP and SOIC of yesterday. Everyone seems to have a QFN with different names associated with it. QFN's are fairly easy to make and are very cost competitive and are now a mature product line. Like SOIC and other legacy products, QFN's should be around for awhile.

TLA – Being the close cousin to QFN, it too is a lead frame based product but has limitless design flexibility. Per JEDEC, TLA is officially classified as a QFN. Yes there are similarities but there are also many differences. Thermally it is comparable to the QFN but electrically it is far superior due to a significant reduction in signal lengths in most cases. The footprint or board area is generally reduced. Like QFN, it is green and RoHS-compliant but TLA can have I/O counts that can often rival many of the Fine Pitch BGA products. With the recent explosion of gold, TLA is an excellent candidate for Copper Wire Bonding. Here are some of the key areas and unique properties pertaining to this TLA package.

Signal Lengths & Board Footprints – As you can see from the examples in Figures 2 & 3, the reductions in board space wire lengths can be significant. Figure 2 shows a typical lead frame

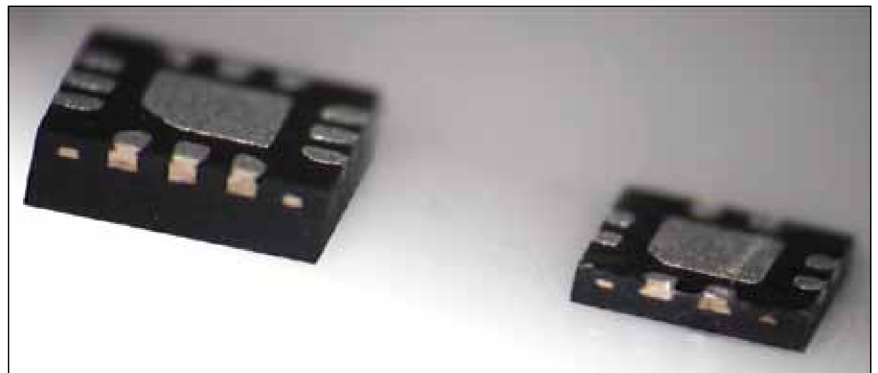
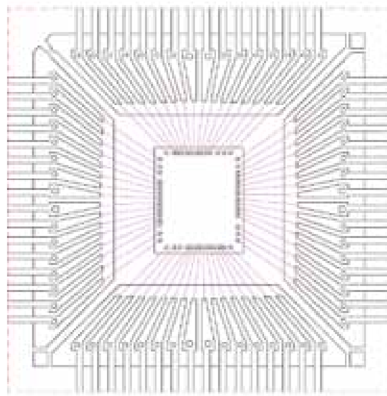
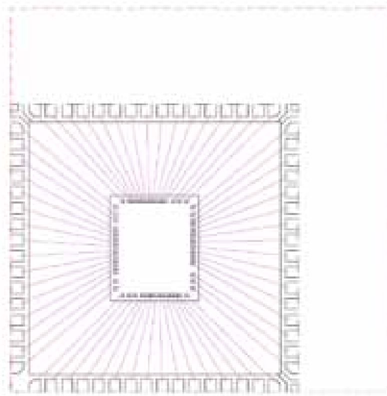


Figure 1. VQFN versus X2QFN leadless package.



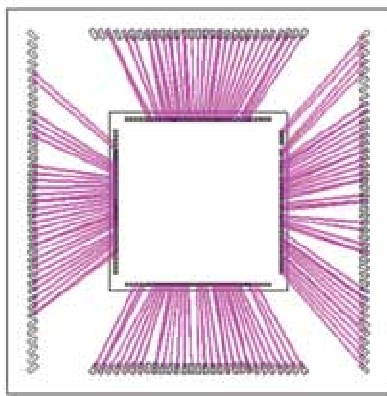
64L 10x10 mm QFP (FP=2.0)
Terminal Pitch = 0.5 mm
Total Signal Length = 336 mm
Overall Thickness = 1.2 mm
PCB Area Ratio = 1.0



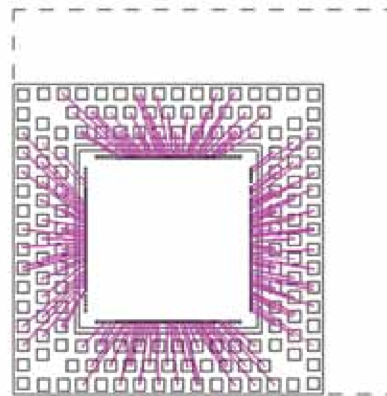
64L 9x9 mm QFN
Terminal Pitch = 0.5 mm
Total Signal Length = 224 mm
Overall Thickness = 1.0 mm
PCB Area Ratio = 0.56

76L 6x6 mm TLA
Terminal Pitch = 0.5 mm
Total Signal Length = 93 mm
Overall Thickness = 0.8 mm
PCB Area Ratio = 0.25

Figure 2. Footprint Comparison between QFP, QFN and TLA.



144 I/O 2L 10x10 mm L-fpBGA
(0.8 mm Ball Pitch)
112 I/O in Use for Wire Bonding
Total Signal Length = 526 mm
Longest Wire = 3.29 mm (130 mils)
PCB Area Ratio = 1.0



152L 8.088x8.066 mm TLA
(0.5 mm Lead Pitch)
112 I/O in Use for Wire Bonding
Total Signal Length = 188 mm (Less 64%)
Longest Wire = 2.44 mm (97 mils)
PCB Area Ratio = 0.65

Figure 3. Footprint Comparison between fBGA and TLA.

	QFN		TLA	
Package Size	I/O Range	Available I/O Count 0.5 mm Pitch	I/O Range	Available I/O Count 0.5 mm Pitch
2x2 mm	8	8	12	12
3x3 mm	12 - 16^	12, 16	20	20
4x4 mm	20 - 24^	20, 24	28 - 44	28, 44
5x5 mm	28 - 44^	28, 32, 44	36 - 80	36, 60, 80
6x6 mm	36 - 60^	36, 40, 60	44 - 104	44, 76, 104
7x7 mm	44 - 76^	44, 48, 76	92 - 128	92, 128
8x8 mm	52 - 92^	52, 56, 92	108 - 152	108, 152
9x9 mm	60 - 108^	60, 64, 108	124 - 176	124, 176
10x10 mm	68 - 124^	68, 72, 124	140 - 200	140, 200
11x11 mm	—	—	156 - 224	156, 224
12x12 mm	—	—	172 - 248	172, 248
13x13 mm	—	—	188 - 272	188, 272
15x15 mm	—	—	220 - 320	220, 320
17x17 mm	—	—	252 - 368	252, 368

(^ with chamfered leads) Blue-Single Row, Red-Double Row, Black-Three Row

Figure 4. Lead Count Comparison – QFN versus TLA.

example while Figure 3 shows an example of how TLA can be used instead of an fBGA application.

You can see that signal lengths are greatly reduced. In these 2 examples, the signal lengths are reduced approximately 72% and 64%, respectively. For an application that is electrically challenged, this reduction in signal and wire length can be very significant.

Design Flexibility – Since this requires only a plating and etch mask from the lead frame vendor, cost is minimal. No additional tooling costs are required for any package size or lead count, thus capital expenditure is zero. Each design can meet JEDEC specs or can be a unique customized package designed to meet the customer's application. The possibilities of design are limitless - different body sizes, pad pitches, down bond rings or pads, isolated power rings, the number of rows of outer leads, multiple die, SiP, etc. If you can think of it, it more than likely can be done.

Manufacturability – Like traditional QFNs, TLA is an etched process. While QFN is etched on both sides prior to assembly, TLA is half etched only on the top side. The back etch on TLA is done after mold. With the lead frame as a solid strip prior to mold, no tape is needed at mold which eliminates the mold flash issues of QFN. Solid strips also enhance the wire bond process; i.e., no tape and no bouncing leads that result to non-sticks. Once the final etch is complete, nothing is tied electrically; thus, it is ready for strip test if required. With no

metal protruding out the side walls, most saw issues are now eliminated during singulation; e.g., faster feed rate and no copper burrs. Like saw singulated QFN, one mold is all that is needed for every design. In fact you can use the QFN molds. Like QFN, materials are green and meet most, if not all, of the current lead free standards.

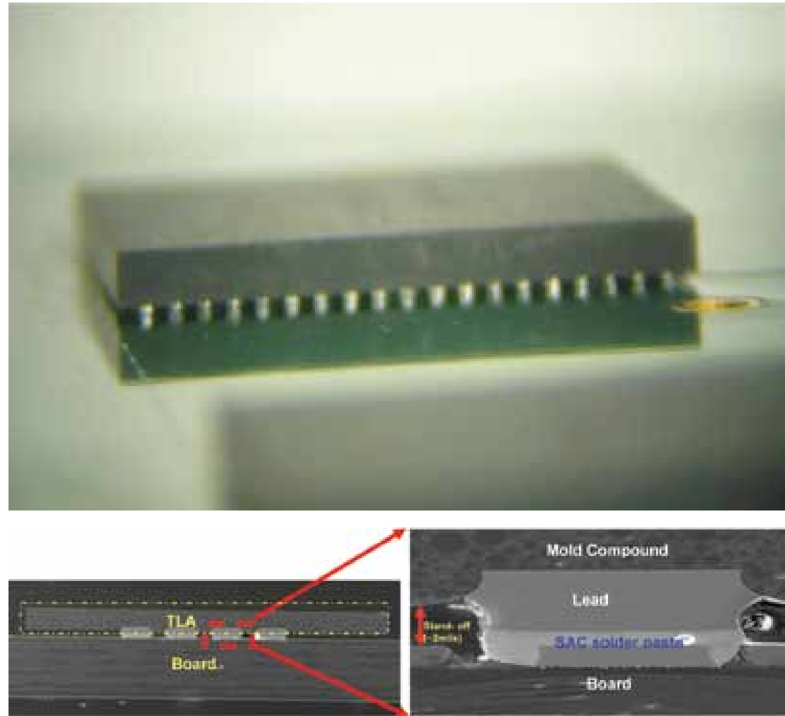
Lead Counts – The biggest advantage is the amount of I/O's on a body size when compared to a traditional QFN. (See Figure 4)

Advantages – There are many, including no capital expenditure or tooling, more parts per strip, higher yields, less gold, no tape & no mold flash, strip test capable, standard assembly process, and so on.

Leads – Another difference between a QFN and the TLA are the leads. Unlike a QFN, where the leads have exposed copper on the sides and are flat and flush with the board, TLA parts have no exposed copper and have a 1-2 mil standoff. With no exposed copper this is beneficial for power and RF designs, saw singulation and strip test. The slight stand off also creates a self centering effect during reflow, similar to a BGA product. (See Figures 5 & 6)

Routability and Reliability – Package design, as well as routability, rules are in place. TLA is not only customized for the customer's die and package needs but can be designed with the board application in mind as well. PCB escape routability issues are addressed in the design stage and should not be an afterthought. Reliability is also a concern for most customers. TLA will pass JEDEC prescribed package qualification and board level reliability tests.

So QFN or TLA? – This depends on what your need is. Small and low pin count parts probably do not need the advantages of a TLA. QFN, in many instances, is the best package of choice. Yet others see an opportunity to add I/O without increasing a body size or they may want to reduce a foot print. Many want to design around their chip and/or board. Others may want to do away with the hassles of Dual Row QFN and reduce the body size as well. Some want to stay away from expensive laminate parts and others may want to just get rid of some of the larger surface mount packages such as QFP. Figure 7 shows the various PCB footprint options for 0.5 mm pitch QFN.



Figures 5 and 6. Cross section of TLA on PC Board.

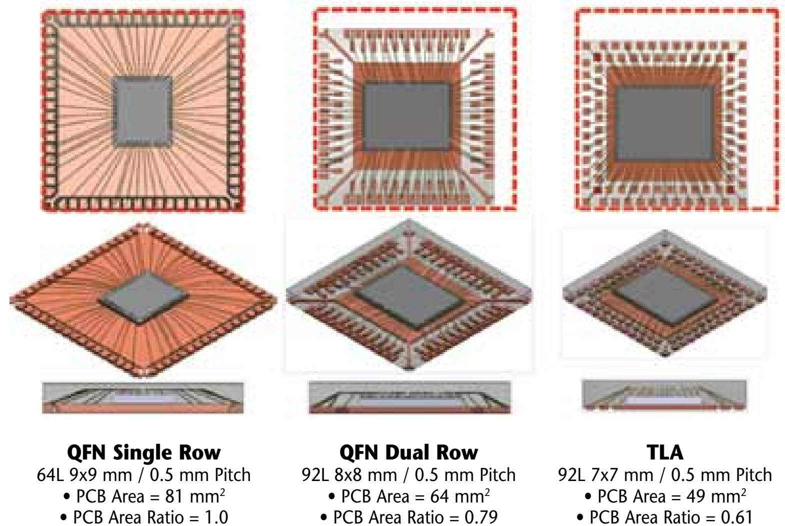


Figure 7. PCB footprint comparison for 0.5 mm pitch QFN.

Conclusion

With the packaging world going more and more toward inclusion of the overall final product design, definitely more and more flexibility is needed. For this very large segment of the packaging world, the way people think about how to design and manufacture packages is changing. We are seeing a shift in the assembly world and the TLA type products are going to be part of this shift. ◆

2.5D/3D Integration Reshapes Semiconductor Industry Supply Chain

John Y. Xie, Ph.D.
Altera Corporation

SEMICONDUCTOR PROCESS technology scaling has been the key driving force for component and system performance evolution in the modern high-tech industry driven by Moore's Law. But increasingly, the traditional process scaling alone can no longer meet system performance requirements, such as throughput, performance, and power budget. Traditional monolithic system-on-a-chip (SoC) and packaging solutions have been increasingly threatened by various competing component stacking configurations from PIP/POP/MCP to silicon-silicon stacking configuration (the so-called 2.5D/3D integration).

2.5D/3D integration is the new driving force to carry Moore's Law and beyond to drive system-level integration, miniaturization, power management, significantly increased data bandwidth, and eventually reduced system cost. It has a ripple effect on the entire semiconductor industry's ecosystem—from wafer processing to interconnect technology and system integration; from industry's infrastructure development roadmap to research institute and academic activities; from more traditionally partitioned technology and solutions to more integrated platform solutions. As an emerging technology, the challenges of 2.5D/3D integration are profound. They encompass various aspects of process technology, integration flow, testing, thin wafer handling, new standards and protocols, EDA tool, design flow and design for test (DFT) methodology, and of course, the new methodologies to architect future microelectronics systems from concept to integration. The industry's effort in developing these solutions will revolutionize the semiconductor industry's entire ecosystem.

Known Good Die (KGD) will break through. People may be able to find a way to avoid KGD issues with multi-chip packaging (MCP); but the 2.5D/3D integration will need to resolve KGD challenges to become a truly cost-effective solution, especially for mid- to large-scale IC-based products and applications. From silicon-package interface to silicon-silicon interface, the number of interconnect interfaces are increased by two orders of magnitude. This will enable substantially increased test coverage (of course, ultra-fine pitch array microprobing is also very challenging). Meanwhile, wafer-level burn-in technology's progress will enable both voltage stress and pre-wafer-sort long duration wafer level BI process. These will bring the KGD technology closer to reality.

Cost sensitivity drives the creation of different stacking technologies and new business solutions. There is a cost premium associated with the introduction of a new technology as well as due to additional processes such as 2.5D/3D stacking, through-silicon via (TSV), wafer bumping and thinning. Low-cost stacking, which may not include TSVs or even an interposer, will bring volume up and stacking cost down. High-end stacking, which usually includes interposer and TSV configurations, will drive 2.5D/3D leading-edge technology's advances. We will need both. These different stacking technologies bring in different players and lead to different solutions. This will stimulate industry-wide R&D activities and promote industry landscape changes.

2.5D/3D integration will lead to the creation of new business and new supply chain models. If we recall the wafer-bumping technology and capacity-development history, there was strong debate 10–15 years ago on whether foundries should establish wafer-bumping capabilities. Today, silicon interposer and TSV manufacturers face a similar question. While the foundry industry brings the vision and capital for the development of silicon interposers and 2.5D/3D integration solutions, end customers are experiencing the challenge of limited options and supply sources. The outsourced semiconductor assembly and test (OSAT) industry is also monitoring and digesting both opportunities and constraints. OSAT companies can develop redistribution layer (RDL)-based silicon interposers, but the density and features, such as the passives on the silicon interposers, will have fundamental density limitations. Demand for interposers offers second-tier foundries a new revenue source, as a typical silicon interposer does not require the most advanced silicon process technology. Most of the second-tier foundry companies could leverage their available capacity to support their revenue and profit goals. With limited capital compared to the full scope of IC fab investment, a backend-dominated interposer manufacturing line can be established at a much lower cost and transition to volume production faster. We should also not forget the simple but interesting fact that the silicon interposer itself will be larger in size than any silicon devices placed on such an interposer—which would contribute positively to overall interposer wafer volume demand.

The increased crossing over of traditional foundry and OSAT partitions on high-end interconnect and assembly integrations are creating new business models. The foundry industry can typically invest at much higher level capital expenditure (CAPEX) strengths than the OSAT industry which operates at lower gross margins with R&D spend at an order of magnitude away from that of the foundries. These R&D efforts, no matter which technology sectors they are from, will eventually benefit the entire semiconductor industry. It will especially offer higher profit revenue opportunities in the lower end food chain. It is worth noting here that with this trend, large foundries and OSAT companies will grow even larger with more integrated technology and solution capabilities, outpacing their peers at today's level. Based on leading

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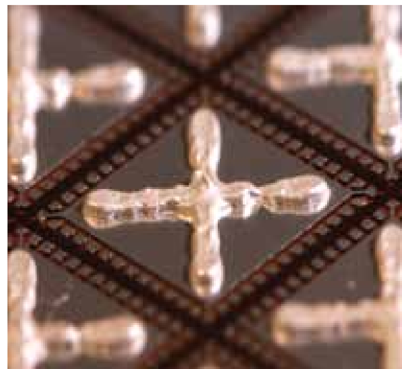
New Pressureless, High UPH Silver Sintering Technology Charges Up Power Device Manufacturers

Nigel Hackett
Henkel Electronic Materials, LLC

SILVER SINTERING IS NOT A new technology. In fact, it has been around for some time. What is new, however, is a groundbreaking material innovation that now allows power device manufacturers to enjoy the benefits of silver (Ag) sintering and do so in high volume without the need for pressure.

For those unfamiliar with Ag sintering, here's the two-second brief: sintering is a process in which particles are joined together by heating the material in a sintering furnace below its melting point until there is particle adhesion. In the packaging market, when Ag sintering is used for die attach processes, it has traditionally also included a pressure mechanism in combination with heat to enable metal joint formation. The challenge with this method, however, is its volume limitation. Conventional Ag sintering techniques require the use of capital-intensive die bonding systems where each device has to be processed individually, which drastically limits UPH rates and monopolizes valuable equipment resource.

But, all of that is history, as a new formulation innovation from Henkel has upended conventional Ag sintering methods by delivering a technology that enables high volume production without pressure. Henkel's novel Ag sintering breakthrough has been designed into its latest die attach formulation, ABLESTIK SSP2000. With this material, because the silver particles are joined via a unique surface tension mechanism, no pressure is required and devices can be cured in a standard batch oven at a temperature as low as 200°C. What does this mean? Incredibly, it means a 200x increase in UPH capability. Yes, you read that correctly – 200x! While traditional Ag sintering methods can produce 30 units per hour on average, Henkel's new technology can enable production of as many as 6,000 units per hour. ABLESTIK SSP2000 has delivered what power device manufacturers have long required – a high UPH and high reliability Ag sintering die attach material in a single formulation. What's more, the material can be processed on standard die bonding systems,



which means that no additional equipment investment is required and the transition can be made easily, quickly and cost-effectively.

While the pressureless high UPH capability is, indeed, remarkable, what is even more noteworthy is ABLESTIK SSP2000's high reliability and thermal resistance performance. In fact, ABLESTIK SSP2000 has the potential to outperform high-lead soft solders – the current die attach material of choice for high power devices – in power cycling capability by a factor of ten. Typically in power cycling testing where solder fails at 200 cycles, Ag sintering technology can reach over 2,000 cycles before its first failure. ABLESTIK SSP2000's thermal resistance and conductivity are superior to solder, offering overall enhanced performance. So, for packaging specialists seeking a lead-free alternative with BETTER results than high-lead solder, ABLESTIK SSP2000 is the obvious choice. For designers and manufacturers of high power devices like IGBTs, this material delivers the ability to reduce the number of chips in a package, saving on valuable device real estate and achieving unmatched capability as well. In short, this is a solution that current solder materials simply can't touch.

All of this capability couldn't come at a more opportune time, as the RoHS deadline for the elimination of lead from power devices is looming. The current deadline of 2014 is less than three years away, at which time packaging specialists must have alternatives in place. Fortunately, Henkel has already resolved this issue with the development of ABLESTIK SSP2000.

For power semiconductor devices, high power LEDs or any application that requires outstanding thermal capability alongside high UPH, Henkel's Ag sintering technology offers an unmatched solution. It is lead-free compliant, affords exceptional design latitude, has superior electrical and thermal performance, is highly reliable and enables high UPH in a no pressure process. When it comes to high power die attach solutions, ABLESTIK SSP2000 has it all.

To find out more about Henkel's breakthrough silver sintering technology or any of our innovative die attach solutions, log onto www.henkel.com/electronics or call the company headquarters at 714-368-8000. ◆

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TECHNOLOGY continued from page 29

OSAT financial reports, it is very obvious that focused investments in high-end assembly technology and capacity expansion are occurring.

High-level integrated manufacturing model will affect sourcing strategy. Another area of business consideration includes intellectual property (IP), product ownership, and security of supply. With silicon coming from multiple foundries and IP providers, both manufacturing integration providers and end customers need to understand and manage the collaboration among the competitors. The issues would include product and IP, compatibility of interfaces (both device-to-device and business-to-business), performance and quality issue ownership, manufacturing and business logistics, forecast and inventory management, and importantly, the security of supply related to product revision and end of life (EOL). The higher the level of the integration, the more likely these problems will occur and need to be predicted and addressed proactively. This could easily lead to challenges such as more product changes, reduced product life cycle, reduced volumes over the product life span, and potential customer disputes. Another issue is non-compatible multi-sourcing solutions due to increased level of integration with rich manufacturing IP from technology power houses. Resolving these challenges require that our industries increase industry-wide collaboration on R&D, prioritize new standard development, and promote technology proliferations.

With all these challenges and opportunities, 2.5D/3D interconnect and integration technology's development and commercialization will not just extend Moore's Law, but will also drive the revolution of the entire semiconductor ecosystem for the next decade. ◆

DR. JOHN XIE has been with Altera Corporation for 12 years. He leads the packaging design engineering, process engineering and supply chain engineering team. Dr. Xie graduated from Department of Physics, Peking University, and holds a Ph.D. in Physics from Institute of Physics, Chinese Academy of Sciences and Post Doctoral from Department of Physics, University of California, Berkeley.

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presentation will outline how all these organizations and GSA work, jointly with their member companies, on developing open standards for 3D-IC planning, design and manufacturing as well as encourage broad standards adoption and cooperation.

Why Are Open Standards So Important for 3D-ICs?

Open standards begin when a collaboration of interested parties results in a consensus on specifications for implementing common requirements.

This is the first sentence of the article "Business Case for Open Standards" by Erik Sliman[1]. As mentioned above, the new 3D-ICs bring 2D designs in die-form – potentially from different sources – into much closer proximity than today's mounting of packaged 2D chips on a printed circuit board allows. However, it also increases power density, noise coupling, thermal-mechanical interactions and amplifies other effects, so far insignificant in 2D designs. It also requires new DFT (Design for Test) strategies, because the increased circuit complexities, combined with the limited number of access points makes test, failure analysis and debug more challenging.

During the transition from discrete components to LSI (large-scale integration) and VLSI (very large-scale integration) circuits we faced very similar challenges, due to the increased complexities, higher speeds and closer proximity of components. Our engineering experts developed design tools, equipment and methodologies to solve all these challenges, from the planning stage to final system test.

Within the last few years an increasing number of engineering teams have started to develop solutions for most of the new 2.5D and 3D IC challenges. Many of these development efforts focus on expanding proven 2D design, manufacturing or test methodologies, to minimize transition times, training efforts and switching cost. Some of the challenges, e.g. simulating thermal-mechanical interactions between thinned dies, TSV manufacturing, wafer thinning and handling, wafer probing, testing during stack-assembly, require new ideas and better solutions. Compared to the transition to LSI/VLSI circuits, a much closer cooperation between more companies is needed to develop and agree upon cost-effective and reliable design- and manufacturing steps. My presentation include an overview of how the various industry organizations are addressing these technical and business challenges.

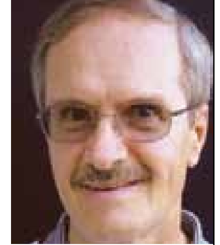
The Importance of Known Good Die

How to assure KGD (Known Good Die) is a very important topic for cost-effective 3D-ICs. Unlike in the 2D world where a bad die "only" makes the packaged part useless and worthless, in a 2.5D or 3D-IC one bad die renders the entire multi-die circuit worthless and causes very expensive yield loss. The second day of the MEPTEC symposium will focus on this and other topics relative to Known Good Die. ◆

(1) This article can be found at http://www.openstandards.net/viewOSnet1C.jsp?showModuleName=businessCaseForOpenStandards

HERB REITER is chair of the GSA's 3D-IC Working Group and GSA consultant since 2008. He founded eda2asic Consulting in the spring of 2002 to increase cooperation between EDA suppliers and semiconductor vendors. Previously Herb worked for 5 years in business development roles at Barcelona Design, Synopsys and Viewlogic. The PrimeTime sign-off wave and the TSMC reference flows # 1 and 2 are highlights of Herb's accomplishments at Synopsys. From 1980 to 1997 Herb worked in both business- and technical roles at VLSI Technology and National Semiconductor to manage alliances and market ASICs as well as ASSPs. Herb earned an MBA at San Jose State University and Master Degrees in Business and in Electrical Engineering at the University and at the Technical College in Linz/Austria, respectively.

OPINION



Industry-wide Cooperation Needed on Design & Manufacturing Standards for 3D-ICs

Herb Reiter, President
eda 2 asic Consulting, Inc.

Reiter will be a speaker at MEPTEC's upcoming symposium ***2.5D, 3D and Beyond – Bringing 3D Integration to the Packaging Mainstream*** *to be held on November 9. It will be co-located with the* ***Known Good Die conference*** *to be held on November 10. See pages 14-18 for more information.*

THE LUNCHEON MEETINGS AND conferences that MEPTEC organizes have turned into very important events for me, because both packaging and test-expertise are becoming much more valuable with the need to implement more functionality in smaller and smaller spaces. PoP (Package on Package) and SiP (System in Package) technologies have already demonstrated how to save space by using the 3rd dimension.

My current focus as consultant to the GSA (Global Semiconductor Alliance), who is a sponsor of this event, is to accelerate market acceptance and ROI (Return on Investment) for 2½D ICs (side-by-side die on an interposer) and 3D ICs (TSVs =Through-Silicon-Vias connect vertically stacked die). While these technologies offer additional benefits, compared to PoP and SiP, they confront our semiconductor eco-system with a range of new planning, design, manufacturing- and test challenges. These challenges and emerging solutions will be important topics at the MEPTEC symposiums on November 9 and 10. My contribution to this conference will focus on the need for and benefits of 2.5D and 3D design and manufacturing standards. I'll also outline why closer technical and business cooperation is needed within our semiconductor eco-system to make 2.5D and 3D ICs cost-effective and more widely applicable.

Moore's Law served us well for about 50 years. Continued feature-size shrinking of 2D (2-dimensional) ICs is becoming significantly more difficult, expensive, time consuming and risky with the 2x nm process generations. Many applications can't justify the rising up-front design and tooling efforts or the increasing variability of parameters nor the yield variations of ICs with today's smallest feature sizes. Many low to medium volume applications can be better served with one of the four implementation alternatives mentioned above. All four combine 2D ICs as building blocks in less space than they would consume when mounted on a printed circuit board and offer other compelling advantages, versus following Moore's Law, such as: Less power dissipation larger complexities, higher bandwidth and shorter latency, cost-effective integration of digital / analog / RF circuitry, extensive IP reuse and, when mature, much shorter time to market / profit.

System designers are especially interested in 2.5D and 3D ICs, because compared to PoP or SiP, they enable these experts to combine more functionality in a smaller space and reduce power consumption further while increasing speed. Designers can utilize legacy designs, in die form, as building blocks and take advantage of economical ways to increase memory – and with it enjoy more differentiating software content in their systems.

Eco-System Considerations

Our industry's most recent major eco-system change was the transition from an IDM-dominated semiconductor business model to a foundry- and fabless IC vendor cooperation. This move has since demonstrated much better ROI than the IDM model, but required some efforts to implement. Foundries and fabless IC vendors had to agree upon hand-off points, clear definitions for exchange formats, sharing of responsibilities and profit margins, logistics rules, etc.

The transition from 2D ICs to 2.5D and 3D-ICs faces similar challenges. To make 2.5D and 3D benefits widely applicable, enjoy economies of scale and lower cost, the design- and manufacturing companies engaged in this eco-system need to cooperate even more closely than the foundry & fabless model or the PoP and SiP designs require. For example: Thermal-mechanical interactions between silicon and copper traces as well as copper-filled TSVs need to be characterized by the manufacturers. Their impact on the thinned die needs to be reflected in the EDA design flows to help designers avoid excessive margins (= extra cost) or poor production yields, due to insufficient margins. You may think: "The few remaining big IDMs have a big advantage here. They don't have to worry about all these changes". Not really! These large corporations are also concerned about hand-off points, responsibilities, logistics, etc. between their own business units. In addition they want to be compatible with the "outside world" to take advantage of economies of scale, utilize 3rd party IP (in die-form), and buy common design tools and standard manufacturing equipment. Last but not least, they expect to minimize integration efforts if/when they acquire another 3D-IC vendor or a supplier.

The GSA was, in its previous form as FSA (Fabless Semiconductor Association), very active in facilitating and accelerating the "IDM to fabless" transition. Now the GSA is committed to do the same for the equally important transition to 2.5D and 3D-ICs. In 2008 GSA formed the 3D-IC Working Group and attracted many participants from the entire semiconductor eco-system to facilitate and accelerate this transition. We also cooperate well with other industry organizations (e.g.: CEA/Leti, EDAC, IEEE, IMEC, ITRI, JEDEC, MEPTEC, SEMI, Si2 and especially the 3D Enablement Center, driven by Sematech, SIA and SRC) to complement these organizations and amplify the GSA's impact. My

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