MEPTEC Report

FALL 2013

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 17, Number 3

MEPTEC CELEBRATES 35 YEARS OF SERVING THE INDUSTRY

SPECIAL REPORT: CHINA'S IMPACT ON THE SEMICONDUCTOR INDUSTRY

page 17

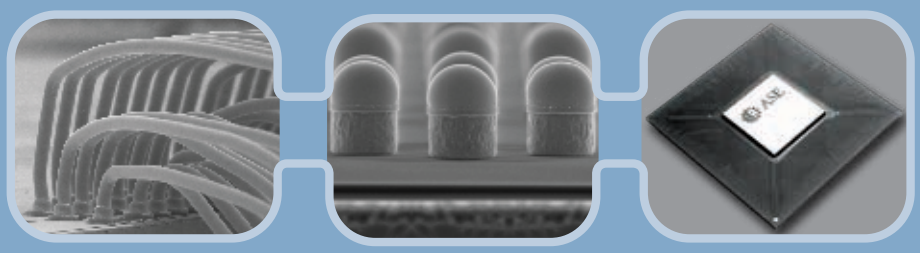
Unisem's turnkey services include design, assembly, test, failure analysis, and electrical and thermal characterization.

page 20

INSIDE THIS ISSUE

ASE GROUP

ASE Group: The world's largest provider of independent semiconductor manufacturing services in assembly, test, materials and design manufacturing.



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A Lesson in the Value of Industry Organizations

Jeffrey C. Demmin
Director OEM Marketing
STATS ChipPAC, Inc.
MEPTEC Advisory Board Member

WHEN IT COMES TO PARTICIPATION in industry organizations such as MEPTEC, I have seen two schools of thought. Most people think that there is probably some value to it, but it is just too hard to fit in anything very meaningful. The "day job" prevents many of us from going to that lunch meeting or volunteering for a conference. The other view is that it is absolutely worth prioritizing, and not just to give back to the industry or learn about technical trends, but also for the very real benefits of the networking. I learned to appreciate the latter view in a highly tangible way when I found myself "between jobs" recently.

Most of us have had to look for employment with some urgency at some point in our careers, and we all know that personal connections are the most likely path to success in that campaign. I was surprised, though, at the extent to which this was true. Over the course of my job search, I kept a running list of the opportunities that I uncovered, and anyone who knows me can probably picture the spreadsheet tracking each opportunity and status, with filters by industry, color coding by location, and sorting by the timing of the next step. The most important column, though, was the one listing the contact associated with each opportunity. It became clear that in those 200+ rows on that spreadsheet, I was making progress only on those with someone I knew in the "contact" column. In fact, there were only two opportunities where I got any kind of reply without already knowing someone there. So much for the automated resume processing systems that link people with dozens of jobs for which they are a perfect match!

It was clear that this job search was the scenario where I could put all of that networking to a real test, and my network came through in a big way. Alumni connections were a good way to get through the first door. My service as the general chair of the IMAPS conference a few years ago let me ping a bunch of marketing folks. My time as an editor helped me contact the analyst community for opportunities and ideas. Volunteering is a good networking tool too – I proofread a whole book for free, just to make some new connections. Even staying in touch with the National Semiconductor packaging group from a long time ago – the Reagan administration – was a useful avenue. Perhaps most importantly, my contribution to the MEPTEC Advisory Board since joining in 2000 really let me leverage a group of very well-connected and active individuals. And, you never know where that useful connection will come from. I honestly got more interviews from chatting with parents on the sidelines of my kids' soccer games than I did at all of the companies where I didn't already know someone. (Another reason to be nice to your spouse – all of those sideline discussions were started by my wife.)

> Electronic connections and visibility on the internet are certainly important these days, but real connections with real people and real hands to shake cannot be replaced.

Bottom line … it really is all about the personal connections, and that's even more true today than ever when it's so easy to apply for jobs electronically – and so easy for you to get steered to the discard pile based on a keyword search or some checkbox criteria. All of those applications appear to swamp each other out, with the beleaguered recruiter or HR professional looking for ways to rule out 90% of the applicants, leaving "only" several dozen to process manually. (A favorite pastime during the job search was seeing how many hundreds of people applied to the really good sounding jobs posted on LinkedIn. It was equally alarming to realize that this was only one avenue for applications, so there must have been some jobs with the applicant count running into four figures!)

Electronic connections and visibility on the internet are certainly important these days, but real connections with real people and real hands to shake cannot be replaced. Participating in the activities of MEPTEC or any other industry organization – whether as a volunteer or an attendee – is a great way to build and maintain your network. I definitely recommend prioritizing such activities, and not just for the stressful times when you need all the connections you can get, like I did earlier this year. Those connections might increase your value in your current job too. You never know how exactly all of that will work, but you can be pretty sure that time invested in an organization like MEPTEC will look like a great investment sometime in your career. ◆

JEFF DEMMIN is the Director of OEM Marketing at STATS ChipPAC. Before that he worked at Tessera Technologies in marketing, corporate development, and IP acquisition. He was previously the Editor-in-Chief of Advanced Packaging magazine and Senior Technical Editor of Solid State Technology magazine. His career started in semiconductor package design at National Semiconductor, and a sequence of engineering roles at nCHIP, Seagate, and Textron followed. Jeff earned a bachelor's degree in Physics from Princeton University and a master's degree in Materials Science from Stanford University.

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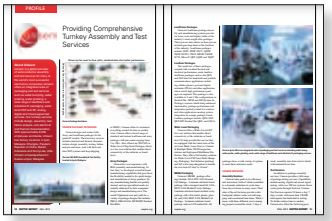
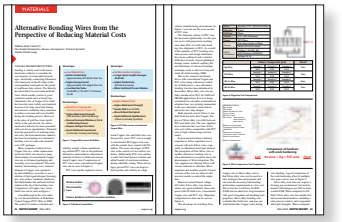
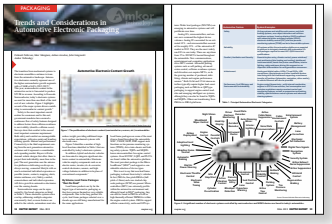
ON THE COVER

MEPTEC CELEBRATES 35 YEARS OF SERVING THE INDUSTRY – The benefits of belonging to an industry organization can be many. MEPTEC Advisory Board Member Jeff Demmin shares his recent experience with "A Lesson in the Value of Industry Organizations" on page 3. Also of note in this issue is the Special Report: "China's Impact on the Semiconductor Industry" on page 17, presented by Ed Pausa of PricewaterhouseCoopers.







DEPARTMENTS

MEPTEC
THE NEXT GENERATION

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Altera Announces Breakthrough Advantages with Generation 10

ALTERA CORPORATION has introduced its Generation 10 FPGAs and SoCs, offering system developers breakthrough levels of performance and power efficiencies. Generation 10 devices are optimized based on process technology and architecture to deliver the industry's highest performance and highest levels of system integration at the lowest power. Initial Generation 10 families include Arria® 10 and Stratix® 10 FPGAs and SoCs with embedded processors. Generation 10 devices leverage the most advanced process technologies in the industry, including Intel's 14-nm Tri-Gate process and TSMC's 20 nm process. Early access customers are currently using the Quartus® II software for Generation 10 product development.

"Our Generation 10 products will strengthen the penetration of programmable logic into new markets and applications and further accelerate the implementation of FPGAs into systems traditionally served by ASSPs and ASICs," said Patrick Dorsey, senior director of product marketing at Altera. "The optimizations we made in our Generation 10 devices allow customers to develop highly customized solutions that dramatically increase system performance and system integration while lowering operating expenses."

Stratix 10 FPGAs and SoCs are designed to enable the most advanced, highest performance applications in the communications, military, broadcast and compute and storage markets, while slashing system power. Leveraging Intel's 14 nm Tri-Gate process and an enhanced high-performance architecture, Stratix 10 FPGAs and SoCs have an operating frequency over one gigahertz, 2X the core performance of current high-end 28 nm FPGAs. For high-performance systems that have the most strict power budgets, Stratix 10 devices allow customers to achieve up to a 70 percent reduction in power consumption at performance levels equivalent to the previous generation.

Early access customers are currently using the Quartus II software for development of Arria 10 FPGA and SoCs. Initial samples of Arria 10 devices will be available in early 2014. Altera will have 14 nm Stratix 10 FPGA test chips in 2013 and Quartus II software support for Stratix 10 FPGAs and SoCs in 2014.

For more information, visit www.altera.com/gen10, or contact your local Altera sales representative. ◆

LSI Delivers Axxia® 5500 Communication Processor for Faster, More Power-Efficient Networks

World's first cache-coherent, 16-core SMP ARM processor

LSI CORPORATION HAS announced it has started delivering the Axxia® 5500 communication processor family to key OEM customers. The Axxia 5500 with 16 ARM cores is designed to meet the performance, integration, cost and power demands of mobile and fixed networks.

The Axxia 5500 family of communication processors offers a number of benefits to datacenter operators, enterprise network managers and network service providers, including:

- Outstanding performance efficiency through a flexible combination of general-purpose processors and specialized acceleration engines
- High-capacity Ethernet switching to drive significant reductions in power, board space and bill of material cost
- Increased network performance through a unique combination of power-efficient ARM Cortex™-A15 processors and CoreLink™ CCN-504 Cache Coherent Network interconnect
- Flexible connectivity provided through the 16 10GbE interfaces
- Comprehensive tool suite and production-quality protocol processing software modules for wireless infrastructure applications

"With AXM5500 in hand, our customers are developing next-generation networking systems with the performance, intelligence and scalability to keep pace with the unprecedented growth in network traffic," said Gene Scuteri, vice president of engineering, Networking Solutions Group, LSI. "The Axxia 5500 multicore family, with its unmatched, highly integrated design and broad features, is an ideal platform on which to build high-performance systems."

More information is available at www.lsi.com. ◆

MEMBER NEWS

AMKOR APPOINTS JOHN STONE AS EXECUTIVE VP FOR GLOBAL SALES AND MARKETING

Amkor Technology has announced that John Stone has been appointed to serve as Amkor's Executive Vice President for Global Sales and Marketing, effective immediately.

Mr. Stone joined Amkor in 2002 and has served in various senior sales management positions during his time with the company. Mr. Stone has a B.S. in Engineering from Purdue University and over 30 years of industry experience in semiconductor package engineering, sales, and sales management. Mr. Stone succeeds Mike Lamble who has left the company after 21 years of service.
www.amkor.com

ASE OPENS WEIHAI PHASE 3 MANUFACTURING FACILITY

Advanced Semiconductor Engineering has celebrated the official opening of its Phase 3 manufacturing facility in Weihai, Shangdong province, China. The new building is part of ASE's expansion plans to increase its manufacturing capacity for discrete packaging and test.

The official opening ceremony was hosted by Dr. Tien Wu, chief operating officer of the ASE Group and J.H. Lee, general manager of ASE Weihai. The event was also graced by senior officials of Weihai city including Mr Tang Guan Yuan, vice

mayor and Mr Zhang Jian Jun, director of the economic development zone.

The new building occupies a land space of 5,120 square meters with a built up floor space of 30,560 square meters. ASE plans to recruit an additional 2,000 employees in engineering, development and operations for the new facility.

www.aseglobal.com

NEW INTERACTIVE WEBSITE LAUNCHED BY GEL-PAK

Gel-Pak, a division of Delphon Industries and leading manufacturer of device shipping and handling carriers has announced the launch of its new interactive website. The site can be accessed at www.gelpak.com.

"The new site was designed with our customers in mind", said Darby Davis, Vice President Sales & Marketing. "It offers a simplified navigation system and makes it easier for customers to find the best carrier for a particular application." The site includes extensive product information to help customers understand Gel-Pak's complete range of device handling solutions.

www.gelpak.com

LSI ANNOUNCES FIRST EVER CASH DIVIDEND

LSI Corporation has declared a quarterly cash dividend of $0.03 per common share. The dividend is payable on September 20, 2013, to stockholders of record on September 6, 2013.

Entegris' Full Suite of 450 mm Wafer Handling Products Selected by Global 450 mm Consortium at SUNY's NanoCollege

ENTEGRIS, INC. HAS announced that its handling and shipping products for the safe, reliable transport and processing of 450 mm wafers were selected by the Global 450 mm Consortium (G450C), headquartered at SUNY's College of Nanoscale Science and Engineering (CNSE) in Albany, New York, for use in the development of 450 mm wafer technology.

G450C is a public-private partnership announced by New York Governor Andrew M. Cuomo in September 2011 to facilitate the 450 mm wafer size transition. It is spearheaded by CNSE in partnership with Intel, IBM, GlobalFoundries, Samsung and TSMC. The new 450 mm cleanroom is located at CNSE's Albany NanoTech Complex within the NanoFab Xtension (NFX) expansion.

The Entegris products selected by the G450C comprise a comprehensive wafer handling solution that includes 450 mm Multiple Application Carriers (MAC), 450 mm Front Opening Pod (FOUP), 450 mm Single Wafer Shippers (SWS), and an innovative packaging system. As part of its agreement with the G450C, Entegris has agreed to provide on-site service which will allow G450C to fully leverage Entegris' industry recognized expertise in engineering wafer handling solutions, ensuring G450C maximizes efficiency and accelerates the proliferation of 450 mm processes.

Bill Shaner, vice president and general manager for Entegris' Microenvironments Division, said: "As the industry pioneer in wafer shipping and wafer processing products, it was important for Entegris to collaborate with G450C, which is leading the global transition to 450 mm wafer technology, to provide early solutions for transporting these larger wafers. Our 450 mm development efforts, which began in 2007, have resulted in innovative and differentiated technology that will serve the needs of the industry's leading companies as they ramp up 450 mm operations."

Additional information about G450C can be found at www.g450c.org.

Visit Entegris website at www.entegris.com. ◆

Entegris, Inc. and 3S Korea Co., Ltd. Enter into Partnership

ENTEGRIS, INC. AND 3S Korea Co., Ltd. announced their partnership for the sale of 450 mm wafer handling products to customers in Korea. Entegris will manufacture its 450 mm wafer handling and shipping products for 3S on a private label co-branded basis and 3S will have the exclusive rights to promote and sell the 450 mm products to Korean customers.

The products covered by this collaboration include the 450 mm Front Opening Unified Pod (FOUP), 450 mm Multi Application Carrier (MAC), 450 mm Single Wafer Shipper (SWS) and related secondary packaging systems used with 450 mm products.

Visit www.entegris.com and www.3sref.com for more.

Toshiba and Amkor Technology Complete Amkor's Acquisition of Toshiba's Malaysian Semiconductor Packaging and Test Operations

TOSHIBA CORPORATION and Amkor Technology, Inc. have announced that the companies have completed Amkor's acquisition of Toshiba Electronics Malaysia Sdn. Bhd. ("TEM"), Toshiba's semiconductor packaging operation in Malaysia. The transaction also includes Toshiba's license to Amkor of related intellectual property rights and a manufacturing services agreement between Toshiba and Amkor.

Under the manufacturing services agreement, Toshiba has agreed to purchase and TEM has agreed to supply packaging and test services for certain discrete semiconductor products and analog LSI products.

Established in 1973, TEM has steadily expanded the scale of its packaging operations, primarily of discrete and analog semiconductors. In recent years, its main product has been power semiconductors.

Toshiba positions power semiconductors as a driver of growth for its semiconductor business and seeks to maximize cost competitiveness across its front- and back-end operations. Transferring ownership of TEM to the Amkor group will allow TEM to take full advantage of Amkor's large scale production and materials procurement capabilities and boost the overall efficiency of its power semiconductor operations.

Toshiba will continue to subcontract power semiconductor packaging and test to Amkor as an important source of key products. As it does so, Toshiba will shift its focus and resources to front-end wafer fabrication for power semiconductors by reinforcing production capabilities at Kaga Toshiba Electronics Corporation, Toshiba Group's discrete semiconductor production facility in Ishikawa Prefecture, Japan.

Amkor expects the transaction to further strengthen its relationship with Toshiba and to grow its semiconductor packaging and testing business. Visit Amkor's website at www.amkor.com for more information. ◆

STATS ChipPAC Celebrates 1,000th U.S. Patent Milestone

Commitment to innovation and strong focus on advanced wafer level technology deliver broad portfolio of intellectual property

STATS CHIPPAC LTD. HAS announced that it has been granted its 1,000th patent by the U.S. Patent and Trademark Office (USPTO).

Since the inception of its Intellectual Property (IP) program in 2000, STATS ChipPAC has filed more than 1,500 patents and published patent applications with the USPTO and more than 900 patents and applications in other countries, of which more than 200 have been registered or allowed as patents in Singapore, South Korea, Taiwan and other countries. This is at least 400 more U.S. patents and applications than other companies in the global Outsourced Semiconductor Assembly and Test (OSAT) industry. STATS ChipPAC has concentrated its IP development on advanced or future technologies such as wafer level packaging, Post Wafer fab Processing (PWfP) or mid-end processing, Through Silicon Via (TSV), flip chip interconnect, integrated passive devices (IPD) and 2.5D/3D package integration. With this strategic focus, STATS ChipPAC has built up a patent portfolio in which advanced or future technologies comprise 60% of its IP.

STATS ChipPAC's patent portfolio has been recognized for its quality, strength and overall importance to the semiconductor manufacturing industry by The Institute of Electrical and Electronics Engineers (IEEE), the world's largest professional association for the advancement of technology. IEEE ranked STATS ChipPAC among the top 10 semiconductor manufacturing companies in the world for the last two consecutive years based on the strength of its IP and technology innovations.

STATS ChipPAC's 1,000th U.S. patent is a strong representation of the priority the Company has placed on the development of advanced wafer level technology. U.S. Patent No. 8,456,002, "Semiconductor Device and Method of Forming Insulating Layer Disposed Over the Semiconductor Die for Stress Relief", relates to innovations in the assembly of embedded Wafer Level Ball Grid Array (eWLB) devices in which an insulating layer provides stress relief during the formation of an interconnect structure in the device. This is part of a family of patents that includes five previously granted U.S. patents for eWLB and Wafer Level Chip Scale Packaging (WLCSP) inventions.

For more information about STATS ChipPAC visit www.statschippac.com. ◆

The dividend will be paid from U.S. earnings and is expected to be treated as dividend income to stockholders for U.S. tax purposes, although the final determination of the tax treatment of the dividend will be made after LSI's fiscal 2013 year end.

LSI intends to pay a regular quarterly cash dividend on its common stock. Future dividends will be subject to Board approval.

www.lsi.com

MICROSS ACQUIRES PREMIER SEMICONDUCTOR SERVICES

Micross Components is pleased to announce the acquisition of Premier Semiconductor Services LLC, a semiconductor services contractor with facilities in Tempe, AZ; Austin, TX; and Clearwater, FL.

Premier Semiconductor supports IC component manufacturers, distributors, contract manufacturers, and OEMs with electrical testing, lead-free and Pb conversion, burn-in, IC programming, IC counterfeit detection, and other back-end IC services. Micross acquisition of Premier supports the companies commitment to provide the finest and most complete range of high-reliability and custom solutions available from any one source for the global marketplace. Premiers capabilities, markets and values complement Micross dedication to integrity, excellence and empowering customer innovation.

www.PremierS2.com
www.micross.com

PLEXUS EXPANDS IN GUADALAJARA, MEXICO

Plexus Corporation has announced that it intends to begin operations in Guadalajara, Mexico, and has entered into an agreement to lease a 265,000 square feet manufacturing facility. The leased building will be built for Plexus by Corporate Properties of America and will be located in the Guadalajara Technology Park. This facility will become a part of Plexus' global network of 24 integrated facilities, providing customers with electronics design, manufacturing and sustaining solutions.

Construction of the facility will begin in August 2013 with expected completion during the fiscal third quarter of 2014.

www.plexus.com

UNISEM AND ACCOTEST TO OFFER 8200 TEST SYSTEM IN SUNNYVALE, CA FOR ENGINEERING AND PRODUCTION SERVICES

Unisem will be adding an AccoTEST 8200 test system to its test facility in Sunnyvale, California, starting in September 2013. The AccoTEST 8200 is a low-cost multisite linear, analog, and mixed signal test system that provides similar or better test capability at a much lower cost with higher throughput.

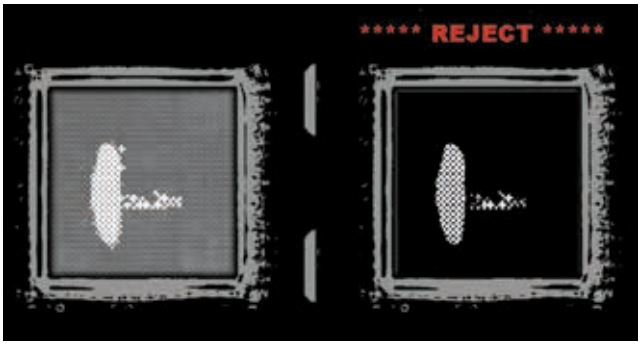
A training course for the AccoTEST 8200 will be held at Unisem Sunnyvale in early September, as part of the launch.

www.unisemgroup.com ◆

Digital Image Analysis Toolbox from Sonoscan

SONOSCAN ANNOUNCES its enhanced Digital Image Analysis Toolbox™ used for automated acoustic analysis of individual IC components, various types of bonded wafers including MEMS devices, and other devices. The DIA Toolbox is used for sorting components automatically into accept/reject or multiple defined categories. It contains many pre-defined common analysis tools, such as:

1. Interface analysis: Non-destructively determines the bond between two surfaces in a package - mold compound to die, for example, or solder bump to die face
2. Wafer bond analysis: Used to quantify the number of voids or non-bonds between two bonded wafers. It can count and sort defects of specific sizes and determine pass/fail criteria based on the quantity or location distribution of each size.
3. Chip on wafer analysis: Measures the quality of the bumps and underfill between the chip and the wafer and outputs a location-specific report.



Scanned image (left) of flip chip is binarized (right) for analysis.

The tool has multiple wizards to quickly establish inspection parameters. The wizard walks the operator through the pre-defined inspection parameters and establishes the inspection criteria rapidly.

Additionally, the user has the ability to easily create new tool variations. Sonoscan also offers customization of the analysis and wizards to meet specific customer needs.

Many standard output formats from the DIA Toolbox can be customized for the laboratory, factory or associated equipment.

Because placement of a component can be imperfect, the DIA Toolbox has a search and locate function. It looks for specific component features (or the edges of features) and uses these to accurately adjust and align the inspection area over the device.

The DIA Toolbox is a very versatile automated inspection capability available on all of Sonoscan's equipment.

Visit www.sonoscan.com for more information. ◆

FINEPLACER® femto Provides Advanced Packaging Capabilities at C2MI

Bonding system installed at MiQro Innovation Collaborative Centre in Canada

FINETECH AND THE MiQro Innovation Collaborative Centre (C2MI) located in Bromont, Québec, Canada, have announced that C2MI has installed a FINEPLACER® femto bonding system in its advanced packaging sector. This automated, sub-micron accuracy system is designed to position and attach small electronic or opto-electronic components on printed circuit boards or substrates.

C2MI, as a Centre of Excellence, provides a state-of-the-art infrastructure for the benefits of its members. This high-technology hub provides support so that innovative concepts can be promptly commercialized. C2MI is active in die-level packaging, complex microsystems, 3D design integration and MEMS development.

With a wide base of systems installed at many prestigious institutions and research centers, Finetech's die bonders provide unmatched solutions for advanced technology environments utilizing diverse applications. The FINEPLACER femto is a fully automated, sub-micron bonding platform that is ideal for product and process development of laser diodes, laser bars, VCSELs, photo diodes, sensors, LED bonding, MEMS, flip chip and micro optics assembly. Bonding technologies supported by the system include thermocompression, thermosonic, ultrasonic, adhesives, curing and soldering (AuSn, C4, Indium, eutectic).

The MiQro Innovation Collaborative Centre (C2MI) is an international reference in the fields of advanced packaging and microsystems. Visit www.c2mi.ca for more. ◆

Altera Demonstrates Interlaken Connectivity with Cavium OCTEON® Multicore Processors

ALTERA CORPORATION HAS announced the interoperability of its Interlaken intellectual property (IP) core on Stratix® V FPGAs with Cavium's OCTEON multicore processors. This accomplishment simplifies an OEM's device decision-making process by ensuring chip-to-chip connectivity upfront.

"Altera's flexible Interlaken IP enabled us to quickly show interoperability between our products," said John Bromhead, director, Solutions and Services at Cavium. "This solution gives our customers the added assurance that when they develop with Altera FPGAs and Cavium's OCTEON processors, the devices will work seamlessly together. The ease of interoperability also helps customers meet tight time-to-market windows."

The Altera Interlaken IP core is ideal for multi-terabit routers and switches for access, carrier Ethernet and data center applications that demand IP configurability to optimize for various traffic profiles, and scalability for next-generation platforms.The Interlaken IP includes Altera's technology-leading transceivers (PMA), PCS, and MAC layers. The PCS layer is hardened within the Stratix V and Arria® V FPGAs, thereby saving customers 30 to 50 percent on FPGA logic resources. In addition to resource savings, the Interlaken IP has been through extensive simulation verification and has been proven to work on internal and customer platforms.

Altera® programmable solutions enable designers of electronic systems to rapidly and cost effectively innovate, differentiate and win in their markets. Altera offers FPGAs, SoCs, CPLDs, ASICs and complementary technologies, such as power management, to provide high-value solutions to customers worldwide. Follow Altera viaFacebook,Twitter,LinkedIn,Google+ and RSS, and subscribe to product update emails and newsletters.

Visit altera.com for more. ◆

Fairchild Appoints Catherine Lego to Board of Directors

FAIRCHILD SEMICONDUCTOR HAS announced that Catherine P. Lego has joined the company's board of directors.

"I am delighted to announce the appointment of Catherine Lego to our board," said Mark Thompson, Fairchild's chairman and CEO. "Cathy's depth of industry knowledge and experience, financial, accounting and business development expertise, and interest and commitment to corporate governance, will be great additions to our board. We are fortunate to have her on our team, and we look forward to working with her."

Lego is a member of the boards of directors, and chairs the audit committees, of SanDisk Corporation and Lam Research Corporation. She will join Fairchild's nominating and governance committee and compensation committee.

Lego, 56, holds a B.A. in economics and biology from Williams College and an M.S. in accounting from the New York University Graduate School of Business.◆

SV Probe Acquires Assets from Tokyo Cathode Laboratory

SV PROBE PTE. LTD. ANNOUNCED that it has entered into a business transfer agreement to purchase certain probe card business, technologies, intellectual property rights and assets of Tokyo Cathode Laboratory. This acquisition will create a stronger product portfolio for SV, place the company in a more competitive position within the IC testing market and give SV Probe a significant advantage with access to the large Japanese probe card market.

SV Probe will acquire TCL's shares in its subsidiaries in Singapore, Taiwan, Hong Kong and Guangzhou, China, along with the assets and business of TCL and its Japan subsidiaries, held or used in the marketing, manufacturing and distribution of certain probe card products. TCL is a probe card manufacturer based in Japan with a substantial production and distribution network across Asia. TCL possesses strong probe card capabilities, specifically CMOS Image Sensor (CIS) and Liquid Crystal Displays (LCD). TCL has developed proprietary cantilever probe materials along with build and assembly processes that extend the capability of its products utilized in different device testing applications. As a result, TCL has gained a number of key CIS, LCD, and logic/SOC customers in Japan and throughout the Asian market.

"TCL's extensive knowledge in probe card technologies and strong customer relationships will create new revenue opportunities for SV Probe," said Mr. Kevin Kurtz, President & CEO of SV Probe. "This acquisition will enable SV Probe to increase its participation in the valuable and significant Japanese probe card market."

Mr. Naotake Okubo, CEO of TCL, discussed the acquisition, "Currently TCL is undergoing Civil Rehabilitation Process. This business transfer agreement will enable our customers to continue receiving high quality products and services from a committed and experienced probe card manufacturer with minimum disruption to their business activities."

For more about SV Probe visit their website at www.svprobe.com. ◆

STATS ChipPAC Delivers Industry Leading Ultra Thin Package-on-Package Solutions with eWLB Packaging

Recent advances in embedded wafer level packaging technology reduce bottom package height to less than 0.3mm for an overall PoP stack height as low as 0.8mm

STATS CHIPPAC HAS ANNOUNCED a new milestone in reducing Package-on-Package (PoP) height with its ultra thin embedded Wafer Level Ball Grid Array (eWLB) technology. STATS ChipPAC has pursued innovative advances in embedded packaging design methodology, process enhancements and cost structure to deliver eWLB-based PoP solutions with an ultra thin package profile height of 0.3mm.

The industry adoption of PoP as a dominant packaging approach in stacking the logic processor and memory into a single solution for advanced mobile phones and tablets has accelerated the need to drive ultra thin package profiles in this technology. Earlier in 2012, STATS ChipPAC utilised eWLB technology to deliver a 30% height reduction in PoP, reducing the overall stacked package height from the industry standard 1.4mm to 1.0mm. Today, through further innovations in eWLB technology, STATS ChipPAC has achieved a 40% height reduction in the bottom PoP architecture to provide an ultra thin z-height of 0.3mm, thereby providing customers with the advantage of having an overall PoP package height as low as 0.8mm with proven board level reliability.

"The emergence of ultra slim devices that are able to deliver exceptional performance continues to grow across the mobility, consumer and computing markets. Our breakthrough technology achievements in package height reduction, increased performance and reliability with eWLB-based PoP solutions enable packaging solutions that provide a competitive edge to substrate-based PoP solutions while remaining cost effective," said Dr. Han Byung Joon, Executive Vice President and Chief Technology Officer, STATS ChipPAC. "We have successfully developed best-in-class, ultra thin PoP solutions below 1.0mm to support the continued success of our leading-edge mobility customers and will continue to extend our innovative technology to attain even smaller form factors in semiconductor packaging technology."

eWLB provides a robust packaging platform supporting ultra high density interconnection and routing of multiple die in very reliable, low-profile, low-warpage packages that are cost effective solutions for baseband processors, RF transceivers, power management components and application processors. For high performance applications such as smartphones and tablets, eWLB technology delivers fine line width and spacing of less than 10um/10um as well as superior electrical performance, providing more design flexibility and a more significant reduction in size than is possible with printed circuit board (PCB) substrate technology.

Further information is available at www.statschippac.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions like this one may deliver a message closer to home.

Priorities First! Or Last? Or Not All?

DO I CONFUSE BEING BUSY WITH being productive? Does being efficient help me reach my goals? What should my goals be?

Maybe I'm too much of a management geek since I spend my "lazy" summer days thinking about these topics instead of working on my tan. Okay, truth be told I don't have many "lazy" summer days and I certainly don't worry about my tan but I do think about these questions and more…

Most of us have our own "management" or "productivity" systems. Some may follow Ivy Lee's famous advice to Charles M. Schwab of Bethlehem Steel **"to write down your top six priorities, in order, for tomorrow and do nothing but them in sequence!"** Others may use David Allen's Getting Things Done (GTD) methodology "for stress free productivity" to which I'm partial. And there are those who work in a chaotic stream of consciousness fashion but may be mistaken for a whirling dervish.

The weakness with all these systems is one's self control to stay on course all (or most of) the time. In today's hyperconnected world, I cannot image most professionals – let alone a C-level executive – being able to focus exclusively on six priorities in order per Mr. Lee. Maybe one or two priorities for a short *[Ed note: Phone rings, author answers. Author then goes off to check email messages that just arrived.]* period of time perhaps enabled by an administrative assistant with the demeanor of a stone wall. It may not only be the lost ability to focus but the continual flow and interruption of data that often changes one's priorities. The world has changed significantly from the one character per second ticker tape world Mr. Lee departed in 1934.

With ever shifting priorities, **it is important to remember the difference between tactics and strategy.** *[Ed note: Author is distracted responding to a text message.]* Priorities are the order in which tactics need to be tackled based on current urgency and importance. Tactics are set based upon short-term actions and reactions whereas strategy is one's overarching high-level goals which should not change on a short-term basis. Typical strategic questions are: What markets should your company pursue? What should be your career progression? How to pay for your child's higher education in ten years?

Tactics are the steps of what activities need to happen – and in what order – to achieve these strategic goals. Tactical examples include: perform a market survey to identify which markets to enter, earn a Masters of Business Administration (MBA) degree to increase the likelihood of being promoted to an executive position, and stop buying coffee at the coffee bar in order to save the money for a college fund. *[Ed note: Author has just gotten up to refill his tea.]*

When you are busy fighting the "good fight" or even the "daily grind", **you may be too focused on your priorities and tactics to step back and worry about strategy.** Large companies often have the luxury of sufficient staffing with people solely focused on "strategic" planning and review. (Of course, the role of "Vice President of Strategic Planning" might cover a multitude of activities beyond planning sometimes akin to a minister without portfolio.) Regardless of staffing, better performing companies, small or large, often rely on a regular planning cycle, sometimes with the help of outside consultant(s), to perform strategic planning. Yes, the team may gripe about doing the work to prepare since it is time away from their tactical work but without it they may never get "out of the trenches."

As one adjusts strategy and/or tactics, human nature due to *loss aversion* biases us against making efficient choices where cost has been sunk. You may have worked very hard on a project or spent a lot of money purchasing equipment. However, from a pure economic and business decision framework sunk costs are irrelevant. **Decisions need to be made on the present value** of past work or costs **and opportunity cost.**

We do not like to concede that many things are not worth what we paid for them even if we know they depreciate. Reality often sets in when we ask someone else to value an item. It is far harder to recognize that past time "invested" is also a sunk cost since you will never get it back. **Like a good poker player, you need to know when to hold and when to fold!** (If you really hate a movie twenty minutes in, aren't you better off leaving the theatre early regardless of ticket price and otherwise enjoy your time?)

Time is one of the most precious commodities (for you and your company) and you need to carefully examine the return on investment for all activities. How do these activities fit into your tactical plan and how well do they align with your strategy? Yes, some professionals make commitments that no longer fit their priorities due to changes in tactics or strategy. Instead of becoming known as someone who over commits but does not deliver, a true professional finds creative ways to gracefully adjust the commitment to everyone's satisfaction.

Summer vacations often provide a good time to "disconnect" from the daily chaos and data overflows. Even if you only have a week planned, take time to step back and contemplate both personal and work strategies. This way you can adjust your tactics and reset your priorities when you return. Of course, resting and relaxing may seem wasteful but we do all need downtime for good health. Please pass me my piña colada; I need to go float in the pool… *[Ed note: Author leaves smartphone on desk unanswered.]*

Let us continue the discussion on my blog http://hightechbizdev.com. I welcome your comments! ◆

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MICROTECH IN HEALTHCARE

By Sam Bierstock, M.D.

Don't Kill the Messenger

AS ONE OF THE FEW PHYSICIANS-informaticists deeply embedded in the MEMS and sensor industries, I find myself in a unique position of being able to deliver this cautionary message. As a consultant to healthcare technology companies of all sizes, and to electronic health record (EHR) and personal health record system (PHR) vendors, I have watched industries peripheral to healthcare dive into the market with absolute confidence about their eventual success, only to flounder and end up on the roadside. Physician adoption of EHRs went nowhere for more than a decade, and is only now getting a foothold because of governmental meaningful use mandates. Without the mandates, adoption would be running about where it was – around 30%.

The MEMS and sensor industries will revolutionize healthcare diagnostics, care delivery, data warehousing and analysis, but the path to this eventual outcome may be either wisely chosen or tortuous. Why have start-ups and mega-entities done so dismally in healthcare? For one simple reason: failure to comprehend what it is like in the trenches – how physicians and other end-users think and act; knowing what it is like to bear the responsibilities for someone's life and wellbeing with every decision and action; being scrutinized for every thought and deed; understanding the thought processes based upon a combination of education, experience and currency (one new article appears in the medical literature every minute – or 45,000 per month): truly understanding that every patient is different and that *caring for them is a human interaction – not an algorithm*.

What seems like a golden solution to technicians, inventors, and entrepreneurs may have nothing to do with making life easier for physicians and may, in fact, create nightmares for them. Thousands of EHR and PHR designers have put millions of hours and billions of dollars into workflow designs that make physicians lives miserable and slow down their productivity.

EHRs in emergency rooms add an average 40% loss of physician productivity and result in between 30 and 40% of the number of people who leave without being seen. They look good in the lab, and conform to the textbooks, but have nothing to do with the world of delivering care.

Healthcare is an industry that can only be fully understood from the inside.

Yet I attend MEMS and sensor meetings and hear technologists talk about the future of healthcare being comprised of data collection via sensors and differential diagnoses and treatment recommendations generated by IBM's Dr. Watson. In fact, such roads to treatment would lead to millions of uselessly expended dollars and lost hours that could otherwise bring forward truly creative products.

I often hear others proclaim with fervor that patients have a right to know everything about their health. If you have ever practiced medicine you know that it just doesn't work that way. The fact that people have a right to information has nothing to do with how they handle it or their need for emotional support and guidance based upon experiential expertise. Produce a hand-held ultrasound device that projects an image to a smartphone and make it generally available and you will happily satisfy the right of patients to know everything about their health and simultaneously create chaos. What happens when a pregnant woman decides to take a look at her unborn child and sees what looks to her like an extra arm or a misshapen head? The result will be a panicked call to the doctor, or an unnecessary emergency room visit in an already overburdened system – not to mention the associated cost to the system and anxiety provoked. Every time a man with chest pain decides not to seek medical care because his smartphone EKG app shows a normal pattern, but dies because it didn't show the pulmonary embolism, or the aortic aneurysm – someone will be held responsible. Who will be held to task when someone's vital signs or more sensitive medical information shows up on Facebook – a clear and punishable violation of privacy and security mandates?

Readers of this publication can relate to the importance of industries working together to solve problems. There wasn't always a time when semiconductor designers, manufacturers and assemblers work together as closely as they do now. This collaboration of the different segments of the industry was, and still is, a very successful partnership. In much the same way, with the explosion of devices and apps for healthcare, the microtechnologists, the physicians and even the ultimate "end user"– the patients – need to work more closely together to make sure the issues raised above are carefully addressed.

Healthcare is not a digital science – there are deep human factors in both the delivery and receipt of health care. My message to the MEMS, sensor and other emerging micro-technology industries is a clear one: Don't get too caught up in your own convictions. Bring in the medical industry experts (not just your physician friend or a doctor you know) and end-users and people who understand just what your product can do and how it will be best applied to contribute to the delivery of healthcare. These are not decisions to be made from the fringe.

In future columns I will address these challenges and issues more fully. If you have some thoughts on the subject please e-mail me at samb@championsinhealthcare.com – I would appreciate your input! ◆

SAM BIERSTOCK is the president and founder of Champions in Healthcare (www.championsinhealthcare.com/www.medicalmems.net), a nationally recognized authority on the adoption of medical technologies by clinicians, and a widely published author.

INDUSTRY INSIGHTS

By Ron Jones

Titans and Mortals

THERE HAS BEEN AN ONGOING battle between the foundries and OSAT's to move into the space between fab and assembly for advanced packages. I have talked about this in several articles over the past couple of years. The foundries had very high fab technology and could do lower tech bumping, wafer thinning and redistribution layers (RDLs), but really didn't understand the world of die attach, wire bond or flip chip. The OSAT's had been processing devices in wafer form for years including bumping, thinning and RDL's, but their fab technology was nothing compared to foundry.

A couple of weeks ago, SPIL announced their "Turnkey OSAT model." They have purchased and installed equipment that is capable of building fine pitch interposers utilizing submicron steppers and dual damascene fab processes. I haven't heard of other OSAT's following this path, but I would expect ASE, Amkor and STATS/ChipPAC to follow at some point.

In early 2012, TSMC announced that it would start providing turnkey services for customers including fab, probe, assembly and test, including middle of line processes such as bumping, wafer thinning, TSV's, interposers, etc. I don't think anybody thought they would become a major player in the OSAT space, but rather they might provide turnkey services for a select list of customers and end applications. UMC and GlobalFoundries did not follow suit and continued to embrace a collaborative approach with OSATs and specialty providers of services between fab and assembly. Not much was heard about the TMSC turnkey model for almost a year, though there were rumors involving Apple and others.

In March, TSMC and Altera jointly announced a turnkey test vehicle utilizing the TSMC CoWoS (Chip-on-Wafer-on-Substrate) process (voted all time worst semiconductor acronym by me). The CoWoS approach could theoretically offer a building block approach for the integration of multiple chips (remember multichip modules?). It reminded me of an SoC approach, but with chips instead of IP blocks.

To my knowledge, TSMC continues the CoWoS approach, but did announce a couple of weeks ago that they would embrace the collaborative model of working closely with OSAT's and 3rd parties for most advanced solutions rather than going it alone with turnkey.

Intel has been dabbling in providing foundry services for over a year for a couple of small fabless companies. In March, Intel announced they would be getting into the foundry business in a bigger way. They came out of the closet with an announcement they would provide foundry services to Altera. They have since announced a couple more customers including Microsemi.

In my opinion, there is a basic difference between the mindset of Intel and that of a TSMC or an Amkor. Contract manufacturers, be they foundries or OSAT's, live and die by capacity utilization. With narrower margins, profitability is heavily driven by the utilization of their high depreciation capital assets. They watch forecasts very closely and add capacity only when they feel it can be highly utilized. An Intel, on the other hand, takes a more linear approach to adding capacity on a steady basis and ahead of the projected need. With very high margins, they want to make sure they have manufacturing capacity in place so it is not a limitation for growth and winning new business.

Enter Brian Krzanich, as the new CEO. He has a strong manufacturing background and is very sensitive to cost. If he can have capacity for new Intel products and also utilize excess capacity with foundry business, he will have better overall profitability than either alone. He has publicly gone on record that he would like to better utilize the manufacturing assets and his elevation to CEO will likely begin to make that happen.

Samsung continues to be aggressive on both product and foundry fronts. They are spending sizeable amounts of capex and spreading its use over various fronts. In June, Samsung overtook Apple in the US smartphone market according to some sources. This week, Samsung overtook Apple as the world's leading mobile handset provider, ahead of Apple and Nokia. Apple may finally find a way to get a divorce from Samsung, but my sense is that Samsung will continue growing despite withdrawals, lawsuits, etc. (update: within an hour of initially submitting this article, there was a press release that Samsung would build 14 nm A9 chips for Apple iPhone 7's. I guess they saw a marriage counselor.)

The titans often establish a leadership position, though sometimes they change direction. This does not mean that others will follow the titans, however. Intel, TSMC and Samsung lead the thrust for 450mm, but few will be fast followers due to shear expense. It seems that our industry is becoming more and more a small group of tier 1 Titans (TSMC, Global Foundries, ASE, Amkor, Intel, Samsung, Apple) and a large number of tier 2/3 Mortals. This in no way says that the Titans will be more successful than the Mortals, however. It also doesn't guarantee ongoing success . . . the bigger they are, the harder they fall. ◆

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Is There a Bump in Your Future? The Growth of Flip Chip and Wafer Level Packaging

Jan Vardaman and Linda Matthew
TechSearch International, Inc.

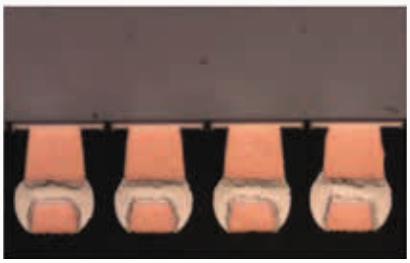
IN THE LAST DECADE, ADVANCED packaging has emerged as an enabler of today's electronic products. The impact of packaging, assembly, and test is increasingly felt in the semiconductor industry and the choice of the interconnect method is important in achieving device performance and form factor. Flip chip and wafer level packaging are expanding into a wide range of applications and device types as companies continue to move designs from wires to bumps.

Flip Chip

Devices such as central processing units (CPUs), graphics processors (GPUs), Application Specific Integrated Circuits (ASIC), and other high-performance devices have been using flip chip in package (FCIP) for many years. FCIP is also expanding in mobile computing, especially smartphones and tablets. In units, the compound annual growth rate (CAGR) from 2011 to 2016 is almost 26 percent, while in number of wafers the CAGR is only 13.5 percent because much of the growth is for small size die such as filters found inside mobile device modules [1].

A History Lesson

While it has become a popular topic at conferences and in magazines, flip chip is not a new idea. Flip chip interconnect was introduced in the 1960s by IBM and the first version used a copper ball for its three terminal transistors called Solid Logic Transistor (SLT) [2]. Flip chip was made famous with the introduction of IBM's evaporation process called Controlled Collapse Chip Connection, often abbreviated as C4. Flip chip interconnect was also developed and used in products at Delco (now Delphi) and Denso in Japan for automotive applications, as well as Citizen Watch for watch



Cu pillar with mass reflow.
Source: Amkor Technology

modules. IBM's technology was licensed to Motorola (now Freescale Semiconductor) and AMD. Intel had a cross licensing agreement and developed its own plating process. With the shift to large 300mm wafers, IBM and the rest of the industry moved from evaporation to plating. With the Pb-free movement, the industry adopted SnAg as the primary Pb-free solution of choice for plated bumps. Using current legal exemptions, some companies continue to ship products with eutectic and high-Pb solder bumps, but most companies have made the switch to Pb-free bumps. Today the industry is experiencing a transition from solder bump to copper pillar, just as it moved from an evaporated bump to a plated process.

Growth of Copper Pillar

Intel's adoption of a copper pillar has helped to create the infrastructure just as Intel's shift from ceramic to laminate technology provided the volume to develop the flip chip infrastructure enabling more widespread adoption of the technology. Intel started with the use of copper pillar in its 65nm and 45nm flip chip product lines, and is using copper pillar technology in its 32nm products. The first products were the "Presler" and "Yonah" processors, but today Intel uses the copper pillar process in all of its flip chip products [3]. Cu pillar with a solder cap has also been used for GaAs and silicon in RF modules for several years. Amkor has been shipping RF Power Amplifier and RF front-end modules with Cu pillar bumps for many years. Drivers included size, performance, and cost. Copper pillar is also shipping in leadframe packages from companies including Amkor, ASE, Carsem, SPIL, and Unisem.

Copper pillar, post, or column as it is often called, is also expected to see greater demand as companies move to fine pitch solutions. There are many forms of copper pillar and a variety of applications. Some copper pillar examples are found in high-end processors and others are found in flip chip packages for wireless products. Copper pillar is also an option for micro bumps used for die attached to interposers and for die stacks. Xilinx's highest performance Field Programmable Gate Arrays (FPGAs) use copper pillar interconnect for the die mounted onto a silicon interposer that is fabricated with TSVs in what Xilinx calls its "Stacked Silicon Interconnect" technology. Texas Instruments (TI) has adopted copper pillar technology in its application processor (OMAP) that is in the bottom package of the PoP [4]. Amkor provides assembly services for this product and TI also has its own internal production line. Companies offering copper pillar bumping, include Amkor, ASE, Chipbond, FlipChip International, JCAP, NEPES, SPIL, STATS ChipPAC, TSMC and Unisem. GLOBALFOUNDRIES and others will offer copper pillar bumping in the next year.

The variety of options come with a set of different material and equipment needs. With pitch trends below 100 microns, some companies are using a thermo-compression bonding process in which the flip chip die is placed on the substrate, uses

a non-conductive paste (NCP) underfill, and is bonded and the underfill cured at the same time [5]. This is a departure from the conventional pick, place, and reflow oven process commonly used. Three types of underfill process and materials are used with copper pillar today: capillary, molded, and pre-applied. The best method depends on many factors including the application, bump pitch, and cost structure.

Wafer Level Packages

Wafer level packages (WLPs) are fully packaged before dicing and include bumped die that are not packaged or underfilled due to thermal stress management concerns. Typically the ball or bump is a larger diameter and has a larger pitch than those found in flip chip bump applications. While some WLPs use a printed bump, most versions use a preformed solder ball. Some WLPs such as MOSFETs make use of an electroless NiAu as the under bump metallization (UBM) with a thicker gold, a printed bump, or a preformed solder ball to achieve a low-cost structure.

As end-users continue with the strong preference for small form factor, low profile consumer products, small packages such as WLPs meet the requirements. Demand for thin packages and greater functionality in smaller spaces drives the increased adoption of WLPs in mobile phones, especially smartphones and increasingly tablets. Many companies are designing wireless devices in WLPs, resulting in growth for 300mm wafers, but demand for 200mm wafers is also increasing.

Traditionally, WLPs were used for a variety of devices with low pin counts and small die sizes. WLPs are used for power MOSFETs, controllers, battery management devices, integrated passives, CMOS image sensors, diodes, EMI filters, and devices for ESD protection. Increasingly, larger devices such as integrated power management and wireless parts, such as RF components including Bluetooth™ and wireless LAN devices, are packaged in WLPs.

Fan-out WLPs

With increased interest in using WLPs for larger die with higher pin counts, an increasing number of companies are interested in using fan-out WLPs. Teramikros (formerly Casio Micronics) offers foundry services for WLPs using its copper post and the technology has been used for many years in mobile phones and consumer products such as watches. Infineon's wireless division (now owned by Intel) developed a "molded reconfigured wafer" technology for its fan-out WLP solution called eWLB. The chip backside and edges are covered with a mold compound and array interconnect solder balls are attached to the active side of the die. This allows the use of fan-out redistribution. The technology is targeted at medium to high I/O count (<300) devices such as baseband processors and multiband transceivers [6]. Several companies have licensed Infineon's eWLB technology, including ASE, NANIUM, and STATS ChipPAC, and production lines have been installed. Fan-out technology has also been developed by suppliers including ADL Engineering, Amkor Technology, Deca Technologies, FlipChip International/Fujikura, J-Devices Corporation, Nepes Corporation, Shinko Electric, and SPIL. TSMC has also announced its own fan-out WLP.

Wafer with electroless NiAu UBM. *Source: Pac Tech Packaging Technologies GmbH*

WLP Growth

WLPs offer a small footprint and a low-profile solution that enables ultrathin consumer products such as smartphones and tablets. The CAGR for WLPs in units from 2011 to 2017 is almost 13 percent for the six-year period, while the CAGR in wafers is slightly over 14 percent. While many wire bond designs are transitioning to WLP, some FCIP is also converting to WLP. Analog devices account for large shipment numbers in both units and wafers, but shipments of devices with RF functions are also contributing to strong growth.

Conclusions

Flip chip and wafer level packaging continues to expand to a wide range of applications and device types. Drivers for flip chip continue to be performance and form factor. Increased demand for thinner, lighter-weight portable products continues to drive WLP growth. For many companies, a bump will increasingly be in their future. ◆

1 E. J. Vardaman, Linda C. Matthew, and Laurie S. Roth, "2013 Flip Chip and WLP: Recent Developments and Market Forecasts", TechSearch International, March 2013.

2 Peter Elenius, "A Short History of Flip Chip and Wafer Level Packaging," *Advancing Microelectronics*, January/February 2013, pp. 6-8.

3 A. Yeoh, et al., "Copper Die Bumps (First Level Interconnect) and Low-k Dielectrics in 65nm High Volume Manufacturing, *2006 Electronic Components and Technology Conference*, May 2006, pp. 1,611-1,615.

4 M. Gerber, et al., "Next Generation Fine Pitch Cu Pillar Technology—Enabling Next Generation Silicon Nodes," *2011 Electronic Components and Technology Conference*, May 31-June 3, 2011, pp. 612-618.

5 Hamid Eslampour, et al., "fcCuBE Technology: A Pathway to Advanced Si-node and Fine Pitch Flip Chip," *2012 Electronic Components and Technology Conference*, May 29-June 31, 2012, pp. 904-909.

6 T. Meyer, et al., "eWLB System in Package Possibilities and Requirements," *International Wafer Level Packaging Conference*, Oct. 11-14, 2010, pp. 160-166.

China's Impact on the Semiconductor Industry

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PRICEWATERHOUSECOOPERS began the study, China's Impact on the Semiconductor Industry in 2004, in response to our clients' interest in the rapid growth of the semiconductor industry in China and the concern that China's production volumes would contribute to worldwide overcapacity and a subsequent downturn. Since then, it has become clear that market growth in China was far more significant to the worldwide semiconductor industry than production volumes. That relationship may now have started to change as China's 2011 semiconductor performance far exceeded the worldwide industry! Both China's semiconductor consumption market and its semiconductor industry growth were more than ten times greater than worldwide semiconductor industry growth.

China's semiconductor consumption market grew by 14.6% in 2011 to reach a record 47% of the global market. Much of this exceptional growth was the result of China's dominant position in the production of smartphones and media tablets. At the same time, China's semiconductor industry grew by 14.4% in 2011 to reach a record $43.5 billion. A significant portion of that exceptional growth was attributed to China's IC design or fabless sector which grew by more than 36% in 2011.

China has become the dominating consumer of semiconductors. Figure 1 shows the growth and distribution of the worldwide semiconductor market by region. The vertical bars represent the size of the total worldwide market and the circles the relative size of each region's market arranged by size with the smallest on the bottom. Through eleven of the last twelve years since 2000 China's consumption growth has outpaced the rest of the world. Since 2001 China's semiconductor consumption has grown

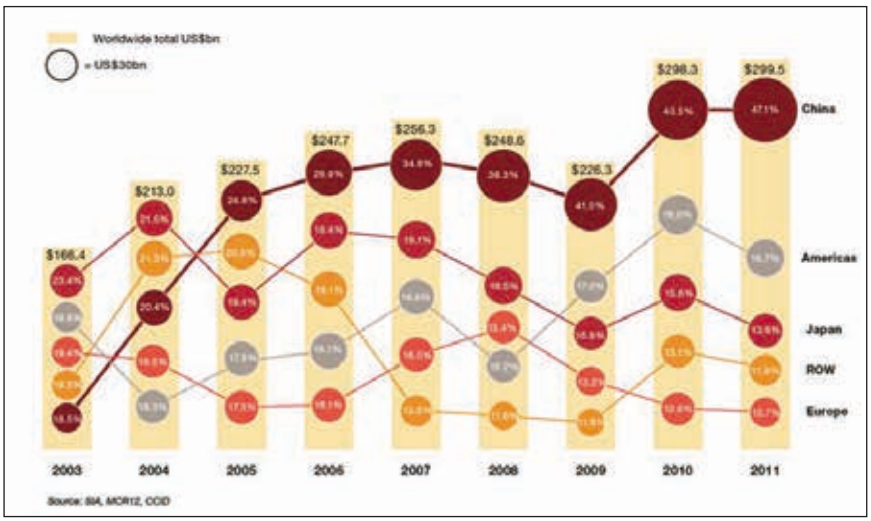


Figure 1. Worldwide semiconductor market by region, 2003-2011.

at a 24% compound annual growth rate (CAGR) compared to a total worldwide growth rate of only 8%. China's share of worldwide semiconductor consumption has grown from 6% in 2000 to 47% in 2011 and from being the smallest regional market in 2003 to the largest in 2005.

China's semiconductor consumption market has grown many times faster than the worldwide market as a result of two driving factors – the continuing transfer of worldwide electronic equipment production to China and the above-average semiconductor content of that equipment. The worldwide technology trend towards mobility has contributed to China's increasing share of worldwide electronics systems production. Even during the global recession in 2008 and 2009 China's electronic equipment production value continued to grow while worldwide production decreased. During the seven years from 2004 to 2011, China's share of electronic equipment production increased from 17% in 2004 to 33% in 2011, and the semiconductor content of that production continued to be about 25% compared to the worldwide average which remained at 20% in 2011.

Whether the Chinese semiconductor market will be able to continue to gain global share will be primarily determined by the future transfer of electronic equipment production. Most industry analysts are predicting that the trend of an increasing share of electronic equipment production in China will continue over the next five years.

The major global semiconductor companies continue to dominate the Chinese market. The largest suppliers to the Chinese market continue to be the same multinational semiconductor companies. There have been only thirteen different companies that have been among these top ten suppliers over the past nine years, eight of which have been among the top ten semiconductor suppliers to China every year from 2003 through 2011: Intel, Samsung, Toshiba, TI, Hynix,

ST, Freescale and NXP/Philips.

Almost two-thirds of all the semiconductors consumed in China were used in components of finished products assembled in China and exported for sale in other countries. This export market has been the major contributor to the growth of China's semiconductor market for the last decade. Since 2003 the consumption of semiconductors for export products has increased by $75 billion and constituted 62% of the overall growth of China's semiconductor market.

At the same time, China's domestic market continues to be of increasing significance to the global semiconductor industry. Since 2003, China's domestic market – the value of semiconductors consumed in China that are used in components of finished products assembled and sold in China – has grown at a 24% CAGR. That market has grown from $10 billion in 2003 to $56 billion in 2011. By itself China's domestic consumption market has made up more than 34% of total worldwide semiconductor market growth since 2003. China's domestic semiconductor market grew to represent almost 19% of the worldwide semiconductor market in 2011. It has had a noticeable impact on the semiconductor industry and has been credited with initiating or leading the industry's recovery from the depths of its decline in 1Q/09.

Chinese OEMs (original equipment manufacturers) influence and/or purchase a significant and increasing number of semiconductor devices. The top 10 Chinese OEMs 2011 Design TAM (total available market) semiconductor consumption was reported to be US $17.7 billion, an increase of almost 24% from 2010. The top 10 OEMs' 2011 Purchasing TAM semiconductor consumption was reported to be US $14.8 billion, an 18% increase from their 2010 reported Purchasing TAM. These values are less than their Design TAM because some of the OEMs (for example Lenovo) will design a product specifying specific key components and then consign manufacturing and purchasing to an EMS (electronic manufacturing services) company.

Although much smaller than its consumption, China's semiconductor industry's share of the worldwide industry is growing and becoming noticeable and significant. It is the reported revenues of all semiconductor companies in China,

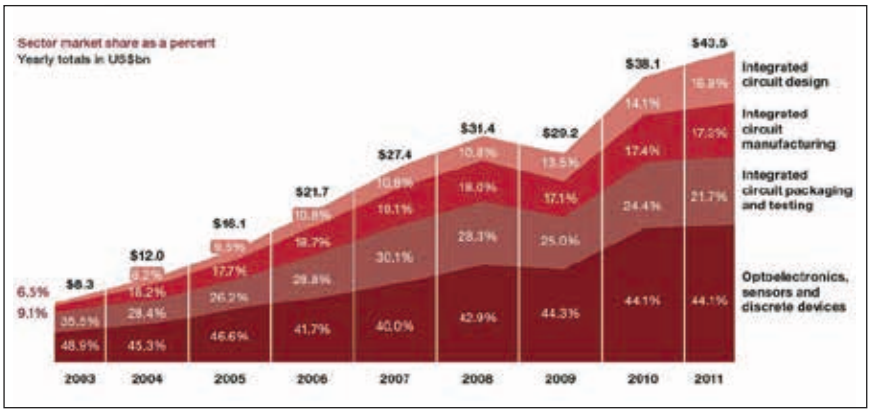


Figure 2. China's semiconductor industry by sector, 2003-2011.

including foreign and joint venture IDM plants, foundries, foreign and domestic SATS (semiconductor assembly and test services), domestic IDMs, and domestic fabless (design) companies. China's semiconductor industry has achieved a ten-year CAGR of 24% (measured in US dollars) from 2001 through 2011. Based upon a comparison with the sum of worldwide semiconductor device sales, plus foundry and SATS revenue, China's semiconductor industry accounted for 12% of the worldwide semiconductor industry in 2011, up from 11% in 2010 and, more significantly, up from just 2% in 2000.

Figure 2 shows the relative size and market share for the four sectors of China' semiconductor industry from 2003 through 2011. The distribution of China's 2011 semiconductor industry was O-S-D (optoelectronics-sensors-discretes) 44%, IC packaging and testing 22%, IC manufacturing (IDM + foundries) 17% and IC design (fables) 17%.

Integrated circuit (IC) design has been the fastest growing segment of China's semiconductor industry since 2000 and is the only segment that has achieved positive year over year (YoY) revenue growth for every year since 2000. Its revenue is primarily from China's indigenous fabless semiconductor companies, which further benefitted from the booming demand for semiconductors used in cell phones, as shipments of mobile handsets designed in China surged by nearly 60% in 2011. China's fabless semiconductor companies' revenue increased in 2011 to constitute about 10% of the $75 billion worldwide fabless IC industry, up from a 1% share in 2001, a 4% share in 2004, and a 7% share in 2010.

Packaging, assembly and test is probably the largest of China's semiconductor manufacturing activities when measured in terms of value added, production revenue, employees, and manufacturing floor space. This relationship is often missed because a significant portion of China's semiconductor packaging assembly and test (SPA&T) production is allocated to the O-S-D industry sector which is reported as a separate sector from the IC packaging and testing industry sector. China continued to gain share of worldwide SPA&T production value during 2011. The composite weighted average of China's 2011 SPA&T production is estimated to be about 31% of worldwide, up from 28% in 2010. The value of China's IC SPA&T production increased by 5% in 2011 to represent more than 19% of the value of worldwide production, while the value of China's O-S-D SPA&T production increased by 18% to represent more than 33% of the value of worldwide production. As a result, the composite of China's SPA&T production value increased by a weighted average of almost 11% in 2011 to represent slightly less than 31% of the worldwide production value. China's increased share of worldwide SPA&T value during 2011 was the result of its increased share of worldwide production volume, especially for LED devices with a corresponding increase in O-S-D ASPs (average selling prices). China's SPA&T production continues to be more heavily utilized for higher volume and lower cost packages and products, with their IC's accounting for 37% of worldwide unit volume and

their O-S-Ds for 70%.

As of the end of 2011, China had 109 SPA&T facilities which represented 20% of the total number of worldwide SPA&T facilities, more than 21% of worldwide SPA&T manufacturing floor space and 23% of reported worldwide SPA&T employees. China's SPA&T facilities continued to rank first in share of worldwide SPA&T manufacturing floor space, a proxy for potential manufacturing capacity, for the third year in a row, ahead of Taiwan (at slightly more than 20%), and Japan (17%). China's SPA&T facilities also ranked first in number of reported employees, with 23% of worldwide SPA&T employees at the end of 2011, ahead Taiwan (17%) and of Malaysia (16%). Of those, 109 SPA&T existing facilities, about 37%, belong to Chinese companies and 14% belong to companies from Taiwan (12%) and Hong Kong (2%). The largest foreign ownership is that of companies from the US who represent more than 18% of China's SPA&T facilities. Seventy-four of these 109 facilities were dedicated to SATS (semiconductor assembly and test services) suppliers of which 40 were owned by Chinese companies and 34 by foreign companies. Eight of the ten largest multinational SATS companies had one or more facilities in China for an average of 22% of their manufacturing capacity in China. A trio of domestic-funded SATS enterprises consisting of Xinchao Group (JCET/JCAP), Nantong Fujitsu Microelectronics (NFME) and Tian Shui Hua Tian Microelectronics (TSHT) are growing rapidly. Two are ranked among the 20 largest SATS suppliers on a worldwide basis. All three have received government support from either China's National Major Science and Technology Project 02 or Western Area Development Plan and all are working to expand their market share outside of China.

China has emerged as a significant source of new companies and financial funding for semiconductor start-ups. According to Thomson Financials, Chinese domiciled companies represented the second largest group of semiconductor IPOs (initial public offerings) completed between 2005 and 2011, constituting 24% of the number of IPOs and 44% of the proceeds realized. During 2011, almost $8 billion of additional fixed asset investments were made in China's semiconductor industry, down 13% from the slightly more than $9 billion investments made in 2010. Of that amount, almost $5 billion was made in the IC industry and more than $3 billion made in the O-S-D sector.

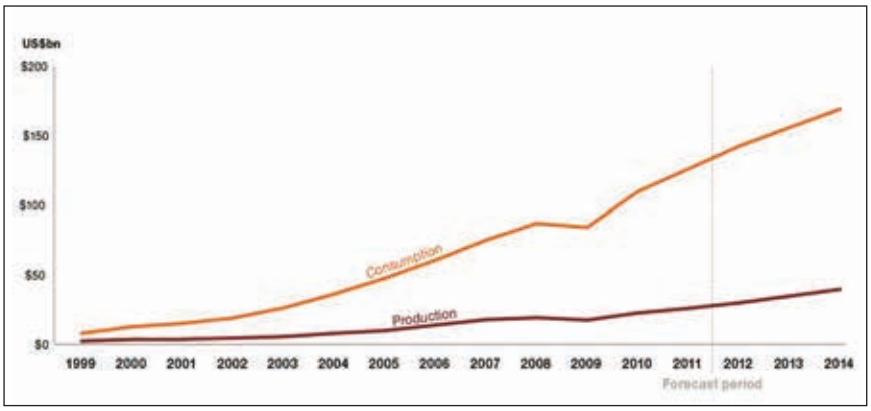


Figure 3. Comparison of China's integrated circuit consumption and production, 1999-2014.

For the 12th Five Year Plan period (2011-2015), China has launched ambitious policy initiatives to develop large domestic markets for specific next generation technologies including mobile Internet, information-based household appliances, 3C convergence, Internet of Things, smart grid, and cloud computing. The government is also increasingly emphasizing indigenous innovation in government procurement programs in order to reduce dependence on foreign technology. The effects of the relevant policies of China's 12th FYP are projected to move China's IC manufacturing industry in two key directions: increasing and accelerating concentration within the sector and increasing the number of firms funded from security market listings.

Figure 3 shows the difference between IC consumption and production in China which we describe as China's IC Consumption/Production Gap. This gap is the annual difference between China's IC consumption and IC production revenues. Both China's IC market consumption and China IC industry production increased to new record levels in 2011. As a result, China's IC consumption/production gap also increased to a new record level in 2011. China's IC consumption/production gap increased by more than $13 billion in 2011 to a new record of $101 billion. It continues to grow despite all of the Chinese government's plans and efforts to contain it. This annual gap has now grown from $6 billion in 1999 to a record $101 billion in 2011 – and Chinese authorities expect that it will continue through at least 2014, providing continuing motivation for the Chinese government's initiatives to increase indigenous production.

China's IC consumption/production gap represents both an opportunity and a challenge for the established multinational semiconductor industry. Over the near term, it continues to represent an unparalleled market opportunity, but over the longer term, it represents a domestic industry void that will inevitably be filled. The question is how will it be filled: will it be a combination transfer and expansion of multinational companies or the emergence and growth of significant Chinese companies? ◆

ED PAUSA is a consultant with the PricewaterhouseCoopers Global Technology Centre. He has had more than 40 years of experience in the semiconductor industry. During his career he has directed 33 plants and subsidiary companies in 18 foreign countries and 11 plants in six U.S. states. Pausa began his consulting career in 1990 after his retirement from National Semiconductor Corporation where he had served as corporate vice president of international manufacturing and services. He began his career in electronics with Fairchild Semiconductor in 1959. Pausa earned a BS in Engineering, a Master of Science in Metallurgy, and a graduate certificate in Business Management from UC Berkeley.

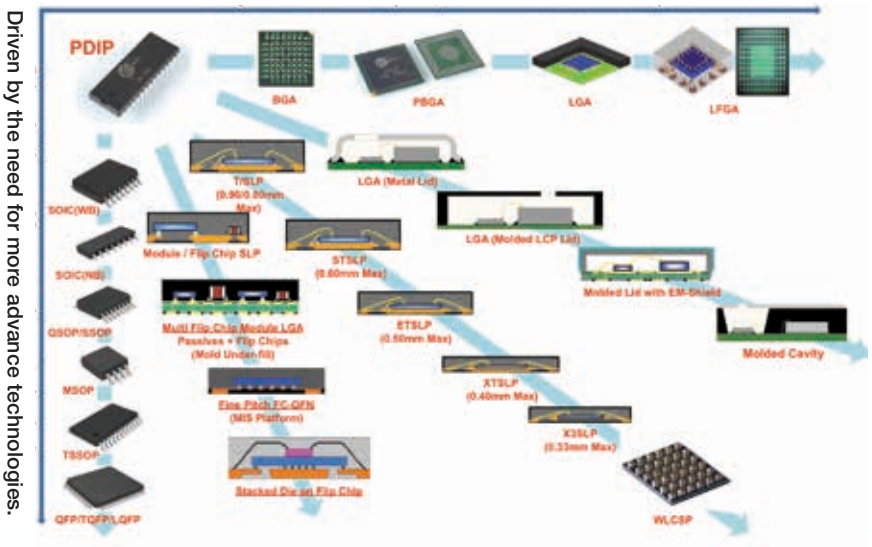
Providing Comprehensive Turnkey Assembly and Test Services

About Unisem

Unisem is a global provider of semiconductor assembly and test services for many of the world's most successful electronics companies. Unisem offers an integrated suite of packaging and test services such as wafer bumping, wafer probing, wafer grinding, a wide range of leadframe and substrate IC packaging, wafer level CSP and RF, analog, digital and mixed-signal test services. Our turnkey services include design, assembly, test, failure analysis, and electrical and thermal characterization. With approximately 8,000 employees worldwide, Unisem has factory locations in Ipoh, Malaysia; Chengdu, People's Republic of China, Batam, Indonesia and Sunnyvale, USA. Unisem is headquartered in Kuala Lumpur, Malaysia.

Unisem (M) BHD Assembly & Test facility located in Ipoh, Malaysia.

Driven by the need for finer pitch, miniaturization &/or better performance.



Unisem Package Evolution.

UNISEM PACKAGE OFFERINGS

Unisem designs and creates both Array and Leadframe packages for the global IC market. Their turn-key services include electrical and thermal characterization, design, assembly, testing, failure analysis and more. And with their real-time WIP systems and drop shipping to OEM's, Unisem offers its customers everything needed for time-to-market wins. Unisem offers a broad range of standard and custom leadframe and array packages with pin counts ranging from 3 to 700+. Also offered are WLCSPs or Wafer-Level Chip-Scale Packages which is a low cost solution that enables direct connectivity at the substrate or board level.

Array Packages

Unisem has vast experience with BGA assembly and manufacturing. In fact, they've developed several in-house manufacturing capabilities that give them the flexibility needed to for quick design and manufacture of Array products. So any manufacturing hurdles are quickly cleared, and any specialized needs are soundly addressed by their competent design and manufacturing crew. The result? Optimized cost and yield for a variety of package designs that include: PBGA, FBGA/LGA, MCM/SIP, Stacked Die BGA.

Leadframe Packages

Unisem's leadframe package assembly and manufacturing systems provide for lower costs and higher yields of the industry's most sought-after packages. Their process innovations in these proven technologies keep them at the forefront of the industry. Leadframe packages include: SOIC, PDIP, PLCC, QSOP, SSOP, SOT23, TSOT, MSOP, TSSOP, SC70, Micro-P, QFP, LQFP, and TQFP.

Leadless Packages

The small size of these packages, coupled with excellent thermal and electrical performance, make leadless leadframe packages such as the QFN and ELP ideal for hand held and portable communications applications including cellular phones, personal digital assistants (PDAs) and other applications where small, high performance packages are required. This package is also available in 2 and 3 Die configurations in Stacked Die, MCM and SIP (System-In-Package) versions which bring enhanced functionality, package performance and integration perfectly suited for wireless and other applications needing system integration in a single package format. Leadless packages include: QFN, ELP, QFN SIP, Stacked Die QFN, and LFGA.

Wafer Level Packaging

Unisem offers a Wafer Level CSP low cost solution that enables direct connectivity at the substrate or board level. To help provide this service they are equipped with the latest state-of-the art Laser Mark, Laser Groove, Camtek & Rudolph Wafer 2D/3D inspection stations and high speed Muhlbauer Die Sorters. They offer a full turnkey solution for Wafer Level CSP from Wafer Bumping, Packaging, Test Solution (probing) and full wafer map integration to handle die size from 0.2 mm^2 to 36 mm^2.

MEMS Packaging

Unisem's MEMS package offerings include: LGA-FLP: LGA Formed Lid Package - Laminate substrate based package with a stamped metal lid; LGA-MCP: LGA Molded Cavity Package. Laminate substrate based molded cavity package with a flat metal, plastic, glass lid; and LGA-MLP: LGA Molded Lid Package - Laminate substrate based package with an LCP molded lid. All packages have a wide variety of options to meet their customers needs.

Unisem Ipoh offers an integrated suite of packaging and test services including wafer bump, wafer probe, wafer grinding, and a wide range of leadframe and substrate IC packaging services.

UNISEM SERVICES

Assembly Services

Unisem takes pride in its efficiency and innovation, both of which contribute to a dramatic reduction in cycle time - from days to hours in many cases. Their state of the art factories provide wafer backgrind, inkless wafer sort and mapping, and accelerated turn times. What's more, with three different crews managing projects around the clock, 7 days a week, assembly runs from start to finish with minimal down time.

Test Services

In addition to package assembly services, Unisem provides a full range of package testing services. Capabilities include analog, digital and mixed signal testing, with over 100 test systems. From wafer probe through final test, Unisem Test Services operate 24 hours a day, 7 days a week, with more than 150,000 total square feet dedicated to testing. To further reduce time-to-market, Unisem also offers the following post-

test services: lead scan, lead conditioning, tape and reel, vacuum packing, burn-in, dry-bake, final pack/stock and drop shipping.

Wafer Bumping Services

Unisem offers wafer bumping services through its subsidiary Unisem Advanced Technologies (UAT). UAT is a 3-party joint venture between Unisem, Advanpack Solutions and FlipChip International. Located at the same premise as Unisem Ipoh, customers receive seamless integration of a wide variety of services under one roof covering wafer bumping, wafer backgrinding, wafer probe, dicing, final test and flip-chip assembly.

UAT offers gold bumps, copper pillar bumps and solder bumps (through ball drop, plating and solder paste printing). Additionally, UAT provides repassivation and bond pad redistribution services. UAT is truly a one-stop center for all your bumping needs.

With growing interest in WLCSP and Flip Chip, Unisem Chengdu Co. Ltd. is Unisem Group's 2nd Wafer bumping and WLCSP production site with space planned for future expansion. Based on Unisem's long-term roadmap, they are position to support up to 50K wafers per month within this facility for bumping. They anticipate that Flip Chip packaging will also be a growth area as today Unisem has already ramped up to over 50M units per month in terms of Flip Chip packaging.

Design/Characterization Services

Design and Characterization services are a key component to making sure Unisem's customers have the best packaging solution for their device. Unisem has the technology, capability, and staff to both design and characterize your unique IC packaging requirements.

UNISEM OPERATIONS

Batam, Indonesia

Unisem's factory in Batam Island, Indonesia, is a one stop shop facility, which provides wafer probe, wafer backgrinding, assembly packaging, final test, and drop shipment. Unisem Batam assembles and tests leaded and array packages on a high volume basis in this 345,000 square feet facility. Located approximately 10 miles from Singapore, Batam is an island that benefits from free trade zone incentives provided by the Indonesian government. The factory is certified to ISO 9001:2008, ISO 14001-2004 and ISO/TS 16949.

Unisem's state-of-the-art assembly and test facility in Chengdu Co. Ltd.

Chengdu, China

Unisem Chengdu Co., Ltd. ("Unisem Chengdu"), the Group's latest state-of-the-art Semiconductor Assembly and Test facility in Chengdu, China, began mass production in July of 2006 in the current total production floorspace of 320,000 square feet. The adjacent Unisem property of 900,000 square feet has been earmarked for the Phase 2 & 3 expansion of the production facility in the near future. Unisem Chengdu offers full turnkey semiconductor assembly and test services including wafer probe, wafer backgrinding, assembly, test, and drop-shipping of finished goods to customers' designated locations. Unisem Chengdu provides assembly service for a wide range of advanced leadframe and substrate packages and the testing of analog, mixed signal and radio frequency devices. Unisem Chengdu is certified with various quality management systems and environmental management systems such as ISO 9001:2008, ISO/TS 16949:2002, ISO 14001:2004 and is a certified Sony Green Partner.

Ipoh, Malaysia

Unisem Ipoh is Unisem Groups full turnkey assembly and test operations located in Malaysia. Unisem Ipoh offers an integrated suite of packaging and test services for semiconductor companies such as wafer bump, wafer probe, wafer grinding, a wide range of leadframe and substrate IC packaging, high-end radio frequency and mix-signal test, tape & reel and drop-shipment services. Unisem Ipoh is certified with ISO 9001:2008, QS 9000:1998, ISO 14001:2004 and ISO/TS 16949: 2002.

Sunnyvale, California

Unisem's test services facility in Sunnyvale, CA provides a full range of test, engineering and other test related services. This 22,000 square foot facility operates 24 hours a day, seven days a week. Sunnyvale serves as Unisem's North American test hub providing expertise in test engineering services. Pre-production capacity is available on a wide range of test platforms. Other test related services available in this location are burn-in, wafer probe, final test, marking, dry bake, lead scan and lead conditioning, tape and reel, dry pack and seal and bar code labeling. Sunnyvale Test is certified to ISO 9001:2008.

UAT

Unisem Advanced Technologies Sdn Bhd ("UAT") (Formerly known as Unisem-Advanpack Technologies Sdn Bhd), is one of the first independent wafer bumping service providers in Malaysia. UAT commenced operations in 2006. This 22,000 square foot facility with class 1K cleanroom supports wafer sizes of 100mm, 150mm and 200mm diameter. UAT is certified to ISO 9001:2008, ISO 14001:2004 and ISO/TS 16949.

For more information about Unisem's products and services please visit www.unisemgroup.com. ◆

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— Michael Shillinger, *Founder, Innovative Micro Technology (IMT), IWLPC Best of Conference 2012*

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Alternative Bonding Wires from the Perspective of Reducing Material Costs

William (Bud) Crockett Jr.
New Product Introduction, Business Development, Technical Specialist
Tanaka Denshi Group

TANAKA DENSHI GROUP WIRE bonding is widely used in the microelectronics industry to assemble the vast majority of semiconductor packages, electrically connecting Aluminum (Al) bond pads on the IC chips to the corresponding bond pads on the plastic or leadframe chip carriers. The Industry has short listed several common Bond wires which usually consist of good conductor metals such as Gold (Au), Aluminum (Al), or Copper (Cu). Gold has been the most widely used material because of its long successful history and extensive reliability data, resistance to surface corrosion and wire ductility during the bonding process. However, as the price of gold has risen significantly in the past decade, the microelectronics industry has been presented with cost driver opportunities. Primarily from the perspective of reducing material costs, the microelectronics industry has been investigating new alternative bonding wires to reduce the material cost of IC packages.

Many companies looked at bare Copper wire as a viable replacement option for Gold wire however many shortcomings of conventional Copper wire use in advanced packaging and assembly were encountered. The main industry shortcomings were; reduced lifespan of Copper wire (productivity and reliability), necessity to use a mixture of hydrogen/nitrogen (forming) gas, wire surface oxidation which limited shelf/bonder life and hard ball formation at the tip of the bonding wire. Comparisons of Copper wire versus Gold wire can be seen in Figure 1.

A breakthrough in the wire industry was the introduction of Palladium Coated Copper (PCC) Wire in 2008. The control of surface oxidation and stability in high volume manufacturing enabled PCC wire as the preferred alternative semiconductor interconnect material of choice to Gold and conventional Copper wire. Comparisons of PCC wire versus conventional Copper wire can be seen in Figure 2.

Advantages

- **Low Material Cost**
- **Better Conductivity** (Approximately 20% Better than Au)
- **Higher Fusing Current** (Approximately 30% Higher than Au)
- **Low Reaction Rates** (Cu/Al IMC @ 150-300˚C 10x Slower Au/Al)

Disadvantages

- **Need N2 or Forming Gas** (Gas Necessary for Copper wb)
- **Higher Mechanical Strength** (FAB Hardness, Work Hardening)
- **Narrow Parameter Window at 1st & 2nd Bonding Process**
- **Require Halogen Free Resin**
- **Need Additional Investments** (Cu Bonder, Forming Gas Piping)

Figure 1. Copper Wire versus Gold Wire.

PCC wire rapidly replaced conventional Copper wire and Gold wire over the past few years. PCC wire is simply a conventional 4N Copper wire core, with the outside layer coated with Palladium. The main advantages of PCC wire is the control of wire surface oxidation. Additionally PCC wire enables a wider 2nd bond process window and added benefit of corrosion resistance during reliability testing. These advantages proved PCC wire can improve bond quality and stability in a high

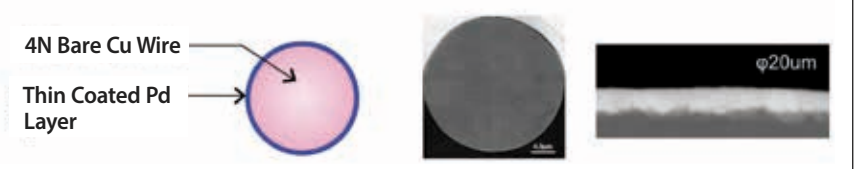
Advantages

- **No Wire Surface Oxidation**
- **Longer Spool Lengths & Longer Shelf Life**
- **Higher Productivity** (Bonder & Looping)
- **Wider 2nd Bond Process Window**

Disadvantages

- **Higher Material Cost**
- **Higher Mechanical Strength**
- **Harder FAB** (Free Air Ball)
- **More Al Bond Pad Splash**
- **Need Additional Qualifications** (If Bare Cu Already Qualified)

Figure 2. PCC Wire versus conventional Copper Wire.



Feature: Excellent control of corrosion/oxidation

Figure 3. Palladium Coated Wire.

volume manufacturing environment. In Figure 3 you can see the cross section of PCC wire.

The shipment volume of PCC wire has increased significantly over the past two years with projections reaching more than 40% of world wide bonding wire shipments in 2013. As a result of the maturity of PCC bonding wire, some process and design limitations have been confirmed such as harder FAB (free air ball), Al pad splash/pad damage issues, reduced capillary life and limitations of advanced bonding techniques such as ultra low loop and stand off stitch bonding (SSB).

Due to the concerns mentioned above with conventional Copper and PCC wires along with recent volatility of Gold prices, a new alternative bonding wire has been introduced to the market. Silver alloy wire was initially introduced in 2011 for LED and DRAM applications. It is now being considered for a broader semiconductor adoption base, now gaining momentum as the new alternative interconnects option for new chip designs.

Bulk material cost for Silver is less than Gold but more than Copper. The price of Silver alloy wire falls between PCC and Gold wire. The wire suppliers have estimated that over time, Silver wire cost will be comparable with PCC wire in high volume usage environments.

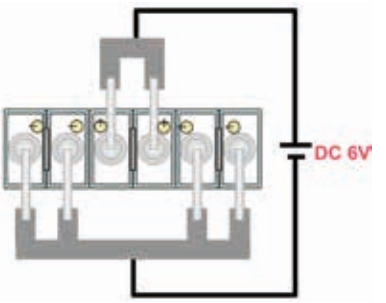
In past microelectronics industry experiences, Silver migration was a concern with pure Silver wires, especially on Aluminum bond pad surfaces. The perception of Pure Silver wire as another alternative bonding wire is often eliminated as an option due to the phenomenon of Silver migration. The wire suppliers are alloying Silver with various materials to eliminate Silver migration and dendrite growth. Current versions of the wire are alloyed with precious metals to control the migration.

Based on current biased voltage (6V) data, Silver alloy wire demonstrates very good reliability when compared with 4N Gold wire, conventional Copper wire and PCC wire. Migration comparison test data can be seen in Figure 4.

The advantage of switching from Copper wire to Silver alloy wire is that Silver alloy wire can be used in a safe, hydrogen free environment and can meet the necessary ball-bonding performance requirements at a low cost. Silver wire has a soft Free Air Ball (FAB) and excellent low loop formation with good elongation and breaking load properties. Silver alloy bonding wire is ductile like Gold wire, and does not work harden like Copper wires during wire bonding. A good comparison of the work hardening effect of multiple wire types can be seen in Figure 5.

Silver alloy wire does not require a forming gas environment, but must be bonded with nitrogen gas (N2) to form a stable FAB. When compared to 4N Gold, Silver alloy wire has similar first and second characteristics, including a wide process window and comparable stitch pull strengths. When compared

Wires	Ag Alloy / PCC / 4N-Au & Cu Wire
Wire Dia.	0.8mil
FAB Size	40µm
Bonder	UTC-1000 (Shinkawa)
Frame	QFP200pin
Device	Size: 6mm x 6mm x 300µm
	Metal: Al-0.5%Cu 0.6µm
HAST Conditions	130deg C 85%RH 96h
	HAST Machine: HIRAYAMA
	Voltage: DC 6V



	Failure / Sample Size (pin)			Result
Ag Alloy	Sample-1	Sample-2	Sample-3	**Pass**
	0/22	0/22	0/22	
PCC Wire	Sample-1	Sample-2	Sample-3	**Pass**
	0/22	0/22	0/22	
4N-Cu Wire	Sample-1	Sample-2	Sample-3	**Pass**
	0/22	0/22	0/22	
4N-Au Wire	Sample-1	Sample-2	Sample-3	**Pass**
	0/22	0/22	0/22	

Figure 4. Migration Test Comparisons.

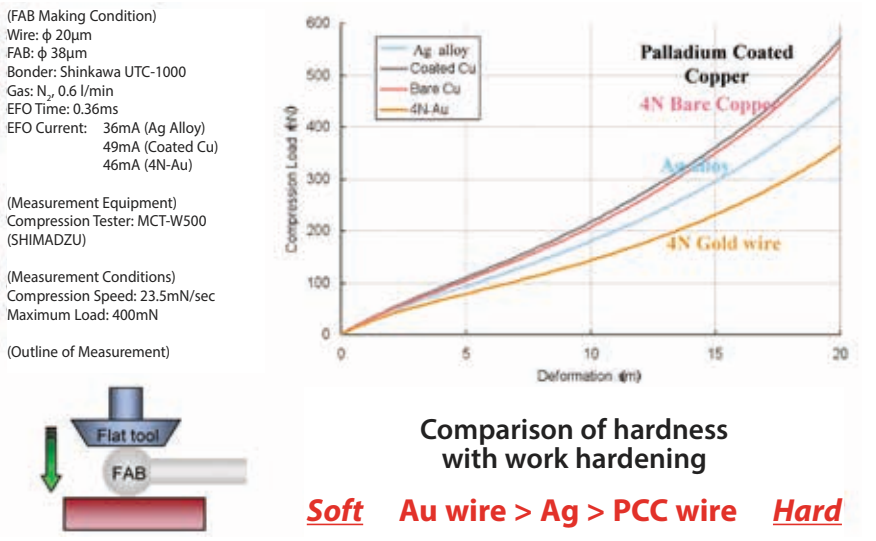


Figure 5. Wire Compression Test Comparisons.

to PCC wire, it has a simpler production process and better first bondability due to softer FAB and less Aluminum splash. Aluminum splash comparisons between Silver alloy wire and PCC wire can be seen in Figure 6.

Silver wire will not be a drop-in replacement for PCC wire, and the electrical requirements and bond pad structure must be evaluated as the weakness of Silver alloy wire is higher electrical resistivity. Since Silver alloy wire resistivity is higher than Copper, PCC or Gold, potential users must determine whether the resistivity will support the electrical requirements of their specific applications. It should be noted, the wire suppliers are working to further improve and lower the wire resistivity of Silver alloy wire closer to Gold wire. Wire resistivity comparisons can be seen in Figure 7.

The main drivers today of Silver alloy bonding wire are cost savings, with secondary focus for performance

(Bonding Condition)
Bonder: Shinkawa UTC-1000
Gas: N2 0.6 l/min.
Die-Pad: Al-0.5% Cu (t=0.8µm)
Capillary: SPT SI (H:25, T:130, CD:38, FA:8, OR:30)
Wire Diameter: 20µm
FAB Diameter: 38µm

Search Level: 120µm
Search Speed: 8.0mm/s
Search Force: 40gf
Bond Force: 40gf
US-Power: 170~230
US-Mode: -2
Pre US-Power: 40
Bond Time: 6.0ms

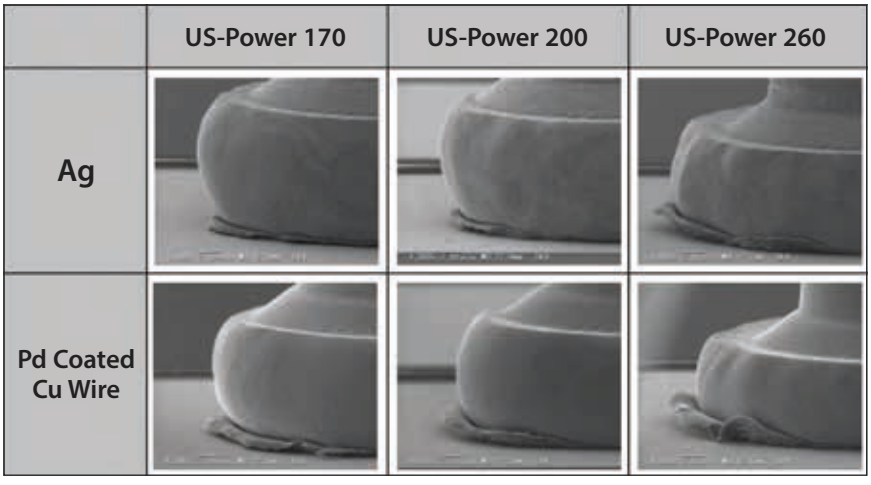


Figure 6. 1st Bond (Al-splash).

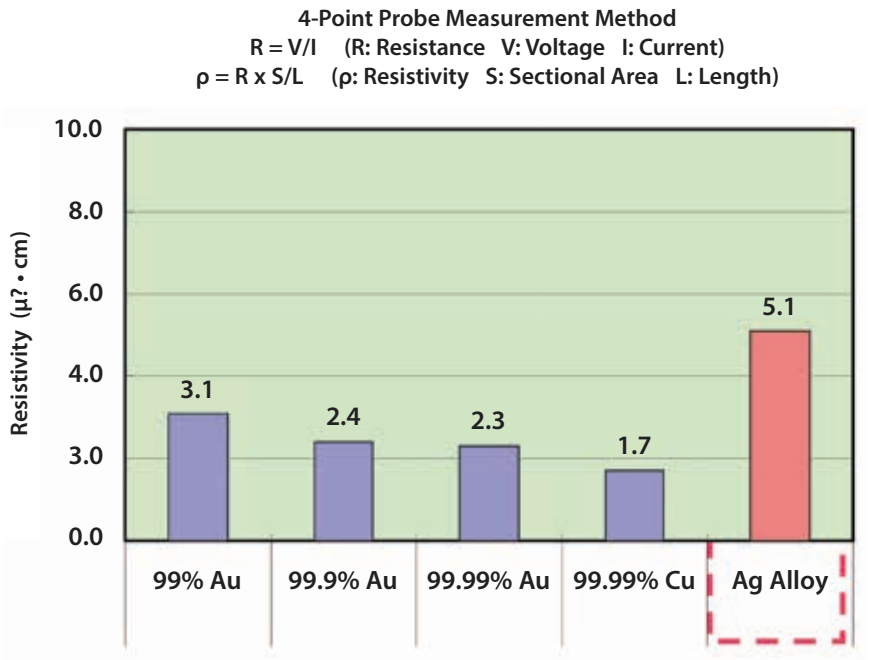


Figure 7. Wire Resistivity Comparisons.

Category	Pd Coated Cu	Ag Alloy	4N Au	4N Cu
Resistivity	**Low**	**High**	**Medium**	**Low**
Reliability	**High**	**High**	**High**	**Medium**
Chip Damage	**High**	**Low**	**Low**	**Medium**
1st Bondability	**Good**	**Best**	**Best**	**Good**
2nd Bondability	**Good**	**Good**	**Good**	**Poor**
Bonding Environment	**N2H2N2**	**N2**	**Air**	**N2H2**

Figure 8. Summary of Wires.

Atomic Symbol: Physical Properties	Au	Ag	Cu
Resistivity (u Ω • cm)	2.3	1.63	1.69
Thermal Conductivity (W/m • k)	320	425	397
Melting Point (k)	1336	1356	1234
Youngs Modulus (GPa)	88	101	136

Figure 9. Wire Properties Summary.

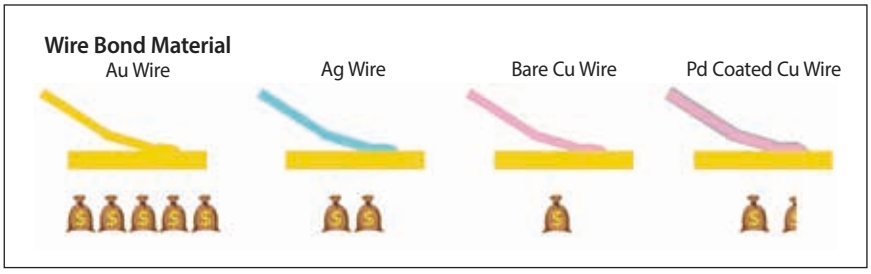


Figure 10. Material Cost Summary.

and reliability improvement. It is fairly easy to switch from Gold wire and Copper wire since Silver alloy wire only requires safe and inexpensive nitrogen gas which is readily available in existing manufacturing infrastructure. Also since Silver alloy wire has a similar level of productivity as Gold wire and sufficient second bond adhesion under almost the same bonding conditions as Gold wire. Silver alloy wire shows good potential as it offers several advantages compared to conventional Copper and PCC wires; mainly, excellent bonding performance and reliability. A Wire comparison table and physical property summary can be seen in Figures 8 and 9.

To summarize the benefits of switching from Copper wire to Silver wire is that Silver wire can meet ball bonding performance requirements, has soft FAB and excellent low loop formation while maintaining productivity on par with Gold wire. Silver bonding wire has good elongation and breaking load properties with non existent 'work-hardening' process issues like copper wire. (See Figure 11.)

In conclusion it is important to note, Silver alloy wire may not work for all applications but it can certainly help support many application areas where cost and performance define a product. Silver wire usage is expected to increase in the next few years in both the LED and semiconductor industries. ◆

For Customer Using 4N Au Wire

- **Similar 2nd Bondability**
  - Wide 2nd Bond Process Window
  - Comparable Stitch Pull Strengths
- **Good Reliability**
  - Longer HTS Life
- **Cost Savings**

For Customer Using Rd Coated Cu Wire

- **Similar Cost**
  - More Simplified Production Process
- **Better 1st Bondability**
  - Less Al Splash

Figure 11. Benefits of Ag Alloy Wire.

Trends and Considerations in Automotive Electronic Packaging

Deborah Patterson, Marc Mangrum, Adrian Arcedera, John Sniegowski
Amkor Technology

The transition from mechanical systems to electronic assemblies continues to transform the automotive landscape. Automotive electronics currently represent one of the higher semiconductor growth segments with a CAGR of 6.8% (2012-2017).[1] This year, semiconductor content in the automotive sector is forecasted to produce $25.9B in revenue. According to Freescale Semiconductor, today's electronic systems account for more than one-third of the total cost of new vehicles. Figure 1 highlights several of the major system drivers contributing to semiconductor content growth pursuant to Freescale's target markets.[2]

Safety is the most important consideration for consumers and to this end, government mandates have ensured a continuous flow of safety features designed to address factors from collision avoidance to survivability (should a collision occur). Surveys show that comfort is the second most important consumer requirement and a strong driving factor in the purchasing decision. Both safety and comfort are nonnegotiable expectations, with price point and branding defining specific features and performance. Connectivity is the third requirement coming from the next generation automotive customer and it represents a considerable and expanding market. Connectivity is also being legislated in multiple countries for purposes of safety. In Europe, for example, eCall legislation requires all vehicles to have connectivity to the cellular network with the ability to dial emergency services in the event of an accident. The draft legislation would require all new vehicles to deploy eCall after October 2015. Buyers will also demand vehicle designs that allow them to project their individuality more than in the past. The next generation sees the automotive platform as delivering an always on, always moving, connected lifestyle with as much customized individual expression as possible (music, contacts, mapping, alerts, interior ambience, etc.) Safety, comfort, connectedness and individual expression will drive growth in automotive electronics over the coming decade.

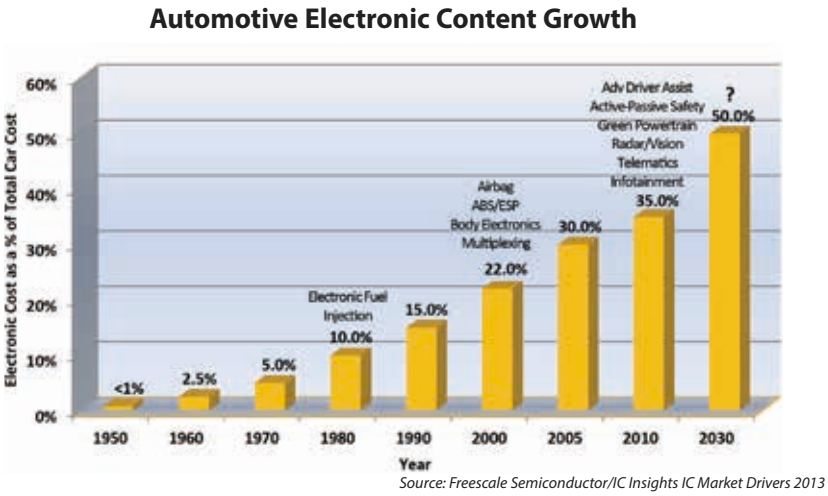


Figure 1. The proliferation of electronic content (semiconductors, sensors, etc.) in automobiles.

Semiconductor usage can be represented by four broad categories as listed in Table 1. These electronic systems often overlap, addressing multiple categories concurrently. And, as more features are added to the vehicle, automakers must also reduce weight, providing additional impetus to replace mechanical systems with electronic ones.

Figure 2 identifies a number of high level functions identified in Table 1 that are controlled by today's electronic systems.

In addition, hybrid and electric vehicles are forecasted to integrate significant electronic content in automobiles. Electronic vehicles employ components such as an electric motor, inverter, dc-dc converter, control electronics, sensors, and high-voltage batteries in addition to/in place of conventional components.[3]

By Volume, Lead Frame Packages "Own the Road"

Lead frame products are by far the largest type of automotive packaging as they have proven themselves very reliable components. Due to the long product life cycle, lead frame packages selected over a decade ago are still being manufactured for the same applications.

Lead frame packages are some of the most diverse found throughout the automobile. SOIC, TSSOP, SSOP, and PDIP packages support such functions as Tire Pressure Monitoring Systems (TPMS), drive train chassis and braking safety systems. TQFPs and MQFPs house microcontrollers for engine control systems. Even SOT/SCs, LQFPs, and PLCCs are found within the automotive platform. The most prevalent package is the *Micro*LeadFrame® (MLF®) and supports a considerable selection of device types.

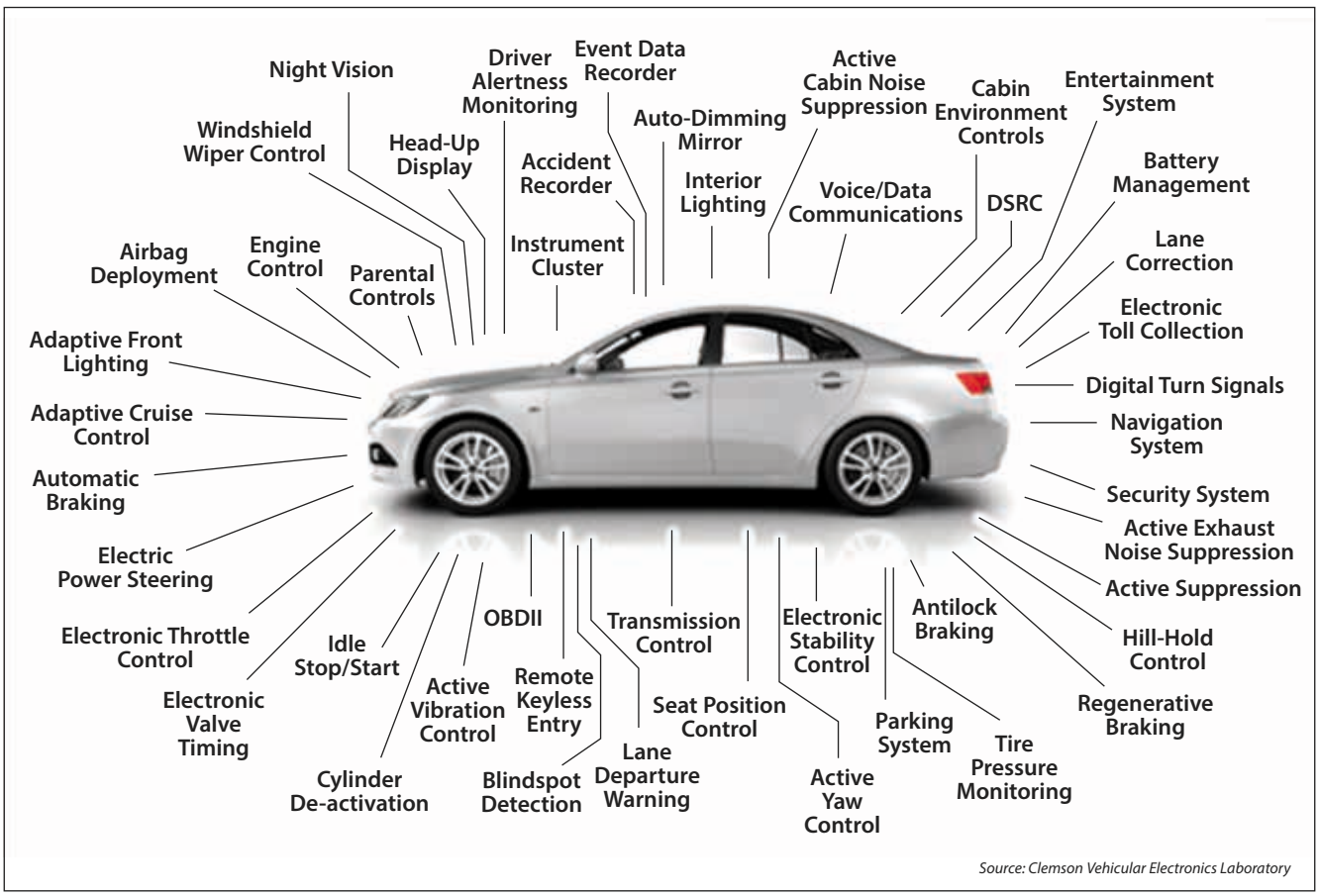
This is not to say that non-lead frame packaging is absent from today's vehicles. In fact, PBGAs, fine pitch FBGAs (ball pitch <1.0mm) and even Stacked Chip Scale Packages (SCSP) are present. Fine pitch packages of 0.5mm are being accepted for certain applications such as Transmission Control Unit (TCU) modules. Microcontrollers (MCU) are extremely

prolific within the automotive environment and, although found in MLF® packaging, they can also be found in PBGAs as well as high thermally efficient TEPBGAs within the engine control system. FBGAs support cellular connectivity, audio and GPS systems. Wafer Level Chip Scale Packages (WLCSP) are emerging in automotive systems and will proliferate over time.

Analog ICs, microcontrollers, and sensors now command the highest device volumes. Analog ICs accounted for an estimated 41% - and microcontrollers accounted for roughly 39% - of the automotive IC market in 2012. They are the most widely used ICs in cars today. There are anywhere from 25 to 100 MCUs located throughout the typical automobile and well over 300 in premium vehicles. New communications, entertainment and computing applications drive MCU content. Advanced parking systems such as self-parking, advanced cruise control, collision avoidance systems and driverless cars require MCUs, as do the growing number of positional, stabilizing, climate and engine performance sensors.[4] Both 16-bit and 32-bit microcontrollers typically require higher lead count packaging such as PBGA or QFP type

Automotive Feature	System Examples
Performance, Fuel Efficiency and Environmental Sustainability	Engine control/powertrain control modules, start-stop, motor driver, etc. Hybrid and fully electric vehicles (HEV/EV) systems. With internal combustion engines used in 87% of new vehicles, fuel consumption and emission regulations require constant control and monitoring systems, as well as suspension and braking stability, speed-distance control systems and advanced steering systems (influencing safety also).
Passive and Active Safety	Air bag systems and satellite crash sensors, anti-lock braking systems, Electronic Power Steering (EPS) and Electronic Stability Control (ESC), Near Object Detection Systems (NODS) and collision avoidance systems, Head-Up Displays (HUD) combined with Advanced Driver Assistance Systems (ADAS) such as parking assist, blind spot detection, advanced cruise control and Tire Pressure Monitoring Systems (TPMS).
Comfort, Aesthetics and Security	Remote keyless entry, climate control (HVAC), power windows/seat positioning (also heating and cooling), dashboard instrumentation; hands-free/noise cancellation; interior lighting, cabin ambiance driving this segment as an important differentiator for next generation consumers.
Infotainment	Audio/visual such as analog and digital radios, HDDs, TV and DVDs, USB connections; smartphones and other handheld devices interfacing with the dashboard supporting a continuous transfer of functions (telematics, navigation, other media); In-vehicle Ethernet will also be provided although not accessible by the consumer due to security reasons; Wi-Fi will be widely available and able to connect to the cellular network as a hot-spot.

Table 1. Automotive Electronic Categories.



Source: Clemson Vehicular Electronics Laboratory

Figure 2. A significant number of electronic systems controlled by semiconductors and MEMS devices are found in today's automobiles.

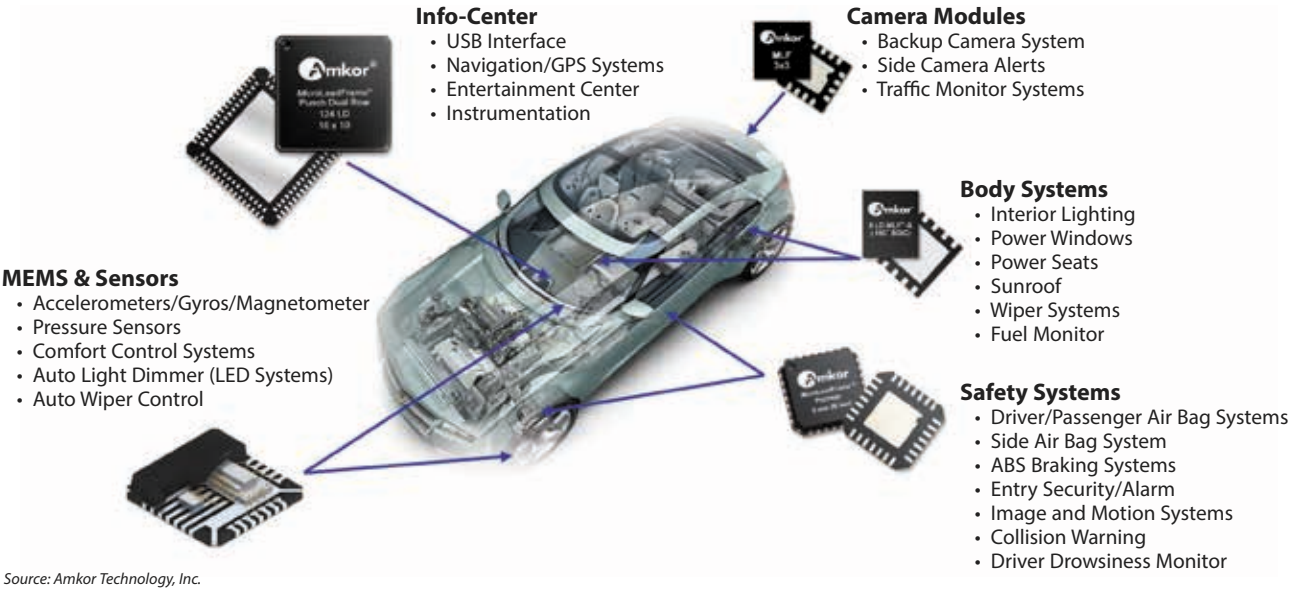


Figure 3. Several device types, from silicon ICs to MEMS, utilize MLF® packages for their wide variety of sizes, long history of excellent reliability, and mature HVM lines.

packaging to support engine control modules and emerging intelligent car systems, although they can also be found in TQFPs and MQFPs. Others are transitioning from PBGA to FBGA platforms.

Consider the MLF®/QFN/DFN

Amkor introduced the MLF® package in 1999 and today, it is one of the most commonly used leadframe packages in the world. The MLF® package ranges in size from sub-2x2mm (an extremely popular group of packages) to as large as 13x13mm. They support single ICs as well as multiple stacked die. MLF® packages are versatile and can be designed with features customizable to a particular application. Package height measures 0.35mm in High Volume Manufacturing (HVM) and a transition to 0.28mm using standard methodology is underway. Lead count as high as 180 in dual row configurations are available and there are no die stacking limitations. Wire sizes tend to run at 0.6mm for gold and 0.7mm for copper. Figure 3 illustrates a number of automotive systems that employ MLF® packages.

There is a very fast and growing migration of dual inline products and TSOP/QFPs to MLF® packages. Low resistivity and thermally enhanced epoxy and solder paste die attach materials have enabled this trend.

MLF® Mean Time to Failure (MTTF) is historically very good. Automotive customers will inspect the package lead to PCB joint looking for well-formed solder fillets to support increased reliability. In anticipation of this value-added benefit, Amkor originated the side wettable fillets and concavity (or "dimple") to allow for the formation of a rugged solder joint as well as its automated inspection. The dimple promotes formation of the fillet using a controlled quantity of solder that is deposited at the end of the lead. Both versions of the MLF® package - saw and punch singulation - offer this feature. Figure 4 shows a close up of the side wettable fillet and dimple (left) that produce solder fillets of controlled volume and location (right).

The Impressive Proliferation of Sensors

Government regulations around the world are playing a determining role in sensor and MEMS adoption. In the US, the 1970s saw fuel economy improvements with pressure sensors in air-intake systems such as Manifold Absolute Pressure (MAP) sensors and Barometric Air Pressure (BAP) sensors. In the 1980s and 1990s, crash detection for airbag deployment ushered in the use of additional pressure sensors and accelerometers. The TREAD Act in the 2000s required tire pressure monitor systems on all new passenger and light trucks to discover potential safety defects in tires, and Electronic Stability Control (ESC) propelled the emergence of both accelerometers and gyroscopes. Today, a growing number of automotive regulations around the globe are increasing the requirements for sensor systems in vehicles, driven by greater safety, reduced emissions and improved fuel consumption. In fact, sensor content in automobiles has grown from 10s to 100s of devices per vehicle.

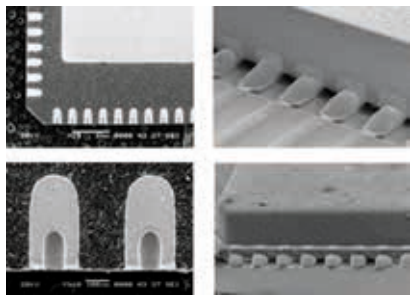


Figure 4. The side wettable lead with concavity (left) creates solder fillets of known volume that enables visual inspection of package to PCB joints. The top right view shows a saw singulated package with a 1.0mm lead pitch and the bottom right view shows a punch singulated package with a 0.5mm lead pitch.

Per Strategy Analytics, the demand for automotive sensors will grow at 6.8% CAGR between 2012 and 2017, rising from $16.9 billion to $23.5 billion.[5] Sensor growth rates vary between the main automotive producing regions of the world. Safety system growth is the largest driver of sensor growth through 2020. Leading automotive suppliers saw 15% to 20% growth as more government regulations worldwide required electronic stability control units, and China adopted airbags en masse.

Sensors were initially introduced in hermetic packages for airbags and anti-

continued on page 32

Automotive

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TEPBGA-2
Microcontroller
(Engine Control Unit)

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Audio
GPS
Diagnostic
Connectivity

CABGA/FBGA
Audio
GPS
Celllular Connectivity

PBGA
Microcontroller
(Engine Control Unit)

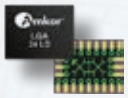
TQFP/MQFP
Microcontroller
(Engine Control Unit)

SOIC/SSOP/PDIP
Tire Pressure
Drive Train Chassis
Braking Safety

DLP
Head-Up Display
Interactive
Dashboard Display

Sensor Packages

Cavity MEMS



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continued from page 30

lock braking systems. These were MEMS structures in cavity packages with pressure sensors representing the highest volume. Although the first packaged MEMS sensors for airbags have remained unchanged in their design for more than twenty years, there has been a phenomenal amount of progress in automotive packaging during this time. Today's MEMS packages are tasked with integrating multiple sensors together. These "fusion sensors" often have diametrically opposing requirements regarding device stress management, package handling and signal propagation.

Sensors in backup systems, Head-Up Displays (HUD), infotainment and diagnostic interfaces are prevalent and moves toward standardization are being undertaken. MLF®, LGA and "cavity MEMS" are three of the most popular package types. Optical sensors are easy to produce in in-frame MLF® and LGA formats. Flow sensors use a cavity in the over-molded format or create a hole in the lid of the package.

The key to sensor packaging is to utilize existing package platforms in order to rapidly ramp to HVM (tens of millions of packages per month), control costs, reduce time to market, and apply existing reliability and quality systems for new product introductions. There is a concerted effort underway to move from custom sensor packages to standard footprints even if the inside of the package may still be quite customized.

MEMS are well suited for a wide variety of automotive applications due to their reliability and ability to ramp quickly to high volume manufacturing. A sample list of sensor types and automotive end-applications are shown in Table 2.

Infotainment Reshapes the Cabin

Infotainment and the new "connected vehicle" will drive the adoption of many newer package families although modifications to pass stricter automotive certifications may dictate changes to materials or construction. Many packages for cellular and tablet applications are not acceptable or marginally so.

Today, OnStar will unlock your doors, start your vehicle remotely, provide tracking data, process diagnostic information and communicate through the smartphone. Voice activated systems as well as MEMS microphones providing in-cabin noise reduction are being designed into high end automobiles. Head-Up Displays (HUD) allow the driver to keep his eyes on the road with the intent of making driving safer amid the distraction of managing more information. Conversely, cars that communicate with each other and driverless automobiles are also being demonstrated for future adoption. Dual or other multi-row packages (MLF®, LGA, cavity, etc.) are expected to emerge for these downstream opportunities. This said, the most popular Infotainment packaging is trending toward FCBGAs.

Figure 5. Illustrated above is an example of head-up display (HUD) technology "leveraging night vision, navigation and camera-based sensor technologies to project images produced by ultra violet lasers onto the surface of the windshield."[6] An alternate approach uses TI's DLP® technology which is fast becoming a new trend in HUD due to its imaging capabilities.

Pressure Sensors	Accelerometers
Manifold Absolute Pressure (MAP) Sensor	Stand Alone Airbag Front Sensor
Barometric Air Pressure (BAP) Sensor	Airbag Peripheral Sensor
Boost	ESC Acceleration Sensor
Fuel Rail	Roll Over Sensing
Cylinder Pressure	Tire Pressure Monitoring System (TPMS)
Vacuum Boost Stop and Start	Integrated GPS
Oil Pressure	Active Suspension
EGR	Safety
Particle Filter	Vibration
Oil Transmission	Electronic Parking Brake
Fuel Vapor (Tank)	Gyroscopes
Brake & ESP	Roll Over Sensing
Suspension	GPS Navigation
Steering	ESC Gyroscope
Side Airbags	Inertial Combos (Accel + Gyro)
Tire Pressure Monitoring System (TPMS)	ESC, Rollover, Airbag, etc. Combos
HVAC Fans	Optical MEMS for Heads Up Displays
HVAC Hydraulics	Magnetometers
Seat Occupancy (Weight)	Microphones

Table 2. Various Sensors and Their System Insertion

Summary

The dynamic and changing landscape of automotive electronics is exciting to witness and inspiring to support. Electronic adoption will continue to progress in almost every area of automotive design, transforming our driving experience beyond recognition. The accelerated adoption of so many package platforms within such a diverse environment presents an abundance of opportunity that will fuel creativity and innovation down the road. ◆

1 Semiconductor Forecast Database, Worldwide, 2Q13 Update, June 2013, Gartner.

2 R. Lineback, B. McClean, B. Matas, T. Yancey, "Integrated Circuit Market Drivers 2013," IC Insights, Inc.

3 Randy Frank, "Hybrid Vehicles Propel Increased Electronics Content," Electronic Design, Oct. 2004.

4 R. Lineback, B. McClean, B. Matas, T. Yancey, "Integrated Circuit Market Drivers 2013," IC Insights, Inc.

5 Mark Fitzgerald, "Global Automotive Sensor Demand to Exceed $25 Billion by 2020," Strategy Analytics, May 7, 2013.

6 Dashboardnews.com, "Technology continues to evolve in the auto industry," Dashboard News, March 6, 2012.

Automotive Assembly Differentiation

THE AUTOMOTIVE INDUSTRY assumes component lifetimes in terms of decades, not years – as well as an expectation of performance in extreme environments. Demanding environmental and reliability standards typically drive a four year development cycle which includes extensive reliability testing and field trials. In the assembly world, the automotive mindset is one of best practices and zero defects. Numerous factors are taken into account to achieve these goals. Systems such as stability control, airbag deployment and anti-lock brakes often require specialized manufacturing flows, materials or inspection protocols to ensure both performance and long term reliability.

Customer Criteria

The OSAT's customers ultimately determine the process and test flows necessitated by the particular automotive system. There are six classes within automotive specifications, each calling out different performance criteria. Therefore, visibility into end use is important in order to choose or design IC packaging with appropriate cost/performance goals in mind.

Material Selection

To tackle demanding automotive reliability requirements, the choice of materials must be considered during the early stages of device design and in consideration of the targeted application. Two examples of materials that can be optimized to address extreme temperature or high stress conditions are Epoxy Mold Compounds (EMC) and Die Attach (DA) materials. In many cases, a high thermal EMC material is required to meet demanding environmental conditions.

In addition, a material's potential exposure to harsh chemicals (oil, gasoline, grease, hydro-chemicals) or external environmental factors (rain, ice) must be considered. Furthermore, extreme vibra-

continued on page 34

Amkor Technology Philippines, an *Automotive Center of Excellence*

All five of Amkor's factory sites throughout Asia run automotive products in high volume. However, it is the Amkor Technology Philippines (ATP) operation that is home to the largest base of automotive qualified products, customers and OEMs. ATP maintains a diverse automotive package portfolio including lead frame, ceramic and laminate packages as well as system-in-package (SiP) products. ATP also provides a full range of test services including die processing and inspection, wafer probe, burn-in, strip test and test development.

Amkor has identified ATP as its *Automotive Center of Excellence*, offering designated manufacturing lines operated by highly skilled and automotive-trained personnel. Automotive demarcated bill of materials, controls and process flows are managed. Moving forward, ATP is further augmenting its focus to:

- Design-in quality across all business processes and manufacturing phases
- Implement firewall concept based process controls
- Endorse a "Zero Defect to Zero Error" philosophy

ATP has passed a significant number of VDA6.3 process audits by direct and 3rd party customers.

The factory was awarded General Motors Supplier Quality Excellence Award for 2012. Suppliers who receive this award have met or exceeded a stringent set of quality performance criteria along with the cross-functional support of the entire GM organization.

The ATP factories contain over 1.3M square feet of manufacturing space and are ISO-9002, QS-9000, ISO 9001, ISO/TS 16949, ISO-14001, OHSAS-18001, ANSI/ESD S20.20 and DSCC / QML (military standard) certified.

continued from page 33

tions and shock excursions during engine component operation, or within traction control, suspension and steering systems, or in brake rotors or wheels may also require specialized materials such as proper wire sizing and type, wire coat, gel-coat, lead frame or special laminate substrate designs.

Supplier Management

It is important for the OSAT to be informed of product utilization in automotive applications. The automotive sector has developed its own supplier assessment and audit processes. One set of rules for doing process audits comes from the German automotive industry (VDA6.3). It is often used to meet the requirements of another specification, ISO/TS16949, aimed at developing quality management systems and emphasizing defect prevention and the reduction of variation and waste in the supply chain. And although the International Automotive Task Force (IATF) contributed to its preparation, many large Asian manufacturers have their own quality management requirements. Therefore, upstream visibility is important and enables the OSAT to become a partner in support of these criteria. The OSAT will communicate through their supply chain, improving supplier quality by raising awareness, documenting specifications, implementing Best Known Methods (BKM), and aligning with provider expectations which may also include downstream compliance certifications or specialized testing.

Conflict minerals/metals remain an area of great importance to the global automotive supply chain. Each supplier must implement procedures demonstrating that the materials procured and sourced are in compliance with government, corporate and customer policies.

Process Flows

Safety, power train and chassis end-use have the highest reliability requirements. In this case, visibility to end-use requirements may generate material, equipment, or process flow options that are customized to meet these more extreme applications.

Automotive processing may include extra cleaning steps or process control monitors. Modifications to basic assembly process steps, such as the use of security wire bonds, may be incorporated into an automotive flow. The security bond reduces the opportunity for any lifting that could occur. Another example of a modified process flow for automotive application is the roughening of the surface of the lead frame to enhance EMC adhesion. Additionally, a die attach material that provides 100% coverage may also be required, such as conductive or non-conductive epoxy or die attach films.

Inspection Criteria

Specialized inspection steps and sampling plans are often employed for automotive applications. This drives additional process steps as compared to a typical commercial process flow. Similarly, the ability to inspect assembled packages on the PCB is an important requirement for automotive builds. Although x-ray inspection can be utilized if the board is thin enough, when both sides of a board are densely populated, inspection can become difficult. Amkor developed and introduced a side wettable leaded package to visually enhance PCB inspection and ensure that proper solder joint coverage is made between the package and PCB. Side wettable leads have become more of an automotive standard (see Figure 4).

Quality Planning

Advanced Product Quality Planning (APQP) was developed in the 1980s by the "Big Three" US automobile manufacturers, Ford, GM and Chrysler. It is similar in concept to "Design for Six Sigma" but for the automotive industry. Downstream adoption of APQP assists in compliance with overall automotive control plans and the intent to maintain the highest manufacturing standards for all constituent components used within a vehicle.

Reliability Testing

The Automotive Electronics Council sets qualification standards and AEC-Q100 outlines critical stress test qualification for automotive ICs and packaging. Electronic components must be rugged enough to operate in these environments at the IC, package and board level.

Electrical Testing/Lot Screening

Post assembly test is the final screen confirming device and package performance to specifications and overall integrity. A fundamental difference between consumer and automotive test is the tie to statistical principles and the handling of "inherent risk". For example, many consumer electronics are allowed to be retested with subsequent passing components deemed "good" product. This is contrary to automotive standards where advanced statistical screening may reject the entire lot. If the automotive sector, in their goal to achieve Zero Defects, cannot fully explain the reason behind a low yield occurrence, it will reject the entire lot as an anomaly with some inherent risk and remove it from the population.

Designated Lines, Trained Personnel

Designated or dedicated lines and equipment are sometimes sought by the customer. These may include specially trained personnel, error proofing systems, or hands-free processing systems. Specific product identification in the WIP may also be featured.

Change Control

Automotive standards are among the most stringent and change management is often measured in years instead of quarters that are more commonly seen in commercial applications. If a safety or reliability concern instigates the change, the timeline will be accelerated although safeguards and rigorous testing are still required. Change control is often undertaken in concert with the customer (incorporating Change Review Boards) to assess technical risk and downstream implications. A proactive issue management infrastructure compliments continuous improvement practices.

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About Amkor

Amkor is a leading provider of semiconductor packaging and test services to semiconductor companies and electronics OEMs. More information on Amkor is available at the company's website: www.amkor.com.

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Mold Compound Advances Require World-Class Capability

Ruud de Wit, Global Product Manager Mold Compounds
Henkel Electronic Materials, LLC

DESIGNED TO ENCAPSULATE today's high-performing semiconductor components, transfer mold compounds deliver critical device protection and performance stability. Indeed, they are essential materials and require expertise to formulate and manufacture, particularly when it comes to the performance needed for modern IC's and power discretes that run at higher voltages in power management applications. Designing mold compounds that can endure in-field stresses and challenging environments takes world-class facilities, a knowledgeable team, the latest production resources and an innovation program that ensures materials for future technology requirements.

While all of the above may be understood, what may be less well-known is the depth and breadth of the Henkel mold compound research and manufacturing capabilities. In fact, Henkel Huawei Electronics' (HHE) world-class mold compound site in Lianyungang, China is the largest mold compound manufacturing facility in the world. At over 34,000 square meters with nearly 600 employees, the three separate production workshops on this campus total the largest global single-site mold compound manufacturing capacity. Henkel has invested significant resource to expand the HHE facility over the last five years, ensuring the highest quality production standards, manufacturing equipment and expert staff.

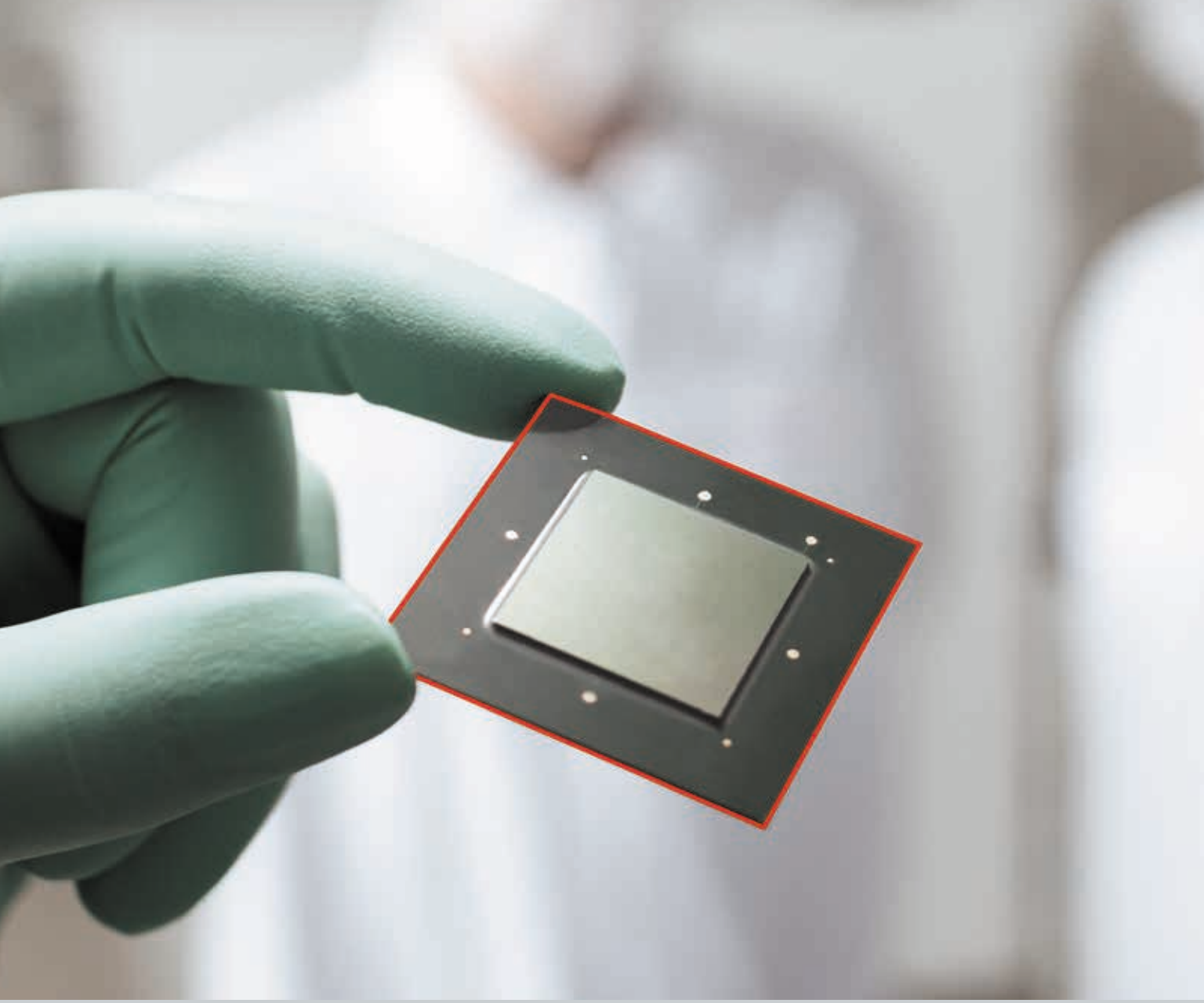
And, this investment extends beyond the Lianyungang manufacturing site. At Henkel's new Mold Compound Competence Center in Shanghai, product formulation, small scale pilot production, pelletizing and full analytical and reliability testing can be done to verify performance. What's more, fundamental mold compound research is carried out in Irvine, California, expanding the technology toolbox with new resins and enabling next-generation research and development for mold compound advances. In all Henkel mold compound facilities, the highest environmental, safety and quality manufacturing standards are employed, ensuring sustainable, high-performance, best-in-class mold compound materials.

The multi-million dollar investment in and expansion of Henkel's mold compound capabilities is significant. State-of-the-art production lines with tight process and metal particle control capable of mold compound production for more demanding devices such as SOICs, QFPs and sensors have been incorporated. Materials innovations focused on higher-end devices running at increasing temperatures and voltages and compatibility with copper wire are a central part of Henkel's development efforts. All told, there are over 20 projects in the pipeline – all designed to bring new components to market faster and more reliably than ever before.

Henkel's commitment to innovating the next-generation of mold compounds means that customers can advance designs, bring new concepts to market and incorporate materials that can cope with emerging device demands. Take, for example, Henkel's new LOCTITE HYSOL series of mold compounds for FULLPACK, D(2)PAK and MOSFET devices. These materials are enabling the next generation of power devices through their ability to cope with the high voltage and high temperature demands of modern power discretes. In addition, established compounds such as the LOCTITE HYSOL MG15F series have been proven with voltages as high as 1200V or more and deliver temperature stability for operating temperatures approaching 200°C. These types of materials are in production on commercialized Silicon Carbide (SiC) MOSFETs, which operate at higher voltages and temperatures as compared to traditional silicon-based MOSFETs, while also reducing energy losses. Enabling the most advanced technologies – such as the transition from traditional silicon to Silicon Carbide – is the advantage Henkel's development expertise, global support structure and world-class mold compound operations deliver.

Mold compound innovation and superior quality manufacturing is happening every day at Henkel – propriety new resin development is ongoing which will enable new ultra-low stress compounds with <0.1% cure shrinkage and glass transition (Tg) temperatures that exceed 250°C. Top semiconductor companies use Henkel mold compounds successfully in production 24/7 and tomorrow's devices are being brought to market today due to the performance and reliability of mold compounds from Henkel. With a broad portfolio of mold compounds for passives, power discretes, IC devices, sensors and more, Henkel's mold compound offer and expertise is unmatched. Now, you know!

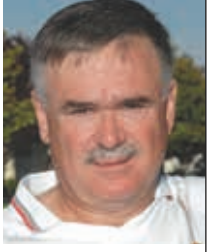
To find out more about Henkel's mold compound product line and world-class capabilities, log onto www.henkel.com/electronics or call +1-888-943-6535 in the Americas, +32 1457 5611 in Europe or +86 21 3898 4800 in Asia. ◆



The smaller the device - the more solutions

No matter where you are or what your process requires, you can count on Henkel's expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel's world-class global team ensures your success and guarantees a low-risk partnership proposition.

Henkel Excellence is our Passion



A Trillion Sensors in a Decade – Jobs, Jobs, Jobs and more

Janusz Bryzek, Ph.D.
Vice President, MEMS and Sensing Solutions
Fairchild Semiconductor

IN 2010 I WAS A CO-ORGANIZER OF an event called the MEMS Technology Summit that was held at Stanford University. At the event attendees heard a talk that presented a vision for 7 trillion "sensory swarms" by 2017. This triggered me to explore high sensor growth opportunities which resulted in a long research that uncovered multiple pointers to the possibility of a trillion sensors in the coming decade.

What was interesting is that the leading market research organizations didn't yet see such growth potential. This reminded me of 2007, when the explosion of gyroscopes was not forecasted. I came to a conclusion, that only visionaries can "invent" new applications coming to the market with an ultrahigh demand for sensors. Based on the success of the 2010 Summit, I decided to ask leading sensor visionaries to present their visions at the TSensors (Trillion Sensor) Summit at Stanford University to be held on October 23-25. Over 40 visionaries have agreed to talk.

Time to market for new sensor technologies historically averaged over 20 years from academic prototypes to high volume production. Based on my MEMS startups experience, I believe that accelerated sensor development to support growth of the sensor market to trillions is possible, but requires a focused commercialization effort. This belief was reinforced by a BSAC/UC Berkeley presentation by Vijay Ullal (now President, Fairchild Semiconductor) calling for creation of "Cooptition", or cooperating competitors, jointly funding development of standard MEMS processes necessary to support accelerated growth of MEMS markets from $10B to an already visible $300B.

Our vision is that the sensor development acceleration will require the following steps:

- "Invention" of new sensor applications likely to enter an ultra high volume demand resulting from emerging global tides such as Abundance[1], Mobile Health, Internet of Things, Context Computing and others.
- Post-processing the outlined visionary applications to extract sensor types, supporting those which would require the development acceleration effort, resulting in a published TSensors Roadmap.
- Formation of working groups focused on developing the acceleration strategy for needed high volume sensor types.
- Executing the acceleration strategy, which will likely require funding of the cooperative effort between academia, industry and Governments, to develop sensors and the required high volume manufacturing infrastructure enabling low cost (design tools, manufacturing processes and tools, packaging, testing, etc.).

One of the extremely positive potential results of this initiative, if materialized, will be the exponential sensor market growth resulting in massive creation of new jobs.

Let's assume an average revenue per employee in developed countries at $250,000/year for component companies and $500,000/year (equal to the 2011 average for the US Nasdaq 100 companies) for smart systems companies. Let's further assume an average selling price of the wireless sensor node at $0.13 in trillion units/year volumes, cumulatively representing 0.1% of forecasted 2023 global GDP. This would then represent a $130 billion 2023 revenue level, translating to 520,000 new direct jobs.

Systems enabled by sensors (including hardware, software, data processing, data storage, etc.) will create much higher revenue. So far, sensor cost in very high volume mobile applications averages about 2% of the system ASP. Assuming this ratio holds, systems enabled by sensors would create 50 times higher revenue, or $6.5 trillion. This would create 13 million new direct jobs.

Typically, the job multiple for indirect jobs resulting from knowledge workers has been between 2 and 4 (depending on region). Assuming conservatively an estimate of 2, this would result in twice as many indirect jobs, for a total of 41 million new direct and indirect jobs in developed countries.

As a reference, the US created only 1.3M new jobs between 2002 and 2012, primarily in Government and medical sectors.

As sensor based systems require a high-tech work force, the majority of created jobs will likely be for knowledge workers. An example of a sensor based system could be Apple's iPhone 4s, which had the following breakdown of 2011 selling price:
3% ($14) assembly (China)
32% ($178) components (global)
66% ($368) Apple's share (US)
100% ($560) selling price

If the iPhone manufacturing/sales model holds for emerging sensor based systems, most of the generated jobs would be for knowledge workers located in the developed nations. TSensors implementations thus have a potential to overshadow most other job creating approaches considered by Governments. It may also force Governments of different countries to compete for these jobs.

One of the most rewarding effects of a trillion sensors will be life-changing global advancements and improvements addressing the world's biggest problems, such as hunger, lack of medical care, pollution, lack of water and energy, as well as improvement of quality of life for all.

Join us at the TSensors Summit to watch the revolution unfold! Visit www.tsensorssummit.org for details.

Contact bcooper@tsensorssummit.org or call 650-714-1570 if you have questions. ◆

[1] Abundance: 2012 book by Peter Diamandis and Steve Kotler, defining abundance as elimination of global problems such as hunger, lack of medical care, energy, water and uncontrolled population growth through exponential technologies, which include sensors.

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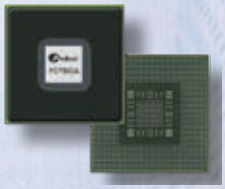

FC^{M}BGA
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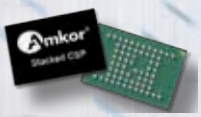
Combo Chip



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LGA
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WLCSP
PMIC
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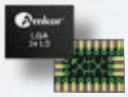
Compass

Sensor Packages



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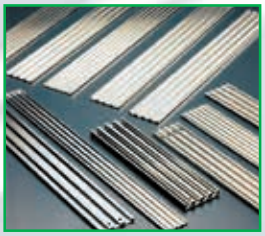
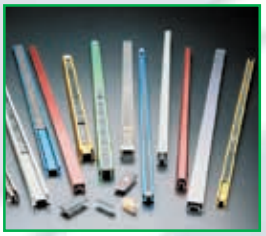
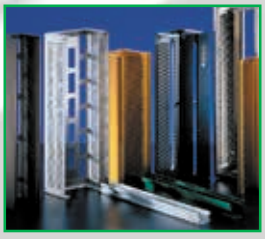
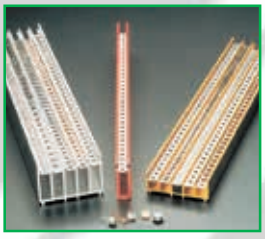

I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines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