MEPTEC Report

SUMMER 2012

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 16, Number 2

2012 Medical Electronics Symposium

Technology, Personal Health and the Economy

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Amkor Technology – employing the industry's broadest operational footprint, with factories located in the heart of the Asian-based electronics manufacturing supply chain.

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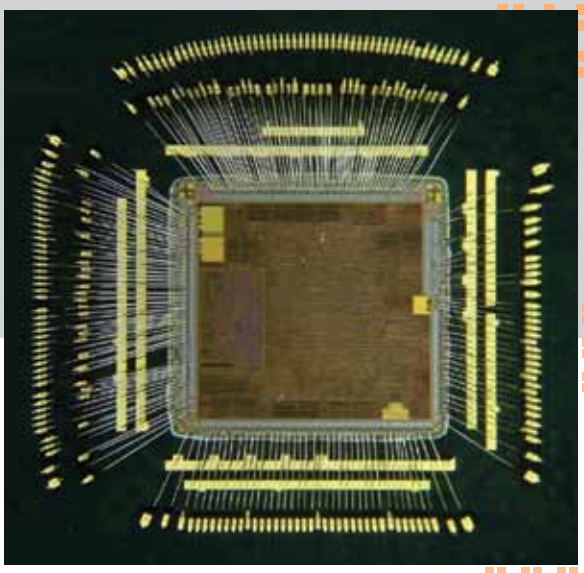
ASE GROUP

Copper Wire



- Cu wire bond as good as gold
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- Leader in high volume production
- Quality and yield equivalent to gold
- High reliability, typically 2x JEDEC

www.aseglobal.com

3D-TSVs Continue to Dominate the Conversation

Bhavesh Muni, Global Business Director
Dow Electronic Materials' Advanced Packaging Technologies
MEPTEC Advisory Board Member

IN THE REALM OF SEMICONDUCTOR packaging, 3D-TSVs continue to dominate the conversation. It seems that suppliers are claiming new innovations almost daily that solve at least one of the many challenges still facing this emerging technology. While 3D-TSVs are far from mainstream adoption, the potential of the technology is clearly a significant driver of the packaging industry as a whole.

For all of the excitement, it is broadly understood that many challenges remain for 3D-TSV-based devices to reach high-volume manufacturing (HVM). The list of remaining critical issues that have yet to be solved illustrates the complexity of integrating so many materials and process steps. Purely viewed from a materials perspective, very few companies are positioned to deliver an integrated material set for 3D-TSV packages, e.g. metallization for bumping, TSV, redistribution; lithography; dielectrics; and assembly materials. Further complicating the picture, companies that provide materials for bumping may have limited knowledge of gap filling, underfill, etc., which hinders development efforts and underscores the value of working with suppliers who can bring comprehensive materials understanding and a broad product and technology portfolio.

Material suppliers and packagers are actively working to address a number of technical roadblocks – such as thermo-mechanical property mismatches, adhesion and voiding. Temporary bonding is also a hot industry topic, as it remains a critical challenge for HVM of 3D-TSV-based device packages. It is a process that requires specific – and proven – materials, yet from the perspective of the leading packaging companies no acceptable solutions presently exist.

Examples like this illustrate that there is a clear and growing need for a comprehensive 3D packaging industry roadmap to enhance the level and accelerate the speed of technology development. Such a roadmap could address specific technical barriers and counteract the fragmentation in the market.

MEPTEC has become an important forum to address these challenges and aid possible solutions by providing opportunities to discuss industry issues and facilitate stronger industry partnerships. Since its inception 30 years ago, MEPTEC has provided a forum for semiconductor packaging and test professionals to learn and exchange ideas that relate to packaging, assembly and test. The organization offers publications, monthly events and large-scale conferences, and has recently become even more dynamic with its expanded Advisory Board. Perhaps most importantly, MEPTEC brings together suppliers from all of the critical disciplines, thereby ensuring meaningful collaboration.

MEPTEC's "2.5D, 3D and Beyond" Symposium last fall was a good example of the value MEPTEC delivers, with its focus on the development of 3D-TSV packaging solutions and integration requirements to facilitate its introduction into mainstream production. The symposium was held in conjunction with the "Known Good Die" Symposium to discuss related challenges associated with testing 3D devices. This synergy supports the value of bringing together partners into an integrated ecosystem to work toward common goals.

I have every expectation that this year's conference in November will continue the conversation. The event will cover a broader spectrum of topics relative to multi-die integration that continue to challenge materials suppliers and packagers, as well as aiming to address the roadmap for multi-die integration. I certainly plan to attend, and hope to see you there. ◆

BHAVESH MUNI is currently Global Business Director for Dow Electronic Materials' Advanced Packaging Technologies business, which is currently offering and developing materials for metallization, lithography, dielectrics and assembly. Bhavesh can be reached at bmuni@dow.com.

More information about Dow Electronic Materials is available at www.dow.com.

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SUMMER 2012

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ON THE COVER

17 2012 MEDICAL ELECTRONICS SYMPOSIUM – "Technology, Personal Health, and the Economy". MEPTEC and SMTA are again partnering to present a two day Medical Electronics symposium which will cover a broad spectrum of topics highlighting innovative technologies and related issues in medical electronic applications and devices.

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15 ANALYSIS – As developing countries see increases in their aging populations, the need for devices to improve the quality of life and maintain health is growing. These factors are driving the demand for medical electronics, and in turn, the growth of flex circuits for a variety of applications.

BY E. JAN VARDAMAN AND KAREN CARPENTER
TECHSEARCH INTERNATIONAL, INC.

18 PROFILE – Founded in 1968, Amkor has become a strategic manufacturing partner for hundreds of the world's leading semiconductor companies and electronics OEMs, providing a broad range of advanced package design, assembly, and test solutions.

AMKOR TECHNOLOGY, INC.
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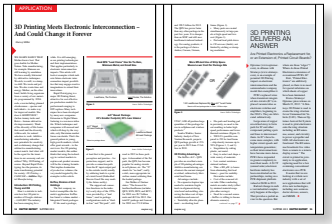
22 PACKAGING – The wide range of applications for medical electronics drives unique requirements that can differ significantly from commercial and military electronics. This is particularly the case for handheld, portable and implantable medical devices that demand increased functionality with decreasing size, weight and power .

BY SUSAN BAGEN, FRANK EGITTO & RABINDRA DAS
ENDICOTT INTERCONNECT TECHNOLOGIES, INC.



24 APPLICATION – Additive manufacturing unleashes new potentials for creativity and evolutionary change that subtractive manufacturing cannot match. And what will be the agent for the transitions in our economy and our culture? Why 3D Printing, of course.

BY HARVEY MILLER

DEPARTMENTS

MEPTEC

THE NEXT GENERATION

The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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Meet the MEPTEC Advisory Board

IN THIS ISSUE WE CONTINUE introducing our fourteen Advisory Board Members. All Board members are listed at the left.

JEANNE BEACHAM is President and CEO of Delphon Industries LLC, a materials manufacturing company that is a leading provider of device packaging materials and services to the Semiconductor and Medical Device Industries. Delphon has Divisions Gel-Pak, Quik-Pak, TouchMark and UltraTape, with offices in Hayward and San Diego, CA, Salem, Oregon and St. Albans, Vermont. Global Customer Sales support and distribution include direct sales along with Manufacturing Reps and International Distributors, Delphon offers global sales and service support. Recently Jeanne was given the Women Entrepreneur of year award for Manufacturing, the Diamond Leadership Award and East Bay Women of Distinction Award. Jeanne also received an award from the San Jose Business Journal as one of the most influential women in business in Silicon Valley and Woman of Distinction in Technology.

Jeanne Beacham
Delphon Industries LLC

KUMAR NAGARAJAN is currently Director of Package Development at Xilinx, responsible for package development, new package qualification and production engineering. Prior to Xilinx, Kumar worked at LSI in Package Technology Development. He received M.S in Material Science from Stanford University; M.S in Industrial Engineering from SUNY, B.S in Mechanical Engineering from Birla Institute of Technology, India.

Kumar Nagarajan
Xilinx, Inc.

SEMI Reports First Quarter 2012 Worldwide Semiconductor Equipment Figures; Billings US$ 10.6 Billion

SEMI has reported that worldwide semiconductor manufacturing equipment billings reached US$ 10.61 billion in the first quarter of 2012. The billings figure is 14 percent higher than the fourth quarter of 2011 and 9 percent lower than the same quarter a year ago. The data is gathered in jointly with the Semiconductor Equipment Association of Japan (SEAJ) from over 100 global equipment companies that provide data on a monthly basis. Worldwide semiconductor equipment bookings were $10.07 billion in the first quarter of 2012. The figure is 9 percent lower than the same quarter a year ago and 13 percent higher than the bookings figure for the fourth quarter of 2011. The quarterly billings data by region in millions of U.S. dollars, year-over-year and quarter-over-quarter growth rates by region are as follows:

Region	1Q2012	4Q2011	1Q2011	1Q12/4Q11 (Q-o-Q)	1Q12/1Q11 (Y-o-Y)
Korea	3.32	2.55	1.66	30%	100%
North America	2.16	2.19	2.75	-1%	-22%
Taiwan	1.77	1.55	2.73	14%	-35%
Japan	1.29	1.24	1.34	3%	-4%
Europe	0.82	0.76	1.25	8%	-34%
China	0.72	0.54	1.04	33%	-30%
ROW	0.52	0.50	0.88	4%	-41%
TOTAL	**10.61**	**9.34**	**11.65**	**14%**	**-9%**

Note: Figures may not add due to rounding. *Source: SEMI/SEAJ June 2012*

The Equipment Market Data Subscription (EMDS) from SEMI provides comprehensive market data for the global semiconductor equipment market. For more information or to subscribe, please contact SEMI customer service at 1.877.746.7788. ◆

MEMBER NEWS

PLEXUS TO BUILD NEW MANUFACTURING FACILITY IN NEENAH, WISCONSIN

Plexus Corporation has announced that it intends to construct a 410,000 square foot manufacturing facility in Neenah, WI. This facility will replace two existing leased facilities in Neenah and will consolidate approximately 1000 employees into the new building. The facility is expected to cost approximately $50 million, with construction expected to begin in July 2012 and to be complete in fall 2013. Plexus is eligible for $15 million in enterprise zone tax credits from the State of Wisconsin through the Wisconsin Economic Development Corporation. These tax credits will be distributed over a seven-year period based on capital investment, job retention and job creation conditions.
www.plexus.com

INVENSAS UNVEILS GROUNDBREAKING PACKAGE-ON-PACKAGE SOLUTION FOR NEXT-GENERATION SMARTPHONE AND TABLET COMPUTING

Invensas Corporation, a wholly owned subsidiary of Tessera Technologies, Inc., has unveiled its bond via array (BVA) technology. BVA is an ultra-high I/O packaging alternative to wide-I/O through silicon via (TSV) that delivers the performance required by mobile OEMs while preserving the proven infrastructure and business model of traditional

package-on-package (PoP). Invensas' BVA technology enables high-performance consumer electronics to overcome the processing demands of next-generation designs without altering existing packaging infrastructure. This makes it an ideal low-cost and highly adoptable solution for mobile device manufacturers.
www.invensas.com

DISCO BECOMES FIRST JAPANESE COMPANY TO EARN CERTIFICATION UNDER THE ISO 22301:2012 BCMS STANDARD

DISCO Corporation has obtained certification under the ISO 22301:2012 Business Continuity Management System (BCMS) Standard. They are the first Japanese firm to obtain this certification (according to SGS Japan) and among the first companies globally.
www.disco.co.jp

ALTERA'S INDUSTRY-PROVEN QUARTUS II SOFTWARE DELIVERS UP TO 4X FASTER COMPILE TIMES

Altera Corporation has released the latest version of its industry-proven Quartus® II development software, the industry's number one software in performance and productivity for FPGA design. Quartus II software version 12.0 provides customers additional productivity and performance advantages, such as up to 4X faster compile times for high-performance 28-nm designs.
www.altera.com

InvenSense Expands into Industrial Applications with the World's First Single-Chip, Integrated High-Performance 3-Axis Industrial Gyroscope

MPU-3300 Breakthroughs Include More Than 100% Lower Noise, 10X Smaller Size, and a 3X Price Advantage vs. Other Industrial Gyroscopes

INVENSENSE, INC., THE leading provider of MotionTracking™ devices, has announced its entry into the industrial market with the introduction of its MPU-3300, the world's first single-chip, high performance integrated 3-axis industrial gyroscope. Leveraging the company's proven high volume production capabilities, InvenSense is providing high performance, high reliability, low power and low cost with ultra-precise positioning and monitoring information for industrial applications.

Drastically cutting the size through integration, MPU-3300 is 10X smaller than currently shipping industrial gyroscopes. Industrial product designers can easily assemble the single-chip, three-axis digital gyroscope into their devices with the highest degree of axis alignment vs. assembling three discrete gyroscope devices. The MPU-3300 also offers more than 100% lower noise compared to alternative offerings, providing accurate measurements for critical industrial applications.

The MPU-3300, with a bias instability of 15 degrees/hour, is highly suited for a range of industrial applications including Attitude Heading Reference Systems (AHRS) which require extremely stable performance for precision-attitude tracking. AHRS systems are found in aerospace, robotics, and other applications where the orientation of a device must be measured. Navigation systems in industrial vehicles, aircraft and ships can also benefit from the highly accurate gyroscope technology while manufacturers of industrial instruments such as hand-held inventory control devices value the low-power consumption of the MPU-3300 at less than 10mW.

The MPU-3300 is available now in mass production and is priced at $35 USD in 1000 unit quantities, an industry breakthrough price point compared to multichip industrial gyroscopes solutions.

To purchase samples or for additional information about the MPU-3300, please visit www.invensense.com or contact InvenSense Sales at sales@invensense.com. ◆

Amkor Technology Announces Plans to Build State-of-the-Art Factory and Global R&D Center in Korea

AMKOR TECHNOLOGY HAS ANNOUNCED that it plans to build a state-of-the-art factory and global research and development center in the Incheon Free Economic Zone, which is located in the greater metropolitan area of Seoul, Korea. The new factory and R&D center will focus on the design, development and full scale production of innovative semiconductor packaging and test services for the world's leading semiconductor and electronic manufacturing companies.

"We are making a strategic, long term investment in our core manufacturing and research infrastructure. It is a commitment to the future," said Ken Joyce, Amkor's president and chief executive officer. "Korea is a worldwide center of excellence for the semiconductor and electronics industries, and with our new site we will be able to attract top engineering talent and a highly skilled workforce."

Amkor has signed a non-binding memorandum of understanding for a site for the new facilities with approximately 186,000 square meters, or about 46 acres. They expect to spend approximately $350 million over the next three to four years to acquire and develop the land and buildings, with approximately $30 million planned for the fourth quarter of 2012 and approximately $70 million planned for 2013.

Construction is expected to commence in 2014 and the facility is expected to become operational by late 2015 or 2016. Amkor expects to equip their new manufacturing and R&D facilities using their normal capital additions budget.

"Our total investment for this project may reach $1 billion over the next 10 years, although spending for a project like this will be spread over many years and can be controlled as needed as economic and market conditions and the cash needs for our business evolve," noted Joyce.

Visit Amkor's website at www.amkor.com. ◆

MEPTEC Announces North Texas Biomedical Device Forum

UT DALLAS
The University of Texas at Dallas

MEPTEC is pleased to announce their partnership with the University of Texas at Dallas and the Dallas Chapter of the IEEE Engineering in Medicine & Biology Society to hold the first *North Texas Biomedical Device Forum*. The event will be held at the Dallas campus of the University of Texas on Wednesday, October 10. Details will be available soon. Contact bcooper@meptec.org if you have any questions on this event. ◆

MEMBER NEWS

XILINX SHIPS WORLD'S FIRST HETEROGENEOUS 3D FPGA

Xilinx Inc. has announced initial shipments of the Virtex®-7 H580T FPGA, the world's first 3D heterogeneous all programmable product. Virtex-7 HT devices use Xilinx's stacked silicon interconnect (SSI) technology to deliver the industry's highest bandwidth FPGAs, featuring up to sixteen 28 Gbps and seventy-two 13.1 Gbps transceivers, making them the only single-chip solutions for addressing key Nx100G and 400G line card applications and functions.
www.xilinx.com

CAD DESIGN SOFTWARE RELEASES VERSION 8.1.0

CAD Design Software, Inc., a leader in integrating mechanical and electrical design tools, has announced the release of EPD version 8.1.0. Many improvements have been made to the software: new features and capabilities; Eighty new commands; focus on Lead Frame Technologies (QFP, QFN); Design reuse (automatic intelligizing); Links to Cadence APD/SiP 16 and higher; Links to Ansys Simulation tools; Net checking improvements and enhancements; Multi-layer processing for Copper/Power Planes and Dielectric layers; Documentation updates; More robust EPD processing engine to handle large designs with high pin counts and nets; CAM processing tools (Panelizing,

links to bondwire machines); Gerber processing and new time-saving functions, plus much more.
www.CAD-Design.com

ALTERA NAMES INDUSTRY VETERAN SCOTT BIBAUD SENIOR VICE PRESIDENT AND GENERAL MANAGER

Altera Corporation has announced that Scott Bibaud, an 18-year veteran of the communications industry, has joined the company as senior vice president and general manager, communications and broadcast division. In this leadership role, Bibaud has oversight of systems solution development and marketing for the communications and broadcast industries worldwide. He reports to John Daane, Altera's president, CEO and chairman of the board.
www.altera.com

ASE CELEBRATES OPENING OF WEIHAI PHASE 3 FACILITY

ASE celebrated the official opening of its Phase 3 manufacturing facility in Weihai, Shangdong province, China. The new building is part of ASE's expansion plans to increase its manufacturing capacity for discrete packaging and test. The new building occupies a land space of 5,120 square meters with a built up floor space of 30,560 square meters. ASE plans to recruit an additional 2,000 employees in engineering, development and operations for the new facility. Over the years, ASE has invested about $200 million on building expan-

Finetech Shows Support for University Research

Finetech will donate a high accuracy die bonder in a drawing this summer that is open to U.S. and Canadian qualified universities and colleges. The multi-application FINE-PLACER® Pico MA bonder, with 5 micron placement accuracy, is valued at $100,000.

In conjunction with the company's 20th anniversary this year, Finetech is celebrating the university R&D segment of their business. With a wide installed base of systems at some of the most prestigious institutions, FINEPLACER® die bonders provide an ideal solution with precision and repeatability in a platform that is perfect for advanced technology environments utilizing diverse applications.

The FINEPLACER® Pico MA is an 'all-in-one' modular platform for advanced packaging and assembly applications – such as flip chip, optoelectronics, 3D, wafer level integration, micro-optics assembly, sensor packaging and precise die bonding.

For more information or to register for the drawing, visit http://www.finetechusa.com/bonders/products/promotion.html. Registration ends July 31, 2012. ◆

Good Reviews for Sonoscan's Gen6™ Acoustic Microscope

LAST JULY, WHEN Sonoscan introduced its Gen6 high-end laboratory acoustic microscope, the designers of the microscope were eager to see reports from the field. One innovation was Sonolytics™ software, an advanced and very smooth Graphical User Interface.

The reports are now coming in. "The big difference," one user commented, "is that the Gen6 system allows me to concentrate on the parts I'm working with, and on getting data and images from those parts, rather than concentrating on the details of operating the microscope." Another user called the software "precisely intuitive" in getting him the results he needs, while also saving time by cutting out unneeded tasks.

Users also remarked that it was very useful to be able to select any resolution from <1 megapixel to 268 megapixels, rather than being limited to prescribed values.

Also new in the Gen6 system was the PolyGate™ module , which lets the operator "slice" a part into as many as 200 thin slices and make an image of each slice during a single scan. Design-

ers of the Gen6 system thought that PolyGate analysis would be most useful in imaging multilayer samples and bulk materials such as ceramic.

What designers did not anticipate was the extent to which inventive users would make thin-slice images of plastic-encapsulated microcircuits in order to determine, for example, whether the die was tilted.

Another Gen6 system innovation is a 500MHz pulser having improved signal stability, important for example in 230, 300 or 400 MHz imaging of flip chip underfill, bumps and related features.

Sonoscan is the leading developer and manufacturer of acoustic microscopes and sophisticated acoustic micro imaging systems, widely used for nondestructive analysis of defects in industrial products and semiconductor devices. For over 30 years, Sonoscan's attention to customer needs and investment in R&D has created systems that set industry standards for speed and accuracy. Key products include C-SAM® systems for off-line and laboratory analysis and FACTS2™ automated production inspection systems.

Sonoscan, Inc. is located at 2149 E. Pratt Blvd., Elk Grove Village IL 60007. Contact Steve Martell at 847-437-6400 x240; email info@sonoscan.com; or visit www.sonoscan.com. ◆

ITC, CAST, IEEE, and Test Vision Team up on Test Programs at SEMICON West

IN COOPERATION WITH INTERNATIONAL Test Conference (ITC), Collaborative Alliance for Semiconductor Test (CAST), IEEE, and SEMI, SEMICON West 2012 will feature the latest trends, technology, solutions and methodologies in semiconductor test. In addition to presentations by industry experts in conference TechXPOTs, an expanded Test Vision 2020 Conference will again be held in conjunction with SEMICON West, providing critical information and networking opportunities for test industry buyers, managers, developers and technologists.

Test Sessions at SEMICON West

At the TechXPOT session in Moscone Center's North Hall on Tuesday, July 10, the afternoon session on *Adding Value through Yield and Better Data Management* will examine how leading IC manufacturers and OSATs are better leveraging data to improve yield, decrease test time and perform effective root cause analysis to lower test costs. Real solutions and techniques in Adaptive Test, closed-loop data management, DFM-aware and layout-aware diagnosis tools, 3D-IC Test, and other areas will be discussed by leading experts from Mentor Graphics, Texas Instruments, Optimal Test, Teradyne, Camstar Systems and Advantest.

On Wednesday, July 11, in a first-ever collaboration with International Test Conference, leading peer-recognized academic and technical presentations on semiconductor test will be presented at the TechXPOT North on the exhibition floor at SEMICON West. Leading papers on cell aware analysis, systematic defect analysis, end-to-end error correction, and timing variation tolerance will be presented by speakers from Mentor Graphics, Carnegie Mellon University, University of California at Santa Barbara, and the China Academy of Sciences.

Test Vision 2020 Expands

Co-organized by SEMI and IEEE, Test Vision 2020 (formerly ATE Vision 2020) has emerged as the premier workshop in semiconductor test and Automated Test Equipment. Attracting executive attendance from a broad cross-section of the semiconductor community, the workshop features a compelling line-up of papers, keynotes and panel participation from leaders in the industry. This year's workshop will expand to one and one-half days, beginning on Wednesday, July 11 at 3:00pm and continuing until 5:00pm on Thursday, July 12. Experts and executives from chip manufacturers, EDA companies, fabless semiconductor companies, outsourced assembly and test firms, and other industry stakeholders will discuss the future of semiconductor testing, and network with colleagues in a friendly, interactive environment.

SEMICON West Goes Mobile

SEMICON West has introduced a new mobile app for attendees, bringing virtually all of the show content to iPhones, iPads, and Android devices. The SEMICON West mobile app, sponsored by Applied Materials, acts as a portable guide to the event, with access to complete exhibitor listings, floor plans, program schedules, speakers, and local information. The new app is available now from the iTunes Store and Google Play. More information about the app is available at: www.semiconwest.org/Participate/MobileApp

For more information about SEMICON West visit www.semi.org. ◆

Fab Equipment Spending: Positive Growth for 2012 and 2013; All-Time Record for 2013

BREAKING THE BARRIER into positive growth for 2012, the end-of-May edition of the SEMI World Fab Forecast shows improved growth in fab equipment spending this year – at US$ 39.5 billion, a two percent year-over-year (YoY) increase. For 2013, fab equipment spending is expected to reach an all-time record high, with $46.3 billion or 17 percent growth from 2012. Even with a small growth rate, 2013 will yield an all-time record high for fab equipment spending, if macro-economic factors do not intervene.

Regions planning to spend the most on fab equipment in 2012 are: Korea (over $11 billion), Taiwan ($8.5 billion), and the Americas ($8.3 billion). In 2013, the largest spending is expected again in Korea (over $12.5 billion), the Americas (over $11.5 billion), and Taiwan (over $8 billion). All product types are increasing equipment spending in 2012 with the largest increase seen in 2012 for Memory and Foundry.

Learn more about the SEMI World Fab Forecast at www.semi.org/MarketInfo/FabDatabase. ◆

sion, equipment purchase, facility upgrading and R&D.
www.aseglobal.com

CRITICAL ION IMPLANT TECHNOLOGY FOR SCALING FUTURE CHIPS INTRODUCED BY APPLIED MATERIALS

Applied Materials, Inc. announces its new Applied Varian VIISta® Trident system, the semiconductor industry's most advanced single-wafer, high-current ion implant system. Used to engineer the electrical characteristics of the chip by embedding "dopant" atoms, the new VIISta Trident system is the only ion implanter proven to achieve the yields necessary for manufacturing high-performance, power-efficient logic chips at the 20nm node.
www.appliedmaterials.com

QUARTET MECHANICS RECEIVES REPEAT ORDER FOR THIN WAFER HANDLERS

A leading provider of CMP/Grinding tool OEM has placed a repeated order for **Quartet Mechanics** wafer handllers to meet their 50-micron thin wafer need. The customer's CMP tool features high flexibility and most advanced technology to meet the growing demand in wafer thinning application for global semiconductor, Data Storage, MEMS, LED, Photonics and Precision Optics industries. The repeated order is another recognition of the superior R&D team work at Quartet Mechanics.
www.quartetmechanics.com
◆

EVENT FOLLOWUP

By Sandra Winkler

On Safari at ECTC

SAN DIEGO, HOME TO THE world-famous San Diego Zoo and Wild Animal Park, also hosts the annual ECTC (Electronic Component Technology Conference) every three years. Attendance at this year's 62nd ECTC, held May 29th through June 1st, was 1,230 – the second highest level of attendance since the inception of the ECTC 62 years ago.

A special session was held on Tuesday morning, titled *"Next-Generation Packaging and Integration: The Transformed Role of the Packaging Foundry."* Chaired by Raj Pendse of STATS ChipPAC, speakers included Robert Lanzone of Amkor Technology, Bill Chen of Advanced Semiconductor Engineering (ASE), Mike Ma of Siliconware Precision Industries (SPIL), Steve Anderson of STATS ChipPAC, and Dan Tracy of SEMI. Capital expenditures are going up by an order of a magnitude with TSVs in the equation, making it difficult for OSATs to fund their own growth. The need for collaboration was brought up not only here, but in many other conference sessions as well. About 3 percent of the top OSATs' revenue is designated for R&D, which is feeding new technologies and helping these companies find new ways to reduce costs.

2.5-D is a hot topic, and is already in production in small quantities; bringing costs down will fuel the growth. TOs cost $35 in 1963 if the purchase price had not been artificially lowered (selling below cost), the industry would not have flourished as it did, when it did. The same will be true of other upcoming technologies—a lower cost will fuel purchasing power. The FOWLP, or fan-out wafer-level package, is opening up new possibilities of new markets.

The Tuesday night panel session, titled *"Power Electronics – A Booming Market,"* was chaired by Rolf Ashenbrenner of Fraunhofer IZM and Ricky Lee of Hong Kong University of Science and Technology. Speakers included Dan Kinzer of Fairchild Semiconductor, Klaus-Dieter Lang of Fraunhofer IZM, Lionel Cadix of Yole Development, Ljubisa Stevanovic of GE Global Research, and Bernd Roemer of Infineon Technologies AG. This technology is hot primarily in Europe, for renewal energies, power supplies, e-mobility, LED systems, smart power electronics, and network control. New materials and technologies will be needed in this market. Aluminum ribbon, copper aluminum ribbon, or copper wire bonding will replace aluminum wire bonding, and silver sintering or diffusion soldering for die attach will improve device life.

The Wednesday luncheon keynote speaker was Gregg Bartlett of GLOBALFOUNDRIES. He mentioned the need for collaboration during design, something that previously didn't occur. This will bring the best minds to the table at the outset. 2.5-D and 3-D really require collaboration to make the whole fit seamlessly together. These technologies offer improved system-level performance and bandwidth with reduced latency and power requirements compared with competing technologies.

The Wednesday evening plenary session on *"Photonics, Expanding Markets, and Emerging Technologies"*, was chaired by Christopher Bower of Semprius, Inc. Speakers included Ashok Krishnamoorthy of Oracle, Jeff Perkins of Yole Développment, Shen Liu of Huazhong University of Science and Technology, Alexander Fang of Aurrion, Timo Aalto of VTT Technical Research Centre of Finland, and Frank Libsch of IBM Corporation. LEDs, photonics integration on silicon, photonics packaging, and photonics to the processor chip were covered in this broad field.

Packaging is 40 percent of the cost of an LED. The cell phone was the first killer application for LEDs; general lighting – otherwise known as HB (high brightness) – will be the next big thing for the LED market. Currently the cost of an LED light bulb is anywhere from $15 to $40 with rebates, compared with less than $1 for an incandescent bulb, putting LEDs out of reach for most residential customers. The cost of an HB LED needs to come down by a factor of 10, which will come about with a lower-cost packaging solution, such as wafer-level packaging.

The photonics industry in general does not have much in the way of standards. Photonics involve using light to carry the signal, rather than an electron. Photonics can be used in large-area data centers and on a single high-powered silicon chip. Uses abound in telecom, datacom, and computers. Because of the current high-cost manual processes to create photonic structures, efforts in recent years have focused on bringing costs down in a number of ways. In fiber-optic telecom uses, getting the package standardized, as in the IC world, has been up in the air for some time. Connecting the delicate fiber structures to a standardized package such as a butterfly package is difficult. Bringing photonics down to the computer level, either inter-chip or intra-chip, involves lowering the costs significantly by incorporating waveguides on silicon, a low-cost material. This is years away from actual production, and will require a killer application to justify spending the R&D costs to make it a reality.

The final evening session on Thursday night was titled "Advanced Coreless Package Substrate and Material Technologies." The co-chairs were Kishio Yokouchi of Fujitsu Interconnect Technologies and Venky Sundaram of Georgia Institute of Technology. Speakers included Yuji Nishitani of Sony Corporation, Tanaka Kuniyuki of Shinko Electric Industries Co., Takeshi Eriguchi of Asahi Glass Co., and Masateru Koide of Fujitsu Advanced Technologies.

Advantages of coreless substrates are several. Wiring capabilities allow direct signaling; all layers can be used as a signal layer. High performance comes from the lowest self-inductance and the highest mutual inductance. A coreless substrate is likely the widest bandwidth substrate structure.

Assembly problems include a higher warpage factor than with a cored substrate. A number of options were presented to overcome warpage issues, including: use of a clamp during chip attach; use of lower CTE insulator prepreg materials; use of a stiffener; and lower temperature soldering.

The program sessions ran for three full days, with six parallel sessions running at all times. Thus the topics to choose among were copious, and included advanced packaging methods such as 2.5-D/3-D, advanced interconnect, wafer-level packaging, LEDs, substrates, optoelectronics, modeling and simulation, materials and processing, RF, applied reliability, and emerging technologies. There was something for just about everyone connected to components, packaging, and manufacturing technologies (CPMT) in this jungle of options. ◆

SANDRA WINKLER is Senior Industry Analyst at New Venture Research (newventureresearch.com), and the IEEE/CPMT Luncheon Program Chair.

INDUSTRY INSIGHTS

By Ron Jones

Crossing Lines

IT'S NATURAL FOR THE BUSINESS model of an industry to evolve as it matures. The first cars built by Henry Ford used parts from outside suppliers. Later he developed the assembly line concept and moved to a vertically integrated model, bringing most of parts manufacturing in house. Over time, auto companies reversed and moved toward a more disintegrated model, again using parts from myriad external suppliers.

As models evolve, we begin crossing lines that were initially considered difficult, imprudent, impractical or impossible. Sometimes the line is crossed, but later the direction is reversed.

Semiconductor Companies – From a Building to the World

The semiconductor industry began with a vertically integrated model. After a couple of years in R&D at Signetics, I took at process engineering job at Texas Instruments in Sherman, TX in 1969. We performed all the integrated circuit design and manufacturing steps, from crystal pulling through final test, in one building. The only things we did not manufacture were polycrystalline silicon, photomasks and ceramic packages, which were manufactured by TI divisions in Dallas. This model was typical of larger IDM's in the 60's.

Driven by numerous factors, IDM's began a disintegration of the semiconductor supply chain, both from a geographical and ownership perspective. We began to cross lines from a vertically integrated business model to more distributed and outsourced business models. Some may get confused between outsourcing (using suppliers to provide goods and services) and off-shoring (moving operations to typically lower cost locations.) Though somewhat related, they are independent concepts. Offshoring can include both captive and outsourced operations.

Due to the labor intensive nature of assembly, IDM's began building factories in Asia (off-shoring) and using subcontract assemblers (outsourcing). For a number of years, final test was considered to be too complex to be entrusted to "low tech" operations doing assembly. By the mid-80's, however, many IDM's began moving testing offshore, both to their factories and to subcontractors.

For many years, IDM's built wafer fabs in North America, Europe and Japan. These were captive operations for the company. The thought of outsourcing wafer fab to subcontractors had all the fears of outsourcing complex test, but on steroids. Needless to say, this changed.

Foundry Models – IDM vs. Pure Play

If you ask what company was the first to offer foundry services, many will answer TSMC in 1987. This is partially correct as TSMC was the first company dedicated to foundry services, but was not the first to offer foundry services. MOSIS, an IDM, began offering foundry services in 1981 and UMC, an IDM, began offering them in 1983. If we look at the top 15 foundries today, 12 are pure-play and 3 are IDM (Samsung, IBM and Magnachip), but this has not always been the case. Having an IDM offer foundry services has potential for conflicts of interest if their captive products are similar to those of their foundry customers. Without going into details, in the mid-90's, UMC made the decision to spin off their product divisions and become a pure-play foundry. TSMC stated early on that they never wanted to be put in the position of being in competition with their customers. Even today, IDM's like Samsung must be very careful as they provide foundry services to companies like Apple and simultaneously offer application processors chips under their own brand. As Intel moves into the foundry space, they will have to make sure they avoid these potential pitfalls.

Foundry Models - Wholly Owned vs. JV

By the mid-90's, the foundry/fabless model was well established and growing rapidly. Business was strong and capacity was limited. Some fabless companies wanted more control over their fate, but not to the point of building their own fabs. During this period, several foundry/fabless JV fabs were built that ensured capacity to the fabless investor. USC, USIC and UICC were JV's between UMC and fabless companies like Xilinx. Each fab was a separate corporation with its own independent management team, but under the UMC umbrella. Over a relative short time line, these fabs were acquired by UMC and the JV concept was scrapped. Chartered did a JV fab (CSP) with HP (now Avago) and a JV fab (SMP) with Lucent (now LSI). TSMC accepted funding from customers in 1995 for capacity additions in Taiwan and in 1996, TSMC did a JV in Camus, Washington with Altera, Analog and ISSI, which is now wholly owned.

There are a number of successful JV fabs, but they tend to be between IDM's, not between foundries and their customers. Examples are Inotera, a JV between Nanya and Micron and IP Flash, a JV between Micron and Intel.

Foundries Do Fab, OSAT's Do Assembly

I've talked about this before. Over the past dozen years, OSAT's have moved into wafer processing with redistribution layers, bumping and back grinding. While this is really not wafer fab, it is processing product in wafer form. In my last column I talked about TSMC moving into the assembly arena with plans to do turnkey processing on advanced products like SoC's involving stacking. TSMC doesn't have a lot of experience in assembly, but they have lots of money and talent. There is still much sorting out in this space with the likely outcome being some of each.

In closing, I'll leave you with this quote by Mark Bohr of Intel, "The foundry model is collapsing." If true and the foundry model is no longer viable, that would be the biggest (reverse) line crossing in the history of the semiconductor industry. Personally, I think the foundry model is alive and well and this statement is merely posturing by a company who has decided to get in the foundry business. I guess time will tell. ◆

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MEMS TECHNOLOGY

By Ira Feldman

Thinking Big: $1 Trillon MEMS Market

JANUSZ BRYZEK (FAIRCHILD Semiconductor) has set a dramatic and ambitious goal of $1 trillion sales for the microelectromechanical systems (MEMS) market in 2022. Even though MEMS market revenue is expected to be "only" $12 billion in 2012, he isn't being called a fool. Having cofounded eight seminal MEMS companies, Janusz is taken quite seriously.

At MEPTEC's *10th Annual MEMS Technology Symposium "Sensors: A Foundation for Accelerated MEMS Market Growth to $1 Trillion"* there were some who doubted the market would grow this large.

In his keynote *"Sensory Swarms"*, Professor Kristofer Pister (University of California and Dust Networks) described the possibilities and challenges of very large sensor networks. Sensor technology has "crossed the chasm" for use in industrial automation applications. Key attributes are the sensor must be reliable, usable anywhere, last for over a decade without requiring service (including changing batteries), and easy to deploy. Hence the interest in wireless self-configuring networks that drop into existing business systems.

In an example of using one million sensors in a steel mill, overall efficiency increased over 5% by moving from scheduled based equipment maintenance to as-needed service. He claims this as one of the biggest performance improvements in the history of industrial steel making. Streetline's distributed network which senses available street and garage parking spaces in major cities and provides real time data to their smartphone application is another example.

There will be more large sensor swarms but that won't get us to one trillion units.

Getting There

In *"Accelerating MEMS Market to $ Trillion / Trillion Units"*, Janusz discussed the growth history and potential of the sensor and overall MEMS market. He highlighted Hewlett-Packard's (HP) Central Nervous System for the Earth (CeNSE) which is proposing a network of a trillion nodes and Bosch's view of 7 trillion devices serving a population of 7 billion in 2017. Challenges needing to be solved for future growth include: no atomic level simulation to reduce the need to build physical devices to check both designs and fabrication processes, device packaging unique to each family of designs, and test methods that are specific to each design. Lastly he identified the need for greater process standardization to enable a foundry model similar to that of the semiconductor industry.

Robert Haak (MANCEF) proposed an industry roadmap in *"Implementing the Trillion Dollar MEMS Roadmap"*. He identified three areas for coordination: "sensor technology itself, technology of data transfer from the sensor, and technology behind the equipment used to process the data." Mr. Haak suggested companies need to move from competition to coopetition to accelerate progress.

Market Numbers

In *"On the Road to $1T?"*, Gregory Galvin (Kionix) reviewed future applications (enhanced location based sensing, augmented reality, health monitoring, etc.). From their experience, MEMS sensors are extremely price elastic and lower prices clearly increases the numbers of units sold.

In terms of the one trillion dollar market, Mr. Galvin calculates since MEMS sensors on average are 2% of the end product cost this would imply a $50 trillion market. This is unrealistic since this is roughly 80% of the world's current gross domestic product (GDP). However, industrial end application (with ~ $7 T GDP) is a reasonable $140 B available market today if they all used MEMS sensors at ~ 2% content. At a 15% compounded annual growth rate (CAGR) this could grow to roughly a $0.5 T market for 1 T units if $0.50 average selling price (ASP).

Jérémie Bouchaud (IHS iSuppli) in *"The MEMS Revolution: from Billions to Trillions?"* noted historical growth sectors for MEMS sensors have already saturated. Smartphones and tablets have gone from explosive growth of 60-90% per year to estimated rates below 25% moving forward.

In *"Integration of the Accelerometer*

— the First Step of the MEMS Revolution", Jean-Christophe (JC) Eloy (Yole Développement) similarly reviewed overall market trends. Gyroscopes and accelerometers are reaching market saturation and combined devices are lowering total unit counts and revenue per function. He does not see a $1T market but other opportunities to add value beyond MEMS sensors.

In his keynote *"Motion Interface the Next Large Market Opportunity"*, Steve Nasir (InvenSense) made an important point about market projections: five years ago no analyst predicted substantial penetration of gyroscopes in mobile devices. This changed when Apple launched the iPhone in 2007 and every other mobile device manufacturer madly scrambled to include gyroscopes. All it takes is one leader to create a substantial market.

Challenges

Stephen Breit (Coventor) in *"Realizing the Full Potential of MEMS Design Automation Software"* discussed reducing the design cycle time and costs of prototype runs by simulating the final design and fabrication processes. Coventor has started to integrate their different design tools to understand both mechanical and electrical designs with the ultimate goal to simulate all device specifications.

In *"High Volume Assembly & Test Solutions to Meet the Rapidly Growing MEMS Market"*, Russell Shumway (Amkor Technology) discussed the proliferation of package types driven by a diverse set of end applications. All of these MEMS devices have device specific test requirements that have to be accommodated too.

Applications

In *"CeNSE: Awareness through A Trillion MEMS Sensors"*, Rich Friedrich (Hewlett-Packard) detailed HP's total sensing solutions. It is not just the sensor but how to make a measurement, interconnect the sensors to data processing equipment, manage large volumes of data, and perform data analysis and visualization. A prime example is how they use up to one million sensors for oil exploration.

The final session, *"MEMS for All of Us"*, started with Tristan Joo (Wireless Communications Alliance) presenting *"Fusing Sensors into Mobile Operating Systems & Innovative Use Cases"*. Even though today's smartphones each have at least five MEMS sensors (out of 12 to 18 total sensors), less than one half of a percent of all applications use these sensors in a meaningful way. As mobile operating systems mature, more support is being built-in to enable implementation of new and innovative sensor solutions.

Each of these companies then demonstrated their MEMS sensor products:

- HillCrest Labs – natural motion based (gesture control) user interface
- Movea – intellectual property (IP) cores for mobile applications
- Sensor Platforms – sensor data integration for "context aware" mobile devices
- Syride – surfing and paragliding sports performance measurements
- VectorNav Technologies – using sensor fusion to increase performance of consumer grade MEMS sensors for more demanding applications
- Xsens – MEMS sensors worn on the body to perform motion capture without cameras

Summary

Is a trillion dollar and/or unit market feasible? Many speakers were intentionally vague and the answer is likely to change drastically depending on the average selling price per sensor.

Key takeaways:

- The value is in higher order solutions not in producing the MEMS sensor.
- The rate of adoption is severely influenced by price. ASPs need be < $1.
- A coordinated roadmap is needed to reduce costs and solve technical challenges.
- Vendors need to educate software developers and product designers to increase MEMS sensor adoption.
- Be wary of market estimates in new markets with new applications as they can be overly optimistic or pessimistic. ◆

This is an abridged version of the posts that Ira wrote on his blog www.hightechbzidev.com

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to commercialization. He follows many "small technologies" from semiconductors to MEMS to nanotechnology engaging on a wide range of projects including product generation, marketing, and business development.

MEDICAL ELECTRONICS

By Guna Selvaduray

Are Excellence in Design and Manufacturing Alone Sufficient?

PRACTICALLY ALL OF US OWN automobiles. The questions we ask, or are interested in, when we shop for an automobile are generally pretty standard: engine size, fuel consumption, cost of ownership, resale value, and the number of creature comforts that are available. These days many automobile companies make it a point of advertising the luxury features their automobiles have, e.g., acceleration time from 0 to 60 mph, and other high performance features. However, automobiles have to meet a number of other requirements before they can be legally marketed. Key among these are the federal safety standards and the emission standards imposed by the states. In order to meet these standards a variety of testing needs to be done; these are tests that the consumer generally does not think about too much, but the manufacturers have to develop and report on. In addition, they have to be economically competitive, with the price being decided by each company.

In the case of medical devices, engineered products have to go through a larger number of rigorous tests, proving safety and efficacy, before they can be marketed. These are overseen by the Food and Drug Administration (FDA) and submissions to the FDA demonstrating safety and efficacy must be done first, and FDA approval obtained, before a product can be marketed for public use. The level of detail required varies, depending on the risk posed by the product, and whether there are similar products already on the market or if the particular product is indeed a first-of-its-kind. The pathway to FDA approval can involve a large number of tests that are not directly related to "electronics", but are nevertheless required. In addition to bench/laboratory tests, these could involve testing in animals, and potentially testing in humans as well. The protocols required for these tests are generally not taught in electrical/electronics engineering curricula. Specialists who are familiar with these protocols are required. In the case of animal studies one needs to bear in mind that the correct animal needs to be identified for the tests, and this depends on the particular function the device will be performing in the human body. When it comes to clinical (human) trials, key among the protocols is the procedure to be followed when recruiting volunteers and confidentiality of the records, in addition to the actual medical procedures. Another important aspect of this process is labeling of the product, clearly describing the use for which it is intended, and uses to be avoided.

The job is not complete when FDA approval is granted. The approval from the FDA permits the manufacturer to sell the product, but there is still the issue of who will pay for the device and the procedure for implanting the device. This aspect of medical device economics is "Reimbursement", and a separate application needs to be made to the Center for Medicare and Medicaid Services (CMS), which determines the amount that will be paid for the entire procedure, including the device. The private health insurance companies generally follow the guidelines set by CMS. Regardless of how unique and clever a new medical device might be, if the cost to manufacture and sell it, and to implant it, is not covered by some form of health insurance, its viability as a commercial product can plummet. There are several companies that have developed unique products, but have not been able to successfully commercialize it simply because the reimbursement process had not been addressed appropriately.

In any product, excellent design and engineering are the core requirements, but a variety of related issues need to be addressed in order to have a commercially successful and viable product. This is particularly true in the case of medical devices because addressing many of the "related issues" is not just prudent practice, but also required by law.

Once the core scientific/engineering idea has been refined, a team consisting of regulatory affairs, reimbursement, clinical trials, and human factors professionals, among others, needs to be assembled to map out a development pathway so that the product can be taken to market successfully, and expediently. ◆

DR. GUNA SELVADURAY is an educator, researcher and consultant. He is Professor in Materials Engineering at San Jose State University.

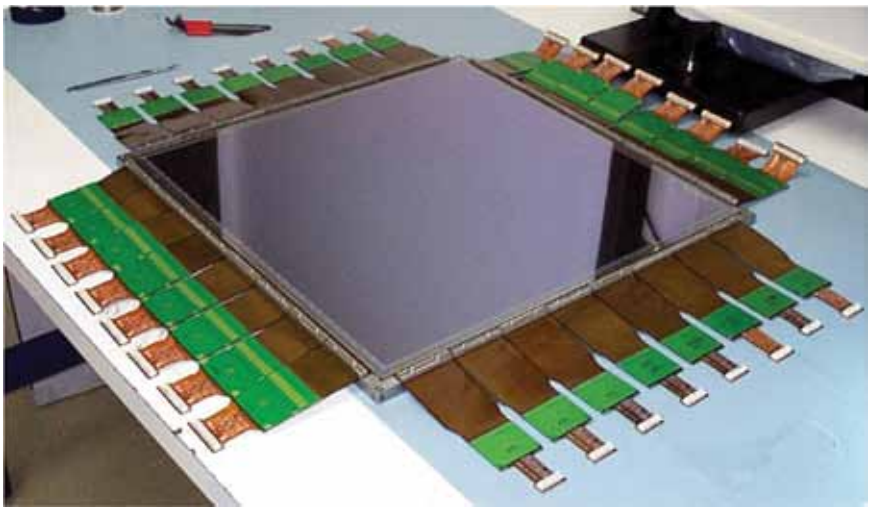
Flex Circuit's Flexibility for Medical Electronics

E. Jan Vardaman and Karen Carpenter
TechSearch International, Inc.

AS DEVELOPING COUNTRIES SEE increases in their aging populations, the need for devices to improve the quality of life and maintain health is growing. These factors are driving the demand for medical electronics, and in turn, the growth of flex circuits for a variety of applications. Flex circuit is selected in many cases for form factor and electrical performance reasons.

Flex circuits are found in some pacemakers, defibrillators, neurostimulators, cochlear implants, and hearing aids. Flex circuit is also used in digital imaging applications such as X-ray, CT, and ultrasound systems and is found in ultrasound probe heads, catheters, and even retinal implants and pill cameras. Disposable products such as glucose monitor strips and blood sensors also use flex circuits. The growth in portable medial electronics systems may increase the use of flex circuit, but having a reliable supply base is critical.

For many flex circuit makers, the requirements for medical electronics remain a mystery. This wide variety of applications may all use flex circuit, but the size, complexity, and form factor differs in every case. For example, X-ray systems use flex circuit to connect the detectors to the amorphous-silicon (a-Si) thin film transistor (TFT) arrays. The flex typically used in digital imaging applications for X-ray and CT is typically 2 metal layers with polyimide thickness of 2 to 3 mils. MRI systems use flex circuit in coils known as phases-arrays.



Digital X-ray Panel. *Image courtesy of GE Healthcare.*

Ultrasound probes use flex circuit to connect the transducer to the electronics for signal processing. With such a wide variety of probe designs, there are also differences is the size and shape of the flex circuits used even within the same application. Ultrasound flex are typically two metal layers and can run up to four metal layers. Some single layer designs are still in use.

Some companies use flex circuit in hearing aids. For example, Valtronic mounts gold stud bump flip chip devices on flex circuit that is manually rolled or folded and encapsulated to form a compact module that saves as much as 80 percent of the space occupied by conventionally assembled circuits and provides greater power efficiency than the conventional wire bond (chip on board).

The difficulty in analyzing this market is that no two examples are alike. Recognizing the need for high reliability in medical applications, iNEMI has a project underway to help develop common tests for flex circuits used in medical applications. Development of common tests such as bend radius and identification of common use stress conditions will enable industry suppliers to better understand the market and enable users to more easily find suppliers that can meet their needs. iNEMI's work has just started and will likely include a survey of the medical flex supply chain (from users to suppliers) to ensure that the most critical gaps are being addressed. Once the initial planning is complete, the group will encourage broad industry participation. ◆

SYMPOSIUM

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Presented In Association With

ASU Ira A. Fulton Schools of Engineering
ARIZONA STATE UNIVERSITY

School of Biological and Health Systems Engineering

2012 Medical Electronics Symposium

Technology, Personal Health and the Economy

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  Personal Health: Concepts Impacting Healthcare
  Keith Lindor, M.D.
  Executive Vice Provost for Health Solutions
  Arizona State University
- **Day Two**
  Trends in 3D Micro-packaging for Emerging Implantable Applications
  Livia Racz, Ph.D
  Division Leader, Microsystems Technologies
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- Business Growth in the Medical Electronics Industry
- Innovative Implantable Technologies
- Emerging Trends in Components for Medical Electronics
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7th Annual MEPTEC/SMTA

Medical Electronics Symposium

Wednesday & Thursday, September 26 & 27
Arizona State University, Tempe Campus, Tempe, AZ

MEPTEC AND SMTA ARE again partnering to present a two day Medical Electronics symposium which will cover a broad spectrum of topics highlighting innovative technologies and related issues in medical electronic applications and devices. There is significant economic momentum and interest in the areas of personal healthcare and the global healthcare industry in general, which continue to drive positive business trends.

This symposium will bring together technical and business professionals from the medical electronic and relevant industries to present current perspectives on the economic and industry trends as well as state-of-the-art technologies for medical applications. Current enabling technology advancements that will be utilized to improve the next generation of existing medical electronic products, along with the challenges associated with the complex regulatory and reliability requirements, will be presented by industry experts.

OLD MAIN on the ASU Tempe Campus, constructed before Arizona achieved statehood, will host the MEPTEC/SMTA Medical Electronics Symposium for the 7th year.

ASU Student Poster Session

Come see ASU faculty and student poster presentations on their medical device and diagnostics that are being developed in the School of Biological and Health Systems Engineering's Harrington Program of Biomedical Engineering. Graduate and Undergraduates are taught about medical device design, the FDA's quality systems regulations and marketing of these devices as well as the research process itself. These biomedical engineering students work in a variety of subfield in BME, ranging from neurostimulation, neural prosthetics, point of care technologies, neural and car-diovascular recording instrumentation, medical imaging agents and instrumentation, cardiovascular flow models, prosthetics and rehabilitation devices, among many others.
Wednesday, September 26 following Day One Sessions.

Presented In Association With

ASU Ira A. Fulton Schools of Engineering
ARIZONA STATE UNIVERSITY

School of Biological and Health Systems Engineering

Technical Sessions:

Day One

- Business Growth in the Medical Electronics Industry
- Innovative Implantable Technologies
- Emerging Trends in Components for Medical Electronics
- Requirements Beyond Electronics to Bring a Product to Market

Day Two

- Medical Standards, Regulatory & Compliance
- Integrating Process Excellence into Design Control
- Advanced Medical Electronics Packaging Technology
- The Future of Medical Electronics Systems

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Nicholas Leonardi, Director of Business Development , *Premier Semiconductor Services*

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Dale Lee, Staff DFX Process Engineer, *Plexus Technology Group*

General Chairman - SMTA
Ron Molnar, Executive Director, *AZ Tech Direct, LLC*

KEYNOTES

Keith Lindor, M.D.

Day One Keynote

Personal Health: Concepts Impacting Healthcare

Keith Lindor, M.D.
Executive Vice Provost for Health Solutions
Arizona State University

Dr. Lindor is the newly appointed Executive Vice Provost for Health Solutions at ASU. He served as the Dean of the Mayo Medical School from 2005- 2011 where he was also a Professor of Medicine in Gastroenterology and Hepatology at the Mayo Clinic College of Medicine in Rochester, Minnesota. ◆

Livia Racz, Ph.D.

Day Two Keynote

Trends in 3D Micropackaging for Emerging Implantable Applications

Livia Racz, Ph.D.
Division Leader, Microsystems Technologies, Charles Stark Draper Laboratory

Dr. Racz is the Division Leader of Microsystems Technologies at the Charles Stark Draper Laboratory in Cambridge, Massachusetts. She is responsible for delivering first-of-a-kind microfabricated sensors and systems in the areas of bioMEMS, inertial instruments, miniature low power electronic systems, and others. ◆

Amkor Assembly and Test (Shanghai) Co, Ltd.

Amkor Technology, Inc.

Broad Capability and Corporate Vision Continues to Strengthen Amkor's Position as a Leading Technology Partner

AMKOR TECHNOLOGY, INC. IS ONE of the world's largest and most accomplished providers of advanced semiconductor packaging, assembly and test services. Founded in 1968, Amkor has become a strategic manufacturing partner for hundreds of the world's leading semiconductor companies and electronics OEMs, providing a broad range of advanced package design, assembly, and test solutions.

Amkor's extensive product portfolio includes leadframe, ball grid array, chip scale and wafer level packaging. Specialty packaging for MEMS and sensors are also supported, along with wafer bumping and redistribution services. Amkor maintains, and continues to build upon, an industry leading position in flip chip and advanced packaging.

The availability of high quality packaging services allows Amkor's customers to focus their resources on semiconductor design and wafer fabrication while utilizing Amkor as their packaging and test partner and, where required, their packaging technology innovator.

As a strategic provider to the semiconductor industry, the following areas represent the four cornerstones of Amkor's business:

- Technology leadership and innovation
- Strategic alliances with customers and partners
- High volume manufacturing with a comprehensive infrastructure, global footprint, and diversified operational scope
- Financial discipline and strength

Packaging is a complex, challenging business defined by the merger of divergent materials, functions, and structures prescribed by third parties. The art and skill of semiconductor packaging lies in the concept of "successful convergence" – preserving discrete die function through seamless integration – and yielding the platforms that become the building blocks for electronic systems. The strength of the OSAT lies in its depth and breadth of experience to identify and implement successful package designs.

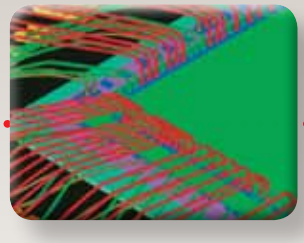
Amkor's product portfolio is a major strength and reflective of the company's ability to respond to both standard and custom packaging requirements. Prompt implementation of programs founded on decades of experience allow for rapid time-to-market. The same experience can also identify downstream needs and recommended solutions outside the conventional definition of a particular package family. Consideration of application, materials or technology trends foster a creative mindset that encourages fresh ways to approach the varied and wide range of packaging options available to service today's dynamic markets.

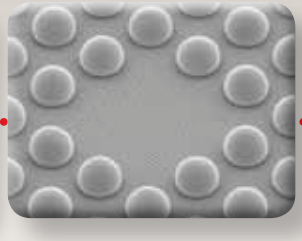
A Progression of Innovation

Over the years, Amkor has introduced numerous industry leading package platforms. The lead frame product line has expanded. Ball grid arrays, chip scale and wafer level packages, complex three dimensional multichip systems, and specialized packages housing MEMS and sensors have been added. Today, Amkor is recognized by many to be a technology leader in the OSAT space.

Accelerating Time to Market

Turnkey IC Design, Assembly, Test and Logistics Solutions





Amkor Design Center:

Every year, thousands of new designs are placed into operation providing an unparalleled level of package design expertise:

- Design chain management
- Design for Manufacturing (DFM)
- Design for Cost (DFC)
- Full design and verification of leadframe, laminate, or wafer level platforms
- Electrical, thermal and mechanical characterization:
  - SiP, RF, mixed signal, high speed digital, substrate design
  - Signal, power integrity, time delay
  - 2D, 3D and Full wave 3D package simulations
  - High accuracy thermal modeling of component level designs, material properties, board layouts (>200 thermal test reports avail)
  - Computation Fluid Dynamic (CFD) models
  - Package warpage, CTE mismatch, stress analysis
- Web-based access & EDA support

Wafer Bump and Probe:

- Wafer bump solutions for 300mm and 200mm
- Redistribution layer (RDL) metallization & technology
- High volume, turnkey wafer level packaging
- Integrated passive construction
- Wafer probe solutions for 300mm and 200mm:
  - Thin wafer handling and full temperature range
  - RF and multi-site
  - All supporting wafer handling, mapping, and processing

Assembly:

- Broad portfolio of products
- Turnkey solutions for wirebond and flip chip
- High-volume manufacturing in 6 Asian countries
- Wafer finishing (TSV) and 2.5/3D assembly
- Wafer thinning, dicing, micro-joining
- Broad portfolio of Pb-free and Green packages
- Amkor assembles around 7% of the world's ICs

Newer package platforms have included Package-on-Package (PoP) with Through Mold Via (TMV®) technology, flip chip molded BGA (FC^{M}BGA) packages, and a makeover of the standard PBGA. Newer technologies such as fine pitch copper pillar micro-bumps and the development of the manufacturing infrastructure supporting stacked CSPs to through silicon via (TSV) architectures have received widespread attention. The industry continues to focus on 2.5/3D and TSV designs. System-in-Package (SiP) approaches are being revisited now that silicon interposers with copper pillar interconnects have demonstrated increased I/O capacity, speed, and bandwidth (reduced latency) and a reduction in power consumption.

As important as the introduction of new packaging approaches are, equally important is the continuous improvement of existing package platforms. Good technology is not easily phased out and replaced – nor should it be without a compelling reason to reexamine fundamental manufacturing assumptions. However, this is a dynamic industry and as materials and equipment evolve, fundamental process flows must continuously be re-examined for performance and yield improvements and for cost reduction opportunities.

Driving the Momentum – Innovation Plus Optimization

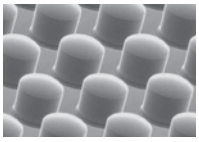
OSATs have the flexibility to continually reexamine their technology portfolio and manufacturing flows in order to stay ahead of market need – and to increase the efficacy of existing product lines. Depth of capability and breadth of application represent two important aspects of a product portfolio. Amkor engineers have a broad base upon which to overlay lessons learned on many platforms to create exceedingly creative packaging solutions. These platforms must not only satisfy performance specs. They must also optimize designs to meet cost objectives and secure a customer's ability to break into a market and, once there, remain competitive.

Hence, both new development and continuous improvement are equally important. The following four technology and product profiles illustrate how Amkor sustains its lead as a *high volume provider* as well as an *innovative partner* of advanced packaging solutions.

Profile 1: Copper Pillar Bumping as a Cost and Technology Enabler

TechSearch has identified Amkor as having the OSAT leadership position on copper pillar bumping for CSPs. From PoP to silicon interposer assisted SiP, commercialization of copper pillar bumping continues to accelerate due to its thermal and electrical benefits, enablement of high density interconnection supporting both high speeds and I/O capacity, and significant reductions in cost of ownership.

High volume adoption of PoP platforms (shown above) containing copper pillar micro-bumps is found in portable electronics devices such as tablets, e-readers, and gaming devices.



Copper pillar micro-bumps (left) also enable the multi-die packaging of high-end processors, graphics, FPGAs, power amplifiers and memory in both 2.5D and 3D TSV formats. The photo below illustrates the interconnection of a four die memory stack with TSVs.

Profile 2: The Pin Gate Molded PBGA A Study in Continuous Improvement (Reduced Cost, Increased Reliability and Yield)

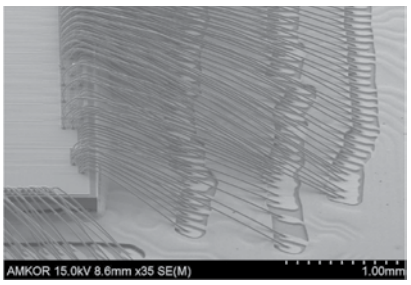
The plastic ball grid array (PBGA) is one such example of a "classic" package platform that underwent a transformation so fundamental as to acknowledge it as an essentially new product, albeit with the same PBGA form, fit and function. The new pin-gate molded PBGA employs an innovative transfer molding process that significantly reduces wire diameters

while retaining wire length. This process moves the placement of the mold gate to the center of the mold cap from its traditional corner position, thereby reducing wire sweep. Higher density substrates are supported and, coupled with the wire sweep control, thinner wires for smaller bond pads are accommodated. This extends wire bonding to 28nm nodes and beyond.

The larger mold cap enables the routing of all active traces and vias underneath, significantly decreasing the risk of solder mask/metal trace cracking on the PCB. Solder mask coverage is increased – and the overall increase in mechanical stiffness protects active traces. Even the flange around the perimeter of the package is more robust and resistant to mechanical damage and bending. And that's not all... the larger bond shell increases wire bond density and accommodates larger die sizes in the same standard package footprint (all 19mm-31mm PBGAs are being converted). And finally, higher yields are expected. The smoother package edge reduces the potential for binding in the test socket or shipping tray, and removal of the corner gate eliminates the historic "Au gate peeling" issue that has plagued the industry since PBGA's inception.

Customers can realize cost savings of:

- Up to 4% with no change to package design, and
- 10-30%+ cost savings when thinner gold wire (0.6mm) – or a changeover to copper wire (below) – is used in conjunction with the new design rules and optimized wire bond layouts.



High density copper wire bonding.

Customers constrained to gold wire bonding within the automotive, aerospace or medical markets may retain gold wire assembly at prices comparable to copper wire usage. When one considers that 75% of the cost of conventional PBGAs is due to the substrate and gold wire, the new pin-gate molded PBGA becomes the most cost effective PBGA package on the market. Amkor's strategy of applying new innovations to older technologies continuously raises the bar for both performance and cost.

Profile 3: FC^{M}BGA Delivers Cost Reduction and Enables Larger Die Utilization

Amkor's flip chip molded BGA (FC^{M}BGA) package enables thinner packaging and improves thermal performance while reducing system cost. Presenting an exposed die format, the package uses a molding compound that replaces traditional capillary underfill to assemble larger die (≤ 20mm) onto BGA substrates (15mm - 42.5mm). Both the die and passive components are assembled simultaneously. This, in addition to eliminating underfill dispense, results in lower cost while improving solder joint reliability.

The technology significantly improves warpage control, especially for bare die and thin core substrates, thereby enabling larger die to be used in systems demanding ultra-low profiles. Passive components can also be mounted closer to the die. A lid or heat spreader attached to the exposed back of the die is optional, depending upon the thermal requirements of the device. This type of package is initially being adopted for high-performance and low-cost applications with FPGA devices being the first to go into production.

Profile 4: The Diverse Applications of MEMS

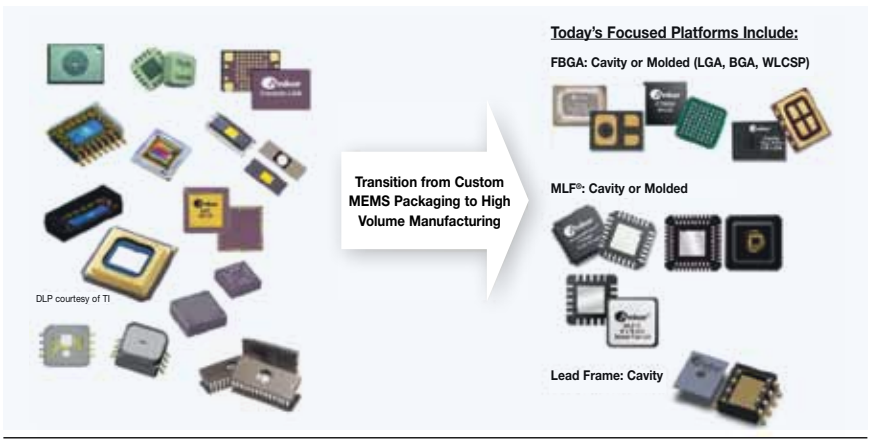
Amkor has packaged MEMS devices and sensors in high volume for over 20 years. The MEMS packaging market now has a CAGR of roughly 20%, more than twice the overall IC package market. Commonalities between MEMS and IC packaging include the drive for miniaturization, integration, and cost reduction. However, early adoption into high grade custom applications has produced considerable variety in MEMS package designs.

Today, the packaging of accelerometers, gyroscopes, pressure sensors, microphones, and magnetometers, either separately or in combination (plus controller die, etc), requires a diverse range of materials and assembly techniques. In fact, it is the lack of standardization that has created so many opportunities in today's MEMS packaging space. There is a clear trend toward the convergence of customizable internal structures (e.g., cavities, micro-channels, ports, optical windows, multi-die, etc.) within the framework of known high volume technologies and standardized package platforms. In such a dynamic market, the greatest advantage that Amkor provides comes from our ability to enable *fast turn-around-time* and a *swift ramp to volume production* leveraging our broad technology and manufacturing capability within this highly specialized area of electronics packaging.

Strategic Partnerships and a Diversified Industry Base

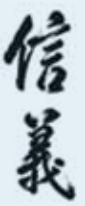
What do customers look for in a "strategic partnership"?

Joint development of long-term technology roadmaps; an adequate level and timeliness of investments to ensure NPI execution; a substantive effort from Amkor to secure manufacturing readiness



and the maturity of new technologies; and the sharing of corporate strategy to help customers understand Amkor's long-term plans.

Amkor has developed longstanding relationships with many of the world's largest semiconductor companies, OEM electronics companies and best-in-class supply base. Amkor believes that solid R&D, pre-production handoff, and production capability have been key factors in attracting and retaining customers. By working with customers and suppliers to develop proprietary process technologies, existing capabilities are extended, time-to-market is reduced, quality increases, and costs are lowered.



Reliability & Trust

These Chinese characters symbolize "Reliability and Trust", the lifelong values of Amkor's founder, the late Honorary Chairman, Hyang-Soo Kim. They illustrate Amkor's strong passion for, and dedication to, the highest standards of integrity, respect, and fair dealing.

Amkor is afforded access to a broad range of technology roadmaps that provide a unique opportunity to assess technology trends. Collaboration with both customers and leading OEMs to develop comprehensive package solutions make it easier for next-generation semiconductors to be designed into next-generation end products. Amkor's focus on research and product development enables them to enter new markets early, capture market share and promote the adoption of their new package designs as industry standards. These deep ties have been fundamental to Amkor's long term success.

Substantial R&D Investment and World Class Manufacturing Infrastructure

The process of defining viable semiconductor packaging requires diversification – and a contribution of competing ideas – with a convergence on the best designs for a given set of device types and price/performance targets. In parallel, commoditization is representative of the process when methods are scaled to high volumes and manufacturing efficiencies drive availability and cost. Therefore, sustaining a leadership position as an OSAT requires close collaboration with customers and suppliers on new development activities, as well as implementing continuous operational improvements within existing product lines. Amkor has made considerable investments in R&D up through the handoff to, and support of, their production lines with substantial capital investment aligned to their customer's technology roadmaps.

Global R&D Center Announced

Amkor recently announced plans to build a state-of-the-art factory and global research and development center in Seoul, Korea. The company expects to acquire a new 46 acre (186,000m^2) site which will house a factory and R&D center focusing on the design, development and full scale production of next-generation semiconductor packaging and test services. As Ken Joyce, Amkor's president and CEO commented, "We are making a strategic, long term investment in our core manufacturing and research infrastructure. It is a commitment to the future." A projected investment of $350M over the next 3-4 years will be used to acquire and develop land and buildings with construction expected to commence in 2014. The facility should become operational in 2015-16. Investment in the project may reach $1 billion over the next 10 years as determined by the evolution of economic and market conditions.

Geographically Diversified Operational Base

Amkor maintains a broad and geographically diversified operational footprint in five countries. Operations comprise more than 5.6 million square feet of manufacturing space strategically located throughout many of the world's most important electronics manufacturing regions. Amkor believes that their scale and scope allows them to provide cost effective solutions to their customers by:

- Offering capacity to absorb large orders and accommodate quick turnaround times;
- Obtaining favorable pricing on materials and equipment by using Amkor's purchasing power and leading industry position;
- Leveraging production utilization across factories and affording crossover capabilities in flip chip, wirebond, bump & probe, MEMS/Sensors, and final test;
- Qualifying production of customer devices at multiple manufacturing sites to mitigate the risks of supply disruptions; and
- Providing capabilities and solutions for customer-specific requirements.

Financial Strength

Financial strength is one of the cornerstones of Amkor's business and the company continues to focus on balancing profitable growth with strong cash flow generation. Amkor's liquidity and balance sheet remains strong and the company is well positioned for future growth. Amkor continues to respond to this demanding industry through improvements in product manufacture, innovative test methods, vigorous supply chain management and greater factory productivity.

Summary

Amkor maintains a long term strategic vision for semiconductor packaging and test. A strong competitive position is maintained through quality, leading edge technology, assurance of supply, price, and test, all offered within a turnkey infrastructure. Many semiconductor companies view packaging and test as enabling technologies requiring sophisticated expertise and technological innovation. Because Amkor is a leading source of new package designs and advanced interconnect technologies, customers are able to reduce their internal research and development costs and get product to market more rapidly.

By supporting a wide range of customers and product types, Amkor is able to leverage factory resources in an efficient and cost effective manner to ensure the best allocation of high volume production. Over 1000 different package formats and sizes are offered, from traditional leadframe IC packages for through-hole and surface mounting, to the latest wafer level, chip scale, ball grid array, and complex TSV SiP solutions. Amkor's broad capability and corporate vision continues to strengthen their position as a leading technology partner. ◆

Amkor Technology®

For more information about Amkor Technology, visit www.amkor.com.

Advanced Microelectronic Packaging

Progresses Leading-Edge Medical Device Technologies

Susan Bagen, Frank Egitto & Rabindra Das
Endicott Interconnect Technologies, Inc.

THE WIDE RANGE OF APPLICATIONS for medical electronics drives unique requirements that can differ significantly from commercial & military electronics. This is particularly the case for handheld, portable and implantable medical devices that demand increased functionality with decreasing size, weight and power (SWaP). Form, fit, function, integrated sensors, batteries, leads, biocompatibility, operational life and reliability specifications define requirements for atypical form factors, unique assemblies and non-standard material sets. Manufacturability and producibility are paramount to the practical implementation of these diverse packaging forms.

A key enabling technology to achieving SWaP for medical electronics is the substrate. In addition to microelectronic assembly services, Endicott Interconnect Technologies, Inc. offers a range of substrate material sets and solutions to meet different form factor and performance requirements. Leveraging off advanced high density printed circuit board fabrication capabilities, Endicott provides laminate chip carrier technologies to meet the needs for rigid, wirebondable organic substrates. Figure 1 depicts this substrate technology implemented to enable increased functionality in decreased form factor for implantable cardiac devices such as implantable cardioverter defibrillators (ICDs) and pacemakers. The 8-layer substrate cross-section shown incorporates high density buildup layers to accommodate reduced die pad pitch and improve electrical performance.

High Density Substrate Technology

When a greater degree of miniaturization is required in a rigid substrate, Endicott offers several proprietary options including CoreEZ® and HyperBGA® semiconductor packaging laminates. Unlike typical printed circuit board laminate materials, these technologies do not contain

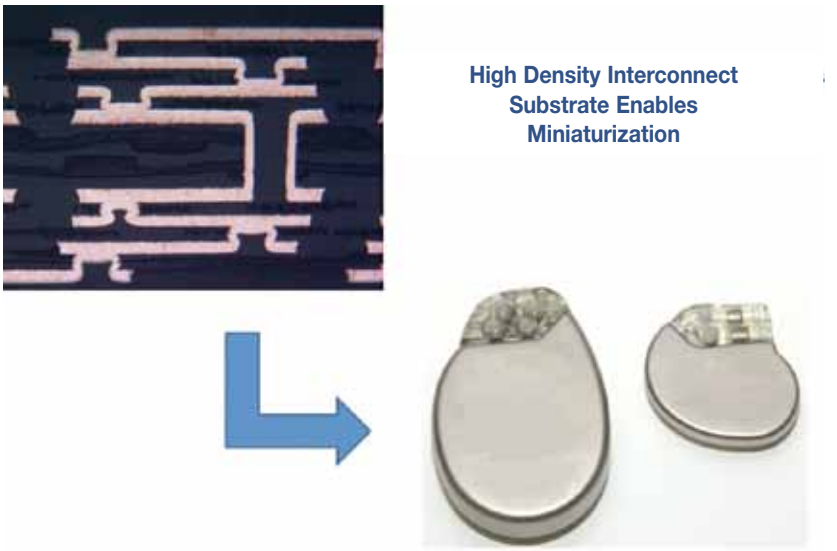


Figure 1. Increased functionality in a decreased form factor with Endicott's Laminate Chip Carrier Technology.

glass cloth. This attribute is significant in that it allows for the formation of higher resolution vias by UV laser drilling as opposed to more conventional mechanical and CO^2 laser drilling. The smaller 50 μm via size minimizes capture pad area requirements and enables a much greater via density, resulting in >4x substrate size reduction as compared to conventional technology. The absence of the glass cloth also results in a smoother dielectric surface finish, enabling higher resolution photolithography for finer line widths and spaces, which results in improved electrical performance. Because of the omission of glass cloth, the dielectric layer thicknesses are substantially less, therefore, the overall laminate stack-up is much thinner. The material sets used in CoreEZ® and HyperBGA® semiconductor packaging laminates are engineered to provide ideal mechanical properties for compatibility with high reliability flip chip die attach. Figure 2 shows a size reduction comparison of the CoreEZ® technology to standard PWB buildup, and an example application for attaining a substantial improvement in image processing capability within a handheld ultrasonic transducer probe.

System-in-Package (SiP)

System-in-Package (SiP) designs that implement embedded passive and active components take SWaP reductions down

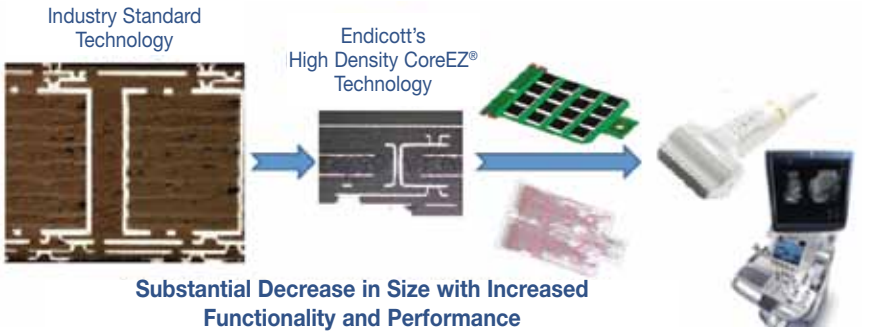


Figure 2. System miniaturization with Endicott's high density enabling technologies.

even further. Eliminating discrete surface components can greatly reduce the overall area requirements for specific designs. Thin film resistors are readily incorporated into the laminate substrate fabrication processing, substantially minimizing the discrete resistor count. Laser trim aids in meeting design requirements for tight resistor tolerances. Thinner, high-density substrate technologies like Endicott's CoreEZ® and HyperBGA® lower inductance, driving down the need for decoupling capacitors in the design. Embedding capacitance layers within the substrate itself furthers the reduction of discrete passive numbers.

New technologies for embedding active die are being developed and implemented into the manufacturing environment. A variety of active silicon die with metal pads, have been embedded and electrically connected to develop highly integrated packages. Current work utilizes embedded active and passive approaches to explore new designs and technologies for SWaP reduction. For example, high density interconnect technology combined with embedded passives and small die and component body sizes have been shown to achieve as much as 27 times reduction in physical size for existing printed wiring board assemblies, with significant reductions in weight and power consumption (see Figure 3). Primary reductions in power are due to reduced interconnect lengths and corresponding load. Shorter interconnects can also reduce or eliminate the need for termination resistors for some net topologies. The concept of SiP can be implemented on various levels depending on the application requirements including full system, partial bill-of-material (BOM) functional modules (e.g., digital processor – memory modules), MEMS sensor packaging, and component obsolescence issues.

Medical devices, especially handheld, portable and implantable, are an expanding market driving the need for unique solutions for increased functionality with decreasing size, weight and power (SWaP).

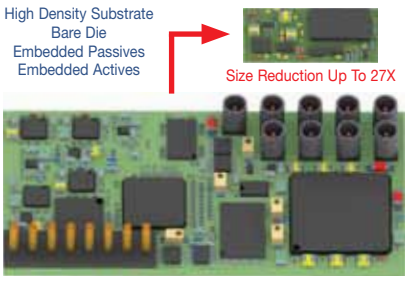


Figure 3. Miniaturization via System-in-Package.

By integrating the building blocks of SiP - advanced substrate technology, embedded passives and actives – coupled with concurrent engineering design-for-manufacture (DFM), advanced packaging solutions have been successfully implemented to reduce electronics volume and advance the capabilities of medical device technology.

Microflex and Ultra Fine Flip Chip Assembly

For extreme miniaturization and unique form factors requirements, Endicott meets these challenges through advanced microflex coupled with ultra fine flip chip assembly. Figure 4 illustrates an example of a highly miniaturized assembly on microflex for use in IVUS catheters, which has been in production for over 5 years with greater than a million assemblies produced. IVUS is a catheter-based system that provides physicians with a 360 degree digital view of the inside of a patient's arteries. IVUS provides for analysis of the amount, location, and type of plaque in the arteries. An ultrasound transducer, or piezoelectric device, is mounted in the tip of the catheter. This transducer is mounted to a thin flexible substrate, along with a number of ASIC die used to control the functions of the catheter lab, i.e., the digital imaging control unit to which the catheter is attached during use. Advantages of IVUS over angiography include, better vessel definition, measurement of plaque thickness and plaque buildup, plaque make-up, stent size and placement determination, and blood pressure changes around a lesion [1]. The capabilities of IVUS are realized through the implementation of ultra-miniaturized electronics within the catheter that allow for image and signal processing to occur at the source of data acquisition. A paradigm shift in the approach to microelectronics packaging was needed to meet these requirements and enable this technology.

For the IVUS catheter assembly, the exceptional thinness of the polyimide flex substrate (12.5 μm) is necessary for the assembly with the PZT transducer and ASIC die to be rolled into a very tight cylinder, having a diameter on the order of 1 mm (about 3.5F). This rolled assembly is then placed at the end of the catheter after attachment of the electronic leads. The use of semi-additive circuitization facilitates manufacture of fine-line circuit features on the flex, and traces narrower than 12 μm have been produced routinely. A smooth copper-polymer interface is ideal for fine line circuitization, and selection of appropriate material processing provides good copper adhesion to the base film. The die are bumped with 22 μm solder-tipped Cu studs on a 70 μm pitch. Ultra fine flip chip assembly utilizing die placement tools with extremely high registration capabilities are required to produce this microflex assembly in high production volumes.

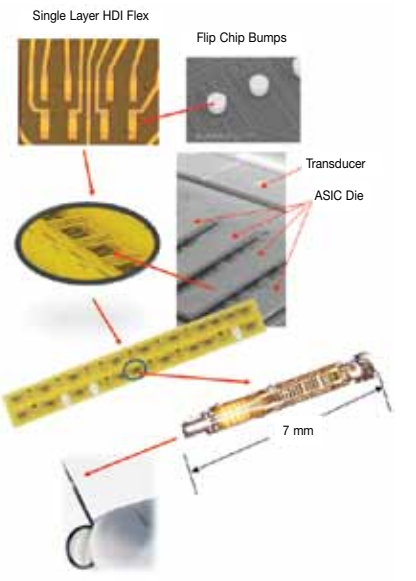


Figure 4. Extreme miniaturization and form factor adaptability with Endicott's MicroFlex and ultra fine assembly capabilities.

Multilayer Microflex

As demonstrated with the IVUS example discussed above, microflex circuits can be used in various applications where requirements for flexibility and space savings limit the serviceability of rigid substrates. However, high-density multilayer cross-sections are required to support the wiring density and electrical performance requirements for SWaP reduction. Here, the desired multi-layer attributes are realized through new structural configurations, by selection of materials and material thickness, both dielectric and metal. For example, flexibility will decrease with increasing total thickness. Thin material structures offer flexibility without inducing significant strains in the materials themselves. Flexible materials with 1-2 metal layers provide the smallest possible roll diameter for systems such as catheters.

Figure 5 (see page 32) illustrates flexible substrates in two types of configurations. The first (Figure 5A) involves pure flexible materials with adhesive layers, having 12 metal layers, and a total cross sectional thickness of about 0.3 mm. This

continued on page 32

3D Printing Meets Electronic Interconnection – And Could Change it Forever

Harvey Miller

WE LEARN EARLY THAT Mother knows best. That goes double for Mother Nature. Take manufacturing, for example. Humans are still learning by emulation. We have usually fabricated by subtractive techniques. We etch, we mill, we stamp, we drill. We waste and pollute. We also waste time and energy. Mother, on the other hand, builds living organisms from a variety of raw materials, programmed by DNA code, even including planned obsolescence – species and individuals – to make way for improved models. She does it ADDITIVELY! (before tummy tucks and Botox – human subtractive dis-improvements). Think of the diversity of life forms that result and the diversity within each, for natural selection to work. Additive manufacturing unleashes new potentials for creativity and evolutionary change that subtractive manufacturing cannot match. And what will be the agent for the transitions in our economy and our culture? Why 3D Printing, of course. Beyond Rapid Prototyping, lies the promise, its main transforming potential for society: *3D Printing + CAD/CAM = **Additive** Digital Manufacturing*.

Introduction: 3D Printing, Young and Old

Here's a statistic to indicate how hot 3D print is: number of Google citations – 4,630,000! The industry has been emerging for a while. It is still emerging, as are printing technologies and their implementations. That applies particularly to electronic interconnection impacts. This article will look at examples which indicate future electronic interconnection impact possibilities that may engage creative imaginations to extend their innovations.

Rapid Prototyping is a major 3D Printing thrust, attractive for cost effective pre-production models for professionals ranging to DIY replicas. Many techniques have been developed by many new companies. Extension to Digital Manufacturing is even more infantile. Which techniques and companies will succeed and which will drop by the wayside, only Darwinian market forces can decide. That's the general pattern in young, high growth markets, which offer great rewards – to the survivors. For 3D printing market models, this author thinks that using the technology in vertical markets to capture end-product revenue will be the winning formula. That implies domination of *production* volumes, the very model targeted by the examples in this article.

EoPlex, Division of Asti Holdings

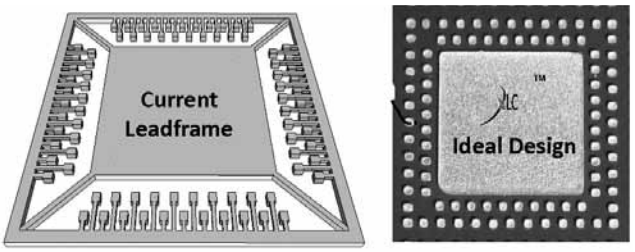
The first company we look at exemplifies the formula's application. EoPlex has found a volume market – Integrated Circuit packages.

IC die need a package; at least that is the general perception and practice – for protection, support, and to provide a connection path from the IC input-output pad to the outside world, usually by soldering leads to a printed circuit board (Embedded Known Good Die may modify the future reality).

The support and connection functions in the industry's early days of the 1970s were provided by a "lead frame", used in package configurations such as "dual-in-line" and "flat pack", still used in 2012 in those packages. A descendant of the flat pack, the QFN, has become popular for analog circuits in cell phones, etc. The "N" stands for "no lead", really a stub, more appropriate tor surface mount soldering than the leaded package.

Jim Walker of Gartner states: "The forecast for leadless/leadframe (includes QFN, SON, DFN, and BCC) for 2010 was 28.7 billion units and 40.9 for 2012. Our total IC package unit forecast for 2010 was 173.8 billion

Ideal QFN "Lead Frame" Has No Tie Bars, Minimum Metal, and Small Size



Leadframe, The Problem — Lead Carrier, The Solution

Figure 1. *Source: EoPlex Technologies*

xLC™ Based Package
23% Smaller Footprint, 50% Less Volume*

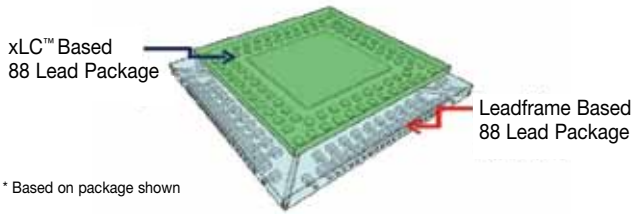


Figure 2. *Source: EoPlex Technologies*

and 190.5 billion for 2012. The QFN has grown faster than any other package in the past few years. It is cheaper than an SOIC and still uses leadframe/wirebond technology. For analog products, it is the package of choice. Amkor, Carsem, Unisem, UTAC, ASE all produce huge quantities of this package for use in cellphone and wireless products."

Sandra Winkler, Senior Industry Analyst of New Venture Research, projects QFN package growth at 15% per year to 2015 from 15 billion in 2010.

3D Printing Advantages

The EoPlex xLC™ QFN provides an excellent example of 3D printing advantages. Additive manufacturing *can eliminate* the ancient stamped or etched, subtractively fabricated lead frame.

Advantages include:

- No expensive kapton tape needed to maintain fragile leads in alignment during wire bond and molding, also saving the labor cost of tape installation and removal.
- Testability after die placement – no shorting lead frame (Figure 1).
- Many parts are created simultaneously in large panels at high-speed and low-cost (Figure 3).
- Pad and lead pitch down to *150 microns* (6mils), not limited by etching or stamping resolution.
- Die pads and bonding pad in proximity, no need to fan out resulting in better high speed performance and lower thermal resistance (Figure 2).
- 500 I-O's possible compared to 150 for lead frame – strip density increase up to 50% (Figures 1, 2, and 3).
- Singulation by cutting plastic, not metal.
- Easy to select and shape a wide variety of materials.
- Low contact resistance sintered surfaces.
- Thin: <300 μM (a bonus from eliminating that lead frame) – great for mobility.

Downsides include:

- Cost of the screened silver inks. Other conducting metals are under study (offset by minimal material usage plus other savings).
- Need for a second source – EoPlex is willing to license alternate source(s).

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More Efficient Use of Strip Space Means Lower Cost Per Package Site

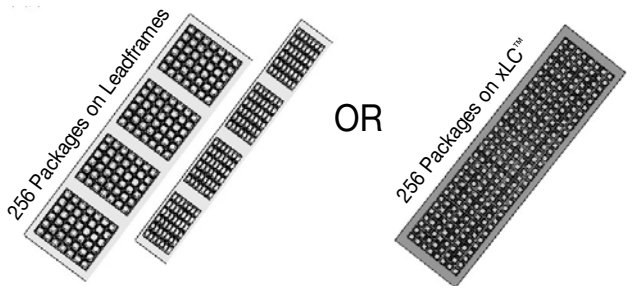


Figure 3. *Source: EoPlex Technologies*

3D PRINTING DELIVERS AN ANSWER

Are Printed Electronics a Replacement for, or an Extension of, Printed Circuit Boards?

Optomec (www.optomec.com), in alliance with Stratasys (www.stratasys.com), is an example of potential 3D Printing impact on electronic interconnections and the semiconductor company model that exemplifies it.

PCB's replaced wires when transistors integrated into circuits (IC's) replaced vacuum tubes as electronic switches and amplifiers, beginning in the 1960's. They are fabricated subtractively.

Large areas of copper are etched away to form pads for IC and other component parking spots and lines to interconnect them. As IC's have become more complex, with higher circuit speeds and temperature generation; as their interconnections have become more dense, PCB's have responded in greater complexity to meet their needs. A $1.5T (annual sales) electronic hardware industry has been constructed on the partnerships, resting on a PCB shipment platform valued at $63B in 2012.

Radical change in such a vast industrial complex only happens at the edges. That provides a partial answer to the question. But where are those "edges"? Where do those Printed Electronics extensions of conventional PCB's fit?

First, "Printed Electronics" are additively placed, so there is no need for special substrates on which sheets of copper have been laminated.

From a Stratasys/Optomec press release on March 23, 2012: "A Stratasys 3D Printer is used to create the wing structure for an Unmanned Air Vehicle (UAV). Then an Optomec Aerosol Jet System is used to print electronics onto the wing structure including an RF antennae, sensor, and circuitry to power a propeller and LED. All electronics are functional. The RF antennae broadcasts live video from a camera to a remote display screen." The circuit is printed in proximity to its application, replacing need for a box containing conventional electronics on a PCB.

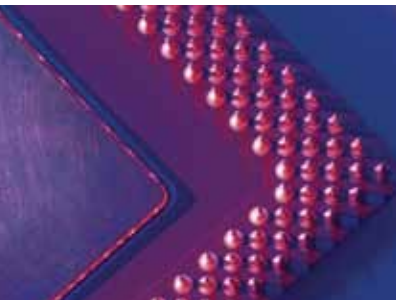
It seems that we are looking at a whole new industry with a set of new applications that will drive new technologies, including new semiconductor devices, sensors, and MEMS. ◆

SEMICONDUCTORS • SOLAR/PV
LEDS • MEMS • FPD
PLASTIC ELECTRONICS
EMERGING MARKETS

The Power of [x]

The Power of [Packaging]

Wire Bond
WFCSP
Flip Chip
3D IC
BGA
FO-WLP



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Contemporary Packaging: Achieving Cost Advantage through Innovation
10:30am–12:30pm, TechXPOT North

IEEE/CPMT Workshop: "THIN IS IN": Thin Chip and Packaging Technologies as Enabler for Innovative Mobile Devices
1:00pm–4:30pm, SF Marriott Marquis

Wednesday, July 11—

The 2.5 and 3D Packaging Landscape for 2015 and Beyond
1:00pm–3:30pm, TechXPOT North

Thursday, July 12—

MEMS and Sensor Packaging
10:30am–12:30pm, TechXPOT North

ITRS Back End of Line Technologies
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continued from page 25

EoPlex 3D Printing Production Conclusions

- All IC lead frame packages are candidates for 3D additive fabrication, *eliminating* that l-f.
- **Most other IC packages are also candidates, including array packages.**
- The higher density advantages might also be conferred on connectors and sockets and for Systems-in-Package.
- Additive fabrication eliminates waste.

Conclusion for IC Interconnections, with Special Relevance to IC Packages

One purpose of this article is to encourage other 3D Printing participants to enter the competitive game. IC Packaging needs you!! Here's why: **Density, density, and more density – the pressure won't stop.**

A $1.4 Trillion Question
(2012 Electronic Hardware Annual Sales)

"Over the 40 years from 1967 when CMOS began to be used, until today, well, actually until 2007, we will have seen one million times improvement in the density of integrated circuits. We saw a million times improvement in the cost to build an integrated circuit, and we saw a million times improvement in the feature size. But you might think about it for a moment, what happens if we have another one million times improvement over the next 40 years?"
Dr. Bill Bottoms to IEEE/CPMT/SCV, IC Industry Veteran, March 23, 2006)

Looking at Just the Next 10 Years: Selected for Impact on IC Packaging Density

From Dr. Bottoms' presentation to IEEE/CPMT/SCV re: ITRS (Roadmap), May 9, 2012:

- Transistor count will exceed 100 billion for complex SiP packages.
- From 2012 to 2022 Max Package I/O Data Rate will increase from 2,500 to 79,879 Gb/s. Number of I-O lanes required per package will increase from 250 to 1,997.
- Photonics is the solution to physical density of bandwidth for SIP.
- Area required for differential electrical IO will drive IO to Optical about 2015.

Brief Discussion of Dr. Bottoms' Prediction of Photonic I-Os

The need for close coupling between photonics and electronics will be the strongest density driver of all, on top of all the mentioned drivers.

A word should be said about SIP (Systems-in-Package) and SOC (Systems-on-Chip). They are manifestations of "MORE THAN MOORE", a new center of ITRS attention. They are part of the solution for the desired objectives – lower power, higher speed. They will drive the need for higher density. SIPs will be looking to 3D Printing as an enabler. ◆

Dr. Bill Bottoms, whose observations are quoted above, is a member of the ITRS Working Group on Packaging and Interconnection. He is also a member of the OEM iNEMI roadmap working groups, so he has views from both the supply and demand sides.

Resources for more information on 3D Printing companies and technologies:

"Will 3D Printing Change the World?" www.forbes.com/sites/gcaptain/2012/03/06

TEKPRO Group –"Digital Manufacturing & 3D Printing/ More than Rapid Prototyping" www.tekprogroup.com provides 3D Printing history)

HARVEY MILLER has watched the semiconductor industry for more than 30 years as an economist, analyst, and database creator. He began his electronics career as a components engineer for computer and telecom OEMs, Burroughs, and GTE among them. At present he's putting it all together, interpreting semiconductor roadmap impacts on the future of interconnection. To contact Harvey email h.miller@ieee.org.

International Technology Roadmap for Semiconductors What is its Significance?

The working groups that put it together are comprised of leading semiconductor technologists from the companies in the industry plus academia plus government laboratories. The Roadmap is a living, changing document that reflects past experience and knowledge, modified by developing new experience and knowledge as semiconductor technology frontiers are pushed forward on many levels.

Coherence among those levels establishes them as goals toward which the entire global industry strives. It covers processing, packaging, and interconnection parameters for the major semiconductor device categories, updated annually.

Driving the ITRS, particularly digital ICs, is Moore's Law, which rose from Gordon Moore's observation early in its history, later updated, that transistor count doubled every two years. (The Intel web site has an authoritative discussion). Electronic industry market development has become dependent on the continuation of Moore's Law – all $1.4 trillion dollars of it. So the stakes are very high.

Visit www.itrs.net for more information about ITRS events and reports.

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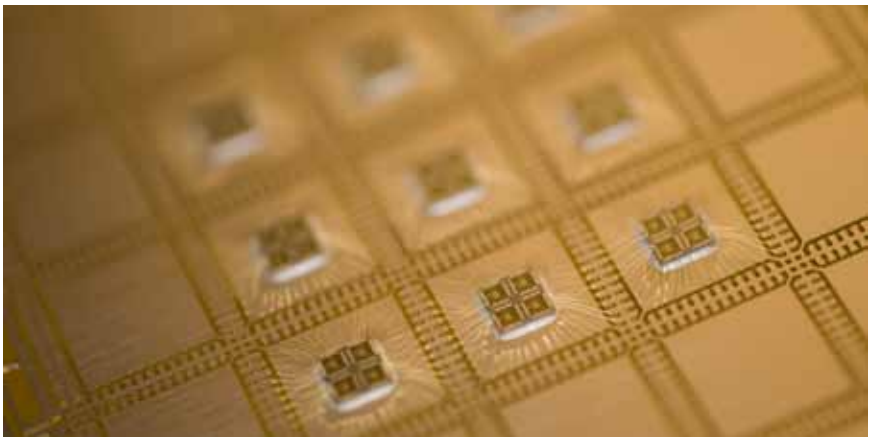
Keeping Packages Cool and Reliability High

New Non-Electrically Conductive Die Attach Paste has Best Thermal Performance on the Market

Scott O'Brien and Paul Gleeson
Henkel Electronic Materials, LLC



EVER-INCREASING FUNCTIONALITY and ever-decreasing device footprints have presented semiconductor packaging manufacturers with quite a dilemma: how to manage the dimensional demands without exceeding thermal limits. As advanced devices get packed with greater function in a smaller space, operating temperature levels increase. If the temperatures are too high, package – and therefore product – reliability can be adversely affected and, in severe cases, result in complete failure.

There are many approaches to thermal management, but addressing heat dissipation and operating temperature at the die level is key to improving the overall product performance. Die attach pastes with good thermal performance and thermal management materials are approaches that are most often used. But, as overall operating temperatures of many packages continue to rise, previous-generation non-electrically conductive material systems may not be robust enough to effectively manage the thermal load.

Recognizing this challenge early-on, Henkel began development of a high thermal, non-conductive die attach paste to address the increasingly demanding heat dissipation requirements of modern semiconductor devices. Quite challenging from a formulation point of view, the materials experts at Henkel devoted significant resources into engineering a die attach paste that would resolve the heat management problems experienced by manufacturers of several types of leadframe packages. The result is ABLESTIK ABP-8910T, a new thermally conductive, electrically isolating die attach paste that can be used for die to substrate attach or for heat sink/lid attach to dissipate heat from semiconductor leadframe devices or other high thermal applications such as automotive.

But, ABLESTIK ABP-8910T doesn't just remove heat; it does it better than any other commercially available non-electrically conductive die attach material in the market. With an outstanding thermal conductivity of 2 w/Mk – nearly five times that of traditional non-conductive pastes – ABLESTIK ABP-8910T sets the new benchmark for thermally efficient die attach materials. In fact, a manufacturer of QFNs that recently replaced a non-conductive material with ABLESTIK ABP-8910T realized an operating temperature reduction of 7°C, which is significant.

Of course, the thermal conductivity isn't the only superior characteristic of Henkel's latest innovation. ABLESTIK ABP-8910T offers a host of other advantages that make it the ideal non-conductive choice for manufacturers of power devices such as SOTs, SOICs, QFNs and QFPs. The novel die attach paste provides excellent electrical insulation that is nearly 1,000 times higher than standard, non-conductive pastes; it delivers high reliability performance at MSL1/260; exhibits good room temperature and high temperature adhesion to a wide variety of metal leadframes, including especially copper, silver-plated copper and PPF; and is effective for a range of die sizes up to 5 mm x 5 mm.

ABLESTIK ABP-8910T's exceptional performance also comes with manufacturing flexibility and ease-of-use at its foundation. With good and stable workability including excellent dispensability, good fillet control, a long open time of up to one hour minimum, stage time of up to eight hours, superb voiding control and 90-second snap cure capability, this material allows semiconductor packaging specialists to easily integrate it into existing processes.

The ability to reliably manage heat with such an adaptable and effective non-conductive material is a tremendous advantage. Put simply, any semiconductor leadframe manufacturer that has a requirement for reducing package operating temperature, raising reliability and incorporating a user-friendly non-conductive material should look to ABLESTIK ABP-8910T. If you want the highest thermal performance available in a non-conductive formulation, this is the go-to material.

For more information on ABLESTIK ABP-8910T or any of Henkel's advanced die attach solutions, log onto www.henkel.com/electronics or call the company headquarters at 714-368-8000. ◆

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Underfilling the Gaps

Rob McKenzie
Dow Electronic Materials

FIFTEEN YEARS AGO, FLIP PHONES dominated the mobile device industry. Now, flip chips are dominating the packaging arena. While it seems that beyond the catchy turn of phrase, one has absolutely nothing to do with the other, it is the consumer demand for the former that has led to the success of the latter. And as the flip phone craze gave way to explosive demands for the smartphone, flip chips matured from an enabling technology for niche applications to the manufacturing mainstream. Looking forward, advanced flip chip technologies such as copper pillars (Cu Pillar) and TSV microbumps are leading to the higher functionality and improved performance that enables smartphones to become even smarter.

Originally developed in the 1960s, it was not until the late 1990s that reductions in manufacturing costs and improvements in underfill materials and substrates allowed the benefits of flip chip technology to flourish. Underfills are a critical and fundamental element within today's prolific flip chips. Without these insulating materials, the stresses induced during thermal cycling would destroy the fragile flip chip solder connections in short order. The role of underfills is simple and yet complex; they evenly disperse and manage the thermal stress induced by the differences in the coefficient of thermal expansion (CTE) between the die and the substrate. As advanced flip chip processes work their way into next-gen 2.5D interposers and 3D TSV microbump applications, advances in underfill materials will be critical to the next generation of flip chip. This article looks at two such materials and processes under development, focusing on how each can solve the issues semiconductor manufacturers face as they struggle to meet the growing demand for higher performing electronic devices.

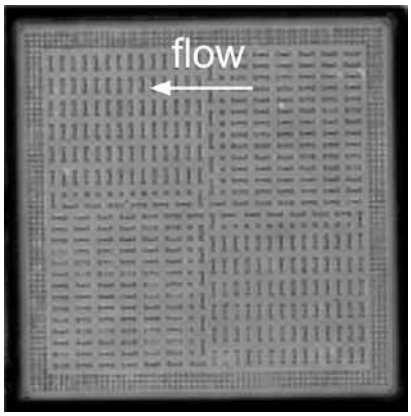

Figure 1. Dow CUF deposited on Si flip chip test vehicle with Si3N4 passivation and Sn/Ag cap/Cu pillars.

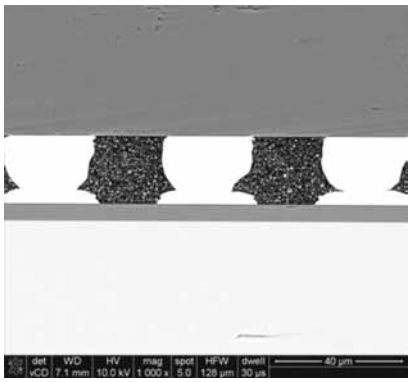

Figure 2. Cross-section of Dow capillary underfill dispensed in 20 µm gap.

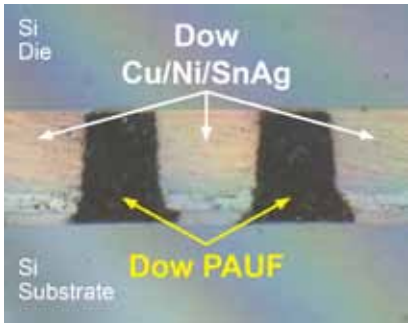

Figure 3. Dow's PAUF demonstrates uniform, void-free coating.

Underfill 101

Currently, the industry offers a number of underfill processes and materials including capillary underfills (CUF), no-flow underfills (NUF), molded underfills (MUF) and wafer level underfills (WLUF). Each of these are designed to address specific applications, and each has its limitations which are rapidly being tested as new design rules and performance requirements continually push the limits of today's formulas and processes. As a result, material suppliers continuously invest in research to improve their offerings in this space.

Specifically, 2.5D interposer and 3D TSV designs are moving toward finer features and pitches resulting in <10μm gaps, <150μm pitches, micro Cu pillar bumps, <20 CTEs and thermal conductivity between 1 – 3 W/mK. To meet these requirements, material suppliers are using sub micron silica particles to meet lower CTE and flow requirements along with thermally conductive fillers to advance their CUF offerings. Additionally, novel approaches to underfill material properties and application processes such as advanced CUF and pre-applied underfills (PAUF) are gaining visibility and consideration for 3D TSV IC applications, particularly as the industry approaches commercialization.

Advanced Capillary Underfills

Capillary underfills have been mainstream for quite some time and have been fitting the bill quite nicely. But with the introduction of package-on-package (PoP) configurations and stacked die, performance criteria of underfill materials have been radically altered to improve stress and thermal management along with flow characteristics. Additionally, a method of dispense that allows for application in bonded die stacks that eliminates any possibility of voiding is required. Further, as new developments

continued on page 32

With Innovation Comes Revolution

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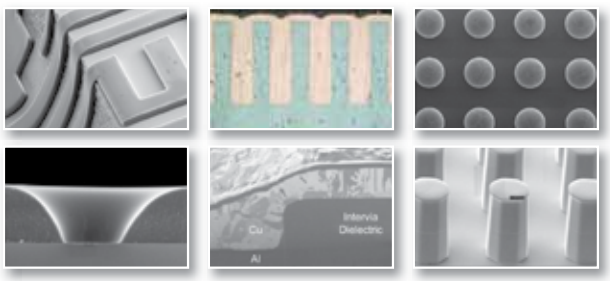

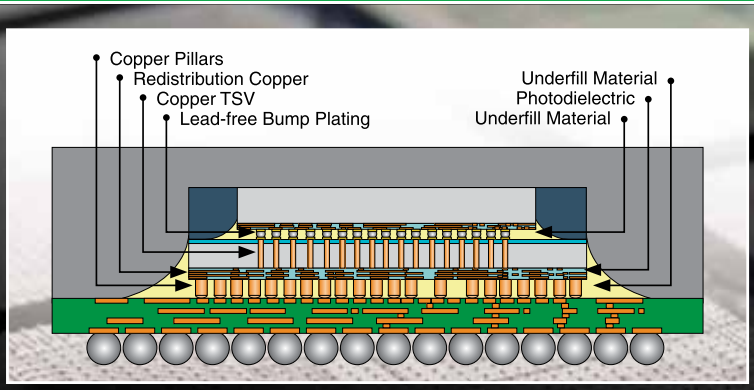

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in PoP that focus on reduced stack height and alternative methods of interconnect such as through mold via (TMV) are adopted, these performance criteria become even more critical.

Under development, Dow's capillary underfill material features low viscosity for void-free filling at fine pitch and narrow gaps, while exhibiting low modulus, low CTE and high toughness characteristics. The flip chip test vehicle shown in Figure 1 demonstrates the material's ability to dispense without voids and striations around the 50μm diameter/150μm pitch features with a 25 μm gap. Void-free dispense of Dow CUF is also shown in Figure 2. Dow's materials are currently undergoing initial reliability testing on Si and organic substrates.

Pre-Applied Underfills

Recent developments in Cu pillar technology have initiated the need for pre-applied underfill. The fine pitch of ultra-thin chips combined with the complex arrangement of vertical stacks further complicates the CUF process. Pre-applied underfill provides the flexibility to be able to stack multiple chips and accomplish bonding as well as underfilling in one process thus eliminating the need for secondary process steps involved with capillary underfill.

Pre-applied underfills come in two flavors: either a laminate non-conductive film or a spin-apply chip level underfill. With each method, Dow Electronic Materials has demonstrated uniform coating and high transparency, in addition to being void-free after curing and reflow with its materials. Good joining is achieved by thermocompression bonding by die-to-die (D2D) and die-to-wafer (D2W) processes, with no delaminaton after thermal cycling (see Figure 3).

PAUF is still a work in progress. While void-free UF has been achieved after curing and reflow, there is still work to be done to make it void-free after thermocompression bonding. Additionally, the process sequence still lacks an established equipment step to perform the processes. While development of the material and processes has been performed and proven on demo equipment, process steps have yet to be optimized. However, progress is being made.

Conclusion

With shorter market windows, more stringent flip chip gap and pitch requirements, thinning wafers and multifunctional ICs, IDMs and OSATs are more often than not partnering with today's top material suppliers in an effort to advance their designs.

As the technology continues to trend toward higher functionality, thinner ICs, smaller footprint and lower costs, underfill material will need to continually evolve to meet the expectations of next generation 2.5D and 3D ICs. Dow Electronic Materials is actively researching and advancing technologies such as advanced CUF and PAUF by addressing the challenging demands and specifications provided by today's industry leaders. ◆

ADVANCED MICROELECTRONIC PACKAGING continued from page 23

structure is readily shaped with a bend radius on the order of 25 mm or higher. The second (Figure 5B), also having 12 metal layers, but a total thickness of just under 0.2 mm, bends with a radius of 3 mm or higher. It can be seen for the same number of metal layers, structures with lower dielectric thickness bend more than structures with thicker dielectric.

Defining the Future

Endicott Interconnect Technology's commitment to leading-edge R&D, including materials and manufacturing technology development, continues to push the envelope on what is possible for achieving greater functionality within atypical form factors for advanced medical devices. As applications evolve, additional requirements for biocompatibility and stretchability are driving material sets new to the electronics packaging world. Coupling innovation with Endicott's solid manufacturing capabilities provides the platform to meet the challenges of advancing medical device technology.

For additional information on Endicott Interconnect's advanced microelectronics packaging solutions, please contact Susan Bagen, Business Development Manager, at susan.bagen@eitny.com or visit their website at www.endicottinterconnect.com. ◆

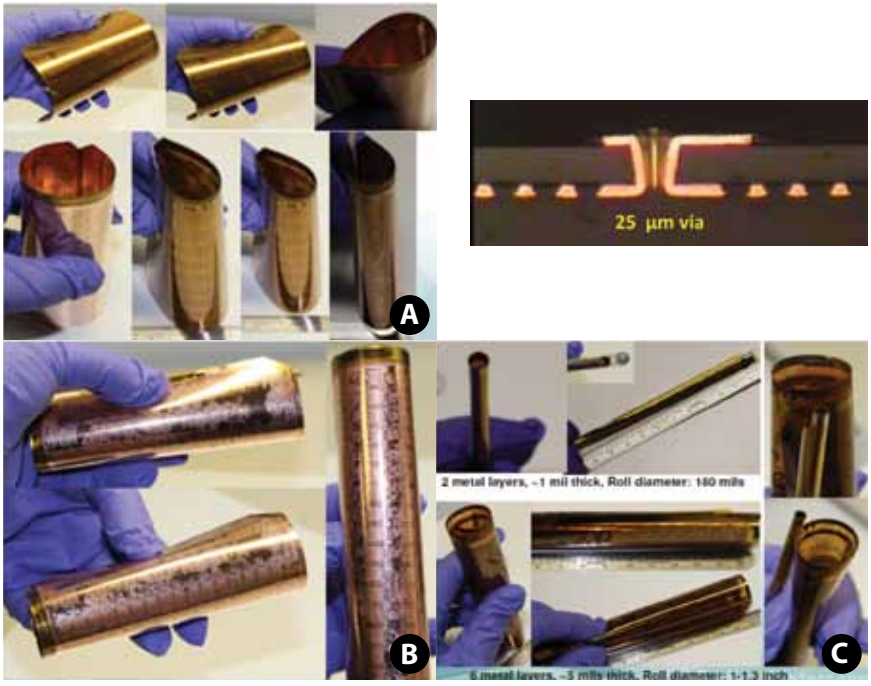

Figure 5. Multilayer MicroFlex featuring (A) 12 metal layers with bend radius ≥1 inch, (B) 12 metal layers with bend radius ≤1 inch, and (C) rollable structures.

Reference
[1] Diagnostic and Invasive Cardiology, January/February 2009 Issue, Reilly Communications Group.

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3D Wave Power

Phil Marcoux
PPM Associates

THE INSPIRATION FOR THIS guest editorial is the recent *Electronic Design Process Symposium* organized for the Santa Clara IEEE Computer Society by John Swan. I started writing this on the first day of the symposium while sitting in a conference room in Monterey overlooking the Monterey Bay. As I gazed out the windows admiring the power of the ocean waves I'm listening to speaker after speaker discuss how the driving force for 2.5D and 3D packaging is now power.

2.5D packaging describes IC die stacked on silicon interposers in BGA packages while 3D packaging is IC die stacked on IC die in a package. The interconnection from die to interposer or die to die may be accomplished using wirebonds, large solder balls, microballs, copper pillars and/or through silicon vias (TSVs).

I've attended and have spoken at several conferences on 2.5D and 3D packaging over the past three years. The rising frequency of such conferences reminds me of similar intensity in the early days of SMT and the euphoric period of MCMs. This conference was different from others I've attended in that the audience was comprised largely of design executives (suppliers and users) who spoke rather candidly about the 2.5D and 3D activities they have commissioned. Most spoke of being in a test chip phase and a number stated that they had emerged from successful tests and were progressing to tape-outs of real 3D products. All agreed that current costs for 3D development are high but the projected benefits appear to provide adequate rewards.

Until this event I had not heard managers state that the power savings alone was an adequate justification to embark on what is currently a fairly expensive undertaking because of the high fabrication costs. In fairness, the user side of the audience was heavily represented by suppliers to the mobile and gaming industries where hardware was mostly battery powered.

According to Jan Vardaman, CEO of TechSearch International, "The tablet and smartphone have replaced the PC as the volume driver for packaging and assembly. Smartphones accounted for 472 million units or almost 27% of the mobile phone market in 2011, and expectations are that it will continue to grow at double-digit rates. Smartphones typically contain more than 20 CSPs (chip scale packages), including some of the most advanced packages, such as package-on-package (PoP) and multiple stacked-die packages. IDC reports that 68.7 million tablets were shipped in 2011, a number expected to increase to approximately 106 million in 2012. Tablets use many of the same packages found in smartphones. Future tablets and smartphones are expected to use 2.5D or 3D TSV technologies; the only question is when volume manufacturing will begin. The consensus is 2013 at the earliest for these applications."

Why the emphasis on power savings? Many of us remember when our cell phones would last for five to seven days on a single battery charge, and now we're lucky if they last five to seven hours.

In other 2.5D/3D conferences heat has been a stated concern. Since silicon has very low mass any pieces of silicon stacked together will rapidly assume the temperature of the hottest piece. Even though the EDPS event favored battery powered applications a couple of speakers addressed the heat concerns with 3D packaging by suggesting the lower power resulted in less heat and therefore less concerns. They also commented that most of the heat dissipating solutions being discussed by several suppliers won't work due to space and other limitations.

Many of the users in attendance stated that the design tool community is not doing enough to meet the new challenges presented by 3D packaging. In response the largest EDA suppliers detailed the new suites of design tools they've developed to assure the successful design, assembly and test of 3D packages. 2.5D EDA tools are readily available since 2.%D interposers can use many of the existing PCB design tools.

According to Herb Reiter, President of EDA2ASIC Consulting, "There is no free lunch, and I'm sure a lot of us are realizing now that there is a lot of work to be done to enjoy 3D benefits. In the short term, EDA providers should agree on data exchange formats, and work with materials and equipment providers to bring accurate models into the design flow. Thermal is a big topic for everybody, and reliability is really what hits you if you don't consider thermal."

My admiration, or was it distraction, by the ocean waves is due in part to my lifelong involvement with the sea. This has given me an ability to judge when the power of the wind and waves is strong, forceful, and unstoppable. Similarly, my long involvement with semiconductor packaging has given me an ability to gauge the power and longevity of new technologies. 2.5D and 3D, as an IC packaging movement, are both receiving unprecedented amounts of funding and attention. Like the waves during that day at EDPS in Monterey, I see 2.5D and 3D as powerful unstoppable forces. ◆

PHIL MARCOUX is one of many SMT and IC Packaging Pioneers. In 2007 he was named "The Father of US SMT" by the IPC. In 1981 he founded AWI, the first US company devoted exclusively to SMT, which was later acquired by SCI Systems. In 1992 he founded ChipScale, one of the first Wafer Level Packaging companies which developed a portfolio of over 36 patents. The patents are now the cornerstone of camera modules commonly found in current cell phones, computers, and games. Today, Phil is an active Business Development consultant in the area of 2.5D and 3D IC packaging infrastructure, design, and assembly. Visit www.oneppm3D.com for more.

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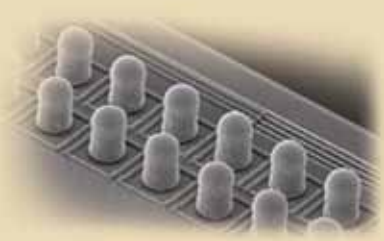

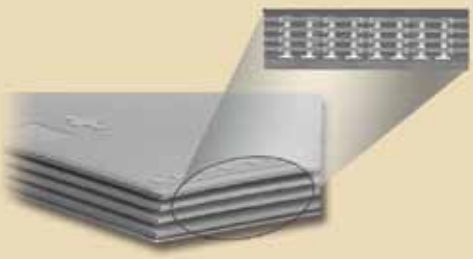

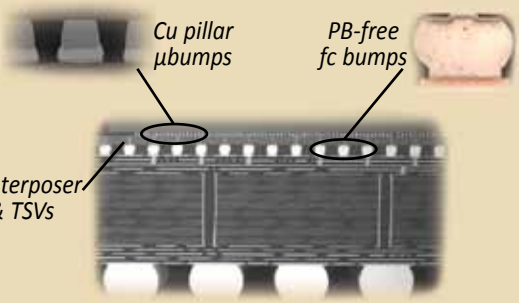

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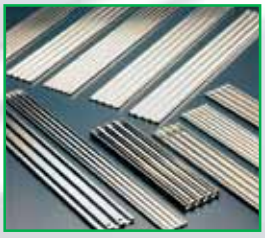
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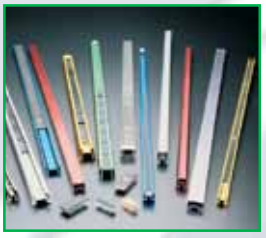
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