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SEMATECH

2.5/3D ~~ICs~~ Systems

Technical AND Business Considerations

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MEPTEC Luncheon, June 13, 2012

AGENDA

- Introduction
- A few market numbers
- Why develop 2.5/3D solutions ?
- What’s different in the 2.5/3D ecosystem ?
- 2.5/3D products TODAY
- Opportunities for MEPTEC members
- Appendix: Additional market data

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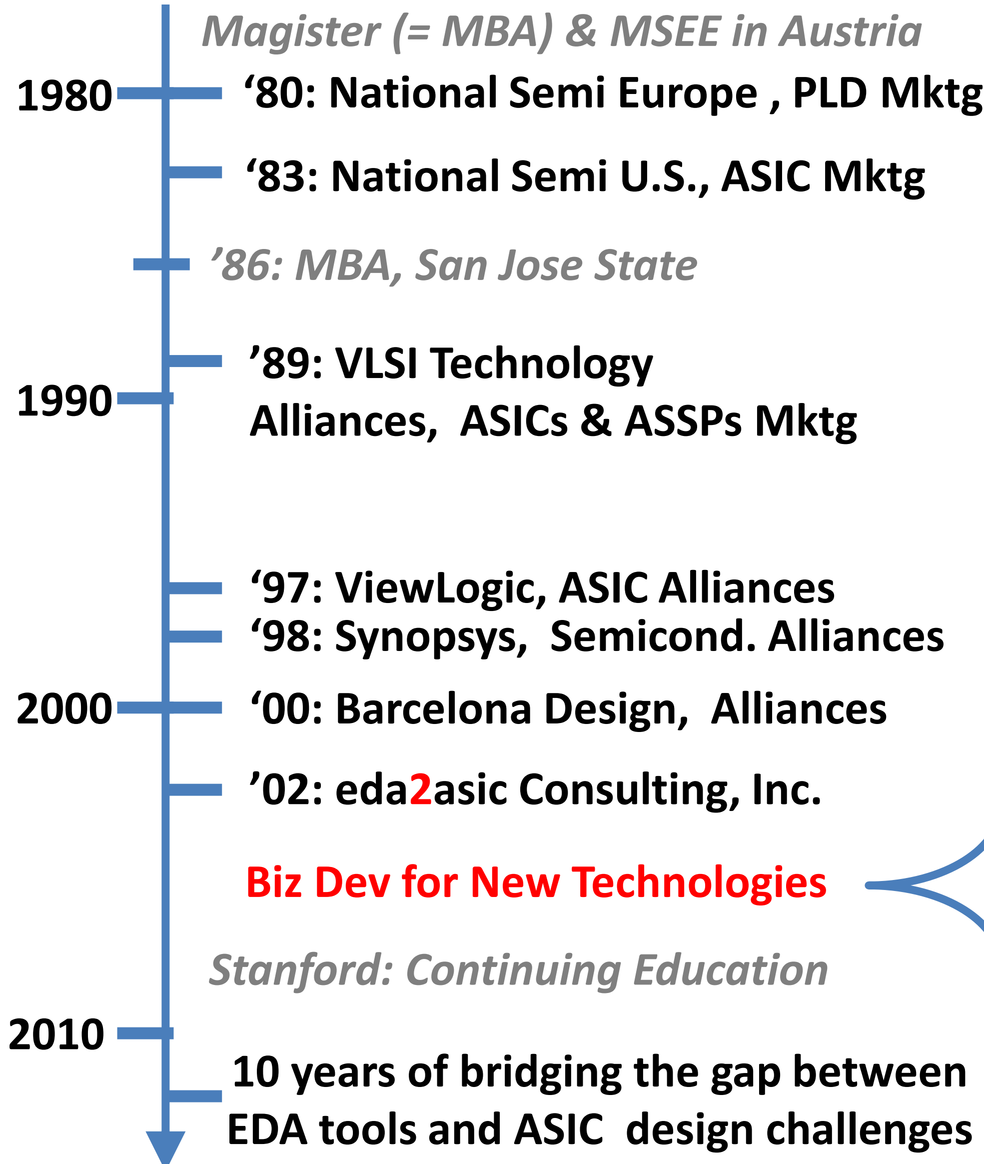
Herb Reiter's Background



Synplicity, Structured ASIC Tools
ReShape, IC Design Flow
Gradient, Temp Analysis, ICs
Flomerics, Temp Analysis, PCB
AMD, Opteron Mktg to EDA
GDA, Design Services Biz Plan
Takumi, DFM Tools & Services
Innovative Silicon, ZRAM-IP
S3 Group, Analog & M/S IP
Philips, Clockless IC Design
Mentor, C→ RTL Synthesis
Mephisto DA, Analog Sizing
Ciranova, Analog Layout
GeorgiaTech, SiP Noise Analysis
Soitec & SOI Consortium, SOI
GSA, 3D-IC Working Group
SEMATECH, 3D Enablement Ctr

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Market Numbers

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2016 Market Size Forecast

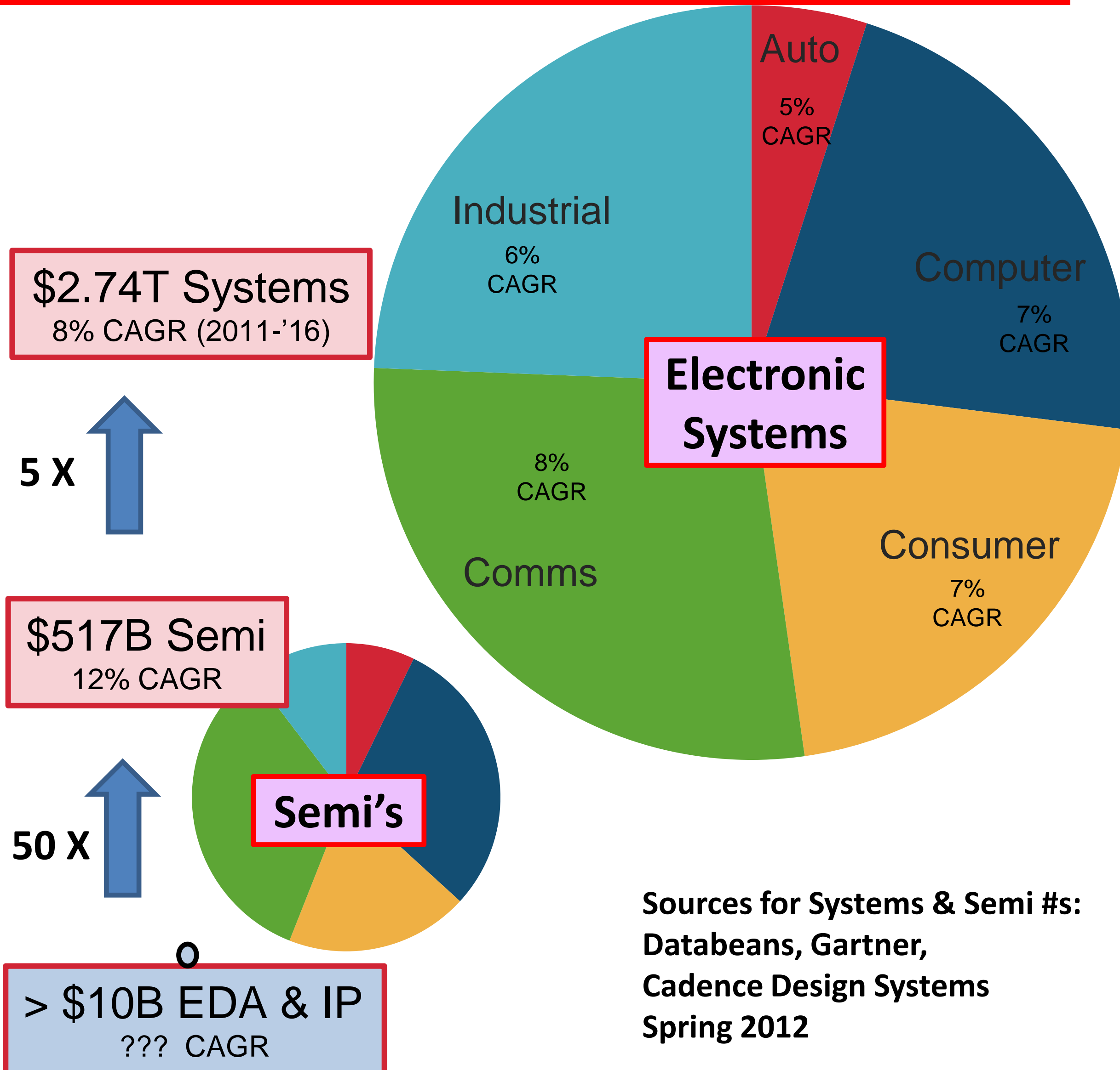
Systems need to get faster AND consume less power.

2.5/3D-ICs can integrate sub-systems, even entire systems at lower power, higher speed and eventually also lower system cost.

If 2.5/3D-ICs capture addit'l 10% of the systems market, they'll grow semiconductor revenues by 50 % !!!

EDA tools for modeling, planning & partitioning, implementation and verification of ICs have a significant impact on the cost-effectiveness of 3D semiconductor solutions.

Relatively minor investments in EDA tools, IP blocks and die-level IP will enable these semiconductor vendors to contribute big to **faster and lower power systems !**



Sources for Systems & Semi #s:
Databeans, Gartner,
Cadence Design Systems
Spring 2012

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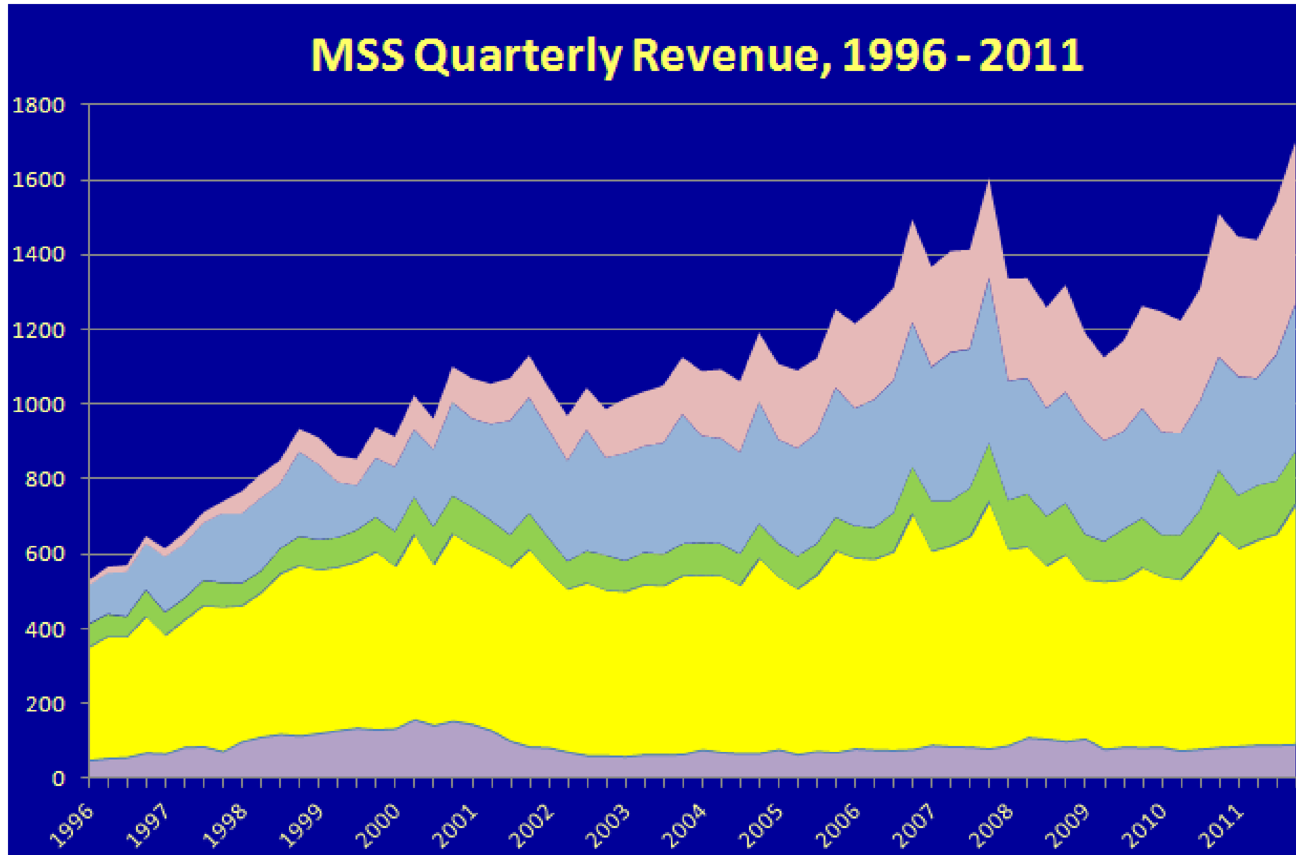
Quarterly EDA Revenues



Silicon IP

IC Physical

PCB / MCM

CAE

Services

http://www.edac.org/mss/stats_mss.jsp

http://www.edac.org/mss/MSS_2012_Category_Definitions_FINAL.pdf

Total EDA Revenues in CY 2011: USD 6.13 Billion

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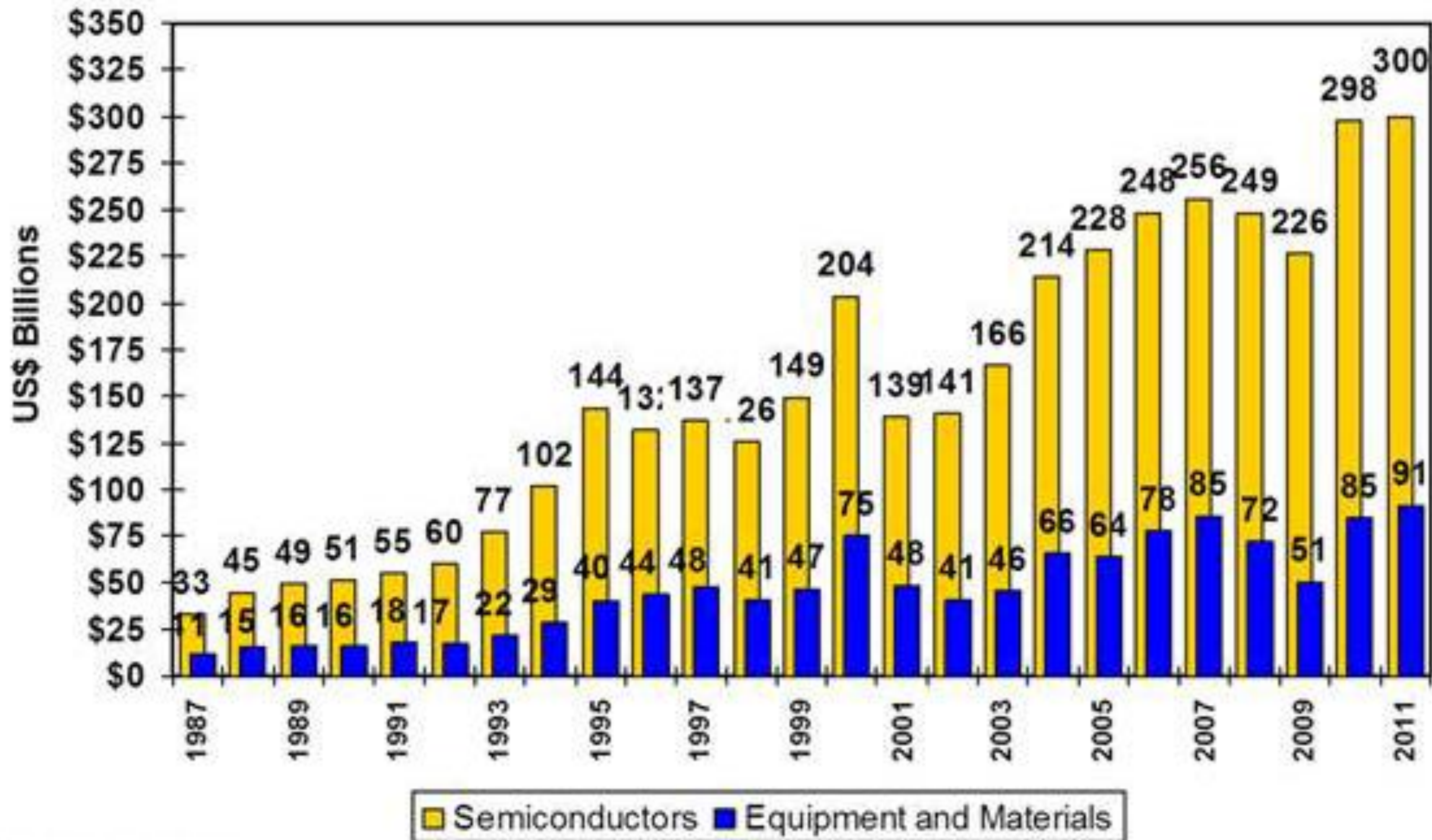
~30% of Semiconductor Revenue is…



http://www.semi.org/en/node/41166

Why Develop 2.5/3D Solutions ?

Key Motivators

- Reduce system cost
- Reduce power dissipation
- Reduce form factor
- Increase system complexity/user friendliness
- Increase performance per Watt
- Increase reliability
- Decrease time-to-market
- Decrease NRE and risk

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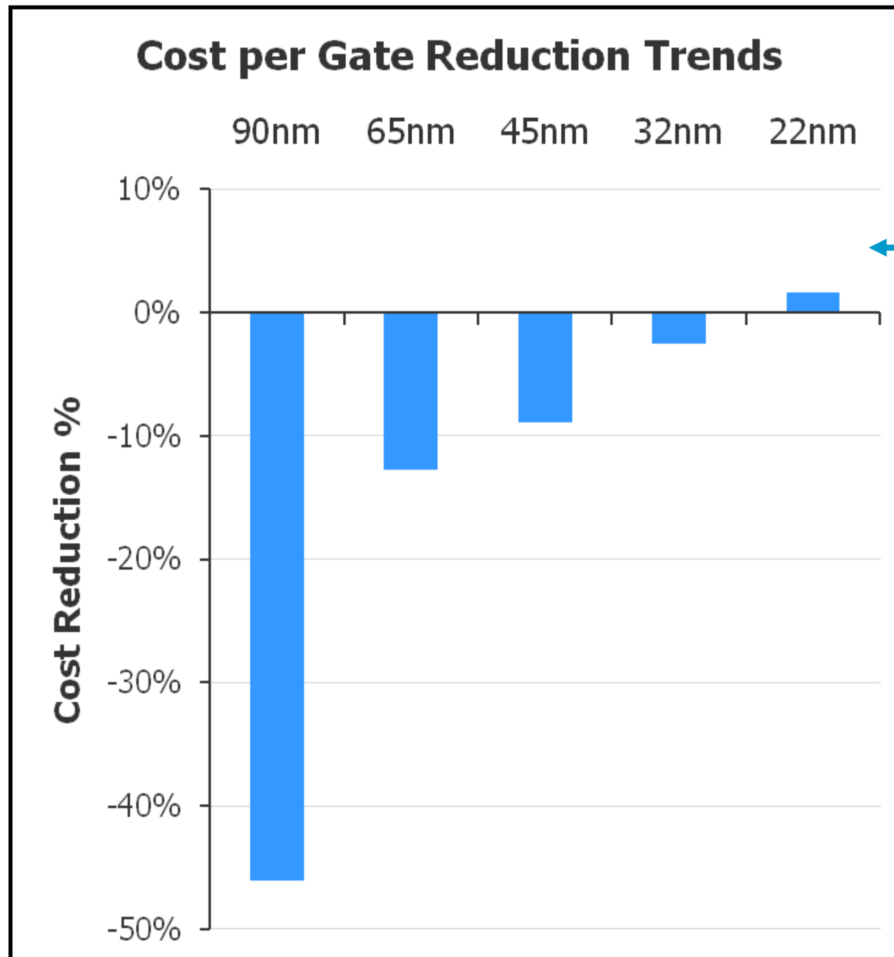
Challenges for Feature Size Shrinking



Source: International Business Strategies 2010

Wafer Fab cost ↑

Cost per gate ↑

Variability ↑

Risk, TTM ↑

Design Cost ↑

Mask Cost ↑

Yield Variations ↑

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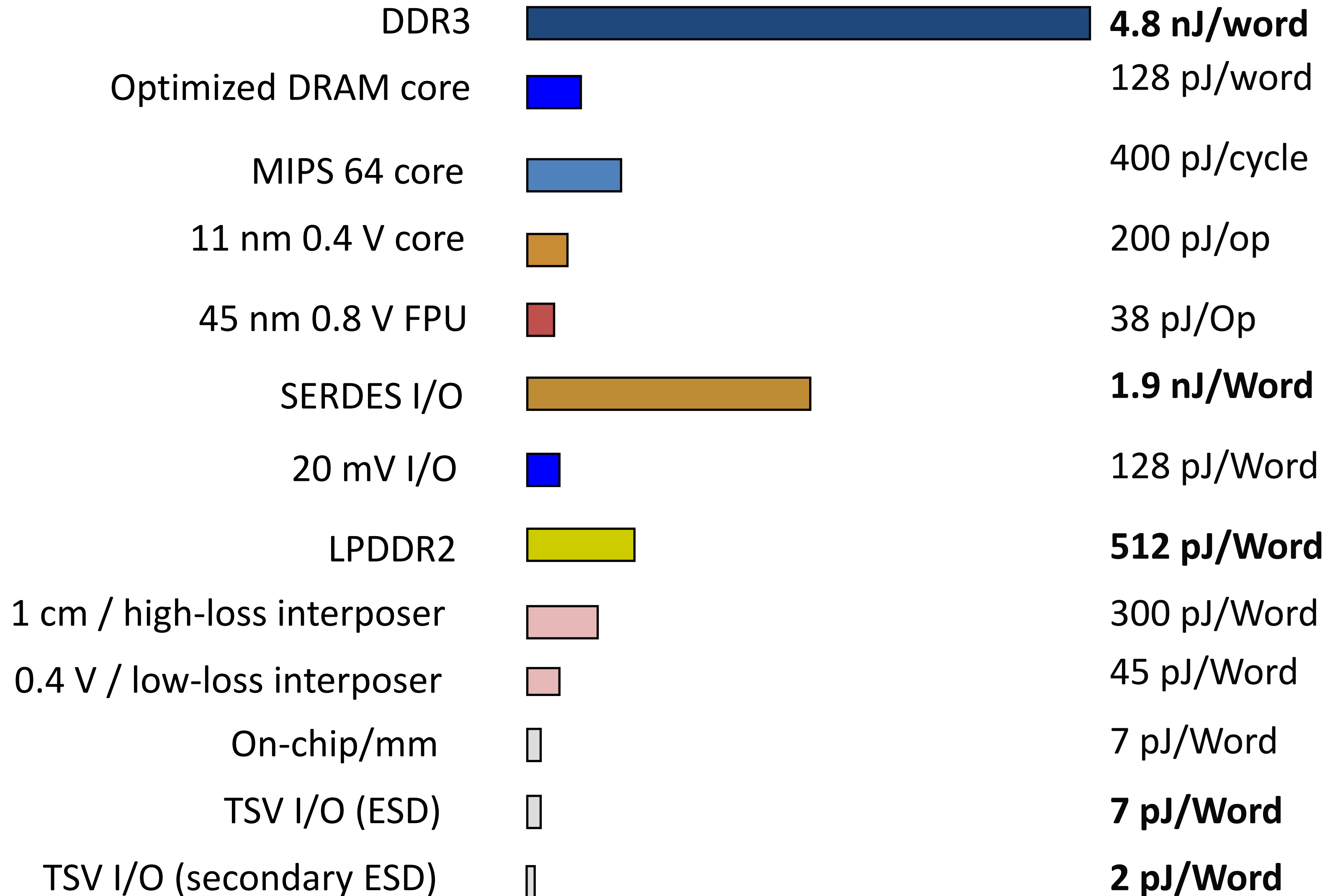
Energy per Operation (64 bit words)

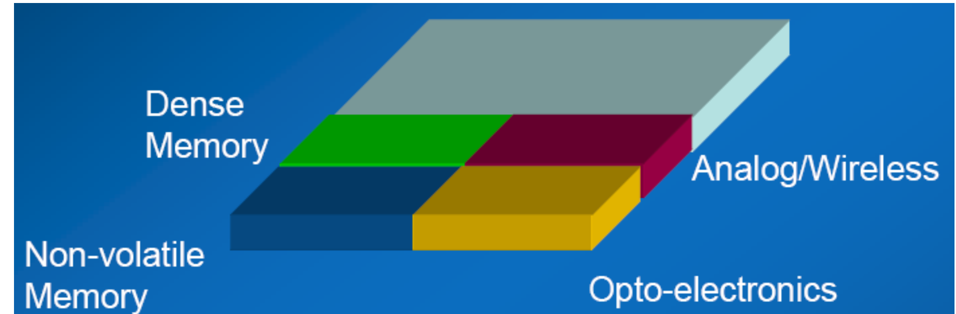


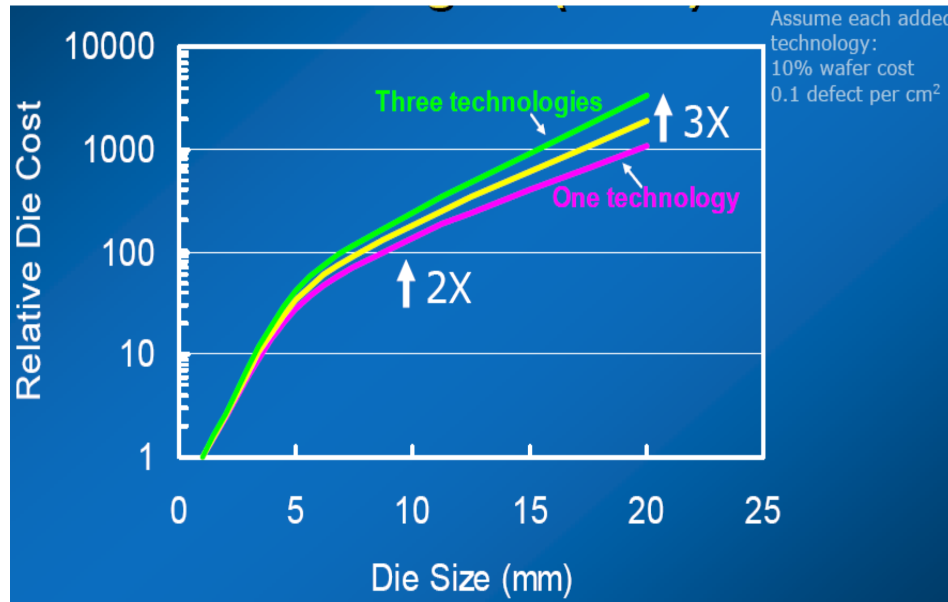
Dr. Paul Franzon, NCSU, June 2012

Cost Comparison for Mixed-Signal ICs

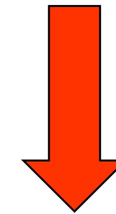
Heterogeneous integration on <u>one</u> die is usually expensive

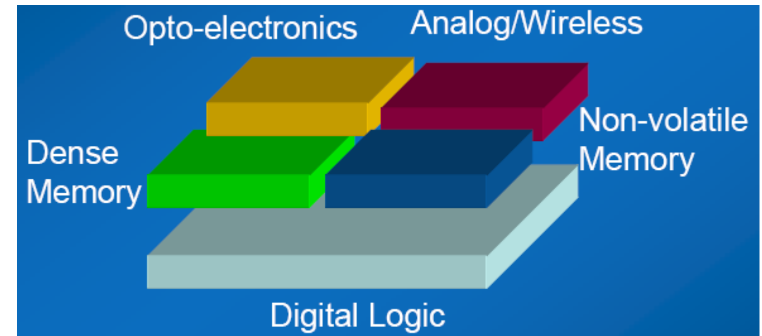
3D stacking reduces cost for heterogeneous integration





Courtesy: Borkar, Intel





Yuan Xie, Penn State Univ.

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TSV Enabled Benefits

ChipEstimate.com

General Benefits of TSVs

Improved ~10x

Improved ~6x

Improved ~200x

Improved ~6x

PCB or PoP

Silicon Interposer

Direct C2C stacking

Number of connections

Capacitance per connection

Average Connection Length

Relative power (proportional to f, c, # connections)

Design Automation Conference, San Francisco, June 2012

cadence

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What's Different in the 2.5/3D Eco-System?

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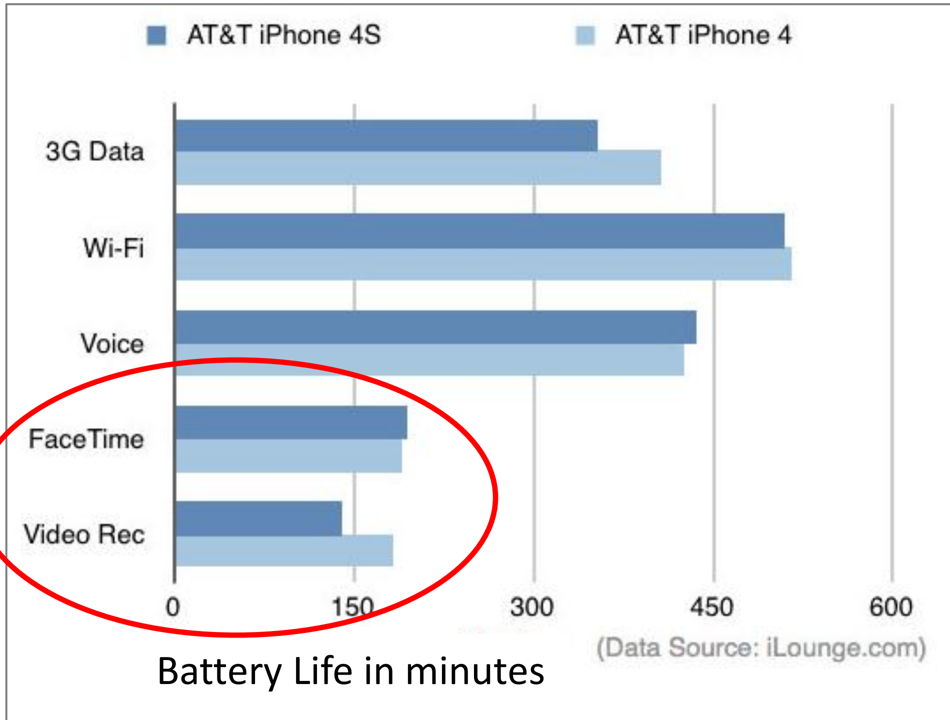
Application Specific Requirements

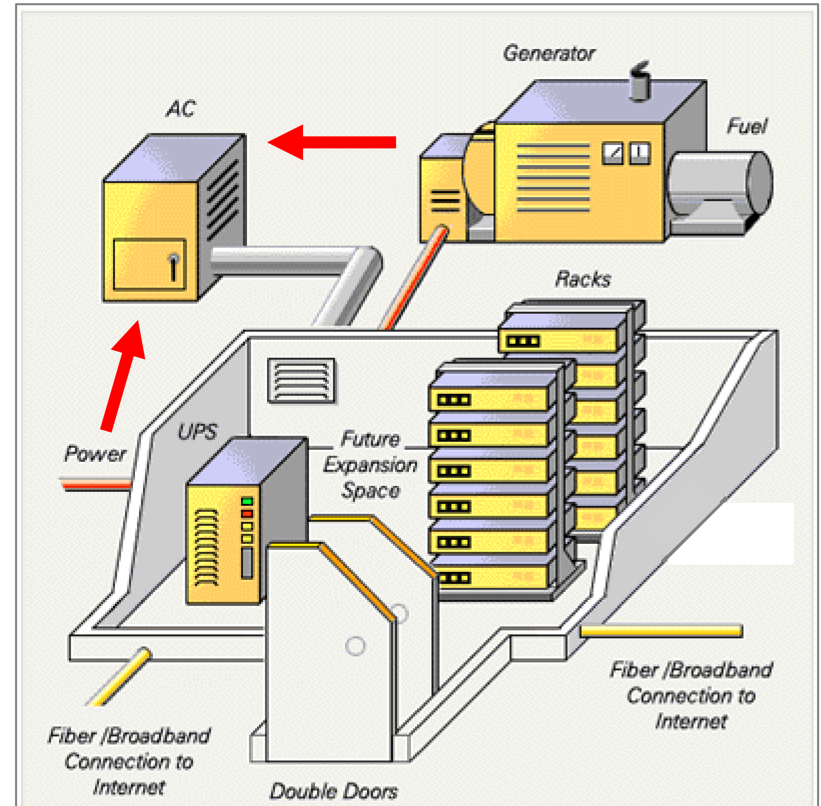
Mobile Devices



http://www.ilshayeb.com/?p=1494

Battery Life and System Price !!!

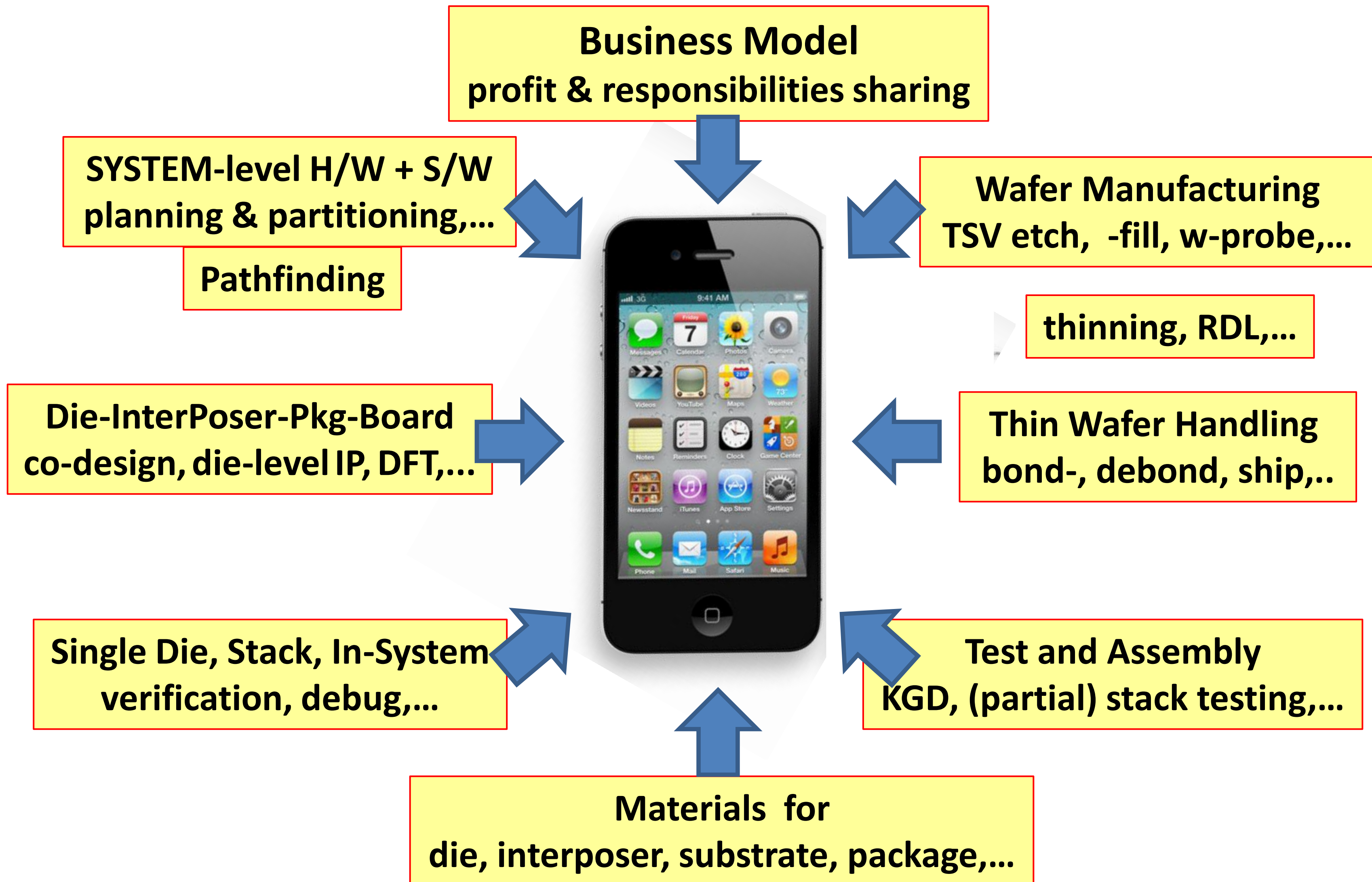
Data Centers



http://www.lbl.gov/Science-Articles/Archive/data-center-energy-myth.html

Operating & Cooling Cost !!!

eda2asic Changes Needed for 2.5/3D-ICs Systems



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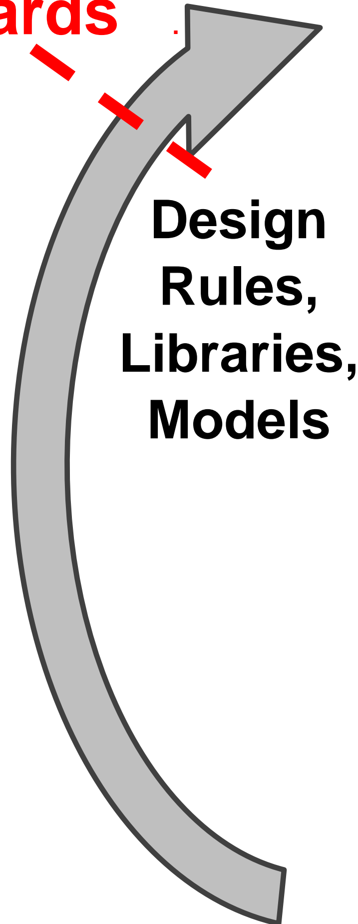
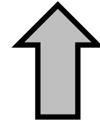
EDA Vendors Driving Standards

Libraries, IP, Dice,…

Standards

Designers



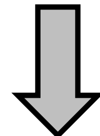


Design tools

Design Rules, Libraries, Models

Design Files and Test Programs

Modeling tools



Manufacturers

Fab, Assembly, Test

Standards for Hand-off Criteria

We Need a Light ...

Standards Organizations

- Capture common requirements
- Help setting R & D priorities
- Manage pre-competitive JOINT development efforts
- Lead consensus towards standards
- Educate users, proliferate & update standards
- Domestic standards organizations, e.g.:

IEEE JEDEC NIST

- …and many more standards organizations in foreign countries

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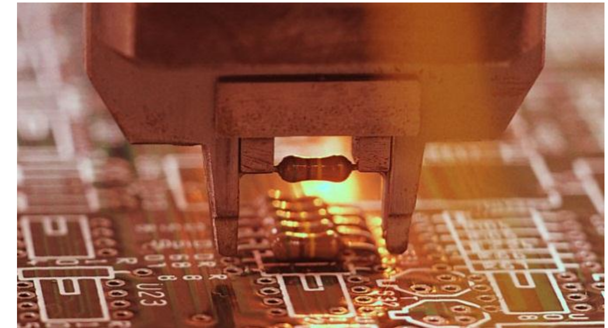
MISSION: Accelerating the next technology revolution



Research | Development | Manufacturing

3D Enablement Center Members: ADI, Altera, ASE, Invensas, LSI, NIST, ON Semi, Qualcomm

3D Interconnect Program Member: Hynix

SEMATECH Core Members: CNSE, Global Foundries, IBM, Intel, Samsung, TSMC

SEMATECH Standards Dashboard at: http://wiki.sematech.org/3D-Standards

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Closed vs Open Innovation Principles

CLOSED		OPEN
The smart people in the field work for us.	1	Not all smart people in the field work for us. We need to work with smart people inside AND outside our company.
To profit from R&D we must discover it, develop it and ship it ourselves	2	External R&D can create significant value; internal R&D is needed to claim some portion of that value.
If we discover it ourselves, we will get it to market first.	3	We don't have to originate the research to profit from it.
The company that gets an innovation to the market first, will win.	4	Building a better business model is better than getting to the market first.
If we create the most and best ideas in industry, we will win.	5	If we make the best use of internal and external ideas, we will win.
We should control our IP so that our competitors don't profit from our ideas.	6	We should profit from others' use of our IP, and we should buy others' IP whenever it advances our business model.

http://www.inventorium.org/2012/04/10/open-innovation/oi/

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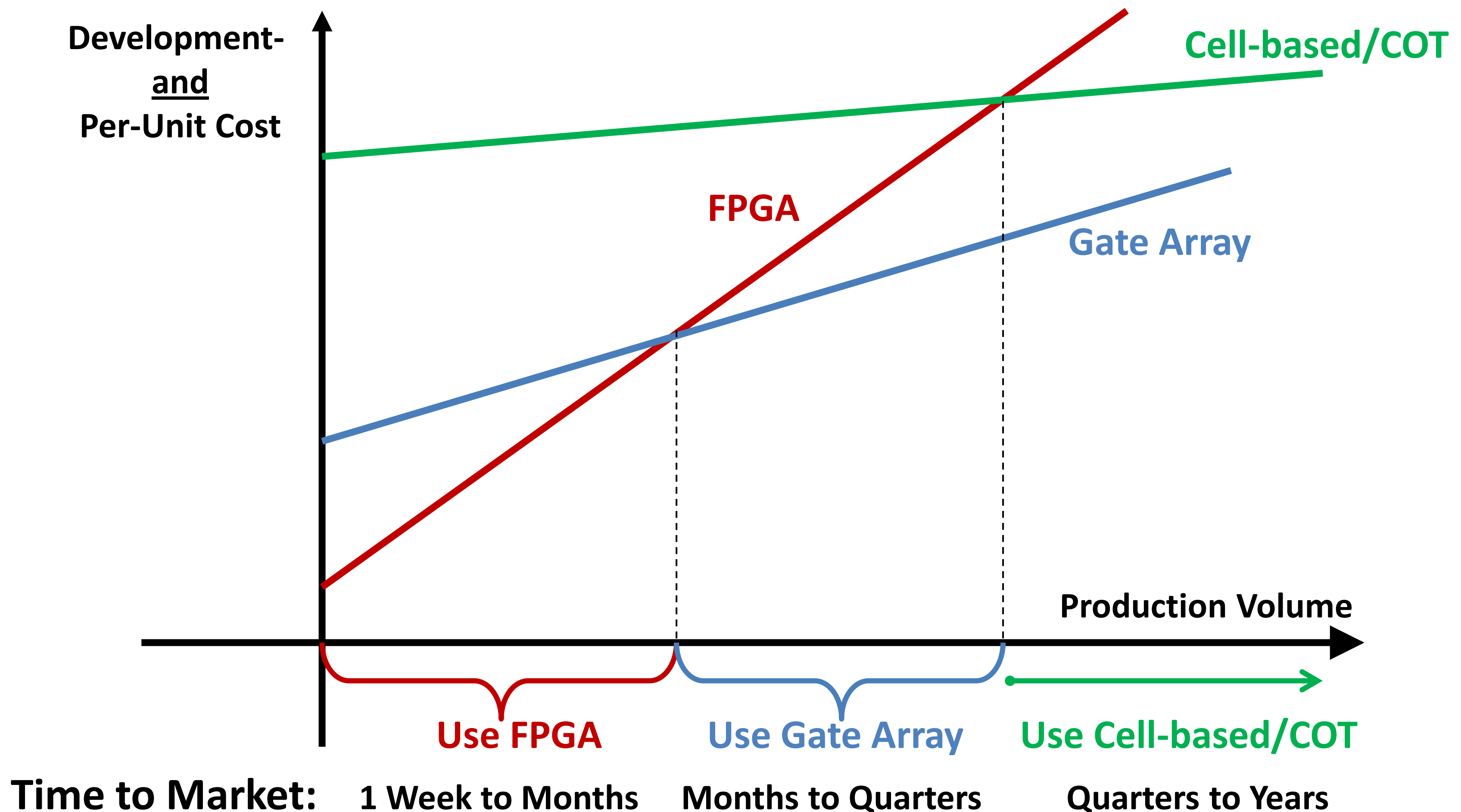
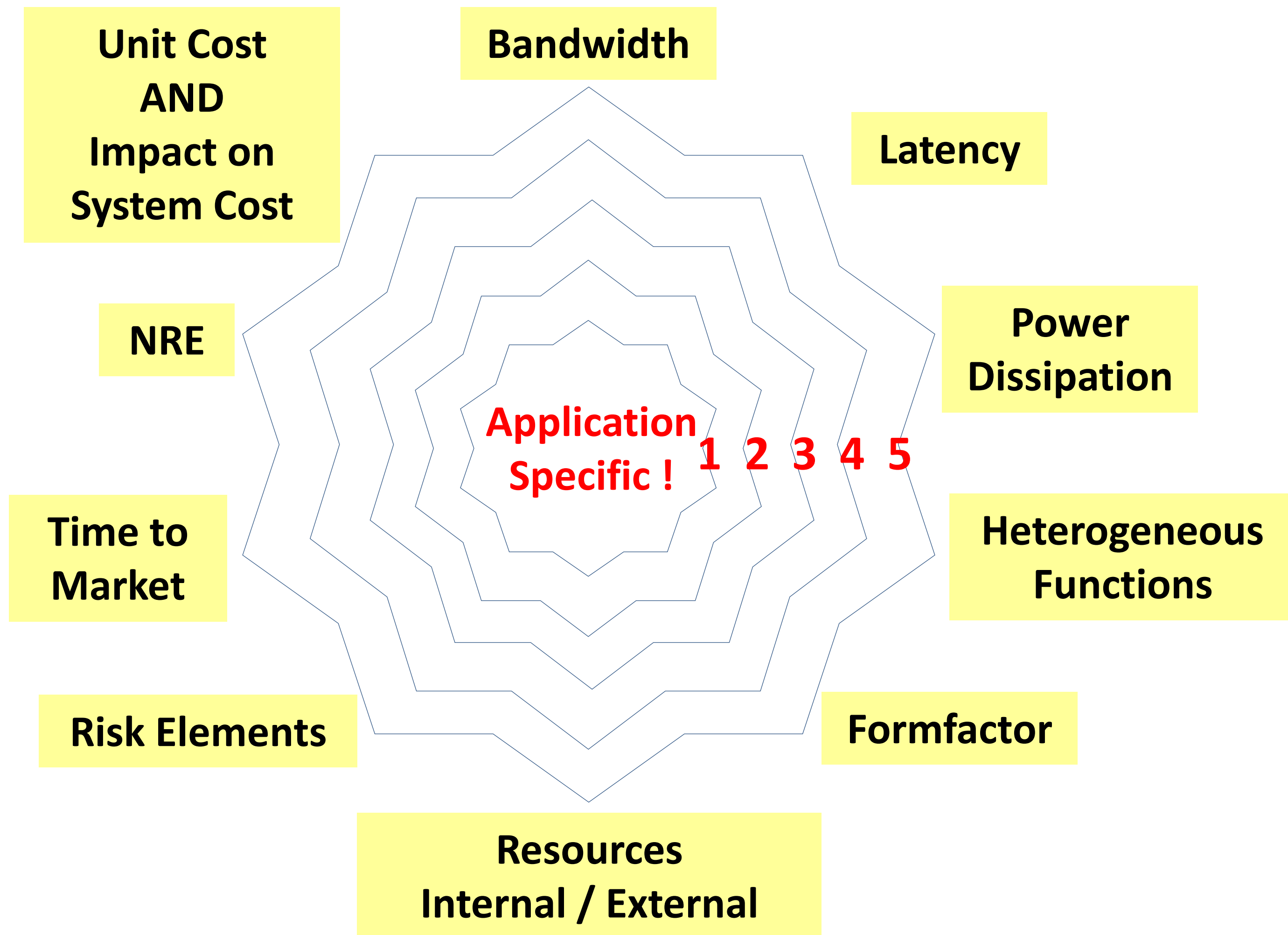
In the Good Old Times ...

Total COST and Time-to-Market were the dominant criteria for technology selection

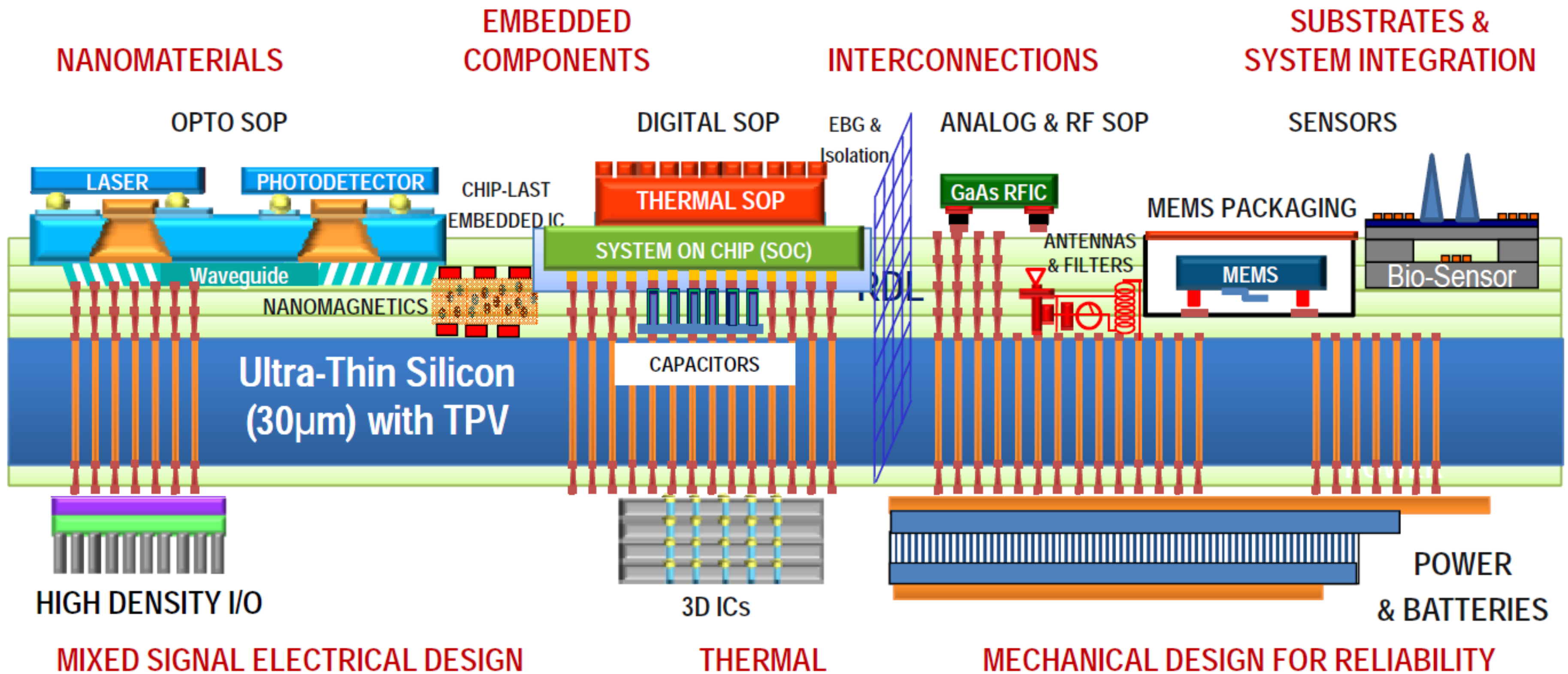


Technology Selection Today

Examples for important technology selection criteria



eda2asic Tomorrow: 2.5/3D System Integration



Source: Rao Tummala, Georgia Institute of Technology, 3D Systems Packaging Research Center, Oct 2010

2.5 / 3D Products TODAY

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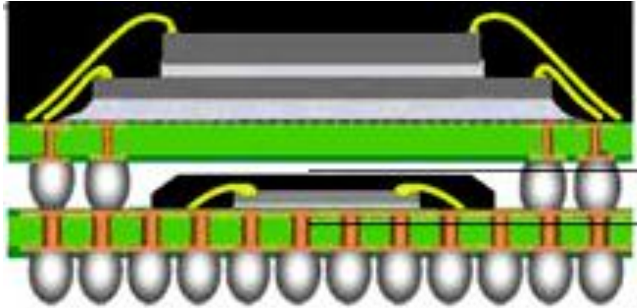
Technology Comparisons



SoC and SiP, combined in a PoP

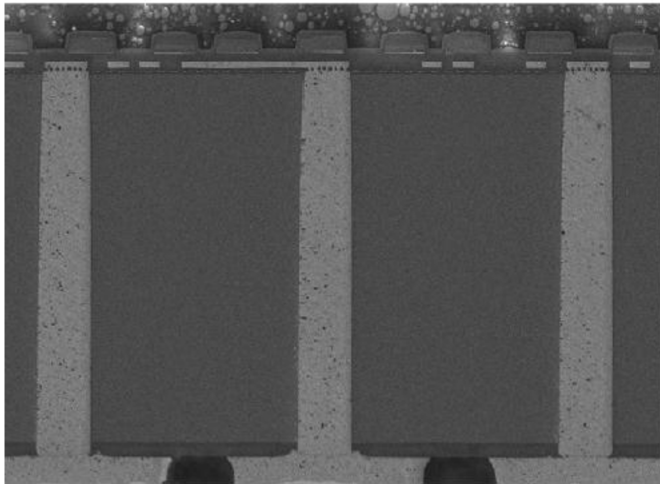
http://www.design-reuse.com/articles/exit/?id=14887&url=http%3A%2F%2Fwww.commsdesign.com%2Farticle%2FprintableArticle.jhtml%3FarticleID%3D196700054

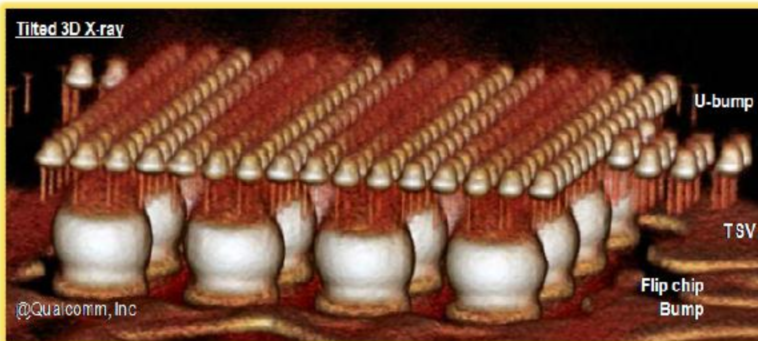
PoP cross-section from www.ifixit.com

	PoP	SiP	Interposer	3D/TSV
Package Thickness				
Power Dissipation				
Access Time				
Bandwidth				
Industry Readiness				Memory Logic

limited | o.k. | good | best

Evolving to "Mainstream" 3D Technologies





~ 100 um
DIE 2 Substrate
Device
DIE 2 BEOL
~20 um
~20 um
uBump
Backside Insulator
DIE 1 : Si Substrate
~ 50 um
TSV
~5 um
TSV
Device
M1
ILD
M2
Mn
DIE 1 BEOL
~100 um
FC Bump

QUALCOMM CDMA Technologies

Copper Pillars vs Solder Bumps

Property	Copper Pillar Bump	Conventional Solder bump
Pitch	<50 um	>70 um
Connection density	>2000 per die	<1000 per die
Height	30 um to 50 um	50 um to 70 um
Electrical	Higher conductance	Lower conductance
Thermal	Higher conductance	Lower conductance
Mechanical	Higher yield strength	Lower yield strength

http://www.edn.com/article/print/521939-Die_to_die_bonding_using_copper_pillars.php

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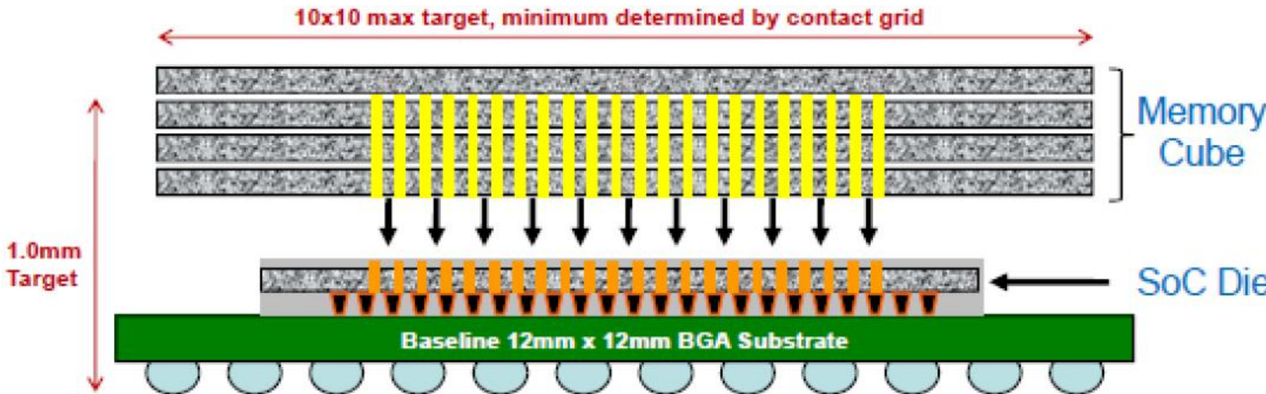
Wide I/O Standard



Channel A / **Channel B** (top), **Channel D** / **Channel C** (bottom)

44	45	46	47	48	49	50							51	52	53	54	55	56
C44	C45	C46	C47	C48	C49	C50							C50	C49	C48	C47	C46	C45
2150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950	3000	3050
VDD2	VDD2	DM15a	DAa	DM14a	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DM14b	DAb	DM15b	VDD2
VDD2	VDD2	DQ123a	NC	DQ118a	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DQ118b	NC	DQ123b	VDD2
DQ108a	DQ124a	VDDQ	DQS7_ca	VSSQ	DQ112a	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ112b	VSSQ	DQS7_cb	VDDQ	DQ124b
DQ109a	DQ125a	VDDQ	DQS7_ta	VSSQ	DQ113a	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ113b	VSSQ	DQS7_tb	VDDQ	DQ125b
DQ110a	DQ126a	DQ122a	DQ119a	DQ117a	DQ114a	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ114b	DQ117b	DQ119b	DQ122b	DQ126b
DQ111a	DQ127a	DQ121a	DQ120a	DQ116a	DQ115a	RST0_n	nb	nb	nb	nb	nb	nb	RST1_n	DQ115b	DQ116b	DQ120b	DQ121b	DQ127b
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb
DQ111d	DQ127d	DQ121d	DQ120d	DQ116d	DQ115d	RST3_n	nb	nb	nb	nb	nb	nb	RST2_n	DQ115c	DQ116c	DQ120c	DQ121c	DQ127c
DQ110d	DQ126d	DQ122d	DQ119d	DQ117d	DQ114d	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ114c	DQ117c	DQ119c	DQ122c	DQ126c
DQ109d	DQ125d	VDDQ	DQS7_td	VSSQ	DQ113d	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ113c	VSSQ	DQS7_tc	VDDQ	DQ125c
DQ108d	DQ124d	VDDQ	DQS7_cd	VSSQ	DQ112d	VDD1	nb	nb	nb	nb	nb	nb	VDD1	DQ112c	VSSQ	DQS7_cc	VDDQ	DQ124c
VDD2	VDD2	DQ123d	NC	DQ118d	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DQ118c	NC	DQ123c	VDD2
VDD2	VDD2	DM15d	DAd	DM14d	VSS	VSS	nb	nb	nb	nb	nb	nb	VSS	VSS	DM14c	DAc	DM15c	VDD2
2150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950	3000	3050
C44	C45	C46	C47	C48	C49	C50							C50	C49	C48	C47	C46	C45
44	45	46	47	48	49	50							51	52	53	54	55	56

Standardized by JEDEC 42.6

Published in December 2011
Twice the bandwidth of LPDDR2 at the same power
Mobile HD video: 12.8 MB/sec

4 channels, each 128 data bits
1200 total connections

1.2V CMOS signal levels
Pad-pitch 40 x 50 microns

Boundary scan to test I/C

Locations of thermal sensors

Exact mechanical dimensions (defined by JC 11)

Courtesy: Intel and JC 42.6

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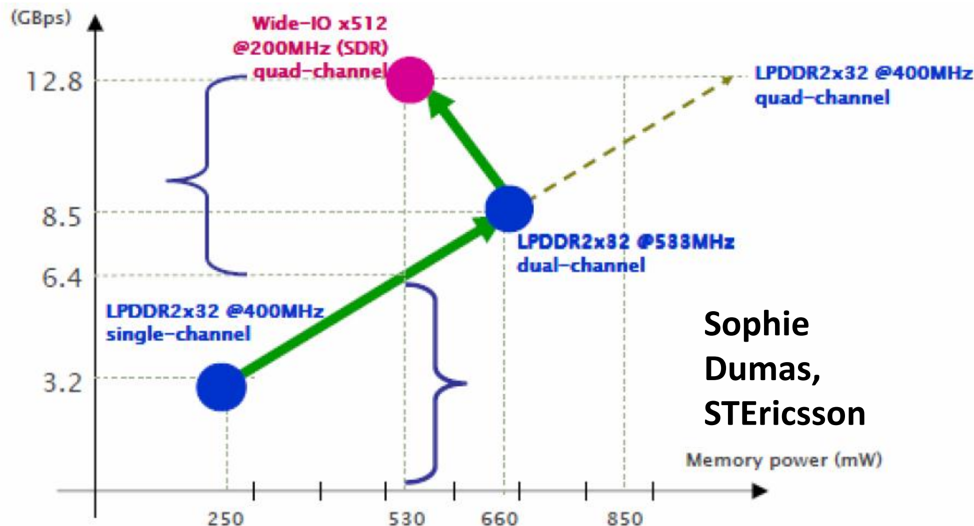
Wide I/O Standard

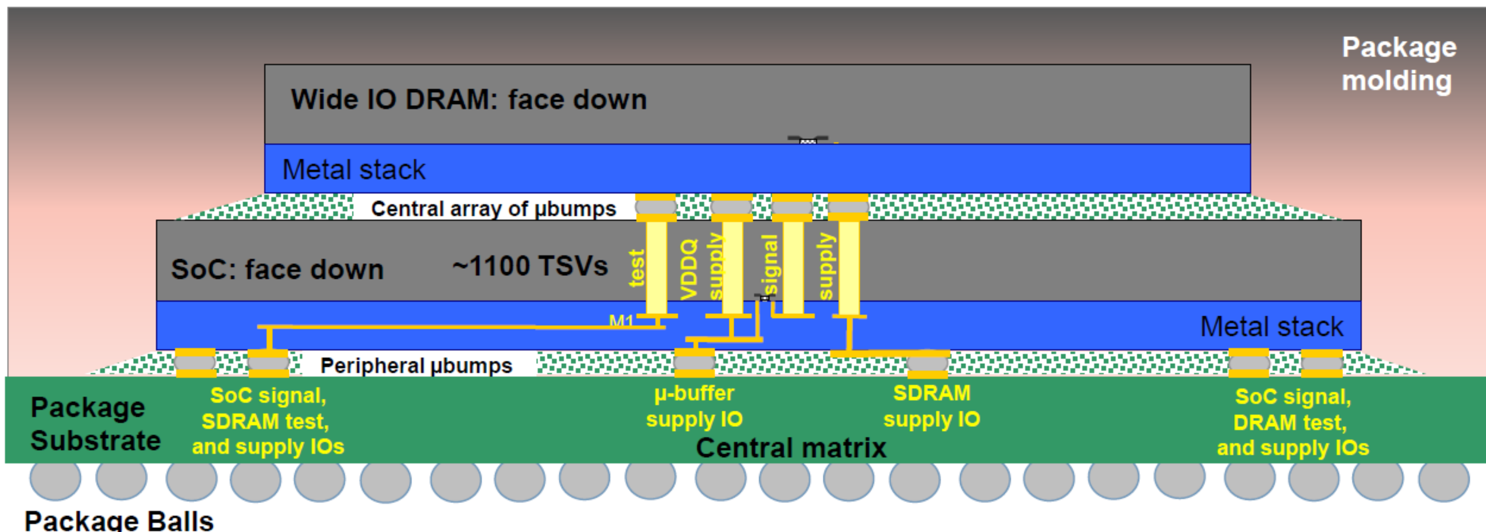


Sophie Dumas, STEricsson

JEDEC (**JC 42.6**) released Q4, 2011 the first Wide I/O Standard

TWICE the Bandwidth at the same Power Dissipation as LPDDR2

Drivers: Samsung, Elpida, Hynix, Micron, Qualcomm, TI, Intel, AMD, ST, Apple, Advantest and others



Wioming Test-Chip

http://eda360insider.wordpress.com/2011/12/14/3d-week-wide-io-sdram-network-on-chip-multicore-tsv-asynchronous-logic-3d-soc-stack-from-cea-leti-and-st-ericsson-hits-all-the-advanced-notes-can-you-say-tour-de-force/

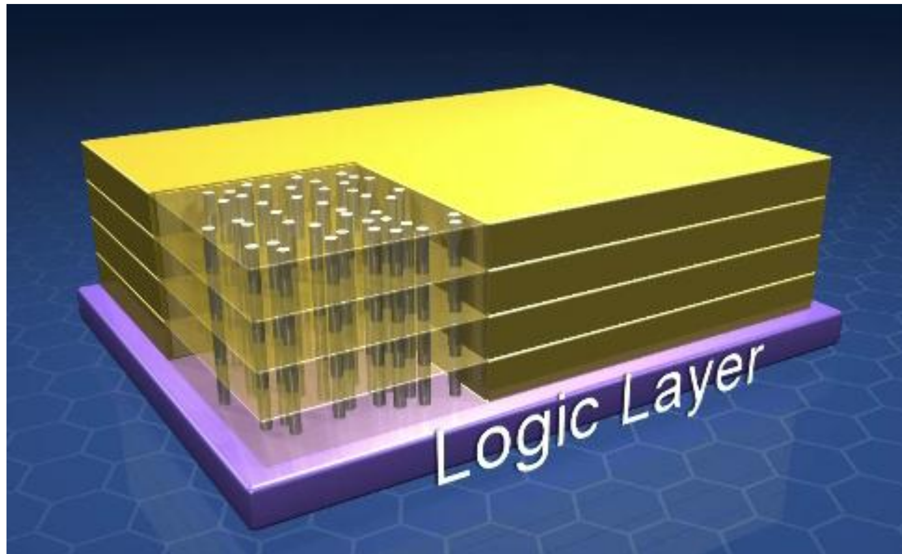
D43D Grenoble - June 30 2011 – Georg Kimmich

3D For Tablets and Smartphones

ST ERICSSON

Hybrid Memory Cube

Hybrid Memory Cube Consortium



HMC Consortium founded by Micron and Samsung in Oct 2011.

HMC combines high-speed logic process technology with a stack of through-silicon-via (TSV) bonded memory die.

A single HMC can provide more than 15x the performance of a DDR3 module.

Utilizes 70% less energy per bit than DDR3 DRAM technologies..

HMC increases density per bit and reduces form factor - nearly 90% less space than today's RDIMMs.

http://hybridmemorycube.org/technology.html

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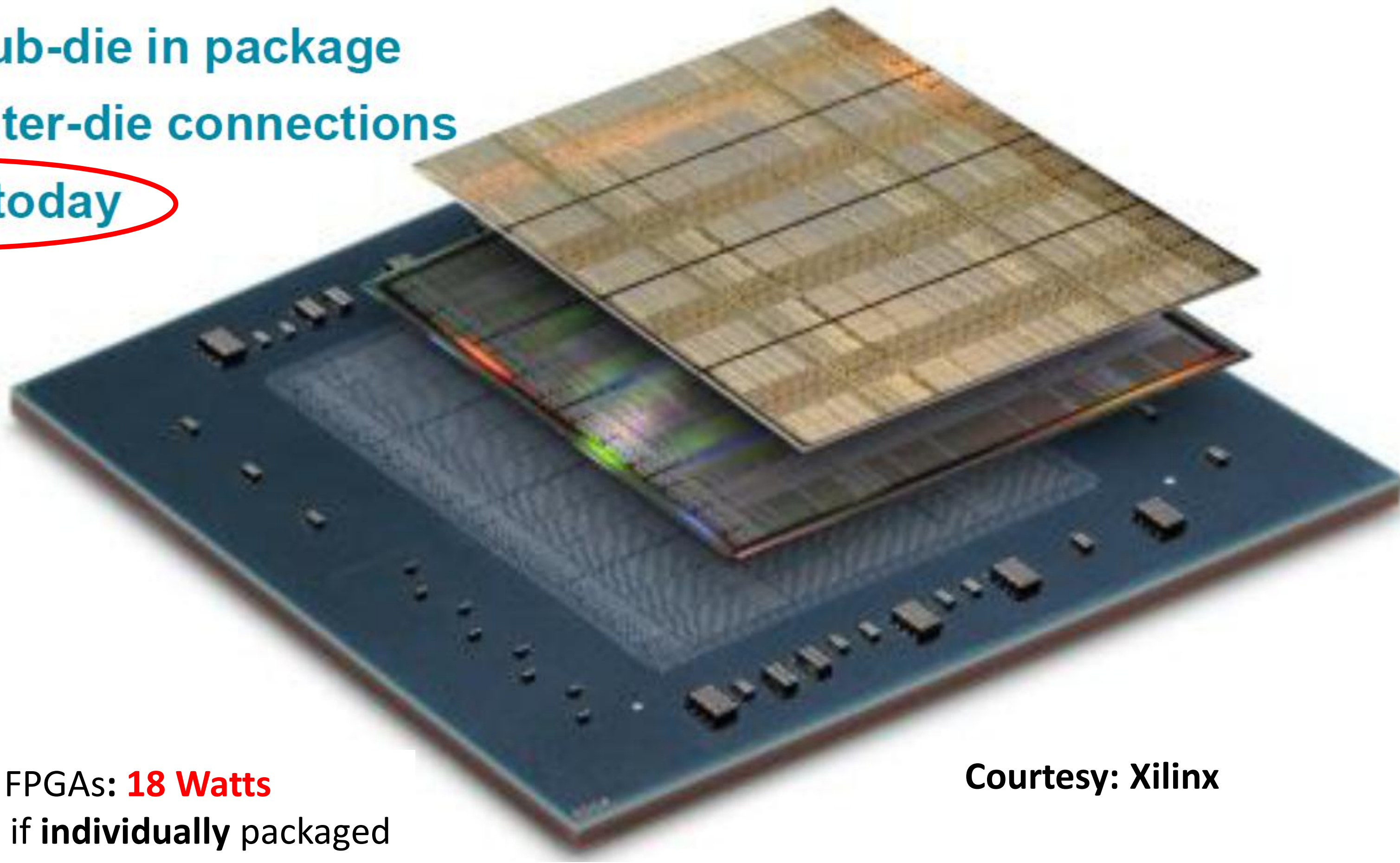
Quad FPGA in a Package

- Virtex 2000T – 2 million logic cells
- 4-layer metal Si interposer with TSV
- 4 FPGA sub-die in package
- >10,000 inter-die connections
- Shipping today



Power of these 4 FPGAs: **18 Watts**
Versus 120 Watts if **individually** packaged

Courtesy: Xilinx

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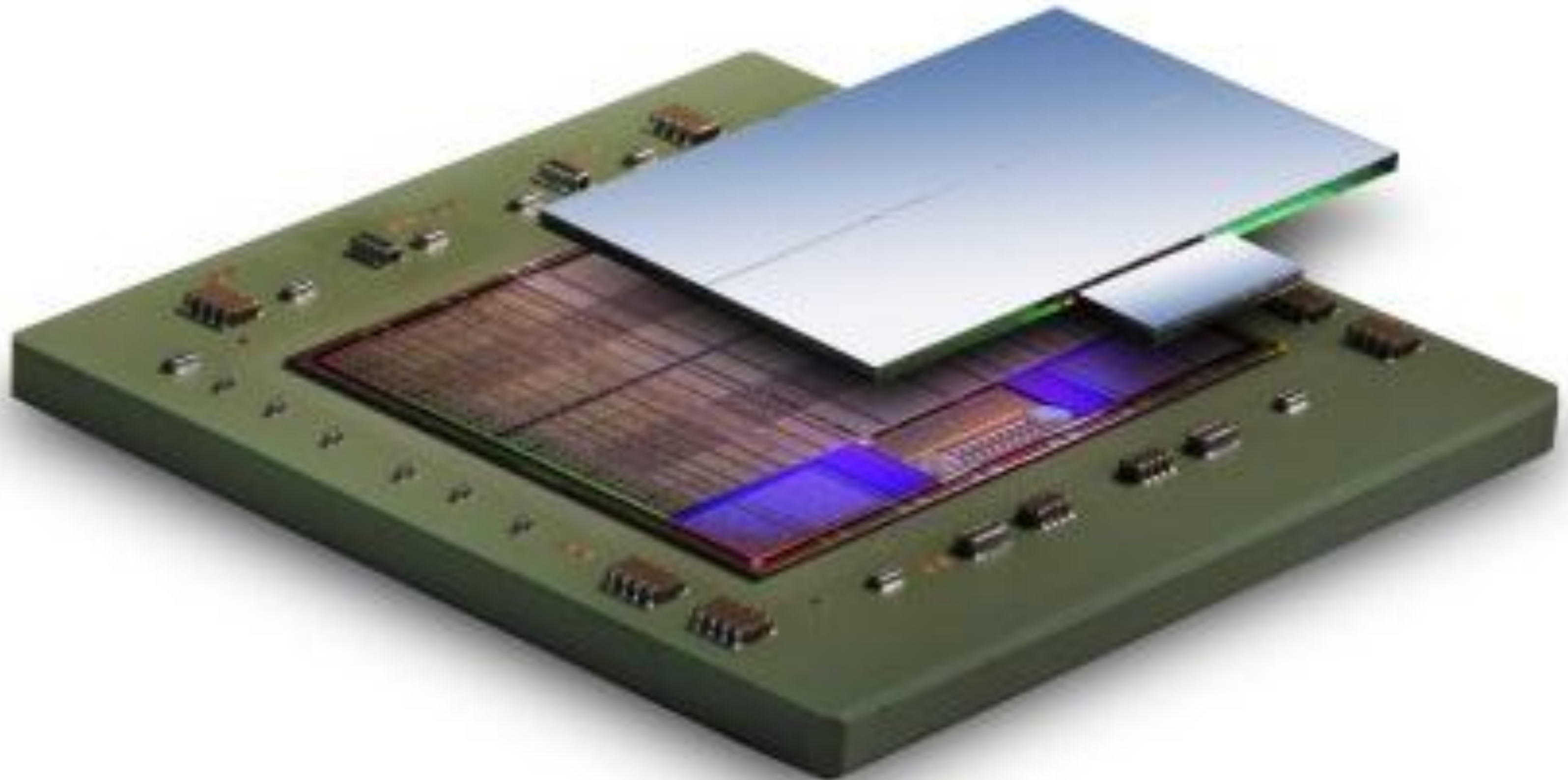
Second 2.5D FPGA from Xilinx

Virtex-7 H580T **Heterogeneous FPGA** announced May 30, 2012

Up to sixteen 28 Gbps and seventy-two 13.1 Gbps transceivers

Single-package solutions for addressing key Nx100G and 400G line card applications



http://www.eetimes.com/electronics-products/electronic-product-reviews/fpga-pld-products/4374071/Xilinx-ships-the-world-s-first-heterogeneous-3D-FPGA?cid=NL_EETimesProducts

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Altera/TSMC Testchip

TSMC's 2.5D Technology:
CoWoS = Chip **o**n **W**afer
on **S**ubstrate

EDA Readiness / Challenges

Flow exists (green) | Existing flows can be adapted (yellow) | Needs EDA support (red)

Focus Areas	Path finding	Tier Design & Verification	Die Stack Verification and Perf. Validation
Design Partitioning & Chip-Package Co-Design	red	green	red
Abstract Views	red	red	red
Physical, Functional, and Timing Verification		green	red
Connectivity Management		green	yellow
SI/PI Analysis	green	green	red
Thermal Analysis	green	yellow	yellow
Thermo-mechanical Assessment	yellow	yellow	yellow
Others: data exchange, scalability of database, etc.			red

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ALTERA.

http://www.electroiq.com/blogs/insights_from_leading_edge/2012.html

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2.5 & 3D Players and Plans

Company	Interposer-	3D Solution
TSMC	2H 2011	2012-2013
UMC		2H 2011
GlobalFoundries		2013
IBM	2011	
Samsung		2012
Elpida		2H 2011
Micron		2012
Nanya		2011-2012
ASE	2012-2013	
STATSChipPAC		2013
Amkor	2H 2011	
SPIL	2011	2012
Qualcomm		2013
Nokia		2012-2013
Xilinx	2H 2011	
Dell		2012

YOLE Micronews
January 2011

http://www.i-micronews.com/lectureArticle.asp?id=6351

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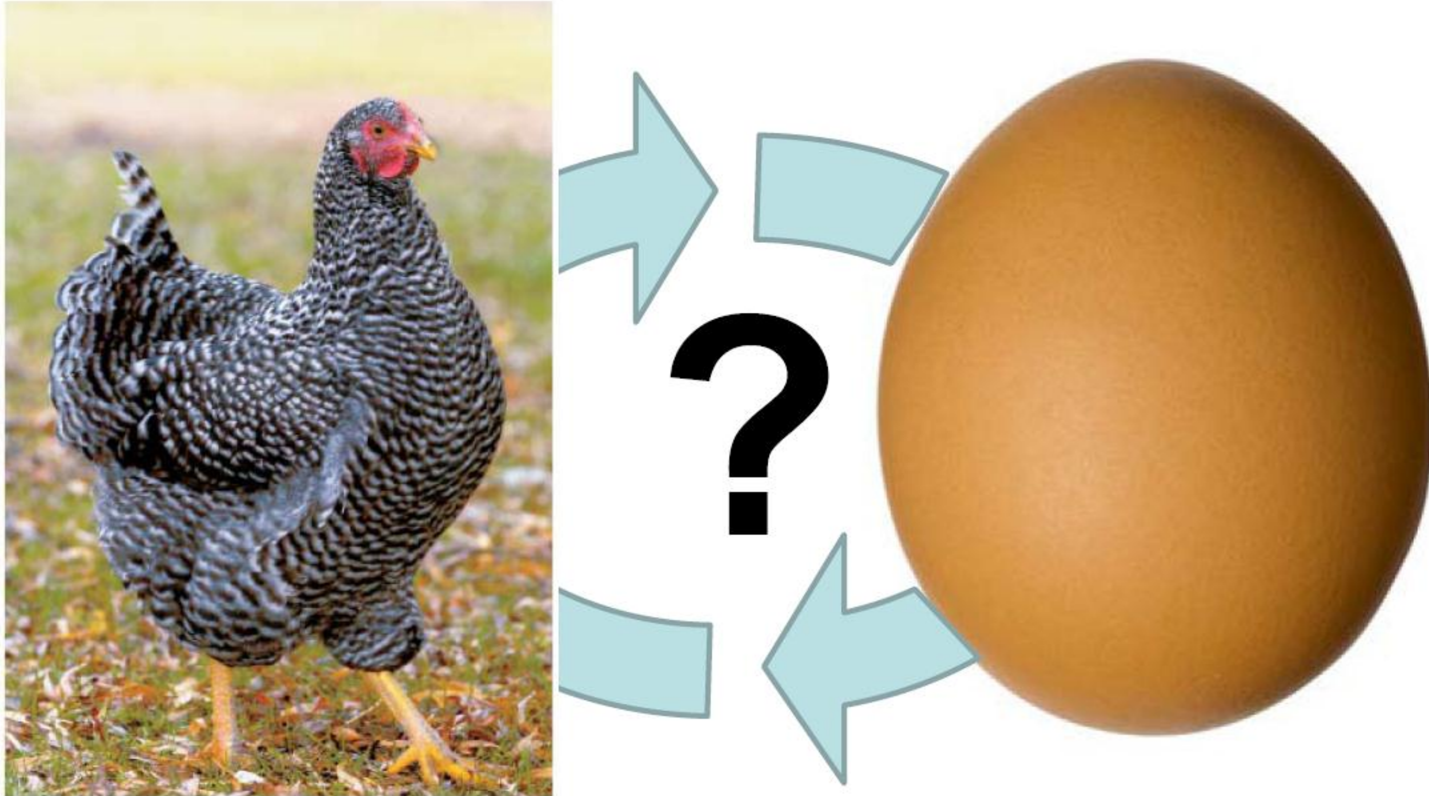
Chicken and Egg Scenario



What comes first ?

Strong customer demand for 3D ICs or a wide range of 3D capabilities?

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Opportunities for MEPTEC Members

MicroElectronics, Packaging and Test Engineering Council

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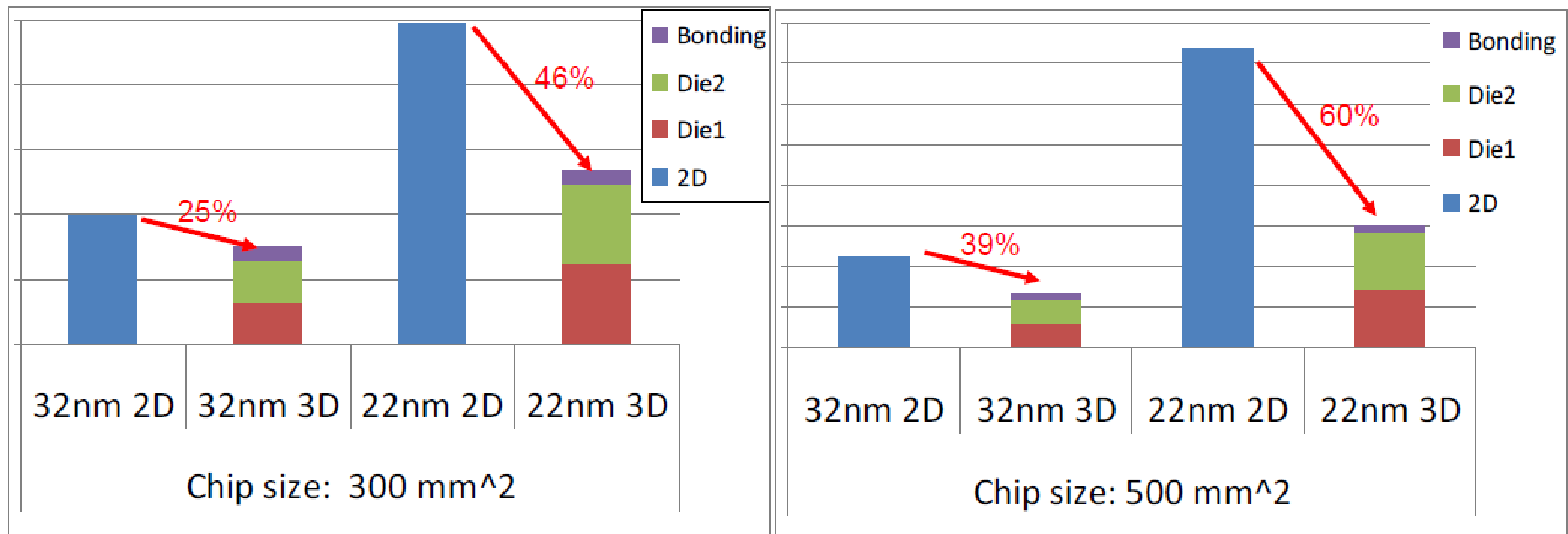
Cost-Effective Billion-Transistor Chips

- 3D stacking offers cost advantage for large chip with billions of transistors
  - Multiple smaller dies with higher yield;
  - Fewer number of metal layers to satisfy routing constraints for smaller chip



PENNSTATE

Source: Yuan Xie, PSU

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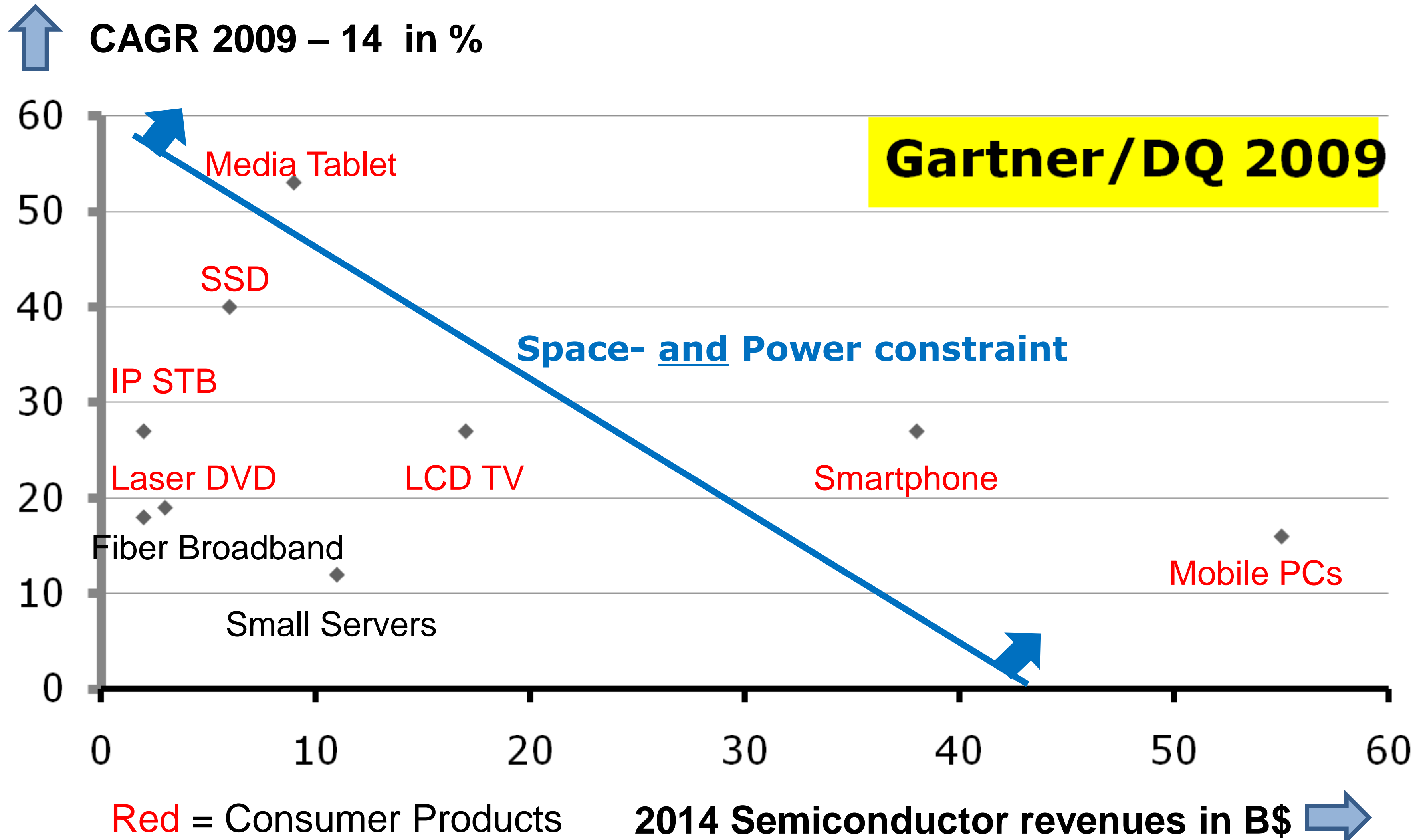
Growth Drivers Through 2014



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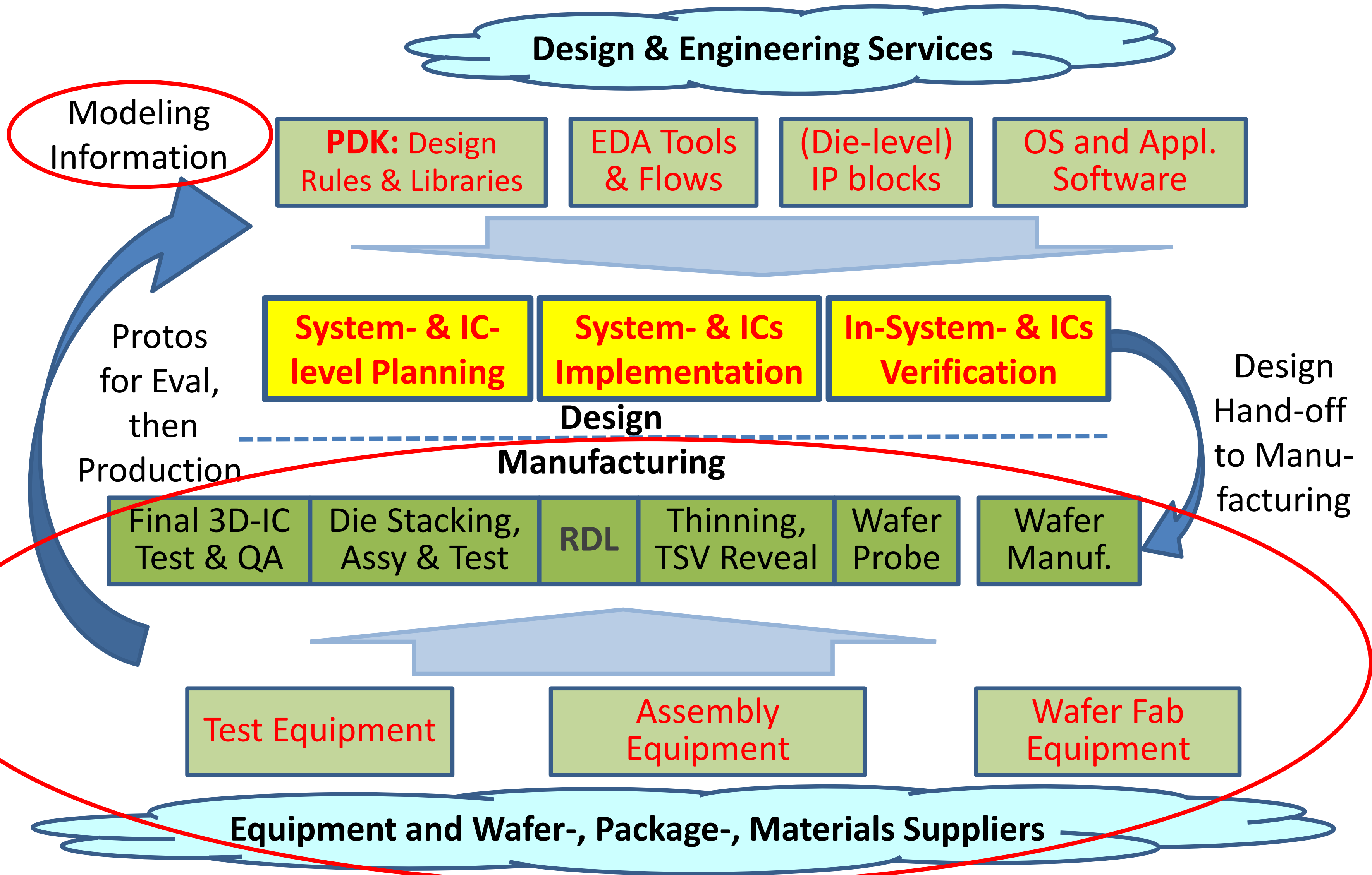
2.5/3D-ICs: Protos to Production



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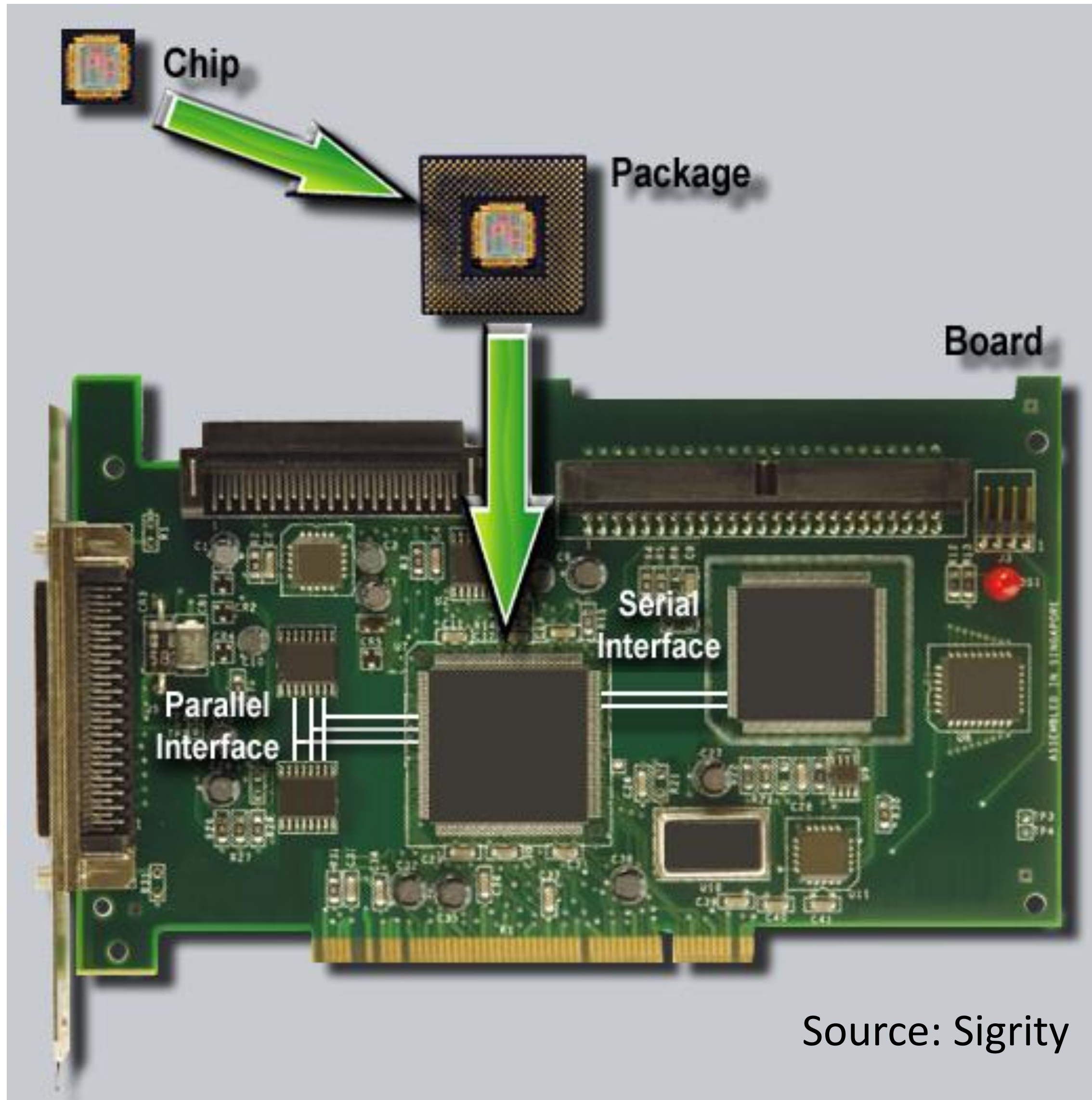
Today: Chip – Package – Board



System-Integration on Printed-Circuit-Boards:

Proven technologies,

Supply chain established,

Business model known,

Customer expectations

are established !

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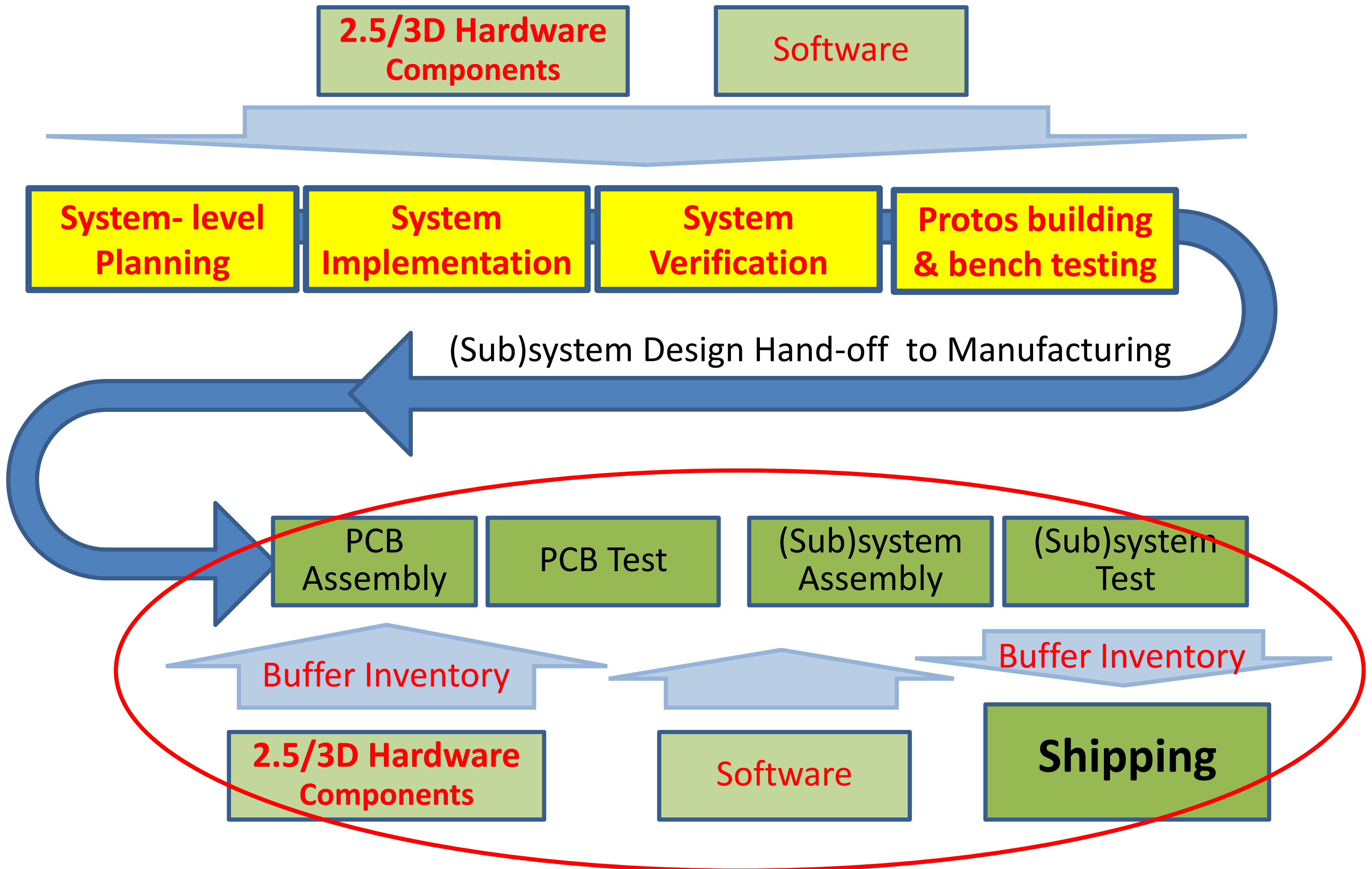
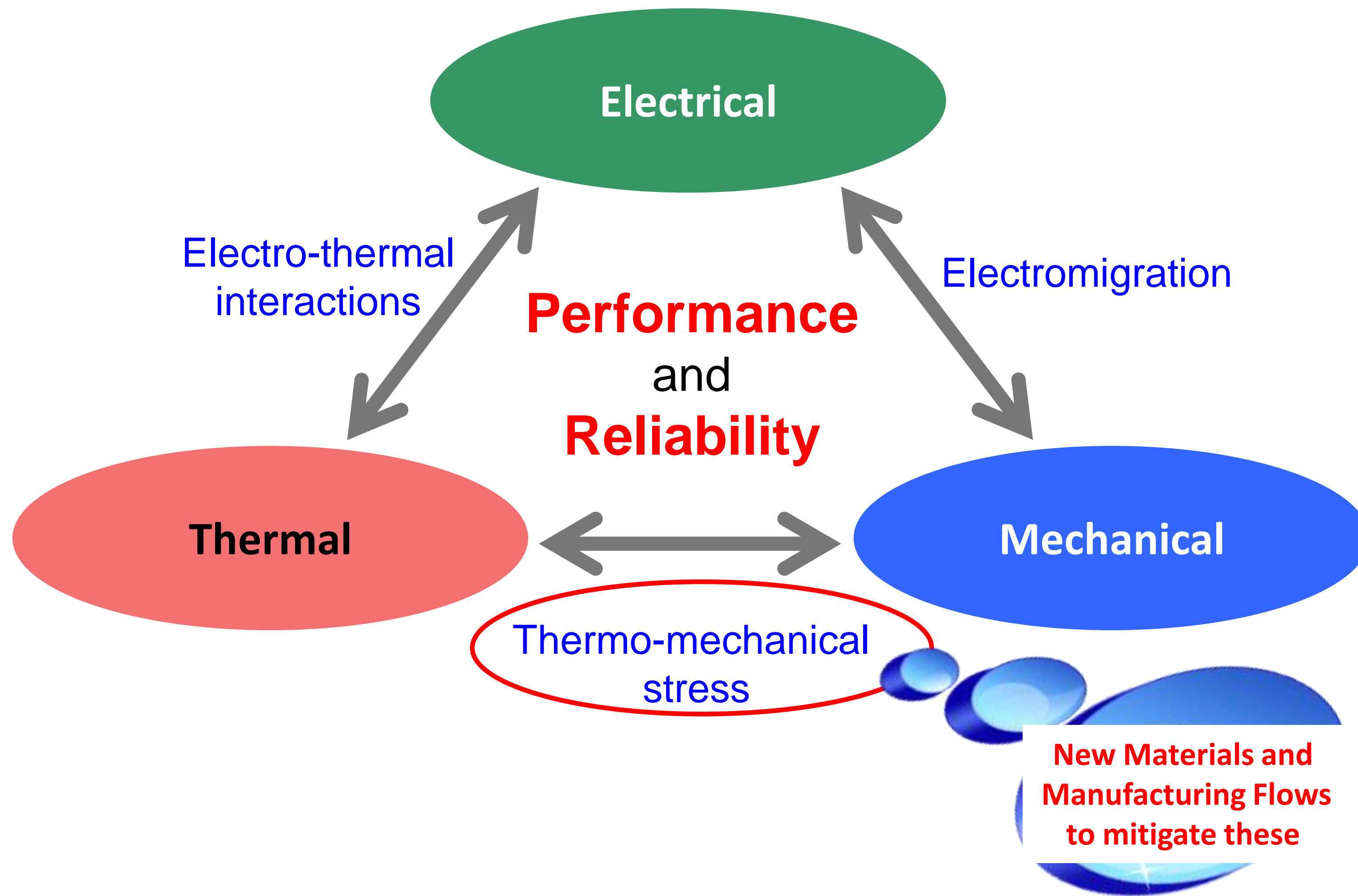
Systems: Protos to Production



eda 2 asic 3D Integration – Impact on System



Ref.: A. Wilde, P. Schneider, P. Ramm, DTC 2010

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3D/TSV Manufacturing Challenges

Wafer manufacturing

- TSV Etching
- TSV Insulating
- TSV Filling (Cu or ..)
- Thermal/mechanical stress
- Via first/middle/last
- Wafer probing
- Size: 5 x 50 → 2 x 40 um

Wafer thinning

- Bonding
- Thinning, reveal
- RDL
- De-bonding
- Shipping/Handling

Stacking/Packaging/Test

- D2D / D2W / W2W
- Alignment Accuracy
- Micro-bumping
- Cu-Cu direct bonding
- Packaging
- Partial/final stack test

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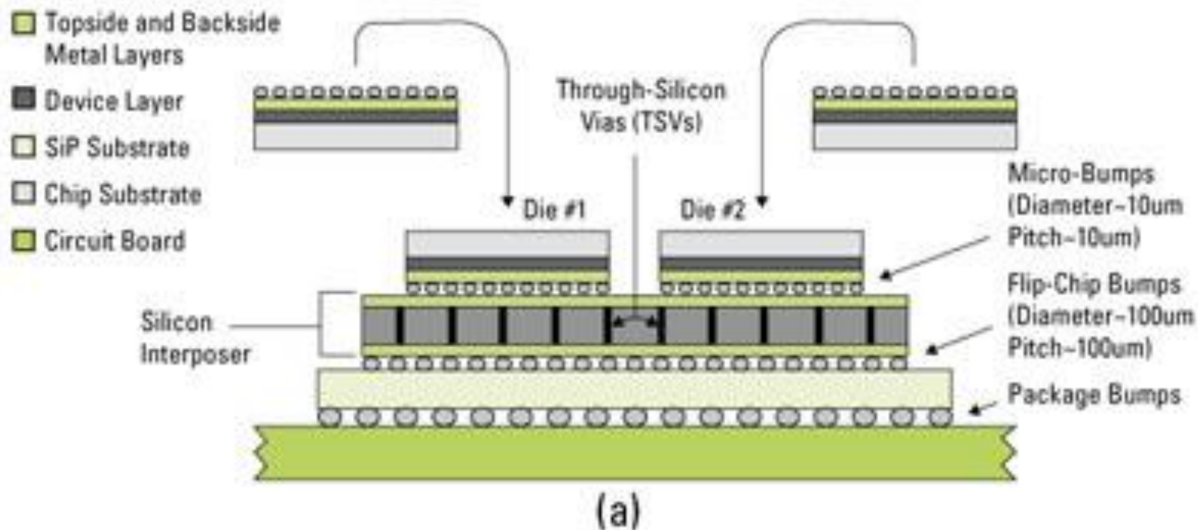
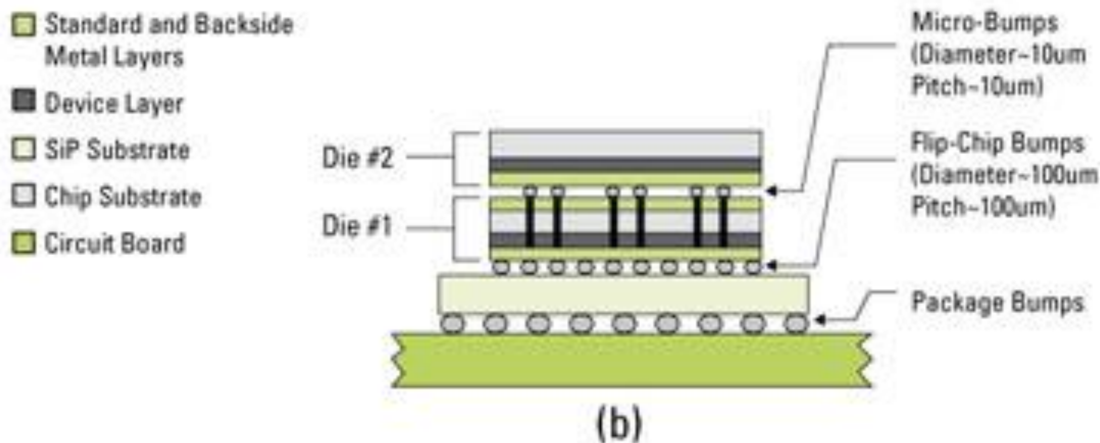
2.5/3D Testing





http://www.gsaglobal.org/forum/2012/1/articles_ge_capital_global.asp

P 1838 Working Group proposed 3D DFT strategy

ITRS works on test roadmap

Industry organizations driving further considerations:

- **Known-good-die**
- **Probe cards (40x50u)**
- **Passive interposer test**
- **Stack accessibility**
- **Mixed-signal test**
- **Stack-in-progress test**
- **Test program(s) generation**
- **Stack overheating @ test**
- **Yield / Redundancy**
- **Who tests (Fab / OSAT)**
- **Who pays for yield-loss…**

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Appendix: Market Data

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Top 10 Semiconductor Buyers

Table 1
Top 10 Semiconductor Design TAM by Company, Worldwide 2011, Preliminary (Millions of Dollars)

Rank 2010	Rank 2011	Company	2010	2011	Growth (%)	Share (%)
3	1	Apple	12,819	17,257	34.6	5.7
2	2	Samsung Electronics	15,272	16,681	9.2	5.5
1	3	HP	17,585	16,618	-5.5	5.5
5	4	Dell	10,497	9,792	-6.7	3.2
4	5	Nokia*	11,318	9,042	-20.1	3.0
6	6	Sony*	9,020	8,210	-9.0	2.7
7	7	Toshiba	7,768	7,589	-2.3	2.5
10	8	Lenovo	6,091	7,537	23.7	2.5
8	9	LG Electronics	6,738	6,645	-1.4	2.2
9	10	Panasonic	6,704	6,267	-6.5	2.1
		Others	195,552	196,413	0.4	65.0
		Total	**299,364**	**302,051**	**0.9**	**100.0**

TAM = total available market
Source: Gartner (January 2012)

http://www.zdnet.com/blog/btl/gartner-apple-jumped-to-top-semiconductor-company-in-2011/67849

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Top 25 Semiconductor Vendors in 2011

Worldwide Revenue Ranking for the Top-25 Semiconductor Suppliers in 2011
(Revenue in Millions of U.S. Dollars)

2010 Rank	2011 Rank	Company Name	2010 Revenue	2011 Revenue	Percent Change	Percent of Total	Cumulative Percent
1	1	Intel	40,394	48,721	20.6%	15.6%	15.6%
2	2	Samsung Electronics	28,380	28,563	0.6%	9.2%	24.8%
4	3	Texas Instruments	12,994	13,967	7.5%	4.5%	29.3%
3	4	Toshiba	13,010	12,729	-2.2%	4.1%	33.4%
5	5	Renesas Electronics Corporation	11,893	10,648	-10.5%	3.4%	36.8%
9	6	Qualcomm	7,204	10,198	41.6%	3.3%	40.1%
7	7	STMicroelectronics	10,346	9,735	-5.9%	3.1%	43.2%
6	8	Hynix	10,380	9,293	-10.5%	3.0%	46.2%
8	9	Micron Technology	8,876	7,365	-17.0%	2.4%	48.6%
10	10	Broadcom	6,682	7,160	7.2%	2.3%	50.9%
12	11	Advanced Micro Devices (AMD)	6,345	6,436	1.4%	2.1%	52.9%
13	12	Infineon Technologies	6,319	5,312	-15.9%	1.7%	54.6%
14	13	Sony	5,224	5,015	-4.0%	1.6%	56.3%
16	14	Freescale Semiconductor	4,357	4,408	1.2%	1.4%	57.7%
11	15	Elpida Memory	6,446	3,887	-39.7%	1.2%	58.9%
17	16	NXP	4,028	3,831	-4.9%	1.2%	60.1%
20	17	nVidia	3,196	3,608	12.9%	1.2%	61.3%
26	18	ON Semiconductor	2,291	3,428	49.6%	1.1%	62.4%
18	19	Marvell Technology Group	3,606	3,393	-5.9%	1.1%	63.5%
15	20	Panasonic Corporation	4,946	3,390	-31.5%	1.1%	64.6%
21	21	ROHM Semiconductor	3,118	3,187	2.2%	1.0%	65.6%
19	22	MediaTek	3,553	2,952	-16.9%	0.9%	66.6%
28	23	Nichia	2,190	2,936	34.1%	0.9%	67.5%
22	24	Analog Devices	2,862	2,846	-0.6%	0.9%	68.4%
23	25	Fujitsu Semiconductor Limited	2,757	2,742	-0.5%	0.9%	69.3%
		All Others	96,073	95,610	-0.5%	30.7%	
		Total Semiconductor	307,470	311,360	1.3%	100.0%	

Source: IHS iSuppli March 2012

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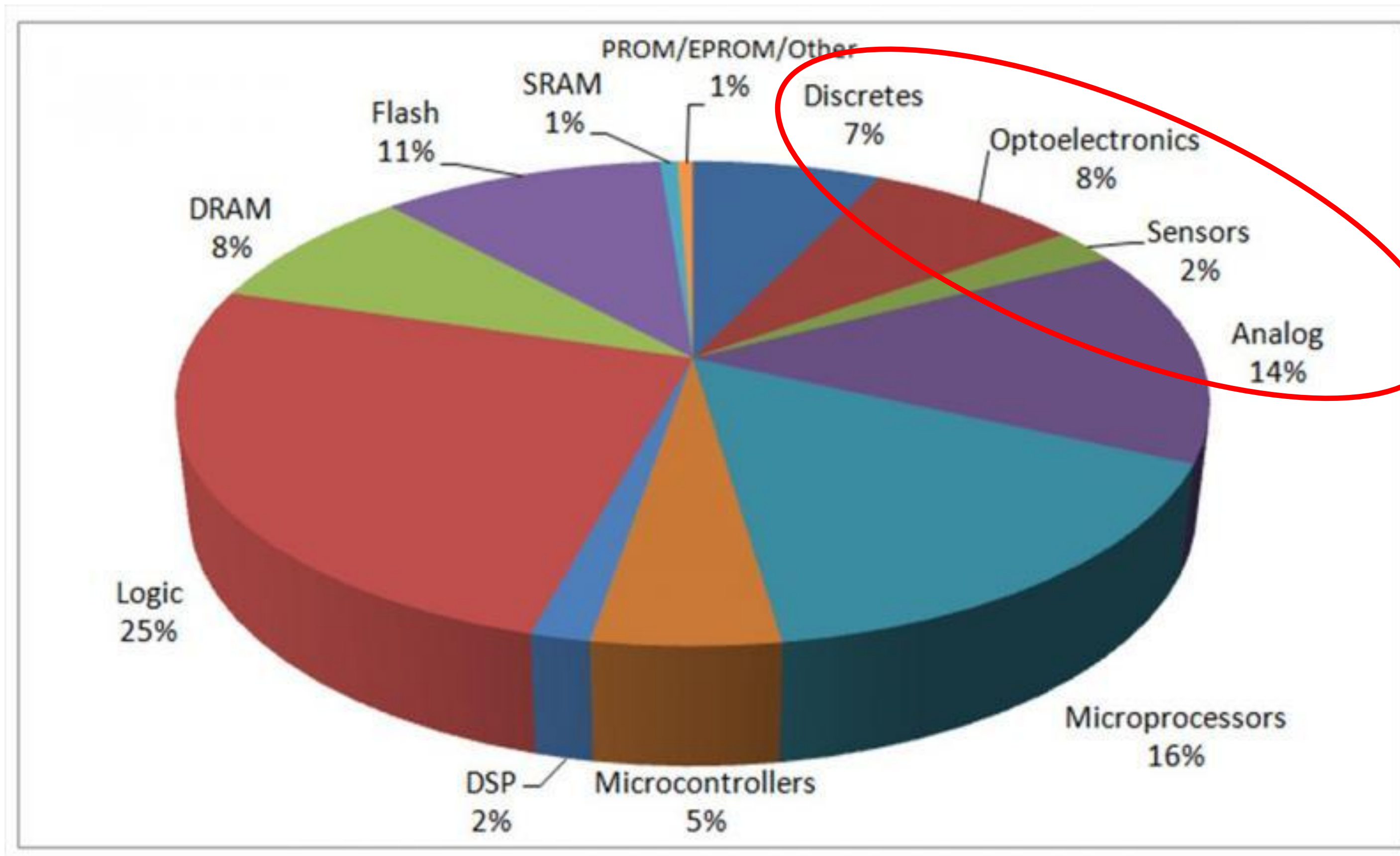
2012 Revenue Shares



Databeans Estimates, Febr 2012

http://www.ems007.com/pages/zone.cgi?artcatid=0&a=81742&artid=81742&pg=2

eda2asic Semiconductor Equipment Suppliers

2011 Rank	AOW	COMPANY	2009	2010	2011	11/'10 Growth
1	EU	ASML	2267.9	5973.1	7877.1	*32%*
2	NA	Applied Materials+	3507.9	7284.0	7437.8	*2%*
3	JA	Tokyo Electron	2323.7	5261.3	6203.3	*18%*
4	NA	KLA-Tencor	1316.1	2431.7	3106.2	*28%*
5	NA	Lam Research	1198.0	3004.6	2804.1	*-7%*
6	JA	Dainippon Screen Mfg. Co.	887.1	1727.3	2104.9	*22%*
7	JA	Nikon Corporation	1342.3	1517.3	1645.5	*8%*
8	JA	Advantest++	430.0	1134.2	1446.7	*28%*
9	EU	ASM International	693.9	1416.3	1443.0	*2%*
10	NA	Novellus Systems	581.9	1316.7	1318.7	*0%*
11	JA	Hitachi High-Technologies	474.4	910.5	1138.7	*25%*
12	NA	Teradyne	552.4	1406.5	1106.2	*-21%*
13	NA	Varian Semiconductor Equipment+++	395.9	971.8	1096.3	*13%*
14	JA	Hitachi Kokusai Electric	212.8	626.4	838.4	*34%*
15	NA	Kulicke & Soffa	262.4	745.9	780.9	*5%*
Total Top 15			**16446.7**	**35727.8**	**40347.7**	
y-o-y growth				*117%*	*13%*	

Worldwide Sales in $ M, equipment and services http://semimd.com/blog/tag/vlsi-research/

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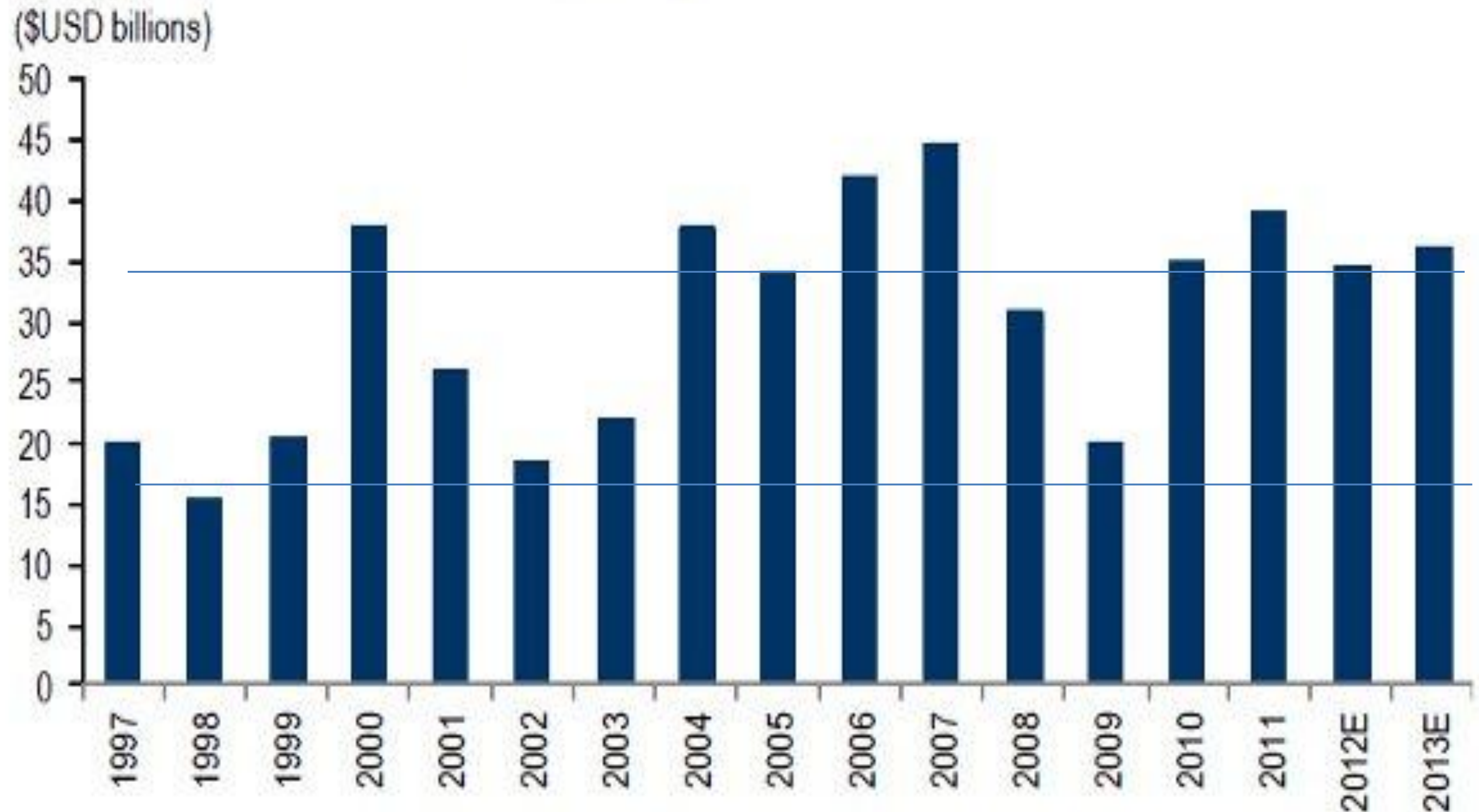
Semiconductor Capex



http://semimd.com/blog/tag/vlsi-research/

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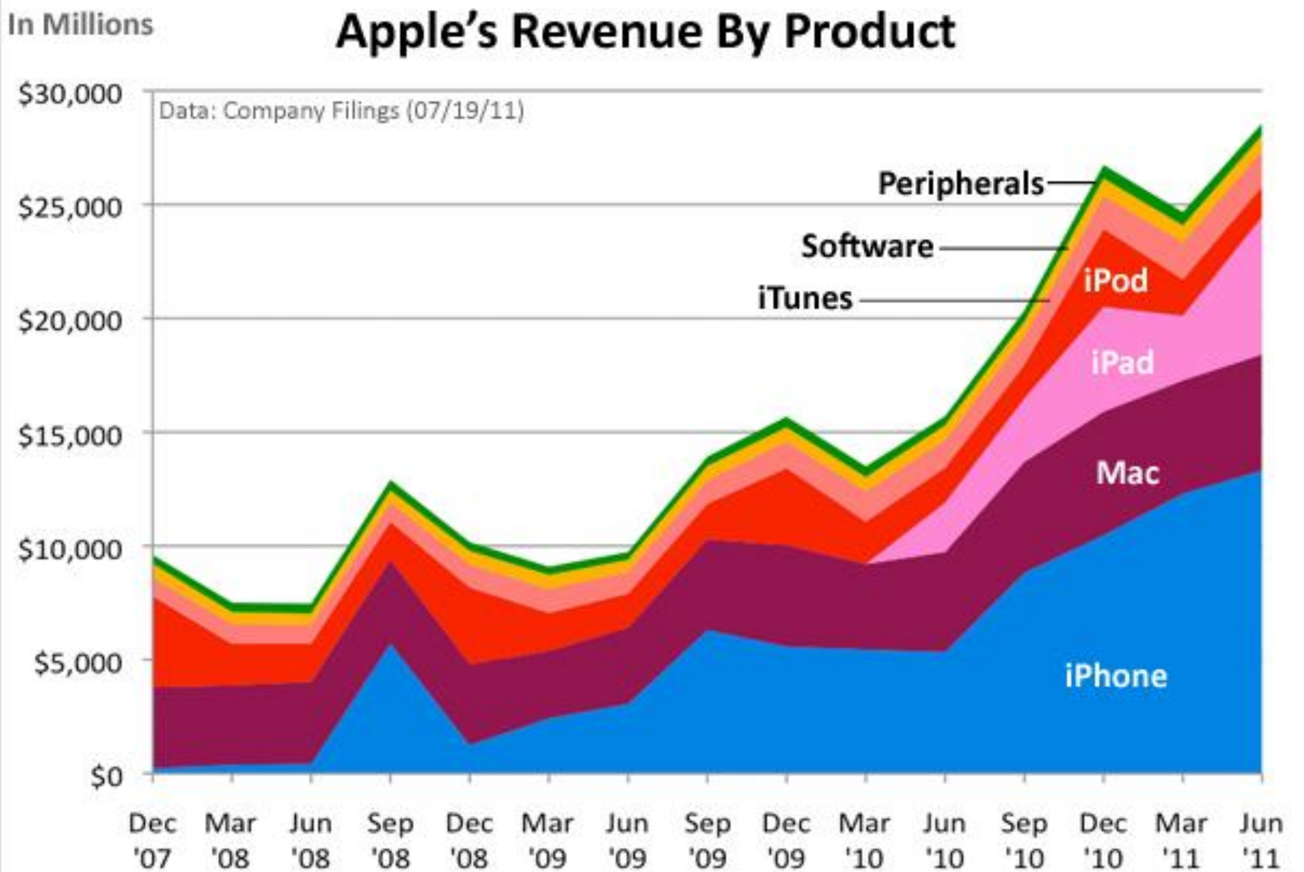
Major Foundries

2011 Rank	2010 Rank	Company	Foundry Type	Location	2010 Sales ($M)	2011 Sales ($M)	11/10 Change (%)
1	1	TSMC	Pure-Play	Taiwan	13,307	14,600	10%
2	2	UMC	Pure-Play	Taiwan	3,965	3,760	-5%
3	3	GlobalFoundries	Pure-Play	U.S.	3,510	3,580	2%
4	5	Samsung	IDM	South Korea	1,205	1,975	64%
5	4	SMIC	Pure-Play	China	1,555	1,315	-15%
6	6	TowerJazz	Pure-Play	Israel	509	610	20%
7	7	Vanguard	Pure-Play	Taiwan	508	519	2%
8	8	Dongbu	Pure-Play	South Korea	475	500	5%
9	9	IBM	IDM	U.S.	430	445	3%
10	10	MagnaChip	IDM	South Korea	405	350	-14%
11	12	SSMC	Pure-Play	Singapore	330	345	5%
12	11	Hua Hong NEC*	Pure-Play	China	367	335	-9%
13	16	WIN	Pure-Play	Taiwan	221	300	36%
14	13	X-Fab	Pure-Play	Europe	317	285	-10%

IC Insights 2011, referenced in (ESNUG 503 Item 6) by John Cooley [05/04/12]



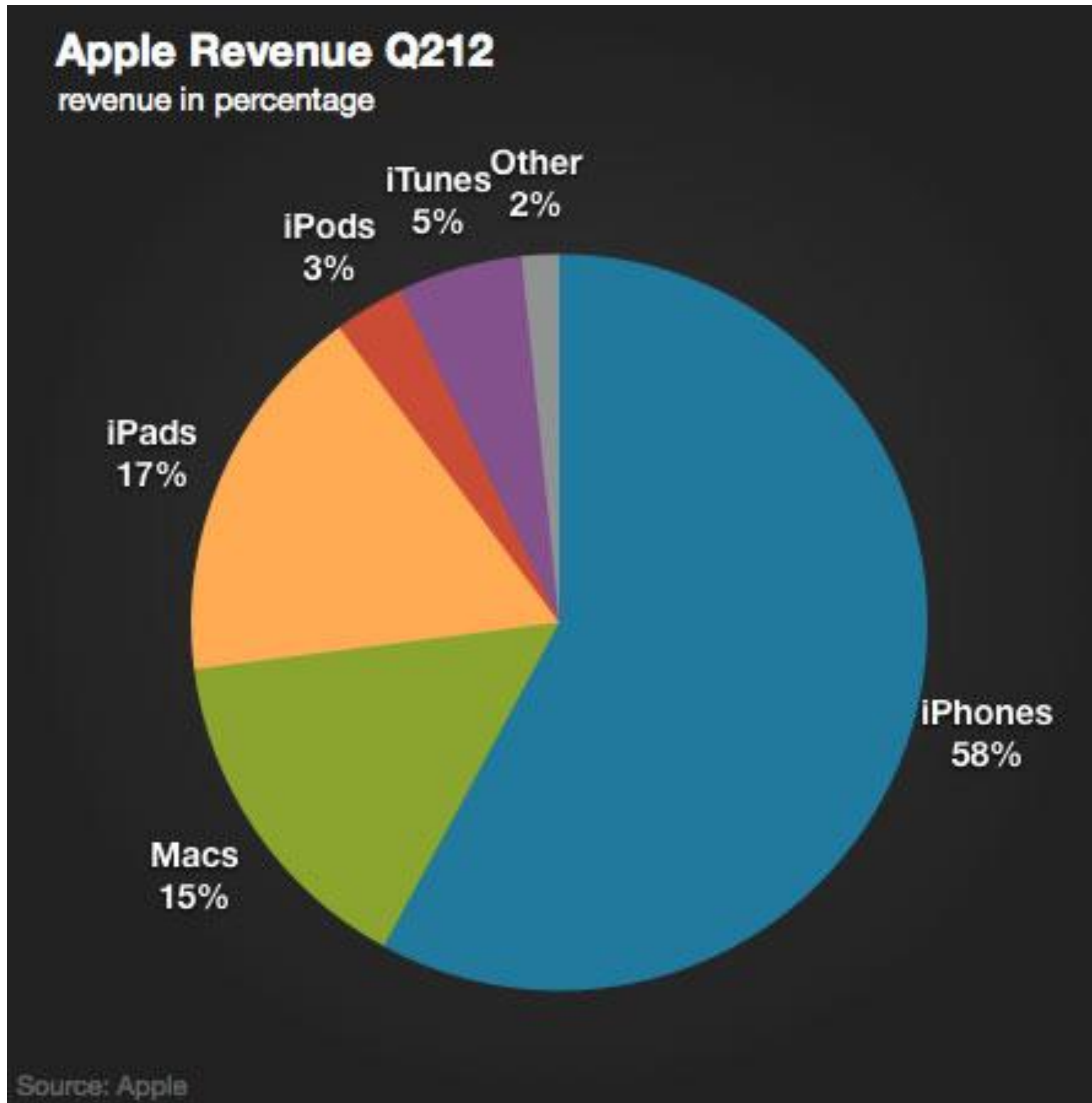
Apple Delivers A Massive Blow Out Thanks To Huge iPhone And iPad Sales

Jay Yarow | Jul. 19, 2011

Apple's earnings are out and it's another monster quarter for the company as iPhone and iPad sales blew away estimates.
It earned $7.31 billion in net profit on revenue of $28.57 billion for the June quarter. Both are records for Apple.
iPad shipments: **9.25 M#/Q**

http://www.businessinsider.com/apple-earnings-june-quarter-2011-7#ixzz1TEhyOPbg

Wedbush Securities are estimating that some **one million iPad 2s sold over the first weekend**



http://arstechnica.com/civis/viewtopic.php?p=22817348

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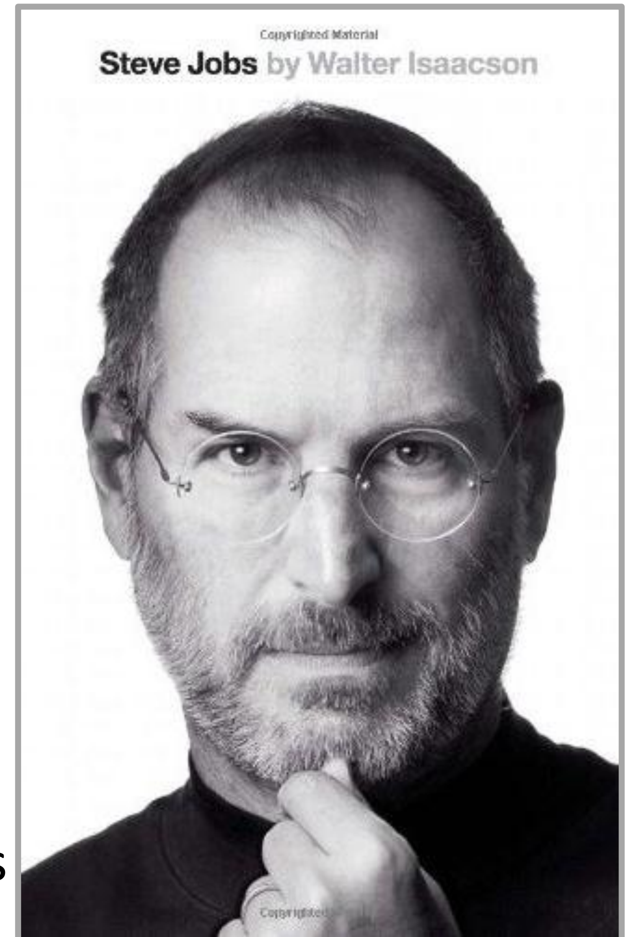
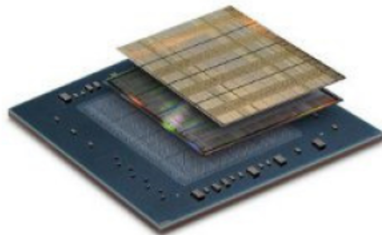
Real Leadership Lessons of Steve Jobs

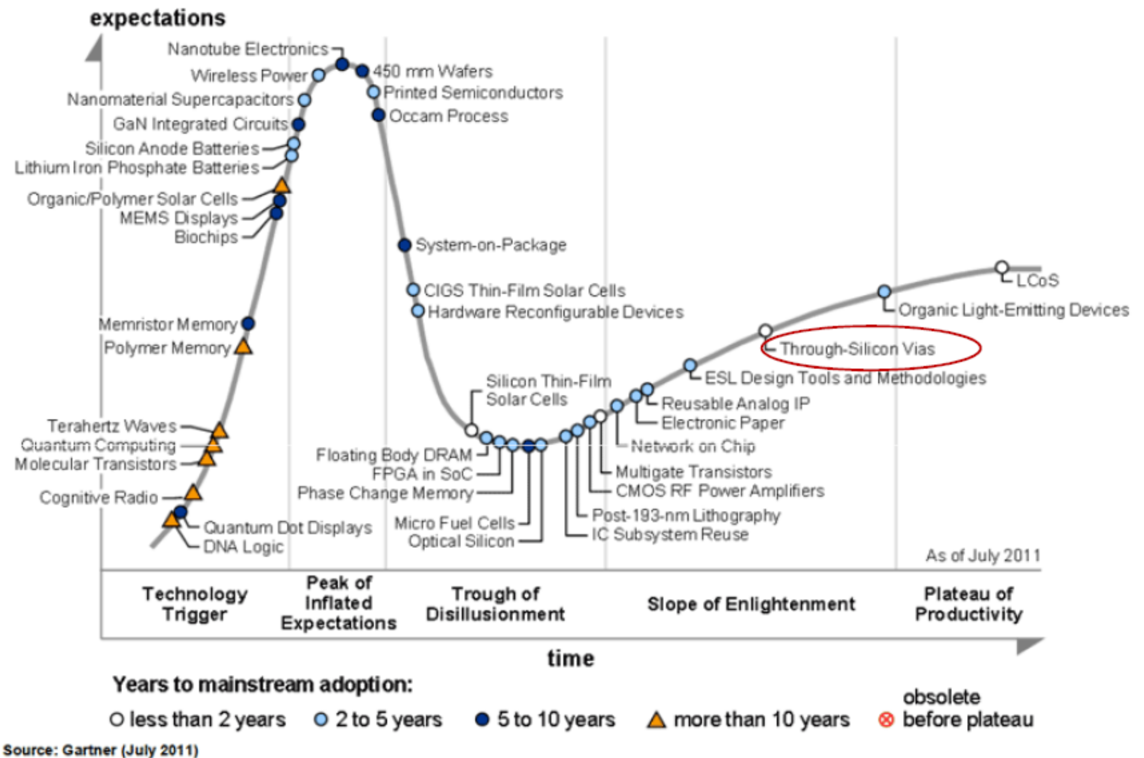
- ✓ Focus
- ✓ Simplify
- ✓ Take responsibility end to end
- ✓ When behind, leapfrog
- ✓ Put products before profits
- ✓ Don’t be a slave to focus groups
- ✓ Bend reality
- ✓ Impute
- ✓ Push for perfection
- ✓ Tolerate only “A” players
- ✓ Engage face-to-face
- ✓ Know both the big picture and the details
- ✓ Combine the humanities with the sciences
- ✓ Stay hungry, stay foolish



http://hbr.org/2012/04/the-real-leadership-lessons-of-steve-jobs/ar/1

2.5D / 3D Stackin' : Everybody is Doin' It





Now on the 'Slope of Enlightenment' !!

QUALCOMM CDMA Technologies