MEPTEC semi

THE GREAT MINIATURIZATION: SYSTEMS AND PACKAGING

Technology Enabling Systems in your Pocket and Beyond

NOVEMBER 10 & 11, 2015 • SANTA CLARA, CA USA

Tuesday, November 10

Session 1: The Genius of Cars – and why Semiconductors Matter
Session Chair: TBD

The automobile industry is experiencing rapid change, mostly due to the rate at which technology is changing personal transportation every year. Cars are becoming highly computerized systems, with many automakers now showcasing concept cars sporting very advanced features. Some of these technologies are still far from mainstream but others are quickly finding their place in showrooms as consumer awareness and demand grows. Sophisticated features, such as autonomous vehicle systems, driver override systems, biometric vehicle access systems, and many more, will heavily rely on the semiconductor industry to help make them reality. This session will explore the automotive semiconductor landscape, delve into emerging application trends, then examine the semiconductor technologies being developed to help bring these to market while meeting increasingly stringent safety, reliability and energy efficiency requirements.

Session 2: High Speed Components and Packaging
Session Leader: Li Li, Cisco

This session will cover components, modules and novel packaging technology solutions for high-frequency, high-speed wired and wireless applications, as well as emerging packaging technologies including embedded/integrated chips & passives, sensors, RFID, and RF MEMS. We will also address package design and development for RF, millimeter-wave & THz applications, and wearable, flexible & printed electronics, SiP, heterogeneous integration for communication applications.

Session 3: Medical and Wearables for Human Health: Connecting the Dots from Silicon through Packaging
Session Leader: Sesh Ramaswami, Applied Materials

Enhancing human health and quality of life has been and will increasingly become a highly valued societal aspiration. This aspiration will be enabled by technology driven products that drive advances in design, silicon processing, novel materials, imaging, sensing and application specific packaging technologies. This session focuses on the market and application spectrum of this continuum and is designed to cover ideas and products ranging from ingestible capsules, implantable devices, analytical equipment for assays and wearable systems for monitoring or augmenting human body function.

Session 4: Power Management and Energy Harvesting: Opposite sides of the Same Coin Battery?
Session Chair: Paul Werbaneth, Invetac

Fully depleted silicon-on-insulator (FD SOI) technologies are making noise these days in the semiconductor industry as a result of their advantages in the faster speed / lower power consumption race. ST Microelectronics, for example, has chosen FD-SOI over FinFETs as a result of FD SOI's ability to cut gate leakage (and thereby power consumption) to a minimum. And, somewhere in the near future, there will be a convergence of low-power devices and energy harvesters in sensors reporting from potentially anything that moves or vibrates. Are power management and energy harvesting opposite sides of the same coin? Are they pulling on the same oar? Speakers in this session and Energy examine both sides of the coin to understand how the industry will extend itself to the network's very edge, where the IoT lives, reporting to the cloud.

Wednesday, November 11

Session 5: Multi Die Integration
Session Chair: Ivor Barber, Xilinx

Multi Die Integration is coming of age as a strategy for system integration enabled by a plethora of maturing technologies such as POP, chip scale, wafer level packaging, 2.5 & 3D Die stacking, integrated CAD tools and continued substrate innovation.

Motives include performance – putting components in close physical proximity – system miniaturization, and integrating disparate solutions such as non-scaling linear, power or opto components or commodity memory stacks with a microprocessor, ASIC or FPGA in the latest logic node.

As the need for "Fogging" (distributed computing at the edge of the Network) increases, so will the need for Multi Die Integration in relatively low cost environments such as autonomous vehicles, smart homes and medical implants.

The session will showcase technologies and highlight challenges in the development of cost effective Multi Die Integration solutions for these emerging applications.

Session 6: On the Road to SiP and Modules
Session Leader: William Chen, ASE

The IoT era is taking shape with a plethora of products now hitting the market, from wearables to health, automotive to industrial, and many more on the horizon, each with its own unique application space, value proposition and price point. With emphasis on function, performance, efficiency, and fashion, these emerging products are poised to create huge impact across the broad spectrum of global lifestyle. Both electronics and IC Packaging are playing key roles, and the industry is developing technologies to address requirements to enable and optimize the functionality of semiconductor devices. System-in-Package (SiP), modules, and heterogeneous integration technologies continue to play a vital role in bringing products from conception to market.

This session will address the core technologies, ecosystem collaborations, and volume manufacturing requirements for SiP and modules, which form the building blocks for IoT. SiP and modules both call for highly miniaturized device integration that breaks new frontiers in performance and efficiency. We'll look at the opportunities and challenges. We'll also discuss the technical innovation in SiP and heterogeneous integration that is helping our industry deliver so global societies can all ultimately realize the IoT era.

Session 7: IC-Package-System Co-Development in the New SIP Era
Session Chair: John Xie, Altera

With silicon scaling running into increased road blocks, the SoC preference has gradually been moving towards SIP to integrate the needed feature and IP within the time and cost budget. This eventually becomes a sub-system level product instead of traditional simple SoC as simple component. It requires more complete and holistic planning and consideration of IC-PKG co-design and extended into system level design as well. This also calls for advancing the IC-PKG-System co-design to co-development and to co-architecting. This is an exciting new trend in microelectronic design field as well as new opportunities for designers of all disciplines, fabless companies, EDA tool vendors and system houses.

Session 8: Wrap-Up Panel Discussion -- The Great Consolidation
Session Chair: Paul Werbaneth, Invetac

The big Silicon Valley story of 2015, one that gained strength and momentum as the year progressed, is consolidation. Be it on the device maker-side, the OSAT-side, the capital equipment supplier-side, or the end customer-side, consolidation has its benefits, primarily in achieving ever greater business efficiencies, but consolidation also has its costs, hidden or otherwise. The panelists will discuss, with active audience participation, the merits and drawbacks of the consolidation spree as they see it, and will consider how consolidation will affect our industry's ability to embrace the challenges presented by the new era of mobile miniaturization.