MEPTEC report
Volume 10, Number 1
QUARTER ONE 2006

A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Dr. Marcos Karnezos has joined the advisoy board of **SunSil Inc.** *page 14*

Palomar Technologies has announced that Bruce W. Hueners has been named company president. *page 14*

Indium Corporation (Suzhou) Co., LTD recently passed its ISO-9001:2000 certification audit. The Suzhou facility joins the company's U.S., European, and Asia-Pacific Operations in achieving certification. *page 15*

DELPHON

Delphon Industries has announced its acquisition of **TouchMark, Inc.** of Hayward, CA. Delphon operates **Gel-Pak**, also of Hayward, and **Quik-Pak** of San Diego under its corporate umbrella. *page 15*

FlipChip International LLC announced that it has started construction of an advanced bumping facility for a new joint venture in China with **Millennium Microtech**. *page 16*

ASM International N.V. has announced that it has sold the world's first 300 mm epitaxial reactor into mainland China. The system was ordered by the **General Research Institute for Nonferrous Metals** (GRINM). *page 17*

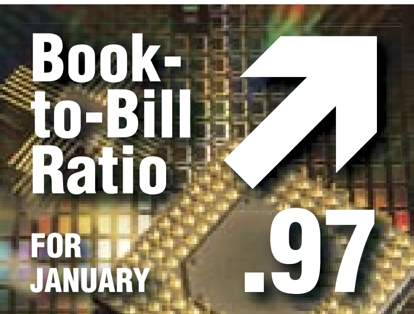
ECTC 2006, the 56th Electronic Components and Technology Conference, will be held May 30 - June 2 at the Sheraton San Diego Hotel & Marina in San Diego, California. *page 31*

MEMBER COMPANY PROFILE

Dummy Packages are used in a variety of applications involving evaluation and calibration of handlers and equipment used in board level assembly, such as pick and place machines and soldering ovens. TopLine has a library of 100 different Lead-Free PCB Cards for mounting Dummy Packages.

TopLine was originally formed in 1989 as a division of National Electronics Corporation, a specialty distributor of electronic components. In 2001 Martin Hart, along with a financial partner, purchased the assets of TopLine from National Electronics and re-incorporated as TopLine Corporation. After its fresh start, Hart expanded TopLine's product range to be a one-stop shop for dummy packages and test PCB boards. In 2004, TopLine built a BGA ball attach pilot line facility in New Mexico giving customers quick-turn on a low volume-high mix assortment of Ball Grid Array packages. *page 22*

Semiconductor equipment bookings increase 27% over January 2005 level. *page 20*



consistent results

Honeywell Wafer Thinning Products — provide unsurpassed consistency and uniformity from batch to batch, improving yield. Thanks to our world-class technologies and production techniques, Honeywell can provide consistent performance and unsurpassed etch uniformity meeting our global customer needs. And as an industry leader in both Research & Development and customer support, our growth strategies are uniquely aligned with yours. Our worldwide, $26B organization brings forward a significant technology heritage, a recognized reputation for high quality standards, and an uncanny ability to respond to new opportunities. It's all about helping you consistently make great products with a partner you can count on.

Honeywell

Count on consistency. Get White Papers and other information by visiting **www.honeywell.com/waferthin** Or call **1-408-962-2000.**

© 2005 Honeywell International Inc. All rights reserved.

MEPTEC report

Volume 10, Number 1
A Publication of
The MicroElectronics Packaging
& Test Engineering Council

801 W. El Camino Real, No. 258
Mountain View, CA 94040

Tel: (650) 988-7125
Email: info@meptec.org

Published By
MEPCOM

Editor
Bette Cooper

Design and Production
Gary Brown

Sales and Marketing
Kim Barber

Contributing Editor
Jody Mahaffey

MEPTEC Advisory Board

Seth Alavi
SunSil

Jeffrey Braden
Braden & Associates

Philippe Briot
P. Briot & Associates

Joel Camarda
Sipex Corporation

Gary Catlin
Plexus

Tom Clifford
Lockheed-Martin

Rob Cole
MiTech USA

John Crane
J. H. Crane & Associates

Jeffrey C. Demmin
Tessera

Bruce Euzent
Altera Corporation

Skip Fehr

Julia Goldstein
Advanced Packaging Magazine

Chip Greely
Qualcomm

Anna Gualtieri
Elle Technology

Bance Hom
Consultech International, Inc.

Ron Jones
N-Able Group International

Pat Kennedy
Gel-Pak

Nick Leonardi
CMC Interconnect Technologies

Abhay Maheshwari
Xilinx

Phil Marcoux
SensArray

Bhavesh Muni
Henkel Corporation

Mary Olsson
Gartner Dataquest

Marc Papageorge
Semiconductor Outsourcing Solutions

Jerry Secrest
Secrest Research

Jim Walker
Gartner Dataquest

Russ Winslow
Six Sigma

MEPTEC Report Vol. 10, No. 1. Published quarterly by MEPCOM, 801 W. El Camino Real, No. 258, Mountain View, CA 94040. Copyright 2006 by MEPTEC/MEPCOM. All rights reserved. Materials may not be reproduced in whole or in part without written permission.

MEPTEC Report is sent without charge to members of MEPTEC. For non-members, yearly subscriptions are available for $75 in the United States, $80US in Canada and Mexico, and $95US elsewhere.

For advertising rates and information contact Kim Barber, Sales & Marketing at (408) 309-3900, Fax (650) 962-8684.

Council Update

Welcome to the first issue of 2006! It was another good year for MEPTEC. Our membership continues to grow, and our popular quarterly symposiums and monthly luncheons are seeing increased attendance with each passing event. We had a cumulative attendance of over 2,000 at our various events in 2005. We've made some changes in our Advisory Board, and are adding some new activities and programs in 2006. One of the new activities that we are considering is bringing our MEPTEC programs to Europe. We will be holding an introductory meeting at Semicon Europa in Europe on April 5. If you are attending the event and would be interested in attending the meeting, please contact MEPTEC at bcooper@meptec.org or call 650-988-7125.

As mentioned above, there are some changes in the Advisory Board. Outgoing Board members include **Mark DiOrio** of **MTB Solutions**, **Ray Petit** of **Pacific Rim International**, and **Doug Pecchenino**. We'd like to thank them for their years and service and support to MEPTEC. Also, **Phil Marcoux** of **SensArray** has stepped down as Executive Director. Phil's job responsibilities at SensArray have made it difficult for him to continue with the level of participation needed to remain as Director. He will remain on the Board as a general member. We'd like to take this chance to thank Phil for his past service, and appreciate his continued support.

We're pleased to announce several new Advisory Board members including **Jeff Braden** of **Braden Associates**, **Philippe Briot** of **Briot & Associates** in Belgium (heading up the European initiative), and **Tom Clifford** of **Lockheed Martin**. Their bios appear on page 4. We'll be introducing more new members in next quarter's issue.

Our next event will be held on Wednesday and Thursday, May 17 -18, 2006 at the Hyatt San Jose hotel in San Jose, California: the 4th Annual MEMS Packaging symposium called *"MEMS Packaging Trends: From Production to Market – Large Volume Drivers for MEMS Technologies"*. The program has been expanded to two days, including a special Academic Workshop and a half-day workshop on MEMS packaging standards sponsored by SEMI. See page 5 for information on this exciting event, or visit our website at www.meptec.org.

For a review of our February 2006 symposium, the *"2nd Annual The Heat is On: Thermal Management Solutions in Semiconductor Packaging"*, see page 6 for **Jody Mahaffey**'s article wherein she interviews participants and summarizes the event. It was a very successful event, with more than 250 attendees. We will be holding a *3rd Annual Thermal Management* event in February 2007; we'll keep you posted as that develops.

One of the feature articles this issue is contributed by **Allan Calamonieri**, VP of Test Business Development at **Carsem**, a long time Corporate member of MEPTEC, on *"Strip Test – Panacea or Pariah?"* He takes a detailed look at this method for handling micro-packages. Allan also presented this topic at both our Sunnyvale and Phoenix luncheons in March; we'd like to thank him and all at Carsem for their continued support. See page 26 for this informative piece.

This was a timely presentation for us since at our annual MEPTEC Advisory Board meeting, Board member **Jerry Secrest** brought up the need for more MEPTEC Test related programs. After some internal discussion and conversations with others interested in test, MEPTEC kicked off its **Semiconductor Test Committee** on April 8 in Sunnyvale following the Carsem presentation. If you're interested in getting involved in this committee, please contact MEPTEC. You'll be hearing more about this initiative in future issues and email communications.

Our other feature article is from **Suss MicroTec, Inc.** and **IBM**, co-written by **Emmett Hughlett**, **Eric Laine**, **Klaus Ruhmer**, and **Dietrich Toennies** of **Suss**, and **Peter Gruber** of **IBM Microelectronics**. It introduces a new solder bumping technology called C4NP (C4-New Process) which was developed by IBM and commercialized by Suss MicroTec. (see page 29) It describes in detail this new way of bumping wafers, and describes advantages and challenges associated with the technology. We'd like to thank Eric Laine for presenting this new technology to MEPTEC members at our January luncheons in both Sunnyvale and Phoenix.

Check out page 32 for **Henkel**'s Technitorial on *"Material Sets Deliver Tested, Reliable Compatibility and Significant Cost Reductions"*, by **Michael Todd, PhD** of **Henke's Electronics Group**.

Our Editorial this issue is contributed by **Dan Neinhauser**, Director of MacroTechnology Works

Issue Highlights

MEPTEC Events Follow-up **6**

Industry Analysis **10**

University News **11**

Industry News **14**

Member Company Profile **22**

Feature Articles

- *Strip Test – Panacea or Pariah? A detailed look at this method for handling micro-packages* **26**
- *C4NP – A New Solder Bumping Technology* **29**

Event Calendar **37**

Editorial **38**

at **Arizona State University**, on *"Industry and Academic Partnership"*. (see page 38) Dan starts out the piece by stating you might be asking yourself why an academic administrator is writing an editorial for MEPTEC. He does a good job of explaining why: to stress the importance of forging strong relationships between academia and industry. This will become even more important for MEPTEC over the next few months. We are pleased to be joining ASU in holding an exciting new event on packaging issues as they relate to medical electronics. Mark you calendars for Thursday, September 21 in Tempe, Arizona – specifically on the ASU campus. More details to follow soon.

Our Industry Analysis coverage this issue is contributed by **Morry Marshall** of **Semico Research Corporation**. We like his optimism; it is obvious in his article titled *"Don't Believe the Flat-Liners, Semiconductor Prospects are Bright"*. He begins his article by stating that Semico forecasts annual growth rates above 17% in 2006 and 2007. He makes a good point by wondering how anyone familiar with the semiconductor industry believes that there will be no major new semiconductor end-use markets, and brings it home by pointing out that no one really understood the potential for PCs when the first microcomputer kits were introduced. See page 10 for this interesting and positive article.

Our Member Company Profile this issue is on MEPTEC supporter and Corporate member, **TopLine**. This is a very interesting look at a company that has a "funny" sounding product – dummy packages. **Martin Hart**, president of TopLine, states that he often encounters "blank stares and even a few giggles" when he explains what he does for a living. However, it is no laughing matter when you realize what TopLine offers to the industry. There is a huge demand for TopLine's dummy packages, and the company is in an enviable position of opening 100 new customer accounts each month. See their story on page 22.

For our University profile this issue we take a look at **Santa Clara University**'s School of Engineering. Written by **Josh Nickel**, Assistant Professor at the Department of Electrical Engineer (and packaging industry veteran – you may recognize his name as formerly associated with some MEPTEC member companies), the article highlights SCU's Center for Nanostructures. One of the Center's most exciting projects involves nano-sensors for biological applications. See page 11 for this report.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

MEPTEC Welcomes New Advisory Board Members

Jeff Braden, President
Braden Associates

Jeff Braden is currently president of Braden Associates, a consulting firm specializing in operations, business and product line strategy, technology and manufacturing for the semiconductor packaging, assembly and test industry.

Jeff's 30 year career includes extensive experience in sales & marketing, product development and manufacturing, primarily in the Out Sourced Assembly & Test and packaging materials segments of the semiconductor industry, where he was most recently the North American President of Signetics High Technology. Prior to Signetics, Jeff was VP of Strategic Operations at STATSChipPAC, where he led the successful operational merger integration of ChipPAC and STATS in 2004, after five years as VP of Product Line Management at ChipPAC. In his product line role, Braden was instrumental in leading key business initiatives and driving growth at ChipPAC with very successful product line and market strategies, negotiating several long-term customer agreements, driving cost reduction and improved operational metrics, and building strong customer focused teams. Earlier career roles included general manager of Olin's Interconnect Technology business and several positions at Indy Electronics.

Jeff has fourteen issued patents and has contributed numerous published technical articles and presentations at industry conferences, and is a past chairman of the SEMI packaging standards committee and the JEDEC JC11.10 and 11.11 package standards sub-committees. Braden holds an Electrical Engineering degree from Mississippi State University, and graduated from the Executive Business Management program at the University of Michigan.

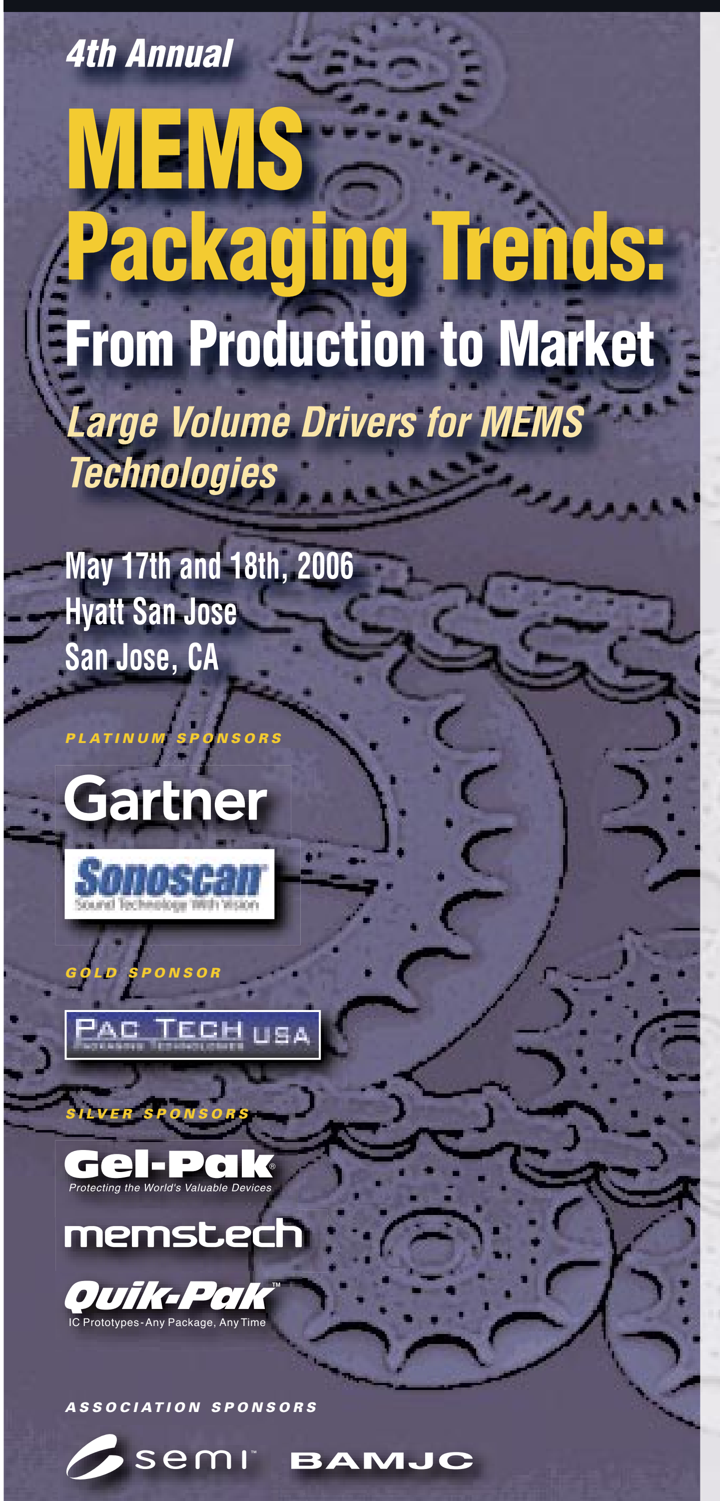
Philippe Briot, Director
P. Briot & Associates

With 16 years of experience in the electronics industry, Philippe is a specialist in component technologies, semiconductor auditing, parts qualification, system engineering and was primarily responsible for the phase 2 of the Plastic Component Program at Thales Group (ex Thomson-CSF). During his six years at Thales, his studies included long-term reliability and moisture sensitivity issues. There, he initiated the corporate technical audit procedures for assembly and test lines and drove the introduction of commercial components in rugged environment applications. He spent five years at PSA Peugeot Citroën, France, and held the position of Quality Assurance Manager with responsibility for component technologies and automotive electronic systems. He managed the development and the production launch of a range of proprietary components currently mounted in most of PSA car production. He also held positions within the European Space Agency, Hewlett-Packard, and the Microwave Research Lab of UCL. He is a founding member of the PURE association, he was a member of the Board of Directors of the Semiconductor Assembly Council and a member of the Technical Committee of the Automotive Electronics Council.

Tom Clifford, Advanced Electronics Packaging Group Leader
Lockheed Martin Space Systems Company

Tom Clifford has a BS in Ch E, and has worked in plastics development, and aerospace electronics hardware industries, for the last 35 years. He supported ablative thrusters on Gemini at McDonnell, insulation materials for Shuttle booster motors at UTC, and worked in development / operations management at Monsanto and Raychem. His duties at Lockheed Martin / Sunnyvale include PWB and CCA out-source management, SMT process development and control, and (as advanced packaging group leader) advocacy for MEMS, BGAs, nano and other new technologies. Currently he is running major t-cycle and vibe-shock test programs on HDI products. He notes that when he started out, "advanced packaging" meant plastic soap bottles and shrink-wrap pallets. Now "advanced packaging" is much, much smaller, and even more challenging. ◆

A SPECIAL TWO-DAY TECHNICAL SYMPOSIUM & EXHIBITS



Micro-machines are no longer relegated to micro-markets. After many years of production in military and automotive applications, MEMS have begun to take off in new high-volume markets such as consumer electronics and wireless, and are predicted to experience rapid growth in these new areas. What new consumer markets will MEMS penetrate next? What are the market drivers that will spur the continued explosion of MEMS into new areas? And what novel applications are just over the horizon? The **4th Annual MEPTEC MEMS Packaging Symposium** will explore these recent developments and how they will impact the packaging industry as a whole.

Expanded to Two Days for 2006, including a Half-day Workshop on MEMS Packaging Standards sponsored by SEMI, and Special University Presentations.

In order for MEMS to continue to penetrate high-volume consumer markets, there is a pressing need to reduce MEMS packaging costs. Standardization is going to be critical in this effort, and **MEPTEC** is teaming with **SEMI** to assist them in developing a proposed set of MEMS packaging standards. With SEMI's global standardization process and a global infrastructure, and MEPTEC's packaging technical expertise through their membership, together they will form a successful team to further MEMS standardization.

University Presentations

The expansion of this event to a two day program will include a special program called **Academic Workshop Presentations**, where we specifically encourage academics/students to present their latest work. This will be a workshop format where ongoing work in various stages of completion will be disclosed, and will allow discussion of results between the students and the audience.

Special Keynote Speaker:

Dr. Albert Pisano
Professor and Chair
Department of Mechanical Engineering
University of California at Berkeley

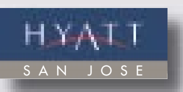
Wednesday, May 17 Sessions will include:

- Session 1: Advanced MEMS Packaging Trends and Market Overview
- Session 2: Enabling Technologies
- Session 3: Test Challenges for MEMS Applications
- Session 4: End User Applications/Future Trends

Thursday, May 18 Sessions will include:

- University Presentations
- Joint MEPTEC-SEMI Packaging Standards Workshop

EVENT LOCATION



Original image courtesy of Sandia National Laboratories

REGISTER ONLINE TODAY AT WWW.MEPTEC.ORG

MEDIA SPONSORS

2nd Annual

The Heat Is On:

Thermal Management Solutions in Semiconductor Packaging

Jody Mahaffey
JDM Resources

Relief From the Heat – Is It Possible? Thermal management issues continue to be a hot topic in the semiconductor industry. In fact, as new devices are developed that require faster circuits in smaller areas, the issues are becoming more and more critical. On February 16th, the MicroElectronics Packaging and Test Engineering Council (MEPTEC) once again brought together industry experts to discuss these thermal management issues at its 2nd Annual, *The Heat is On: Thermal Management Solutions in Semiconductor Packaging* symposium. We asked some of the speakers from the conference what types of issues they addressed in their presentations.

Many of the issues with thermal management are on-going problems that continue to be worked on at all levels of the supply chain. **Eric Tosaya** is Director of Packaging Engineering at **Advanced Micro Devices** and was the Technical Chairman for the MEPTEC symposium. He said that, "At this time, in the X86 microprocessor area, the challenges are basically the same today as they were a year ago. Even though we have made a transition to dual-core, which reduces the need for operating at maximum frequencies, you still have system thermal limitations (server, blade server, desktop, value desktop, mobile & value mobile) that are determined by the thermal density, even for a dual-core processor. Dual-core and future multi-core processors require better thermal sensing and control."

Another of these on-going areas of concern according to **Abu Eghan**, Principal Engineer at **Xilinx**, is thermal model delivery. "JEDEC has been working in this area to address a neutral file concept. It seems to me that this has been slow in coming. While this challenge has been identified and worked on, the longer it waits the more critical it becomes." Eghan presented in the *"System Level Challenges and Solutions"* session of the symposium.

As we found out from last year's presenters, there are many types of devices which require special thermal management solutions such as CPUs, GPUs, drivers, power converters and mass storage. Today there are new developments that may be causing even more problems. "In the DRAM application, the upcoming transition to Fully-Buffered DIMMs has added an additional chip with a power consumption of ~6W (AMB) to each DIMM, increasing the thermal challenges for the memory subsystem significantly," explains **Ulrich Hansen**, Director of Marketing for **Staktek** and speaker in the *"System Level Challenges and Solutions"* session of the symposium. "Increasing the airflow is not always possible without violating the applicable acoustics specifications."

Some people are wondering just how far future developments can go without addressing some of the thermal management issues first. **Van Carey**, Professor, Mechanical Engineering Dept. at **UC Berkeley** believes that while increasing chip heat flux levels has been a long standing issue, the expected heat flux levels of future chip designs are generating concerns about whether successful thermal management strategies are even possible at such levels. Carey presented in the *"Technology and Market Overview"* session of the symposium.

For this year's symposium, MEPTEC expanded its program to include thermal management issues relating to networking equipment. **Herman Chu**, Technical Leader, Cisco Router and Service Provider Technology Group at **Cisco Systems** says that the thermal issues for networking equipment are different from those of computing hardware as the overall board powers are similar but the heat concentration for each is different. Chu gave the keynote presentation at the conference and discussed *"Power Trends in Networking Electronics and Computing Systems"*.

Coming from the device side, Eghan sees it from a slightly different perspective explaining that, "Thermal issues for networking may seem different on the surface, but the basic issues remain pretty much the same as those in the computing market. While the environment and the long term reliability may dictate choices, the bottom line is to seek a good heat transfer coefficient in both cases. From the component stand point, the deliverable to both is similar – we give the system designers an efficient die, software tools to constrain them in power consumption, and provide the models and other tools that allow them to select the solution that is appropriate for their environment."

From past experience Tosaya believes that the real difference exists in the greater density of devices and the larger size of the network equipment versus a multiprocessor server product. A network core router can require the dissipation of more than 5,000W/system whereas a server product is an order of magnitude less.

Hansen believes that although thermal management issues are significant in both applications, several factors add to the challenge in the computing market. Some of these issues are:

- More heat-generation sub-systems in computing (e.g. hard drives, larger memories, high-end graphics cards in Desktops and notebooks).
- Desktop and notebook computers and some servers are located at the individual user's workspace, not in a data center or wiring closet, and are therefore requiring stricter acoustics, limiting the options in designing the cooling system (i.e. they can not be cooled with fast-spinning fans).
- Mobile devices remain challenging due to the smaller and smaller formfactors, increased battery life expectations and strict acoustics specifications.

This year, MEPTEC also expanded its program with more discussions on test and burn-in, as this is becoming an ever-more frequent discussion area for high temperature devices. Most of our experts agreed that temperature control is a key issue for both test and burn-in. Tosaya explains that, "Higher thermal densities require active device level thermal management. Maintaining a tightly controlled process window, i.e. thermal con-

trol during test and burn-in requires improved thermal solutions and control systems."

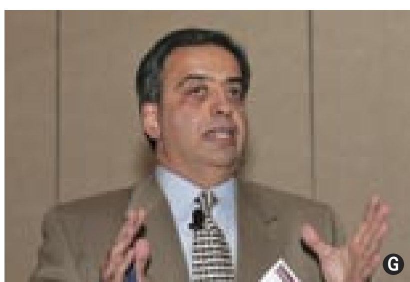
Interestingly enough, according to **Skip Fehr**, Industry Consultant and Session Chair for the *"Thermal Modeling, Burn-in and Test"* session, "With newer, high-powered devices, burn-in is more about the oven cooling capability than heating." As the core temperature of the device increases, it becomes more difficult to maintain a cool environment during burn-in. This usually limits oven capacity which increases burn-in costs.

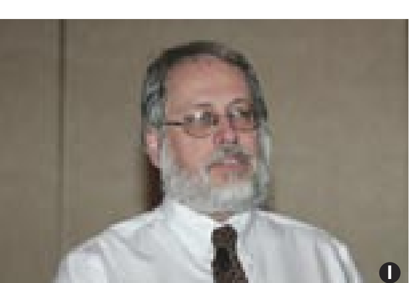
Along those lines, Eghan adds that, "For the large FPGAs, this may be more of an opportunity than an issue. The power generated by the devices supplements the oven temperature to get the targeted max Tj. The on-board system monitor comes in handy to do the power management feedback. This is not an issue for newer boards. Older legacy boards without such feedback and system monitor capability can be a challenge."

Dr. James Forster, Senior Manager, Materials Technology at **Wells-CTI** says that his company "has developed a revolutionary new solution which allows users to extend the capabilities of their existing ovens and infrastructure during burn-in. This solution has been adopted and proven at a number of semiconductor companies and has allowed the cost effective burn-in of new devices." Forster discussed more about the advances being made in thermal management at burn-in during the *"Thermal Modeling, Burn-in and Test"* session of the symposium.

Chu of Cisco says that some of the issues with burn-in of high power and high power density devices have proven to be problems with device surface contamination due to high performance Thermal Interface Materials (TIMs), specifically when using a reusable test head with reusable TIMs that have ultra-high performance.

Most of our experts admitted that they haven't seen any revolutionary advancements





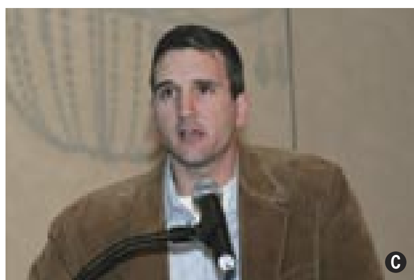
All photos by Bill Shu

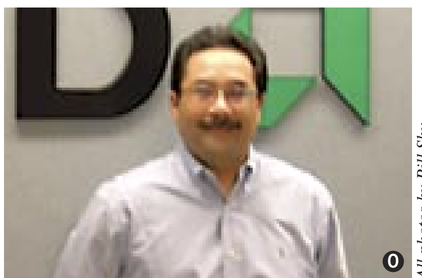
MEPTEC's February "The Heat Is On" symposium speakers included: (A) Keynote speaker Herman Chu from Cisco. (B) Professor Van P. Carey from the University of California at Berkeley. (C) Debendra Mallik, Intel Corporation representing ITRS. (D) Sandra Winkler, Electronic Trend Publications. (E) Devesh Mathur, Honeywell Electronic Materials. (F) Scott Allen, Henkel Corporation. (G) Kaveh Azar, Advanced Thermal Solutions, Inc. (H) Nanda Gopal, Gradient Design Automation. (I) Dr. James Forster, Wells-CTI. (J) Jerry Tustaniwskyj, Unisys Corporation. (K) Abu Eghan, Xilinx, Inc. (L) Ulrich Hansen, Staktek. Not pictured is Bidyut Sen of Sun Microsystems.

MEPTEC Event Follow-up

The Heat Is On: Thermal Management Solutions in Semiconductor Packaging

February 16, 2006 - San Jose, California





All photos by Bill Shu

A MEPTEC symposium Session Leader Julia Goldstein, Advanced Packaging Magazine. B Session Leader Gerald (Skip) Fehr. C Session Leader David Stiver, Google. D The exhibits drew a good crowd throughout the day. E The team from Advanced Technology Solutions. F Attendees enjoyed mingling with exhibitors during breaks. G The SEMPAC team. H A few folks from exhibiting company Honeywell Electronic Materials. I Scott Allen of Henkel Corporation. J Jim Abendschan mans the Spectra-Mat exhibit. K Mausumi Sarkar at the Pac-Tech USA exhibit. L All the way from France – the Epsilon team. M Doug Greenwood from Thermal Engineering Associates (TEA). N Co-chairman Nick Leonardi of CMC Technologies. O Co-chairman Eric Tosaya of Advanced Micro Devices.

in the area of thermal management over the past year, but that doesn't mean that things aren't improving. All levels of the supply chain continue to work toward solving different issues. According to our experts, most of the advancements have come at the device and system design level and in thermal modeling and characterization software.

Tosaya says that AMD has seen improvements both in the characterization capability of their thermal lab as well as improved device process/design that helps to reduce overall thermal power.

Eghan feels that the most significant changes at Xilinx have come at the device level and for FPGA, tools that are predicting power usage, while software optimizations geared towards constraining power have also made some inroads.

Hansen says that his company has developed a new module technology called Arcti-Core™ which is a next-generation electronic sub-system solution designed for superior thermal performance.

While advances are being made, new devices are still being developed which will tax the thermal issues even further. For instance, "The deployment of the Xilinx large Virtex 4 devices (V4-FX) within the last year has extended the top end of the heat generating capability window for FPGA devices," says Eghan. "Though the use of triple oxide transistor to address leakage has been helpful, static power in some of these large devices still poses a significant thermal challenge."

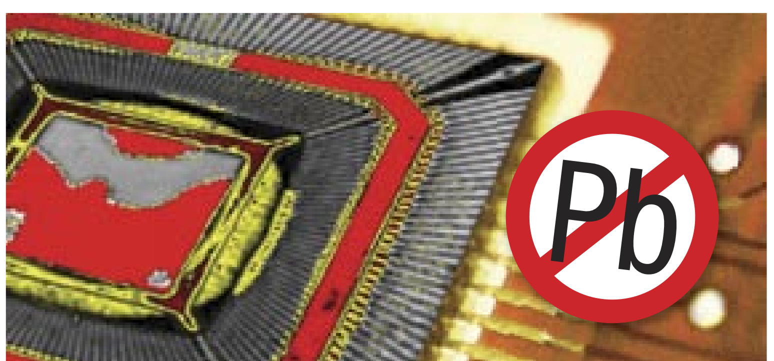
According to Hansen, dual-die DRAM devices are also presenting new challenges. "The increase in memory density with a very compact device form factor has increased the thermal management challenge at the sub-system level by making it more difficult to thermally couple multiple dies in a single package to the system-level cooling solution."

Tosaya agrees saying, "On the device front, the march continues with finer process technologies that enable lower voltages and lower capacitance/transistor to reduce power but conversely companies are also packing more transistors per square mm into the device which increases power."

So the thermal saga continues. Although it's doubtful that a great, new cure-all will appear in the near future, everyone will keep pushing forward, taking small steps towards improvements. The real challenge becomes keeping up with other areas of development so that thermal management doesn't become the semiconductor development bottleneck.

The 2nd Annual *"The Heat is On"* symposium was co-chaired by **Eric Tosaya** of **Advanced Micro Devices** and **Nick Leonardi** of **CMC Interconnect Technologies**. Session leaders included **Julia Goldstein** of **Advanced Packaging** magazine, industry consultant **Gerald (Skip) Fehr**, and **David Stiver** of **Google.** ◆

In 3 months, you'll have to
GET THE LEAD OUT!
Can your ICs take the heat?



Upcoming standards will prohibit the use of lead solder.
That means higher temperatures and higher risk of failure.

Qualify your parts at a SonoLab® near you,
and protect yourself from getting burned.

847.437.6400 • www.sonoscan.com

Chicago, IL • Silicon Valley, CA • Phoenix, AZ • Boston, MA • England • Philippines • Hong Kong • Taiwan • Singapore • Shanghai

Don't Believe the Flat-Liners, Semiconductor Prospects are Bright

Morry Marshall, VP of Strategic Technologies
Semico Research Corporation

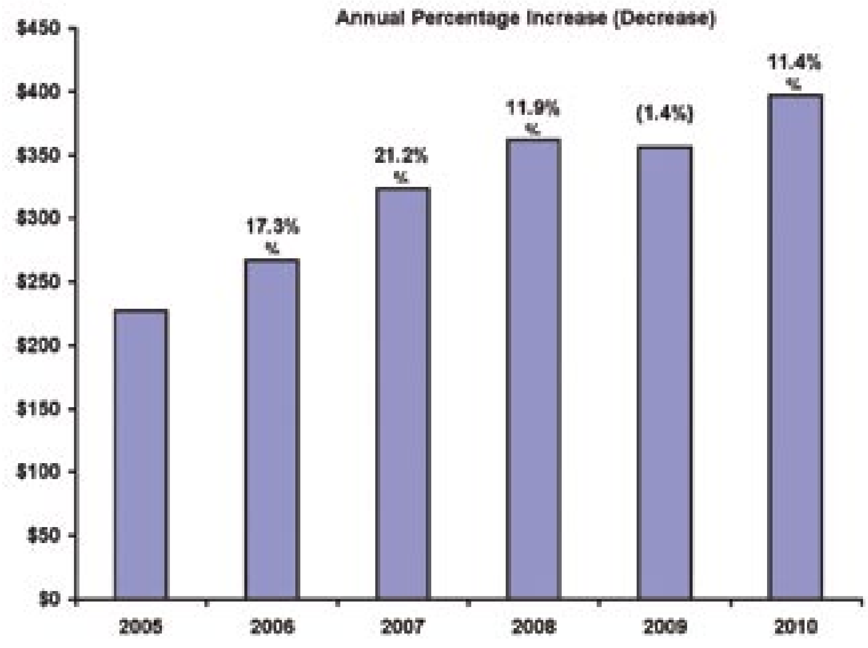
As indicated on the chart below, Semico Research Corporation forecasts annual growth rates above 17% in 2006 and 2007, decreasing to 11.9% as a downturn begins in the second half of 2008. Conventional wisdom is more pessimistic. According to CW, the major semiconductor end-use market drivers have matured; there are no replacements in sight, and semiconductor sales are becoming mature. Therefore, semiconductor sales will be limited to a nearly constant annual percentage growth rate of less than 10% for the foreseeable future. There are two primary reasons this pessimistic forecast will not become a reality: the semiconductor sales cycle and a host of emerging semiconductor end-use markets.

The boom or bust semiconductor sales cycle has become so familiar that no one should need reminding of it. In spite of that, some analysts declare during every downturn that the semiconductor cycle is dead and that semiconductor sales growth is going to flat-line. Then, the cycle repeats, proving that it is far from dead.

The semiconductor cycle is in play today. Delays in purchasing equipment in the years following the 2001 semiconductor sales downturn will contribute to ASP increases and sales growth in 2006 and 2007. Decisions to purchase equipment during that period of sales growth will contribute to a downturn beginning in 2008. As long as the cycle exists, annual semiconductor sales growth rates will not be constant or nearly constant for any extended period of time.

How can anyone familiar with the semiconductor industry believe that there will be no major new semiconductor end-use markets? The list of markets created or revolutionized by the semiconductor industry is long, including PCs, the Web and cell phones for example. It would have been difficult to forecast the ultimate size of many of these semiconductor end-use markets at their beginnings. For example, how many saw the potential for PCs when the first microcomputer kits were introduced? It is equally difficult to visualize the ultimate size of today's emerging markets. Consumers are going to create digital networks with attached storage to connect their TVs and entertainment systems with their PCs digital cameras, music players and other portable digital devices. The resulting markets will be huge. Twenty-somethings are going to drive large, new markets for video on portable media players and cell phones. There are many other consumer applications that are on the edge of the available technology today but will become a growing reality very soon.

Semiconductor sales will not flat-line! The industry is becoming more mature; but it is far from reaching a steady state growth rate. The semiconductor cycle will continue to cause swings in annual semiconductor sales growth rates; and emerging applications will create major new end-use markets, some not yet imagined, that will increase semiconductor sales for years to come. ◆



Five-Year Forecast for Total Worldwide Semiconductor Sales ($US B)
Annual Percentage Increase (Decrease) (%)

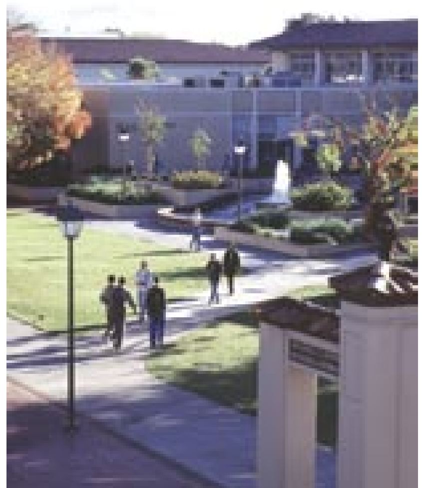
Santa Clara University's School of Engineering

Josh G. Nickel, Assistant Professor
Department of Electrical Engineering
Santa Clara University

Santa Clara University's School of Engineering has been educating the student community since 1912, and is recognized as one of the finest programs in the country. In US News and World Report's 2006 edition of America's Best Colleges, SCU's engineering school was ranked No. 14 in the nation. The university's location in the center of Silicon Valley, its engaged and accessible faculty, and its state of the art equipment have come together to create a powerful learning environment. In addition, the school's small and personalized classes help students develop a foundation for engineering theory and offers opportunities for hands-on experiences.

Daniel Pitt, dean of the School of Engineering, joined SCU four years ago, in 2002, after 23 years of experience in industry. "I value the balanced and rigorous education our students receive. Through coursework and team projects, our students gain multidisciplinary experience in electrical, computer, and mechanical engineering that, combined with a strong foundation in theory and lots of design opportunities, prepares them to contribute to whole-product design that incorporates both function and form," he said.

The challenging yet fun curriculum balances theory and practice, providing research opportunities and practical design experiences during an undergraduate's four-year tenure. In fall 2005, the engineering school enrolled 464 undergraduate students. On average, the student-to-faculty ratio is 12 to 1. Therefore, the students receive plenty of attention from the faculty and are able to form genuine friendships with teachers and mentors. Senior design projects, which are often interdisciplinary, are presented to industry and alumni judges. Graduates of SCU have risen to such prominent positions as president of IBM, CTO of Intel, senior vice president of Cisco, CEO of Extreme Networks, and chairman of Cirrus Logic.



The school offers a number of majors including computer engineering, electrical engineering, civil engineering, mechanical engineering, and general engineering. Three undergraduate minors are also offered: computer engineering, electrical engineering, and general engineering. The civil, mechanical, and electrical engineering programs were accredited in 1937.

SCU's School of Engineering also offers graduate-level degrees and non-degree programs to full-time students and working professionals. About 700 graduate students study at the school each quarter, choosing their focus from the 300 graduate-level courses presented each year that cover almost all the fundamental engineering disciplines. The engineering school's graduate offerings include a five-year B.S. and M.S. dual degree program (for SCU engineering undergraduates only), a master of science degree program, an engineer's degree program, and a doctorate (Ph.D.). Graduate-level courses are offered at various times throughout the day, allowing working students to choose times that work best with their individual schedules.

One of most well-known centers at the school is The Center for Nanostructures.

MEPTEC University News

Founded in 1912, the Santa Clara University School of Engineering educates technical experts that bring competence, conscience, and compassion into everything they do... on campus and in their professional careers.

This center has more than 25 members, including students and faculty from SCU and the University of California, Santa Cruz; colleagues from NASA Ames Research Center (Moffett Research Park) and the Korea Advanced Institute of Science and Technology; and industry partners Hitachi, Cadence, and Alta Microtec.

"The center is focused on studies of interconnects and interfaces in advanced materials and devices. Its expertise in materials and electrical characterization techniques is channeled toward the discovery of new structure-property relationships, leading to the development of next-generation technologies in nanoelectronics and nanobioelectronics," said Cary Yang, professor of electrical engineering and the center's director.

Researchers are actively engaged in several projects at The Center for Nanostructures. One of the most exciting projects involves nano-sensors for biological applications. Applications are potentially numerous and groundbreaking. In today's "faster is better" microelectronics, bandwidth and power demands are stretching Moore's law. Limitations due to signal integrity and thermal management are now create the paramount design bottlenecks. Some of the most promising nanotechnology that has venture capitalists investing, researchers burning the midnight oil, and the microelectronics industry buzzing are carbon nanotubes and nanofibers. Relatively new and still largely a research endeavor, they have nevertheless received considerable attention as the future material of choice in microelectronics. They are extremely versatile, with large electrical and thermal conductivity ranges. High-speed characterization of CNT interconnects has been identified as a key initiative for their application in microprocessors and other architecture components. The center's external partners usually provide fabrication services, but measurement equipment is available in-house, including a Cascade Microtech probstation, vector-network analyzer, impedance analyzer, and processing tools.

Another of the school's centers is the Engineering Design Center. This center has a network of more than 120 high-end workstations grouped into Windows, XP, Sun Solaris Unix, and Centos Linux. All of the workstations have large LCD flat-panel displays and unrestricted Internet access. The Design Center supports a variety of industry-standard technical software packages as well as a variety of programming language compilers.

There are more than 25 major commercial software packages of engineering applications for student use. Enrolled engineering students also have access to an Oracle database, Apache Web servers, and a Unix e-mail server. Data storage is provided by two Linux-based Network Attached Storage arrays (NAS) with a current capacity of approximately 9 TB, giving each student 500 MB of dedicated disk storage. Two of the labs are equipped with large projection screen capabilities, which can be connected to computers, and VCR or DVD players.

As dean, Pitt encourages people to visit the school and see for themselves what makes it a leader among engineering schools. "I invite any reader to visit the campus to see for yourself the first-rate machine shop, the robotic systems laboratories, the scanning electron microscope in the nanotechnology laboratory, and the Design Center with the latest in CAD tools of all sorts, or visit us online." ◆

For more information about Santa Clara University School of Engineering programs and facilities go to www.scu.edu/engineering.

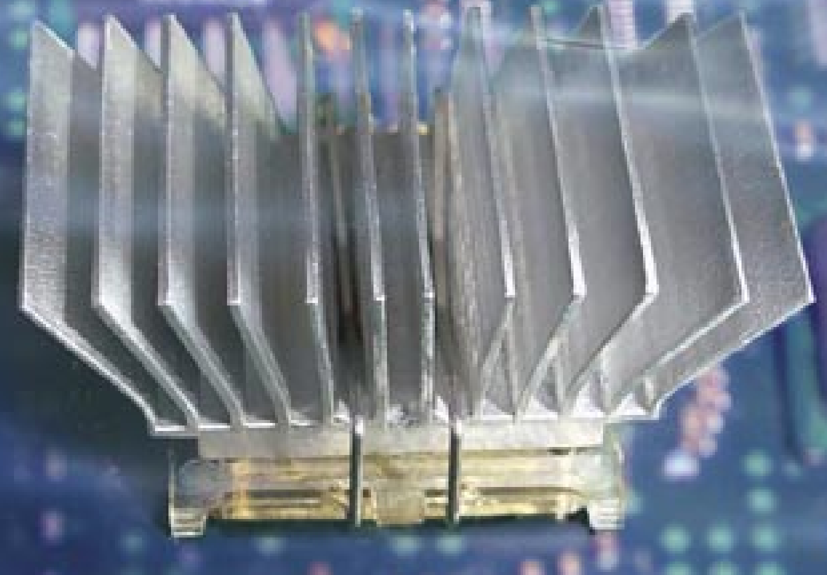
Students and laboratory equipment in Santa Clara University's Center for Nanostructures.

Clip 'N Cool

The easy and reliable cooling solution

maxiGRIP™ Ultimate Heat Sink Attachment System is the new clip-on mounting method for fast, safe, and secure heat sink mounting

- No sink threading, cracked dies or detached components
- Extended cooling surface
- Easy heat sink removal and re-attachment



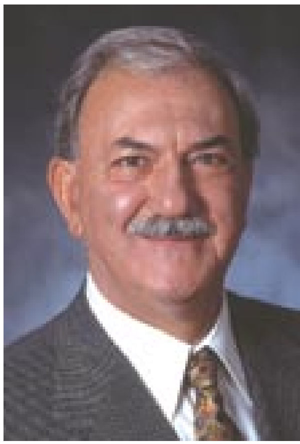
Innovation in Thermal Managment™

Advanced Thermal Solutions, Inc.

www.qats.com

© All Rights Reserved

Dr. Marcos Karnezos Joins SunSil Inc. Advisory Board



ALAMO, CA – Dr. Marcos Karnezos, whose wide-ranging semiconductor industry experience exceeds 26 years, has joined the advisory board of SunSil Inc.

SunSil is a leading international technical sales and marketing organization headquartered in Silicon Valley. SunSil represents many companies in the wafer processing, assembly and test sectors of the semiconductor industry.

Dr. Karnezos, who holds a doctorate in physics, was most recently special technology advisor to STATS ChipPAC, a leading semiconductor packaging and test foundry. Previously, he served as vice president of technology at both ASAT and Signetics KP.

Other Advisory Board members are Dr. Thomas H. Di Stefano, Dana Ditmore, Dr. Vivek Dutta, Hamid Farzaneh, Cemal Mehmet, Dr. Mak Shinohara and Dr. Samuel Wang.

For more information visit www.sunsil.com.

Carsem Appoints New Director of Marketing

SCOTTS VALLEY, CA – Carsem has announced that Mr. Oliver Davis joined the company as the Director of Marketing and is replacing Mr. Paul Smith, who announced his retirement effective at the end of February. Mr. Davis is based in the Scotts Valley, California office and reports to Mr. Rick Flowers, Carsem's V.P. of Sales for North America.

Mr. Davis has over 26 years of experience in the semiconductor industry. Prior to joining Carsem he was the Director of Sales and Engineering at Signetics High Technology and prior to that he was a Senior Sales Account Manager at ASAT, Inc. His previous positions in the industry include Test Operations Manager at Chips and Technologies and the Northwest Regional Manager for Field Service of ATE equipment at Schlumberger Technologies.

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, Suzhou, China and sales offices across the USA, plus the UK and Taiwan.

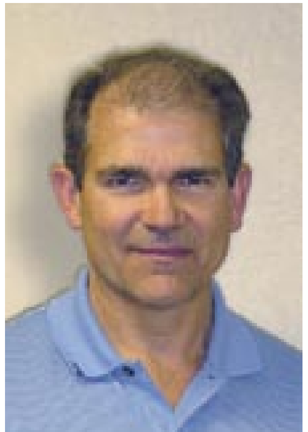
Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Todd Fielitz Appointed OEM Account Manager for DeWeyl Tool

Todd Fielitz has been appointed OEM Account Manager for DeWeyl Tool, and will be based in Arizona. Todd brings 18+ years of experience in semiconductor and microelectronic assembly packaging technology and technical sales to his new position.

In making the announcement, David Pasfield, DeWeyl Tool's Director of Sales & Marketing, stated that "Todd's considerable experience on the manufacturing floor as well as on the side of selling assembly products, in particular his familiarity with wire and die bonding equipment, will be a real asset to our company. We look forward to the benefit of his experience and skills and welcome him to the DeWeyl Tool family." Todd can be reached at Tel. (520) 836-3861, Fax (520) 836-2922, or E-mail todd.fielitz@direcway.com.

Bruce Hueners Named President of Palomar Technologies



CARLSBAD, CA – Palomar Technologies has announced that Bruce W. Hueners has been named company President. Mr. Hueners joined Palomar Technologies in 1981 when it was Hughes Aircraft and most recently held the position of COO. He was instrumental in elevating Palomar to the role of market leader in the optoelectronics industry, orchestrated a series of acquisitions and partnerships for Palomar, and has played a major role in expanding Palomar's business in the U.S., Europe and Asia.

Mr. Hueners has considerable experience and extensive engineering knowledge in the microelectronics, microelectronic packaging and interconnects, microwave and RF, and optoelectronics fields. He collaborated in the development of laser interferometric measurement and die attach and wire bond systems and processes, has written more than 50 technical papers, and currently serves on the editorial board of Advanced Packaging magazine. He is on the Board of Directors of the San Diego World Trade Center and represented San Diego on their recent trade mission to China.

Prior to joining Palomar, Hueners was Advanced Manufacturing Engineer with the Semiconductor Products Department at General Electric where he developed mechanized processes for high-volume optoelectronic assembly. Hueners received a BS degree in Mechanical Engineering from the University of Southern California, an MBA from Indiana University, and a Certificate from the Executive Program for Scientists and Engineers at UCSD. He is a member of IMAPS, SMTA, IEEE, and the Optical Society of America. Bruce's interests include astronomy, gardening, and golf.

For more information, visit www.palomartechnologies.com or call 760-931-3600.

F&K Delvotec Selects Siemens AG as Partner for Die Bonder Product Series

OTTOBRUNN, GERMANY – Siemens business unit Electronics Assembly Systems (EA) took over the die bonder product series of F&K Delvotec Bondtechnik GmbH, Ottobrunn, Germany on March 1st. Consequently all research & development, manufacturing as well as service and consulting are now provided by the EA business unit Optical Solutions. By adding automatic machines for special processing of dice in large numbers EA intends to expand their leading position as manufacturer of production solutions for the electronics assembly industry.

Combining the technology-leading F&K Delvotec know-how in the area of wire and die bonding with Siemens' experience in the area of chip assembly and high speed SMT-manufacturing allows customer requirements in electronic module production, medical industry and flight technology to be met even better in the future.

The Siemens unit Automation and Drives (A&D), Nuremberg, is the world's leading sup-

plier of automation and drive technology. The range covers standard products for the manufacturing and process industry, electric installation technology and system solutions, e.g. for tool machines, up to industry branch solutions with the automation of complete automotive production lines or chemical plants. A&D also offers software for the integration of production and business economics (horizontal and vertical IT integration) as well as for the optimization of production processes.

More information about Siemens EA is available online at www.siplace.com.

More information about F&K Delvotec is available at www.fkdelvotec.com.

Carsem's China Factory Achieves ISO/TS 16949 Certification

SCOTTS VALLEY, CA – Carsem's factory in Suzhou, China has recently achieved ISO/TS (Technical Specification) 16949: 2000 Certification from TUV Rheinland Group, an internationally accredited quality evaluation company and third party registrar. The factory is a 172K sq. ft. (16K sq. m.) facility that is located in the Suzhou Industrial Park, which is in the province of Jiangsu 50 miles (80 km) west of Shanghai.

The ISO/TS 16949:2002 is a Quality Management System specific to the automotive industry, which includes all the requirements of the ISO 9001:2000 Quality Management System standards. The quality systems are currently endorsed by BMW, Daimler-Chrysler, Fiat, Ford, General Motors, PSA Peugeot-Citroen, Renault SA and Volkswagen AG, and are supported by various automotive trade associations such as AIAG (USA), SMMT (UK) and VDA (Germany). ISO/TS 16949, coupled with customer-specific requirements, define the quality system requirements for use in the automotive supply chain and provides for a global registration scheme.

Carsem-Suzhou has been shipping production volumes since July 2004 and currently offers full turnkey assembly and test services for the entire range of MLPQ (Quad) and MLPD (Dual) packages, which is a saw-singulated version of QFN & SON compliant packages per JEDEC's MO220 and MO229 standards.

Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, telephone (831) 438-6861, fax (831) 438-6863. For more information visit www.carsem.com.

Advanced Applied Adhesives Expands Sales Representation in North America

SAN DIEGO, CA – Advanced Applied Adhesives (AAA) has announced TechRep International (TRI) as its sales representative for Southern California, Texas, Arizona, and Colorado. Additionally, TRI has been appointed to serve certain national accounts outside the aforementioned territory. With the recent introduction of several new state-of-the-art, Self-Filleting™ die attach adhesives to their already extensive product portfolio, AAA is now positioned to supplement the company's existing network of sales representation and to aggressively grow its market share.

"TRI was selected because it has an established reputation within the microelectronics industry calling on tier one accounts nationwide," stated Frank Husson, President of AAA. "They will bring immediate exposure of our die attach adhesives and custom formulation capabilities to several large OEM customers as well as contract assemblers."

Advanced Applied Adhesives offers a wide range of conductive and non-conductive die attach adhesives for Leadframe, BGA, and Stacked Die applications, featuring low bleed, low CTE, and low stress capabilities. Several B-stage materials are also available for BOC (Board-on-Chip), Bottom Die Attach, and Wafer-Back-Coating applications.

AAA has a strategic alliance with Designer Molecules, Inc. (DMI), a sister company with common ownership. Also founded by Mr. Husson in 2001, DMI's business model is focused on the design and licensing of unique molecules, including adhesive molecules for specific customer requirements. DMI's co-founder, Dr. Stephen Dershem, a key inventor of the first BMI liquid monomer, is also a principal of the company.

For more information about AAA call 858-348-1125 or visit www.appliedadhesives.com.

Indium Corp. Suzhou Awarded ISO-9001:2000 Certification

Indium Corporation (Suzhou) Co., LTD recently passed its ISO-9001:2000 certification audit. The Suzhou facility joins the company's U.S., European, and Asia-Pacific Operations in achieving ISO-9001:2000 certification.

ISO-9000 focuses primarily on "quality management". Certification means that Indium Corporation (Suzhou) has processes, procedures, and standards in place to enhance customer satisfaction by meeting or surpassing quality goals, and continues to improve its performance by developing and implementing continuous improvement programs to ensure future performance objectives are met.

A team of individuals, led by Lily Liu, performed training, set up procedures, and executed internal ISO audits in preparation for the independent audit, which was conducted by outside auditors.

For more information about Indium Corporation's ISO Certificaion, visit Indium's website at www.indium.com, or email askus@indium.com.

Semiconductor Packaging Company Invests in New Venture

HAYWARD, CA – Delphon Industries announced its acquisition of TouchMark, Inc. of Hayward, CA. The move is part of an ongoing strategy to merge innovative technologies in order to provide unique materials and services for the packaging, shipping and process handling of high value technology devices. "With TouchMark's expertise in high quality pad printing on a wide variety of surfaces, we will be able to offer our customers an even greater degree of customization for their unique packaging needs" says Jeanne Beacham CEO of Delphon Industries.

Touchmark, established in 1992, provides customers with high quality pad printing services such as company logos, graphics, and part identification. Services are available for prototypes or full production parts and range from printing on large panels to microscopic printing for medical applications. The company also provides graphic design and assembly services.

Delphon Industries, LLC was started in 2004 in order to provide a platform for future growth in merging innovative technologies. The company specializes in bringing together unique packaging solutions in order to meet the specific needs of its customers. Under its corporate umbrella, the company operates Gel-Pak of Hayward, CA and Quik-Pak of San Diego, CA.

Gel-Pak products are used in a wide variety of industries that require the proprietary Gel solution for the safe shipping and handling of leading edge technologies. When companies around the world need to transport valuable devices without risk of damage, they rely on products made by Gel-Pak.

Quik-Pak uses its patented Open-Cavity Package technology and complementary assembly services to produce IC

prototypes for semiconductor and MEMS manufacturers, and Fabless IC design firms. Quik-Pak can process any plastic package at any time.

K & S Announces Agreements to Divest Test Businesses

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. (K&S) has announced a plan to tighten its focus on semiconductor assembly equipment and materials and create value for its shareholders.

K&S has signed a definitive agreement to sell its wafer test assets to SV Probe, PTE, Ltd. K&S has also signed a definitive agreement to sell its package test assets to Investcorp Technology Ventures II, L.P., which is managed by the Technology Investment Group of Investcorp, a global investment firm. In both cases, the transactions are subject to closing conditions.

Scott Kulicke, chairman and CEO of K&S, discussed the decision to divest these businesses: "We've made significant progress with these businesses over the last few months, including introducing new products, completing our planned product moves into China, and gaining market share. However, this progress has come at the expense of diverting focus away from our goal of being both the technology leader and the low cost supplier in our core assembly markets, and that's unacceptable." He added, "We came to the conclusion that our test customers would be better served by suppliers focused solely on test. In selecting both SV Probe and Investcorp, we've found buyers committed to continuing to meet the high standard of customer service that has characterized K&S's ownership of these businesses, and we've structured the sales agreements to insure customers a seamless transition."

Mr. Kulicke concluded, "K&S's core strengths lie in the semiconductor assembly arena. We expect that focusing on that business will result in an expanding customer base while providing better financial performance and value for our shareholders."

Kulicke & Soffa's web site address is www.kns.com.

FlipChip International Breaks Ground on Joint Venture with Millennium Microtech

SHANGHAI, CHINA – FlipChip International LLC announced that it started construction of an advanced bumping facility for a new Joint Venture in China with Millennium Microtech, Shanghai. The Joint Venture will provide wafer level packaging and flip chip bumping services to the domestic and international semiconductor market. The JV is owned respectively by FlipChip International and Millennium Microtech (Shanghai) Co., Ltd. (MMS). The JV will be referred to as FCMS and be located at MMS's existing Pu Dong facility.

Bob Forcier, President and CEO of FlipChip International, stated, "We are very excited to have achieved such a stellar partner with our new FCMS China joint venture. Pu Dong is one of the most active semiconductor regions in the world and we believe the combination of MMS and FCI is a powerful entry into the Chinese market with advanced flip chip bumping and wafer level packaging. The domestic consumption of flip chip devices is expected to maintain double digit growth for the next three years and is an essential packaging technology for wireless portable devices and video phones"

FlipChip International, LLC is a privately held supplier of products and services for the wafer bumping and wafer scale packaging semiconductor market. FlipChip International, LLC is a wholly owned subsidiary of RoseStreet Labs LLC, a supplier of products and services for wireless infrastructure in the life science, renewable energy and homeland security markets.

MMS is a subsidiary of Millennium Microtech Holding (MMH). MMH provides fully integrated semiconductor packaging and test services including dicing, tape & reel, wafer probing and back-grinding through MMS and Millennium Microtech (Thailand) Co., Ltd.

ATS and NTS Partnership Provides Combined Design, Validation and Compliance Testing

NORWOOD, MA – Advanced Thermal Solutions, Inc. (ATS), a global provider of testing, design and products to cool electronic equipment, has partnered with National Technical Systems Corporation (NTS), a leading provider of quality, conformance and certification testing, quality registration, and managed services.

The partnership of these leading companies offers a unique, single-stop resource for manufacturers with thermal management issues and who need the services of a certified testing laboratory to show compliance with equipment standards. Advantages to OEMs include faster delivery of test results and certifications, and joint expertise to resolve problems more efficiently. Bottom line benefits include cost-savings and faster time-to-market.

Test and design services are now available in North America and Western Europe. ATS has facilities in Massachusetts, California, and Holland. NTS laboratories are found throughout the United States as well as in Europe, Canada, Germany, Japan, and Vietnam.

Information about Advanced Thermal Solutions is available at www.qats.com or by calling 781-769-2800. For more about National Technical Systems, visit www.ntscorp.com or call 800-270-2516.

StratEdge High Frequency Package Chosen for Device Life Testing in Accel-RF Equipment

SAN DIEGO, CA – StratEdge announced that one of its DC to 23 GHz Low Cost Commercial (LCC) packages is used by Accel-RF as a platform for life testing of high frequency devices. Accel-RF, San Diego, California, makes fully integrated, automated systems that characterize RF and DC performance degradation to predict device life expectancy. In addition to the package, StratEdge provides microelectronic assembly services to Accel-RF, including gold-tin eutectic die attachment and wire bonding.

During life testing, devices are subjected to temperatures of up to 250 degrees Celsius while operating at high frequencies. The devices need to be mounted in the test equipment. The StratEdge package provides a convenient way of doing it. Since Accel-RF equipment is used to test devices of many configurations from different manufacturers, it is essential that the package used be flexible enough to accommodate a wide variety of sizes.

The StratEdge 580286 LCC package has a 0.250" x 0.250" (6.35mm x 6.35mm) cavity dimension that will accommodate most devices that need testing. It features a flexible pin-out of two RF leads and eight DC leads for easy connection of the device to the package. The package combines a copper composite base with a patented microstrip-imbedded microstrip-microstrip transition design. This composite metal base provides thermal conductivity and expansion compatible with compound semiconductor devices.

ASM First to Enter Mainland China with 300 mm Epitaxial System

BILTHOVEN, THE NETHERLANDS – ASM International N.V. has announced that it has sold the world's first 300 mm epitaxial reactor into mainland China. The system, shipped in Q4 2005, was ordered by the General Research Institute for Nonferrous Metals (GRINM), one of the largest Chinese research institutes for semiconductor related applications.

"Although initially used for 12 inch silicon epitaxial wafers, the Epsilon® 3200 system going into our Beijing facility was chosen specifically to expand into studies of silicon germanium (SiGe), strained silicon as well as other new research areas," said Dr. Hailing Tu, president of GRINM.

"In addition, ASM's track record in providing state-of-the-art processing for some of the world's most advanced IC technologies weighed heavily in our selection process," Tu added.

The main use of the Epsilon 3200 is for epitaxial growth of silicon and SiGe alloys. This includes advanced blanket and selective epitaxial growth processes for recessed and elevated source/drain structures as used in state-of-the-art CMOS transistors, as well as the integration of strained silicon in SOI wafer technology.

For more detailed information, visit the ASMI web site at www.asm.com.

SUSS MicroTec's NC-1 Non-Contact System Wins International Award

MUNICH, GERMANY – SUSS MicroTec AG has announced that the world's first and only non-contact probe system, the NC-1, has been honored with the "Best in Test" award from the leading industry journal Test & Measurement World. As one of twelve products selected by the editors, it is the only probe system to be presented with the award, which recognizes particularly innovative and useful test products.

The NC-1 Non-Contact System uses a patented technique to acquire signals from very small features without loading the circuit under test or relying on optical emissions. The NC-1 supplies both voltage and timing information, and the integrated atomic force probe enables deep sub-micron scanning and positioning. To extract measurements from the device, the tip of the probe is stimulated with electrical pulses after being placed above the area of interest. The forces generated between the tip and the device under test are then measured and analyzed by the NC-1 software, and the signal voltage waveform is extracted. This data is presented to the user in an easy-to-read format.

CDS Announces the Release of Version 7.4

SAN JOSE, CA – CAD Design Software announces the release of the latest version of their advanced layout tools. Two years in development, Version 7.4 is the largest and most extensive expansion of CAD Design Software's high-end EDA tools and is the culmination of extensive collaborative relationships with many industry leaders in the U.S., Japan, and Asia in the Semiconductor Packaging, Hybrid/MCM, IC Test, and RF/Microwave fields.

"Because of our ongoing partnership with the top industry leaders, we have not only been able to rapidly implement enhancement requests, but have been able to jointly develop new layout solutions for emerging technologies as well as create previously unavailable 3D manufacturing verification systems. This has resulted in our most advanced and expanded 3D layout solutions for leading-edge IC packaging, IC Test, RF, and MCM layout", said Gordon Jensen, president of CAD Design Software.

More robust, sophisticated algorithms for faster processing and CAD Design Software's award-winning Bond Wire Optimization and 3D design tools are among the hundreds of enhancements and improvements that help reduce design time, improve overall time-to-market, and verifiably improve yields.

Version 7.4 is available now from CAD Design Software and its channel partners.

For more information call 408-436-1340 or visit CDS on the web: www.cad-design.com.

SUSS MicroTec Wins Multiple Orders with New Mask Aligner Concept

MUNICH, GERMANY – SUSS MicroTec AG has announced that it has already received eight orders for a total of thirteen machines for its brand-new MA200Compact. Seven machines have been installed last year; the rest will be shipped in 2006. The MA200Compact is a production full-field exposure system featuring a new concept, which enables the use of cost effective mask aligner technology in areas where 1X steppers used to dominate. All customers chose the MA200Compact over alternative systems due to its high precision, low cost of ownership and flexibility for processing wafers of different sizes and photo resist thickness.

Thick resist photolithography is an indispensable element of MEMS processing, wafer bumping and advanced wafer level packaging in general. The MA200Compact can be equipped with high resolution exposure optics enabling near vertical sidewalls at highest aspect ratios in resist films up to 100 microns and thicker. In

• FREE Wireless Internet Access
• 176 spacious guest rooms
• Full service restaurant
• In room coffee makers, refrigerators, hairdryers, irons and ironing boards, am/fm clock radios and digital safes
• On demand movies
• Voice mail
• Heated outdoor pool and Jacuzzi
• Banquet/meeting space for 250
• Japanese Tatami rooms
• Minutes from Light Rail, Santa Clara Convention Center and Paramount's Great America
• 24 hour San Jose Airport transportation
• Special group rates and packages

The only full services Ramada in Silicon Valley
(408) 245-5330
1217 WILDWOOD AVENUE • SUNNYVALE • CA 94089

addition, the MA200Compact supports SUSS SupraYield, a patented package of technology enhancements, which increases resolution, improves overlay accuracy and boosts wafer yield. SupraYield enables cost effective mask aligner technology to meet even the most demanding performance criteria.

Electrically Insulating Die Stack Adhesives Now Available

SAN DIEGO, CA – Advanced Applied Adhesives (AAA) has announced the availability in production quantities of a new series of electrically insulating die attach adhesives featuring a low coefficient of thermal expansion (CTE) that reduces CTE strain. Designated AAA2300, the series is comprised of AAA2300, AAA2301 and AAA2303.

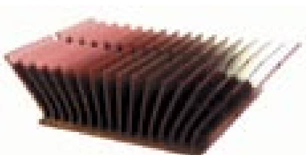
Low bleed in nature, AAA-2300 is suitable for pyramidal-die-stack on bleed-prone nitride passivated die that is without polyimide final passivation. Designed for a 1 mil or thinner bondline, the ultra fine silica filler in AAA2300 has been proven to not damage the bottom die; even without the polyimide buffer layer.

The lower CTE AAA2301 and AAA2303 are for same-die-stack applications requiring a gap filling bondline in place of a dummy die. The materials fill the gap all the way to the die edge to provide firm support to the top die for wire bonding. The low CTE of the materials protects bonding wires from breaking in temperature cycling and thermal shock. Lower in density, the AAA2301 has a price advantage on a per volume basis while AAA2303, having the lowest CTE among the 2300 series, endures extended cycles of thermal stresses without early fallouts.

Each adhesive in the series is solvent-free and will cure to a void-free bondline in a fast ramp, snap cure oven or in a box oven for batch processing.

For further information about the AAA2300 series, call (858) 348-1125 or email info@appliedadhesives.com.

Heat Sinks Deliver High Performance in Low Airflow Conditions



NORWOOD, MA – Advanced Thermal Solutions has introduced maxiFLOW™ heat sinks for cooling BGAs and other hot components in the restricted air flow conditions typical of today's condensed electronic packages. MaxiFLOW heat sinks feature a low profile, spread fin array that maximizes surface area for more effective convection (air) cooling. The heat sinks are fabricated from extruded aluminum which minimizes thermal resistance from the base to the fins, reduces weight, and keeps costs low. Tests on maxiFLOW heat sinks using an air flow rate of just 100 lfm (linear feet per minute) show that device junction temperatures (Tj) can be reduced by more than 40 percent below the temperatures achieved using other heat sinks.

For more information, contact Advanced Thermal Solutions at 1-781-769-2800, or visit www.qats.com.

Europractice and UMC Offer 90nm Multi-Project Wafer Prototyping and Production Service

LEUVEN, BELGIUM and HSINCHU, TAIWAN – IMEC, Europe's largest independent research center in the field of nanoelectronics, and UMC, a world-leading semiconductor foundry, has announced the extension of IMEC's Europractice IC Service with the offering of UMC's 90nm process technology. UMC and Europractice have collaborated closely for many years in offering UMC's Silicon Shuttle® Multi Project Wafer (MPW) platform for pro-totyping and production services to European companies and academia. The availability of 90nm technology will be of particular interest to European-based companies and institutes with low-volume manufacturing needs, such as universities, research centers, start-up companies, and companies with niche markets.

Europractice IC Service, coordinated by IMEC, offers companies ASIC services to help them bring their products to market quickly and cost-effectively. Under the UMC-IMEC foundry agreement, Europractice customers have easy access to UMC's advanced technologies for prototyping and low-volume production, including 0.25, 0.18, 0.13 micron and now 90nm technologies.

For smaller scale research or student designs, Europractice offers a very cost-attractive mini@sic prototyping program. This program reduces prototyping costs for small designs to less than 20% of normal foundry shuttle prices.

For more information visit www.europractice.imec.be.

UMC's Integrated DFM Solutions Target 90nm SoC Designers

HSINCHU, TAIWAN – UMC recently announced its comprehensive design-for-manufacturing (DFM), yield optimization offering targeted to customers developing 90nm SoCs. The package incorporates DFM elements into standard-cell libraries, SPICE models and design flows to provide the customer with yield-enhancing knowledge throughout the design and manufacturing stages.

UMC's DFM Value Service, a key part of the DFM package, includes a comprehensive design for diagnostic platform that enables UMC to test, map out and pinpoint physical failures on customers' chips quickly, without the extensive and drawn-out process of exchanging information back and forth between the foundry and customer. Through this approach, engineering teams spend less effort on the diagnostic process and thus they can quickly enhance yields, gain faster time to market, and have lower production costs.

Customers seeking to utilize UMC's integrated DFM solutions should contact their account manager or go to the MyUMC total online supply chain customer information portal at www.umc.com.

Los Angeles to Host IPC Printed Circuits Expo, APEX & Designers Summit in 2007

BANNOCKBURN, IL – IPC – Association Connecting Electronics Industries® announced that its co-located IPC Printed Circuits Expo®, APEX® and Designers Summit conference and exhibition will take place February 20-22, 2007, at the Los Angeles Convention Center in Los Angeles, California. The event will be one of the largest exhibitions for the electronics interconnection industry in the world.

Relocation from Anaheim was required when the Anaheim Convention and Visitors Bureau indicated that the show was less desirable for the Bureau than other events which promised to book more hotel rooms in relation to the amount of exhibit and meeting space used. As a show with a lot of equipment, set up and tear down take up two halls in the Convention Center without a proportional use of hotel rooms. The Bureau indicated that they could not ensure meeting the needs of IPC's show for meeting and exhibition space if another event with greater area

hotel usage wanted the Convention Center during dates previously reserved by IPC.

Los Angeles was selected by the volunteers of the IPC Trade Show Committee after reviewing several options. The Los Angeles Convention Center is a state-of-the-art venue with excellent facilities to accommodate the show's growth and many meetings and programs. All activities will take place under the Convention Center's roof.

For more information about IPC Printed Circuits Expo, APEX and Designers Summit, visit www.GoIPCShows.org or e-mail shows@ipc.org.

Semico Maintains Optimistic 17.3% Annual Growth Projection

PHOENIX, AZ – Semico's Inflection Point Indicator (IPI) ticked up a notch in December to 16.2, surpassing last month's re-stated IPI of 16.1. The IPI has risen above 16 for four of the last five months, and has been on an upward trend since May 2005.

Given than Semico's IPI has proven to accurately forecast the worldwide semiconductor market 8 to 9 months in advance, the elevated May-to-December 2005 IPI points to the state of the market between January and September 2006. Guided by the IPI, Semico is projecting a strong market this year, with positive growth in all four quarters and a 17.3% annual revenue growth.

Semico's optimism is founded on the momentum generated from strong year-end numbers. Final worldwide semiconductor revenue shipment data just released by the SIA showed total revenue shipments in December were $21.8 billion, an increase of 10.6%. Year-over-year, December 2005 revenue shipments were up 12.2%. Overall, 2005 finished with 6.8% growth, with total worldwide semiconductor revenue shipments reaching $227.6 billion.

A number of other indicators further supports Semico's forecast. Robust demand has a number of companies reporting stronger-than-expected results. TSMC, for example, reported both revenues and net income increased both sequentially and year-over-year in 4Q05, topping the company's previous guidance. TSMC also reported the foundry was running at full capacity.

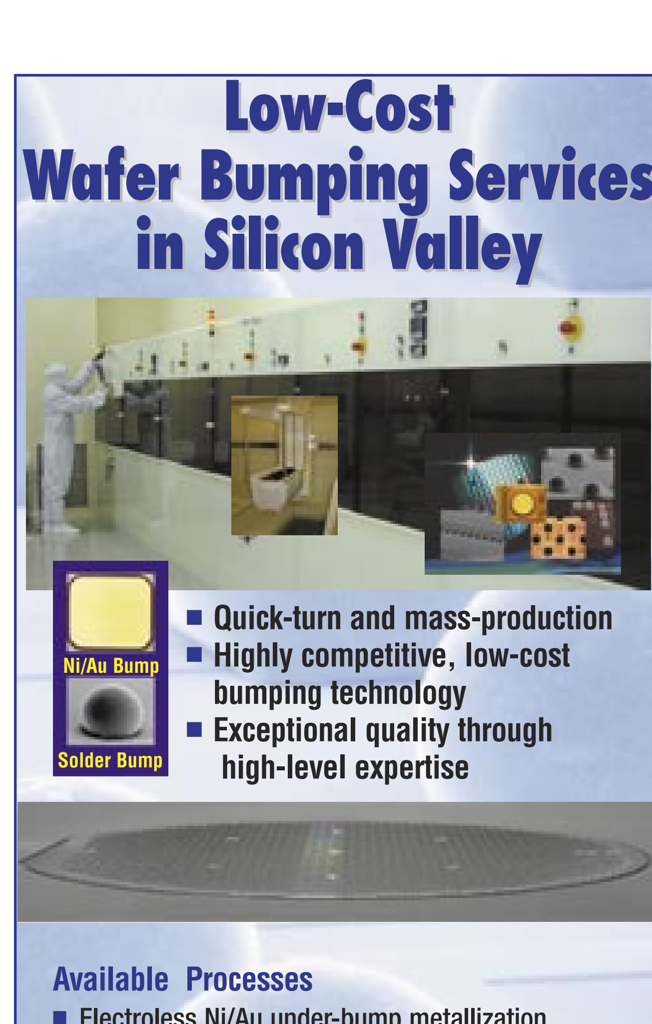
Another indicator supporting their optimistic forecast is inventory – the dreaded word of the year in 2004. December inventory levels for Electronic computers, Non-defense communications, and Electronic components are significantly lower than they were a year ago, substantiating a healthy market in which inventories are not an issue.

Consumers are certainly doing their part to drive semiconductor growth. Retail sales excluding autos were up 2.2% in January, the greatest increase since 1999. Including autos, retail sales were up 2.3%, the best showing in 20 months.

The consumer confidence index surged in January to 106.3, the highest level since June 2002. The unemployment rate fell to its lowest level since July 2001, sliding to 4.7%, indicating the labor market is strong. American assessments of current economic conditions and positive views of their job market will spur purchases of new gadgets.

If the activity at the 2006 3GSM World Congress in Barcelona is any indication, demand will be hot during the next couple of years for replacement products and new gadgets. Mobile phone operators are teaming up to roll out interoperable instant messaging and VoIP services, and 3G is a part of many operators' technology migration strategy. In a sign of the times, Israeli operator Cellcom has announced the launch of a reality show that is accessible only to mobile subscribers.

It seems like yesterday that camera phones were just emerging, and now Johnson Electric Holdings Limited has launched a high-precision motion technol-



Available Processes
- Electroless Ni/Au under-bump metallization
- Ni/Au bump for ACF or NCP assembly
- Solder paste stencil printing
- Solder ball drop for wafer-level CSP
- Solder jet for micro-ball placement
- BGA and CSP reballing
- Wafer backside thinning and wafer dicing

Special Features/Technologies
- Over 10 years experience
- U.S. Government certified
- 4- to 12-inch wafer capability
- Wafer pad metallization: Al and Cu
- Solder alloys: eutectic SnPb37, lead-free, low-alpha, and AuSn
- Fluxless and contactless bumping for MEMS and optoelectronics
- Ni/Au interface for wire-bond applications

PacTech USA—Packaging Technologies
328 Martin Avenue • Santa Clara, CA 95050
Tel: 408-588-1925 • Fax: 408-588-1927
Email: info@pactech-usa.com

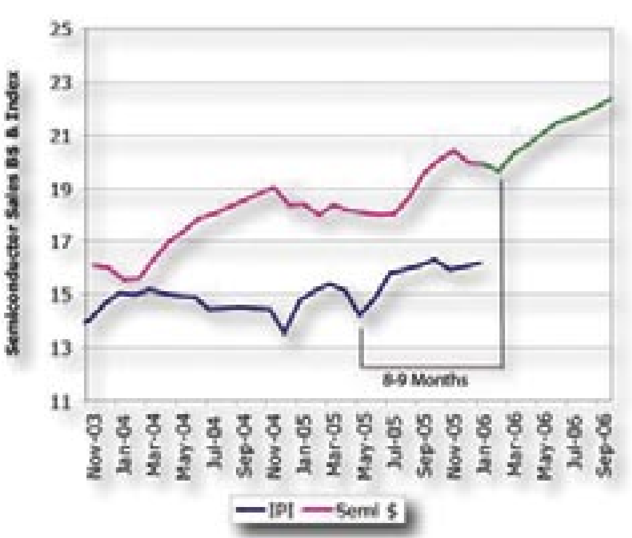
www.pactech-usa.com

ogy module for in-focus zoom in camera phones. Innovation has always spurred growth, and the trend continues in the cell phone market.

The advent of new cell phone types will add to the already solid worldwide semiconductor unit shipment levels. In 2005, unit shipments increased 6.5%. This positive trend is expected to continue into 2006, with unit growth projected at a solid 10.5%.

Geographically speaking, in December both the Americas and Asia Pacific posted revenue growth stronger than the worldwide average of 10.6%. Asia Pacific registered the greatest improvement, boasting a growth of 14.9%, while the Americas posted 11.8%. In contrast, Europe and Japan had only single-digit growth, 5.9% and 2.7%, respectively.

Overall, Asia Pacific continues to make gains in the industry. This region increased its worldwide revenue shipment market share, from 41.7% in 2004 to 45.4% in 2005. This came at the expense of every other region. Japan felt the greatest pain, dropping 2.1 percentage points, followed by Europe, which fell 1.2 percentage points. The Americas remained relatively stable, falling from an 18.3% share of revenue shipments in 2004 to 17.9% in 2005. ◆



Semico's Inflection Point Indicator (IPI) ticked up a notch in December to 16.2. Guided by the IPI, Semico is projecting a strong market this year.

North American Semiconductor Equipment Industry Posts January 2006 Book-To-Bill Ratio of .97

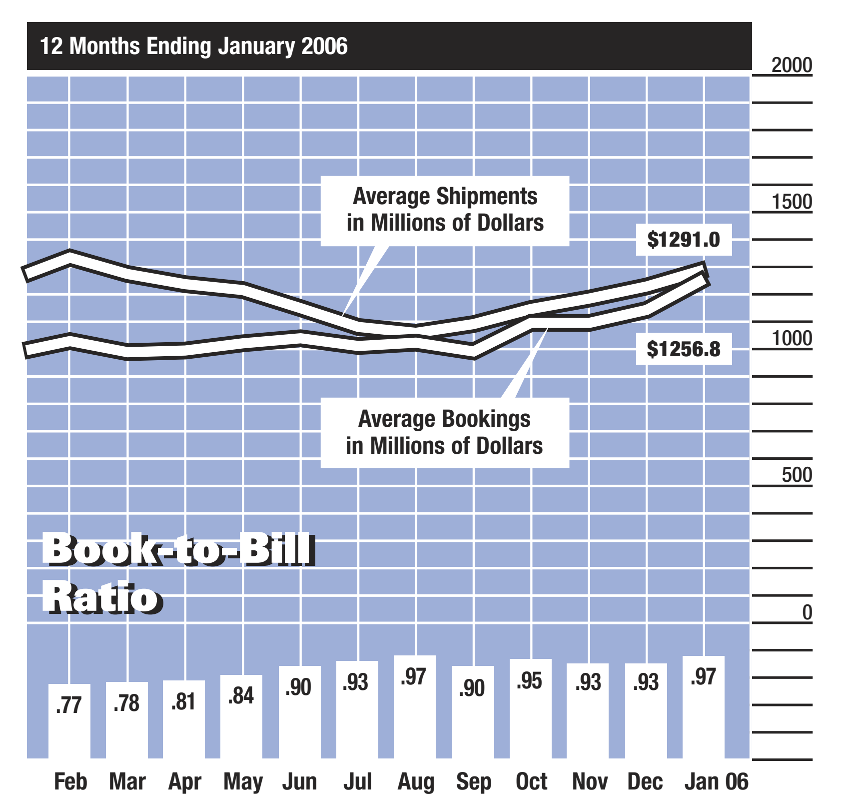
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.26 billion in orders in January 2006 (three-month average basis) and a book-to-bill ratio of 0.97 according to the January 2006 Book-to-Bill Report published recently by SEMI. A book-to-bill of 0.97 means that $97 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in January 2006 was $1.26 billion. The bookings figure is ten percent higher than the final December 2005 level of $1.14 billion and over 27 percent higher than the $986 million in orders posted in January 2005.

The three-month average of worldwide billings in January 2006 was $1.29 billion. The billings figure is over five percent above the final December 2005 level of $1.22 billion and almost three percent higher than the January 2005 billings level of $1.26 billion.

"January 2006 bookings for North American-based semiconductor equipment providers are at the highest level since November of 2004," said Stanley T. Myers, president and CEO of SEMI. "These year-end numbers reinforce the optimism in the capital equipment industry, and indicate continued momentum and steady growth for the year ahead."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

2006 Del Mar Electronics Show

Southern California's Design & Manufacturing Expo

Del Mar Fairgrounds
Del Mar, CA
www.vts.com

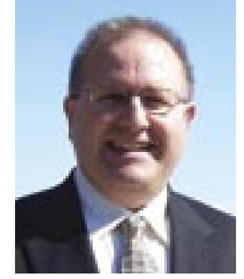
Wed. April 26
Thurs. April 27

Free Parking
Free Admission

Exhibit for only $900
includes electricity, carpet, wireless internet and an audience of over 7,000 industry professionals.

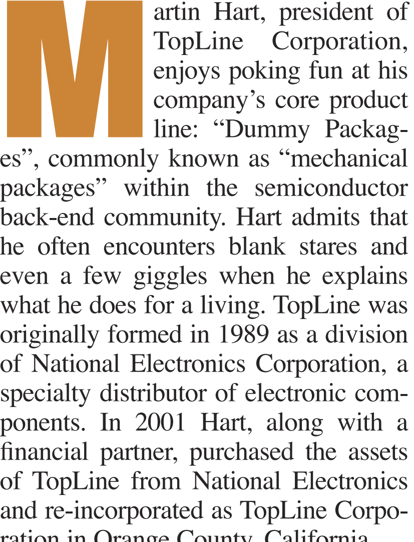
It's the RoHS homestretch! RoHS questions answered by leading national experts. Visit show web site for details and registration. Roundtable luncheon included--only $99.

www.vts.com



Martin Hart, President
TopLine Corporation

One Stop Shop for Dummy Packages



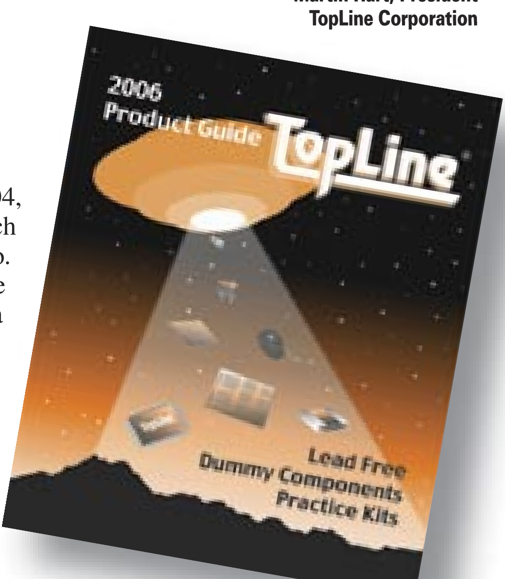
Martin Hart, president of TopLine Corporation, enjoys poking fun at his company's core product line: "Dummy Packages", commonly known as "mechanical packages" within the semiconductor back-end community. Hart admits that he often encounters blank stares and even a few giggles when he explains what he does for a living. TopLine was originally formed in 1989 as a division of National Electronics Corporation, a specialty distributor of electronic components. In 2001 Hart, along with a financial partner, purchased the assets of TopLine from National Electronics and re-incorporated as TopLine Corporation in Orange County, California.

Applications

After its fresh start, Hart expanded TopLine's product range to be a one-stop shop for dummy packages and test PCB boards. Dummy Packages are used in a variety of applications involving evaluation and calibration of handlers and equipment used in board level assembly, such as pick and place machines and soldering ovens. Dummy Packages often are assembled with a mirrored silicon die and daisy chain wire bonding (to the lead frame) to give customers a true mechanical equivalent IC package which can be used to perform vibration testing and temperature cycling after board level assembly.

Outsourcing to MEPTEC Members

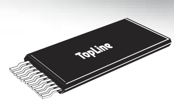
TopLine typically sources package assembly to MEPTEC member companies such as SPEL Semiconductor, Lingsen, Unisem, FlipChip International, IPAC and others. In 2004, TopLine built a BGA ball attach pilot line facility in New Mexico. Hart claims that TopLine's pilot line gives customers quick-turn on a low volume-high mix assortment of Ball Grid Array packages. Each



TopLine's 160 page Product Guide describes 500 different mechanical Dummy Packages available in SnPb and Pb-Free lead-frame and BGA.

TopLine®

TSOP - Type 1
Thin Small Outline Package



Dummy Component Ordering Information

Lead Nbr	Lead Pitch	Case Size Includes Leads	Tape Info Width	Tape Info Pitch	Tray Part Number XO1	Qty	13" (330mm) Tape & Reel Part Number XO1	Qty
28	0.55mm	8 x 13.4mm	24mm	12mm	TSOP28ST21.6-T1	234	TSOP28SE13A21.6-T1	1000
28/32	0.5mm	8 x 20mm	32mm	12/16mm	TSOP28/32T19.7-T1	156	TSOP28/32E13A19.7-T1	1000
32	0.5mm	8 x 20mm	32mm	12/16mm	TSOP32T19.7-T1	156	TSOP32E13A19.7-T1	1000
32	0.5mm	8 x 13.4mm	24mm	12mm	TSOP32ST19.7-T1	234	TSOP32SE13A19.7-T1	1000
40	0.5mm	10 x 14mm	24mm	16mm	TSOP40ST19.7-T1	160	TSOP40SE13A19.7-T1	1000
40	0.5mm	10 x 20mm	32mm	16mm	TSOP40T19.7-T1	120	TSOP40E13A19.7-T1	1000
48	0.5mm	12 x 20mm	32mm	16mm	TSOP48T19.7-T1	96	TSOP48E13A19.7-T1	1000
56	0.5mm	14 x 20mm	32mm	24mm	TSOP56T19.7-T1	96	TSOP56E13A19.7-T1	1000

PART NUMBER

Options	Suffix
Standard	Blank
Daisy Chain	-DE
Isolated	-ISO
Alloy42	A42
Lead Free	-TIN (Sn100)

Thousands of visitors come to TopLine's web site (www.topline.tv) each month to download package outline drawings and to check for new packages.

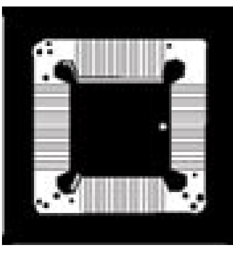
year, TopLine prints a comprehensive catalog with over 500 different packages and lead-frame finishes. Customers use TopLine's catalog an easy-to-read semiconductor package reference guide. Aficionados often remark that they still use old versions of TopLine's product guide going back over 15 years as a viable reference tool.

Open Tooled Packages

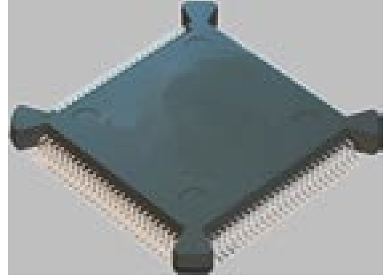
TopLine's mission is to stay abreast of the ever-evolving semiconductor package road map. As packaging foundries develop open tool for new packages, TopLine purchases such mechanical packages for its stock so that customers will have instant availability of Dummy Packages to develop feeders and handlers for board level assembly machinery. Dummy Packages provide customers a low cost solution without wasting money on expensive electrically functional ICs.

Failed IC Packages

Some new packages fizzle out and never gained market traction. For example, the TAPEPAK® MCR – Molded Carrier Ring (JEDEC MO-94 and MO-109) introduced in 1993 never achieved significant market acceptance.



The TAPEPAK is essentially a QFP (Quad Flat Pack) with flat leads secured by a molded tie-bar ring. The TAPEPAK was supposed to solve coplanarity problems cause when gull-wing QFP packages were transported. But board level customers never embraced this brilliantly conceived package because of the high cost of the equipment required to excise the carrier ring and form and trim the leads into a gull-wing shape. Another example of a failed package was The Panda Project 3-tier PQFP (JEDEC MO-198 circa



1997). Unfortunately, Panda's package got swept aside because the market favored the BGA (Ball Grid Array).

Even the ubiquitous bumper BQFP package has gone the way of the buggy whip and 8-track tapes. These obsolete packages were distributed by TopLine to assist the industry to develop feeders and handlers for placement and soldering equipment.

Niche Market

"The dummy components business is definitely a niche market", remarks Hart. "TopLine invented the one-stop venue for Dummy Packages and we have attracted a few competitors who try to emulate TopLine's panache for dummies. We work diligently to offer customers off-the-self solutions for Dummy Packages, in a world market covering 40 countries," cites Hart.

When TopLine first opened its doors in 1989, the 0.65mm pitch MQFP100 (14mm x 20mm) was just coming into limited production. At the time of TopLine's inception, no one had heard of the dummy components business. TopLine's fledgling management had no idea how many customers would be interested in buying mechanical packages. "TopLine first catalog printing was only for 250 copies," laughs Hart. Since the first edition catalog was released in 1989, TopLine has gone on to print over 250,000 copies coveted by customers all over the globe.

World Demand for Dummies

To satisfy a worldwide demand for Dummy Packages, TopLine had to create a distribution network covering 40 countries. TopLine's authorized distributors are able to log into TopLine's intranet to access real-time information on inventory stock levels, orders in the pipeline and pricing. By providing its distributor such pertinent information, customers are serviced 24/7. At any time in the world, a customer is ordering Dummy Packages from one of TopLine's authorized distributors. Throughout the North American market, TopLine has a network of 16 rep firms visiting customers. You'd think that the market would be saturated by now," says Hart, "but TopLine still opens 100 new customer accounts each month."

Lead Free Demand

"With the RoHS (Restriction of Hazardous Substances) initiative going into effect in July 2006, a new crop of customers are purchasing lead free and green mechanical packages to prove out their Pb Free board level soldering processes. Surprisingly, customers are even buying lead free throughhole (DIP, SIP, DO and TO) Dummy Packages in increasing amounts.

Typical Customers

Customer profiles cover a wide swath of the electronics industry. EMS companies such as Flextronics, Solectron, Celestica, SCI-Sanmina, Benchmark and Elcoteq are constantly improving their Lead-Free SMT assembly processes and require a wide range of mechanical packages. Process engineers at multinationals such as Hewlett Packard, Siemens, Honeywell and Thales have an insatiable need for Dummy Packages. Defense contractors such as Northrop Grumman, Rockwell, Lockheed, Raytheon and even NASA use Dummy Packages for training employees, evaluating machinery and experimentation. Socket mak-

ers such as Johnstech, Enplas, Wells-CTI and others use Dummy Packages during development and testing. Pick and place machine mounting makers such as Assembleon, Universal, Panasonic, Siemens, Casio, Techwin and a dozen others consume huge amounts of Dummy Packages while during development and acceptance testing. Surprisingly, even IC manufacturers such as Motorola, Infineon and Intel find it convenient to purchase mechanical packages from TopLine.

Customers use Dummy Packages for a wide range of applications involving test, evaluation, training, practice, trials and experimentation. More than 20 applications for using Dummy Packages have been identified, and every so often someone thinks a new use.

What's Hot?

So what types of packages are in hot demand these days? The most asked for are lead free. That includes all types: BGA, flip chips, QFN, QFP, TQFP, SOIC, SSOP, TSOP, TSSOP, and SOT. Even DIP and TO packages are requested. Often customers want the same package with different lead-frame plating: SnPb, Sn100, SnCu, SnBi and NiPdAu so that they can do comparative analyses. Array products such as BGA, CBGA, CSP and LGA are the most popular, with occasional requests for CCGA – column grid arrays. To meet customer demand for very large BGA packages, TopLine plans to expand its ball attach facility in Socorro, New Mexico. Up to 100 x 100 matrix dummy BGA packages have already been built, though most customers require only up to 44 matrix (45mm square) dummy BGA packages.

Dummy Business Growth

So what's in store for the dummy business during the next 5 years? TopLine thinks that demand for dummies will remain strong as process engineers worldwide continue to experiment and make improvements with board level assembly processes. Each time a new package comes to market or a new lead-frame alloy is introduced, demand surges as customers try to integrate it into their production portfolio. Customers, with large R&D budgets are always first to demand new packages. Over time, smaller customers and customers in developing nations follow in suite. Some customers are just now getting around to using BGA components in their board level designs. That is why they say that smart engineers do it with dummies.

For more information about TopLine, visit their website at www.topline.tv or email Martin Hart at hart@topline.tv. Calls are welcome at 949-250-4001.◆

©2005 Hyatt Corp.

INTRODUCING HYATT SAN JOSE'S NEW GRAND BED.™

Introducing Hyatt's new Grand Bed, ultra-plush pillows, the softest of sheeting, and a thick down blanket — all piled atop an irresistible pillow-top mattress. The Grand Bed, found exclusively at select Hyatt Hotels and Resorts. Beginning January 1, 2006. This is not your typical hotel story. This is the Hyatt Touch.™ For more information, call 408 993 1234 or visit **hyattsanjose.hyatt.com**.

Strip Test – Panacea or Pariah?

A Detailed Look at this Method for Handling Micro-Packages

Allan Calamoneri, Vice President
Test Business Development
Carsem

When dealing with low lead count micro-style packages, the era of multi-million dollar automatic test equipment (ATE) platforms is no longer a viable consideration to provide a reasonable end market selling price. ATE capital equipment costs for this market are now equivalent to the costs of the device handling equipment used to move the device to the testing position. The focus for cost reduction has changed from reduced capital costs to maximizing overall efficiency and utilization of capital. With this changing focus, the strip test option for handling micro-packages deserves serious consideration.

In general, most of today's micro-package devices have test times less than one second and utilize handling equipment that allows for multi-site parallel test capability. It is this multi-site capable test and handling equipment that is the primary focus of the latest efforts in maximizing overall efficiency.

To improve efficiency, one must first develop a way to measure the success or failure of a particular approach to maximizing efficiency. A simple economic model is needed that accurately determines the UPH (units per hour) of the associated handler-tester combination. Since different companies handle depreciation and fixed cost allocations differently, the UPH model is the best way to make a comparison between setups. Solution evaluators should develop 3 models over time: a theoretical model based on equipment specification and manufactures estimates, a practical model based on initial data for specific applications gathered from experts in the field, and a real model which is specific to a manufacturing location based on the systemic choices made in the design process and the learning curve experiences of the production environment. Each of these models will contain the fundamental parameters associated with UPH including per unit test times, per unit index times, per unit set-up times, per unit delay times associated with the jam-rate, per unit post processing time and finally per unit delay time associated with socket cleaning and maintenance.

A simple model starting point is **UPH = 3600/ (per unit test time + per unit index time + per unit set-up time + per unit jam delay + per unit post processing + per unit socket maintenance delay**). The test time and index time variables are independent variables and the remaining variables are dependent on lot size, which needs to be specified for a true comparison. This model becomes more complicated for strip test as the index time will vary with strip design and includes a strip-to-strip index time as well as an intra-strip index time.

With a UPH and customized economic model in hand, one can address some of the key fundamental challenges that must be overcome in order to improve and maximize efficiency. Focusing on the device handling portion of the equation will significantly reduce the scope of the overall challenge. Four primary challenges to be addressed for micro-package handling that can potentially influence the economics and overall quality in a positive way are;

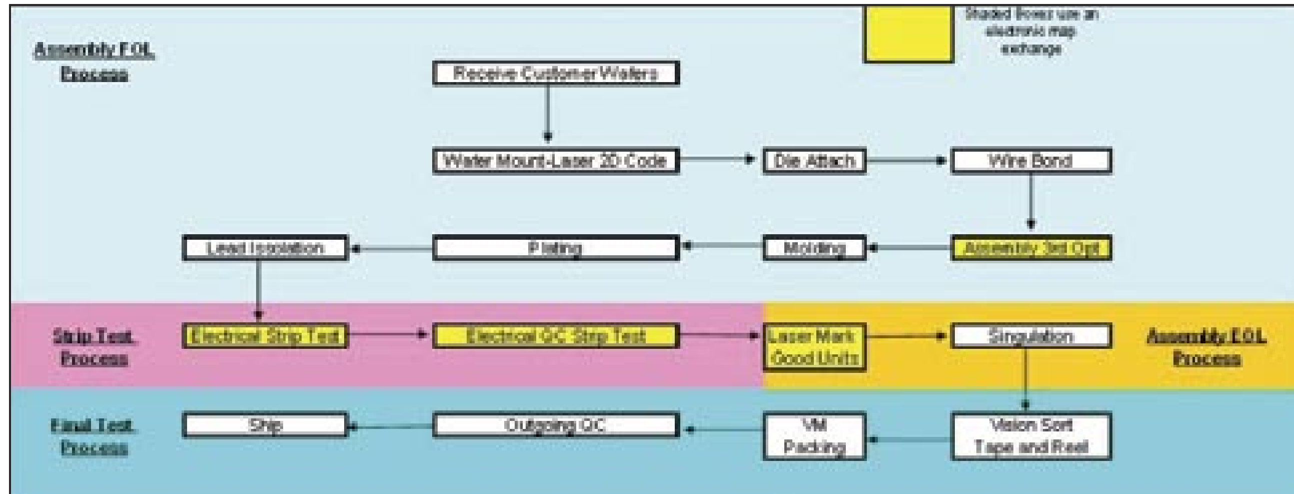
1. Mechanical tolerances and device presentation
2. Socket and contactor performance (electrical and mechanical)
3. Degree of test parallelism allowed
4. Running Efficiency (time actually spent testing devices) including device trace-ability and data integrity

The three traditional options for moving singulated devices to be tested into the test position are gravity feed, pick and place, and turret based bowl feed. There are significant mechanical tolerance challenges in dealing with tiny packages with these three handling methods.

Gravity feed handlers, which can handle up to eight test sites in parallel, have a great deal of difficulty with parts not sliding out of the tubes or parts "piggy-backing" and jamming in the gravity rails and in the contactor areas due to the light weight of these tiny packages. Recent improvements have reduced the time to clear these jams, but not the occurrence of the jams in the first place.

Pick and place equipment, also capable of supporting up to eight test sites simultaneously, has not traditionally been designed to handle these small packages, as they are primarily tray input. The high-speed motors used to move the pick and place arms on the handlers are neither repeatable nor accurate enough to provide consistent placement of the devices through the different stages of the handler. Additionally, the number of units in a single tray creates a problem if the trays are bumped causing hundreds of devices to misalign instantaneously which would be unrecoverable from a UPH standpoint.

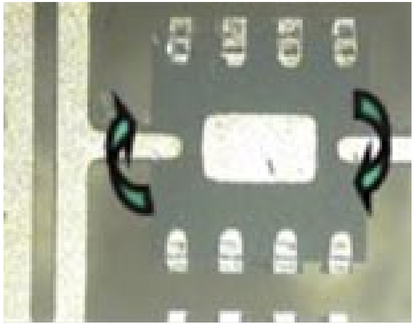
To deal with the mechanical tolerances associated with these small packages (3mm x 3mm and smaller), the bowl feed turret-based approach is the most robust industry-proven solution. The primary limitations of the bowl feed approach are the limit on the number of test site positions when a direct dock plunge to board electrical performance requirement is needed. Current technology limits this to dual site, which is far from optimal.



Most mechanical tolerance limitations for micro packages can be overcome with the strip test approach. From the process flow, you will see that strip test incorporates both the traditional assembly steps with traditional test steps.

Strip test deals with these tolerance issues by handling the devices while they are still in strip form. Equipment jams in full strip format are equivalent to a single unit. Typical mean time between jam values associated with strip test for small packages run in the range of one per 20,000 units as compared to traditional bowl feed and gravity feed numbers running one per 1,000 units. As the number of sites increases on gravity feed handlers and plunge to board bowl feed handlers so too does the number of moving parts and the associated mean time to alarm (stoppage). It should be noted that the strip test approach is very similar to the overhead wafer probe approach and jams in wafer prober indexing are almost non-existent.

Strip test does have some difficulties associated with mechanical tolerance issues, most notably post isolation, pre singulation unit tilt and misalignment, which can create problems in the socket mechanical and electrical performance.



Although the strip test flow is not devoid from problems, it is a radical change from the traditional assembly and test process, and does provide for great improvements in per unit jam delay performance.

Looking at the test contactor and the time-to-change, clean and replace contacts can also have a significant impact on the overall equipment efficiency. Typical equipment efficiencies measured by the actual time spent doing initial prime insertions is defined as the first pass yield. In general, for typical devices and current handling methods these efficiencies run in the 60-70% range. Typical efficiencies and first pass yields for strip test are in the 80-90% range.

The number of socket insertions between cleaning will vary, but for modeling purposes, 10,000 insertions can be assumed for traditional handling methods. Socket pins typically last on the order of 250,000 insertions. In addition, new lead (Pb) free solders have impacted the number of insertions between cleanings and the total number of insertions allowed before the individual socket pins fail. Socket pin replacement cost has become a significant factor in the total cost of test.

Since the strip test process contacts the device from above, the amount of cleaning required is reduced and practical numbers for pogo pin based contactors on a strip handler run 20,000 insertions and the pins can be insitu auto-cleaned significantly reducing the socket maintenance delay parameter and thus increasing the UPH. There are still problems associated with strip test contactor performance including solderability issues especially for Kelvin contact, but these issues can be dealt with by design such as testing leaded devices in live bug rather than dead bug position.

Another concern is the degree of parallelism or multi-site capability associated with each of the different small package handling methods. As stated earlier, the multi-site capability of the traditional micro-package handling methods tops out at octal (8) site. For strip test handling the magnitude of parallelism is no longer limited by the number of test sites available on the handler because the handler's software is capable of handling up to 128 sites. Additionally, the overall parallelism and strip processing efficiency can be dramatically improved upon if the design of the strip optimizes the number of devices that can be tested at once and this should be balanced with the number of intra-strip indexes that need to be done. This design process can also favorably impact the per unit index time parameter. Index times associated with pick and place and gravity feed handlers are equivalent to 0.5 seconds per group of devices. In contrast, bowl feed handlers index in 0.38 seconds, but typically index one unit at a time. Plunge-to-Plunge index times for strip

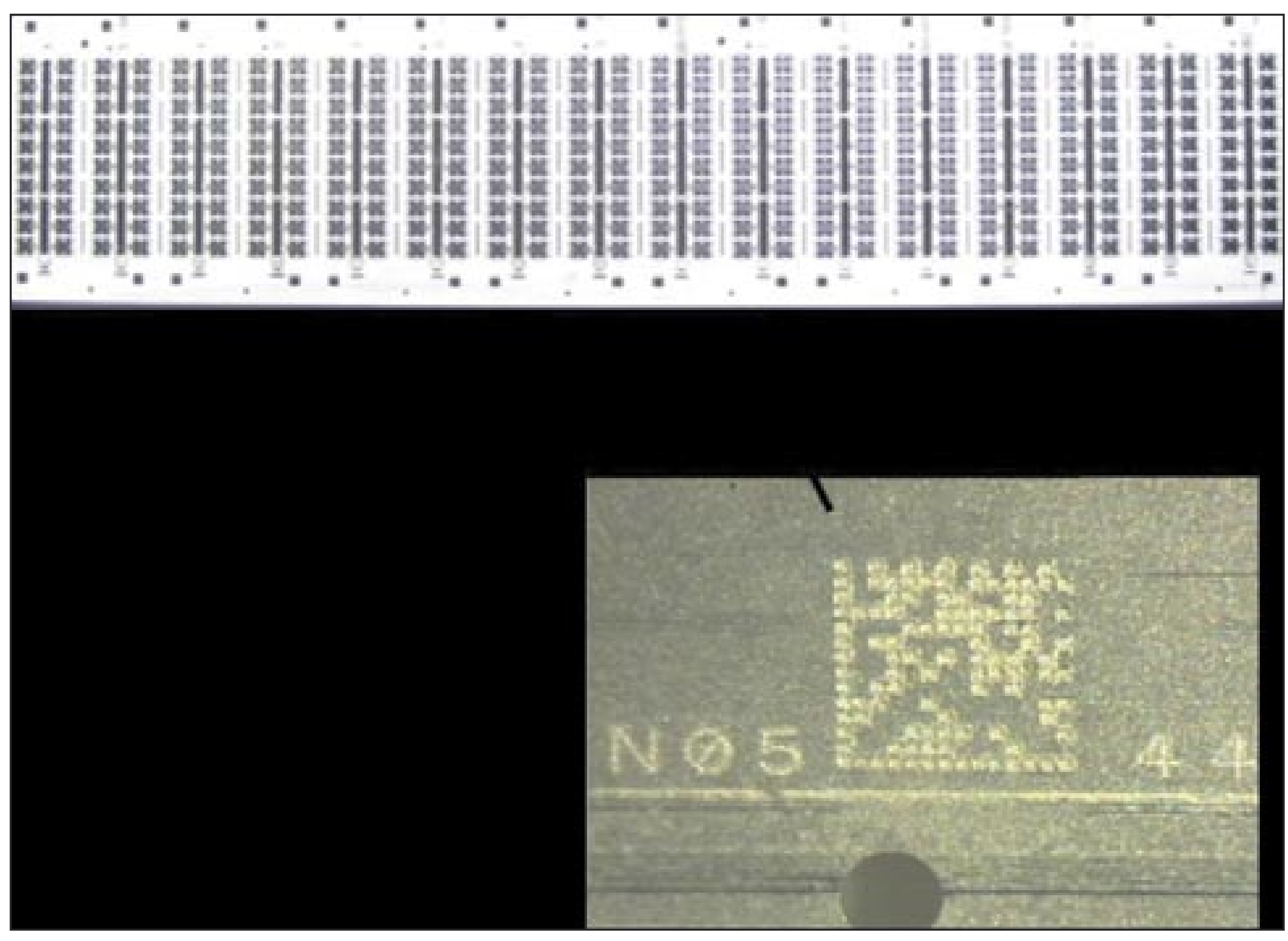
test handlers are about 0.2-0.3 seconds for intra strip indexing for moves of less than 17mm. Strip to strip index times are 3.0 seconds or less. With typical device strip counts in the hundreds, the strip-to-strip index times are considered negligible.

The final challenge to be addressed is the running efficiency, which is dominated by the set-up time and post processing time parameters in the UPH equation. Strip test change-over times are similar to other handling methods, but since typical strip test set-ups can have UPHs over 90,000, the per unit set-up times are long relative to the actual time it takes to test a lot. The UPH modeling parameters are greatly impacted by lot size for the strip test approach. Additionally, the amount of production material required to maintain a set-up is also quite large. Since large lot sizes and high volume are required to maximize the efficiency of this handling method, strip test may not be the panacea for many products, especially lower volume products. With this understanding, rapid changeover processes, similar to a racetrack pit crew, can improve the number of applications where strip test is used. As greater experience is developed, the UPH model can assist in determining the best approach for each given application.

Currently, the strip test approach for device handling is seen as an industry value added approach with the benefits being shared by subcontractors, the equipment manufacturers and the semiconductor customer. Although the strip test flow is a radical change from the traditional assembly and test process, is does provide for an improvement in the data integrity and die trace-ability. It is this data integrity and die trace-ability portion of the running efficiency challenge that will drive the next several years of the test time parameter and UPH improvement processes.

Using the Two D Bar code on each strip and overcoming some minor software challenges, data integrity and die trace-ability from (x,y) wafer location all the way to final test can be achieved. This new focus, called adaptive test, will help make test runtime decisions based on individual device data acquired in previous manufacturing steps. This is one of the greatest opportunities to improve the overall efficiency of the test and assembly process and is driven by the strip test approach.

In conclusion, the many challenges associated with micro-package handling have been met with a myriad of solutions over the last several years, but with the new focus on increased efficiency and capital utilization, no single solution provides greater potential to maximize efficiency and improve capital utilization like testing the devices while they are still in strip format. Strip test has improved micro-package handling by systematically addressing each of the parameters associated with the theoretical, practical and real UPH models and provides the functionality for future improvements through die trace-ability and support for adaptive test methods.◆



C4NP – A New Solder Bumping Technology

Emmett Hughlett, Ph.D, Eric Laine and Klaus Ruhmer, SUSS MicroTec, Inc.
Dietrich Toennies, Ph.D, SUSS MicroTec Lithography GmbH
Peter Gruber, IBM Microelectronics

More and more high-end microelectronic devices are being packaged by using solder bumps as the method of interconnection. The two main technologies used are FlipChip in Package (FCiP) and Wafer Level Chip Scale Package (WLCSP). The main difference is that FCiP devices are placed on a substrate which then interconnects to the PC Board (PCB). WLCSP devices connect directly onto the board.

There are various solder bumping technologies used in volume production. These include electroplating, solder paste printing, evaporation and the direct attach of preformed solder spheres. FCiP demands many small bumps on tight pitch whereas WLCSP typically requires much larger solder bumps. All these established technologies have important limitations for fine pitch bumping especially when it comes to lead-free solder alloys. The most commonly used method of generating fine-pitch solder bumps is by electroplating the solder. This process is difficult to control and costly, especially when it comes to lead-free solder alloys. These challenges in the transition to lead-free solder bumping has led the European Union to grant exemptions from the ban of lead in certain solder bumping applications. However, the pressure to move to lead-free continues for the entire industry.

C4NP (C4-New Process) is a novel solder bumping technology developed by IBM and commercialized by Suss MicroTec. C4NP addresses the limitations of existing bumping technologies by enabling low-cost, fine pitch bumping using a variety of lead-free solder alloys. C4NP is a solder transfer technology where molten solder is injected into pre-fabricated and reusable glass templates (molds). Mold and wafer are brought into close proximity and solder bumps are transferred onto the entire 300mm (or smaller) wafer in a single process step. C4NP technology is capable of fine pitch bumping while offering the same alloy selection flexibility as solder paste printing. The simplicity of the C4NP process makes it a low cost solution for both, fine-pitch FC in package as well as WLCSP bumping applications.

Process Flow

Traditional wafer bumping technologies such as solder paste screen printing, electroplating or evaporation are implemented using a wafer processing line. Every wafer runs through a sequence of processing steps depending on the particulars of the technology used. C4NP utilizes a significantly different approach. Instead of processing wafers through a series of steps, so called molds or solder bump templates are being processed. The wafer itself only gets exposed to one single process step during solder transfer.

The molds are manufactured out of thermally matched glass and are standardized in size. A 14” x 14” mold is used to bump 200mm or 300mm wafers.

Mold plates are covered with an array of etched cavities representing the particular bump pattern of the wafers processed. The volume of the individual cavities must be accurately controlled as they directly influence the bump height and bump size after solder transfer. Molds are manufactured using a wet-etching process. The C4NP processing line incorporates the following main process steps (Figure 1):

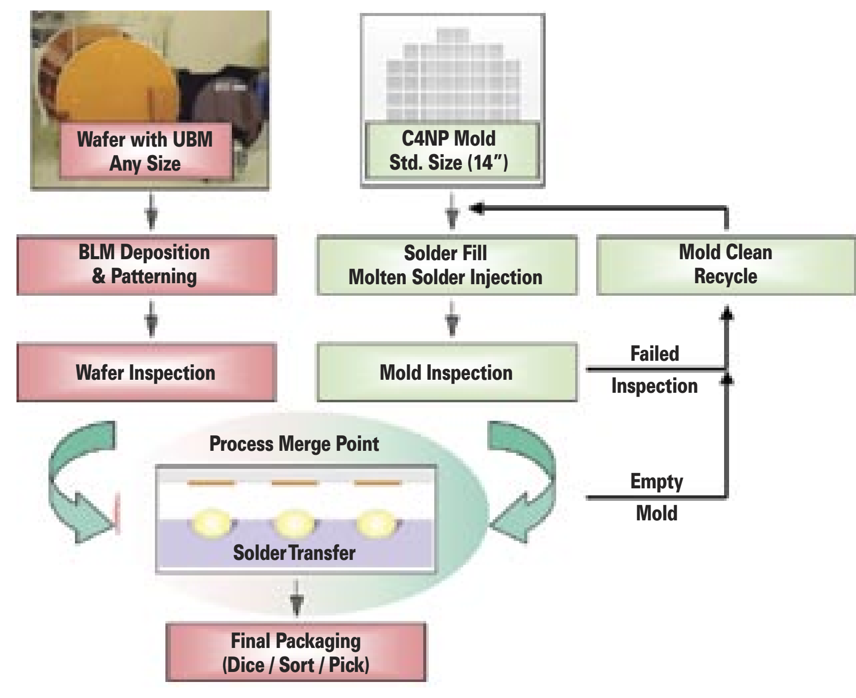


Figure 1: C4NP Process Flow

Step 1: Empty Mold:
A batch of empty molds is brought to the line.

Step 2: Mold Preparation:
During Mold Preparation, the empty molds are being filled with molten solder via a unique Mold Fill Tool (MFT). In addition, the filled molds are automatically inspected using the Mold Inspect Tool (MIT) for a variety of fill defects.

Step 3: Mold Stock:
The filled molds are stocked until wafers are available for solder transfer.

Step 4: Solder Transfer:
During solder transfer, the previously prepared wafer meets the filled mold. Wafer and mold are being aligned and an in-situ thermal transfer and reflow process creates all solder bumps over the entire wafer in one process step.

Step 5: Mold Clean:
After solder transfer, the molds are being cleaned via a standard wet cleaning process and recycled for the next process sequence.

Manufacturing/Reliability Data

Early manufacturing data from IBM shows the C4NP process to be very robust. For a 200mm wafer with 14.7mm square chips and over 280,000 bumps per wafer, measured bump heights were 101.3 um, with a 2.7 um sigma. This tight distribution is due to the precise volume control enabled by the mold making process. This wafer pattern was a 225 um pitch array design.

Initial reliability data on both Pb/Sn and lead free solders shows no inherent failure mechanisms attributed to the C4NP process. This includes JEDEC Level 3 and 4 preconditioning, DTC (-40 to 115˚C), ATC (0 to 125˚C), HTS (150˚C), HAST (110˚C, 85% RH, 3.7V), and DTC (-55 to 125˚C). This is as expected, since the ball shear strengths for C4NP and plating are equivalent, even after multiple reflows.

An interesting feature of the C4NP process is that a defect after mold fill does not necessarily result in a defect as transferred to a wafer. The C4NP process has produced wafers at less than 10 ppm defective after solder transfer on a consistent basis.

Suss is now designing and building the first high volume tool set, capable of more than 300 wafers per day. This will involve robotic handling of the wafers and a cluster concept for the solder transfer operation, which is the gating process.

A detailed cost model has been developed which accommodates many inputs. This allows users to compare bumping costs, capital, and expense funds for various wafer bumping options. Input fields for the cost model include wafer starts per day, part number mix, chemical distribution and waste costs, equipment depreciation, direct and indirect labor costs, yields, and many other parameters. This allows the model to be customized for a particular customer application.

Advantages and Challenges of C4NP Technology

The approach of processing molds instead of wafers for the purpose of generating solder bumps on wafer level has several intrinsic advantages over alternative technologies. The main advantages are reduced cost and full flexibility with regards to lead-free solder alloy compositions. In addition, C4NP enables the reduction of solder ball size and ball pitch meeting the roadmap requirements for process generations to come. Last but not least, a solder transfer process such as C4NP minimizes the number of steps on the valuable wafers. Fig. 2 displays a qualitative list of criteria important for wafer level solder-bumping.

The challenges are largely surrounding the topic of mold cost and mold supply. Every wafer design (part number) requires multiple glass molds. These molds have to be manufactured and will have to be managed and stored within the wafer bumping operation.

In addition, C4NP represents an entirely new way of wafer bumping. The inherent challenges of building up a worldwide infrastructure and generating industry wide acceptance of the technology have to be addressed.

Conclusion

C4NP Technology is a new way of bumping wafers. It holds advantages over existing wafer bumping technologies by lowering cost and enabling lead-free. There are also challenges associated with the technology which will have to be addressed. Initial manufacturing and reliability data show the technology to be very robust. Scale up to high volume manufacturing is well underway. A detailed cost model is available to assist potential users in comparing the economics of C4NP versus other bumping technologies. ◆

Eric Laine *is a C4NP Technology Specialist for Suss MicroTec, supporting global sales and marketing. He holds a Bachelors degree in Chemical Engineering and a Masters in Advanced Technology. He has over twenty years of experience with IBM in electronic packaging manufacturing and development, and multiple patents.*

As Director at SUSS MicroTec, **Klaus Ruhmer** *is responsible for Global Sales & Marketing of C4NP Equipment. Klaus, a native Austrian who came to the US in 1996, holds a bachelor degree in Electronics and has worked in the semiconductor equipment industry for over 10 years. Klaus started out as a service engineer and developed his career through various technical and sales positions within SUSS.*

Criteria	C4NP
Equipment Cost	Competitive
Equipment Space	Industry leading
Facility Requirements	Minimal wet chemistry
Chemical Usage	Minimal wet chemistry
No. of process steps on Wafer	Industry leading
Wafer Turn-Around Time	Industry leading
Pitch & Bump Size	FCiP to WLCSP
300mm Capable	Yes
Lead Free Capability	Multiple alloys
Voids	Industry leading
Infrastructure	In progress
Industry Acceptance	In progress
Process IP& Royalties	License

Figure 2: Advantages and Challenges of C4NP

The 56th Electronic Components and Technology Conference

May 30 - June 2, 2006

Sheraton San Diego Hotel & Marina

San Diego, California

The only event that encompasses the diverse world of integrated systems packaging

HIGHLIGHTS

- 38 technical sessions, including 2 poster sessions
- 16 CEU-approved professional development courses
- Technology Corner Exhibits, featuring more than 70 industry-leading vendors
- Emerging Technology Sessions, including Biomedical, Nano-Scale and Organic Device Packaging
- Panel Discussion – 3D Interconnect
- Plenary Session – Packaging Solutions for Future Technologies
- Third iNEMI Workshop on Tin Whiskers
- CPMT Academic Conference

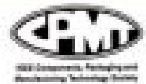
More than 300 technical papers covering:

- Advanced Packaging
- Modeling & Simulation
- Optoelectronics
- Interconnections
- Materials & Processing
- Quality & Reliability
- Manufacturing Technology
- Components & RF
- Packaging Education

Don't miss out on the industry's premier event. For more information, visit:

www.ectc.net

CONFERENCE SPONSORS:



Hysol LOCTITE Multicore

Henkel News

Stress Free Technology

March 2006

Henkel

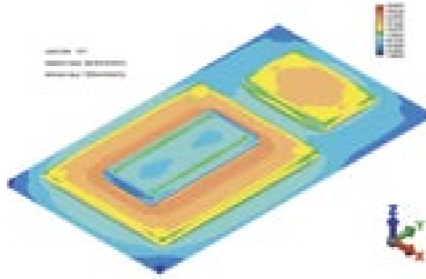
Material Sets Deliver Tested, Reliable Compatibility and Significant Cost Reductions

Michael Todd, Ph.D., Electronics Group
Henkel

As the industry continues to move toward smaller devices with increasing time-to-market demands and the changing regulatory challenges of "green" and lead-free manufacturing, creating a reliable package cost-effectively is arguably one of the biggest obstacles to overcome in today's semiconductor packaging market. In the abbreviated product development cycle that is characteristic of most new devices, packaging specialists must design, prototype, test and build new products while ensuring guaranteed material compatibility and long-term reliability – a monumental task to say the least.

As defined, a material set is a group of materials such as mold compounds, die attach materials, underfills and encapsulants that are all specifically designed to work together in a synergistic manner to provide maximum product reliability. Traditionally, material set compatibility testing has been conducted in-house with various materials tested one against the other for synergistic properties. This, though, can be very time and cost intensive as a new package design with three different materials puts incredible testing demands on the engineer. Materials have to be sourced from two or three different suppliers and all of those materials – which can amount to nine different sets of materials or more – have to be tested for various levels of reliability. When one considers the amount of time and cost involved in this process, it is obvious that a robust and cost-effective solution to material set development is long overdue.

Much like the product design and manufacturing outsourcing efficiencies that have been realized by OEMs in the electronics market, the same approach is now attracting attention and delivering a viable solution for the development of new devices and compatible material sets. Many electronic device manufacturers are engaging with materials developers and suppliers who can provide products designed to work together as a reliable and cost-effective material set and supported by a global applications group. Essentially, with this approach, the need for multiple product evaluations and vendor approvals is eliminated.



An example of a computer generated Stress Field for a Non-Optimized Material Set.

In practice, the viability of this approach is being validated everyday. One recent example of the benefits realized through compatible material set development was put forth by the electronics group of Henkel and is just one example of how a material supplier's product expertise can deliver a material set solution for outstanding product reliability. Lab data has validated testing that confirms that stress on a mold compound (MC) can be predicted by varying the dimensions and design of the die attach (DA) material, proving that the stress on one material is significantly affected by changing the other material in a DA and MC material set. From this data, compatible and tested material sets have been developed for various applications. Henkel has developed numerous other material sets that are designed to deliver robust performance, compatibility and long term reliability.

However, let the buyer beware. While there are many suppliers who "supply" more than one material, the material set approach is only viable if that supplier can deliver real cost reduction through unmatched engineering expertise, synergistic material set testing, reliability testing, state-of-the-art facilities and total global support. A material set development program should include the following resource: full production capabilities to simulate actual electronic production, reliability testing facilities, complete application engineering capabilities, electrical test resources and failure analysis facilities.

In addition to these resources located in one, streamlined facility with a full staff of technical experts, material set design and development should comprise Finite Element Analysis (FEA) design to determine the materials influence on interfacial stresses and package warpage, material system development to optimize overall package stress through material property design and develop compatible material systems, package and application testing to determine performance capabilities and material compatibilities, and material set process optimization to optimize process parameters and process windows while providing new process technologies.

Having all of these factors in place will reduce product development cycles of robust, reliable products at significantly lower costs. Customers should expect their materials partners to offer extensive resources, high levels of expertise and the ability to provide compatible material sets for emerging package requirements. Henkel is breaking new ground in this area and currently is one of the only materials suppliers worldwide with these broad capabilities. As the industry transitions to more complex products, more challenging technologies and increasing regulatory demands, only those suppliers with the expertise to partner with customers from product design through to production and provide global support will be successful. ◆

Hysol® LOCTITE® Multicore®

Not enough hours in the day?

Henkel's material sets let you get back to more *'important'* office work.

"So much to do, so little time" is a common dilemma for today's manufacturers. But, it need not be this way. Henkel's material sets will save you time for more pressing concerns.

Can you really afford to spend the time necessary to qualify, test and guarantee compatible products? If not, mistakes are inevitable. Fortunately, Henkel's Material Sets solve this dilemma by delivering proven package performance - stress reduction, compatible chemistry and material interface designs. Using the cross-qualified Hysol mold compounds, QMI die attach adhesive and underfills, this complete solution saves you up front design time and reduces overall maintenance time and costs. And you get the support of a world-renowned electronics specialist – Henkel is the Single material solutions provider you've been waiting for.

Henkel Americas: +1 949 789 2500 Henkel Europe: +44 1442 278 000 Henkel Asia: +852 2233 0000

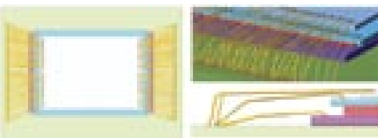
electronics.henkel.com

CAD DESIGN SOFTWARE'S

TRUE 3D DESIGN TOOLS...

ARE WHAT INNOVATIVE DESIGNERS ARE USING.

Problem Hidden in 2-D   Problem Solved in 3-D



Hidden manufacturing problems can be discovered before manufacturing with TRUE 3-D software design tools.

Bondwire Optimization, DRC and Placement Tolerance Issues

are addressed in design...exactly where they should be, AND...you will experience design time decreases of up to 50% using CDS's EDA solutions. Order your FREE demo and experience the power of **TRUE 3D**.

Call 1-877-CAD-USER or email sales@cad-design.com

www.cad-design.com

Microelectric Design & Turnkey

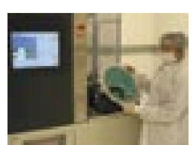
BGA, CSP, SIP, Stacked Die, RF, DUT, High Speed & Composite PCB Subtrate, Interposer

Singulated Technology is a printed circuit substrate design & engineering firm delivering quick-turn chip package (BGA) design, engineering & simulation services.

www.singulated.com

email@singulated.com

NOW! 300mm WAFER DICING



CORWIL is the leader in wafer backgrinding, wafer dicing and visual inspection to commercial, military and medical specs. CORWIL's newest addition in dicing equipment is a fully automatic, latest state-of-the-art 12 inch dicing saw that strengthens CORWIL's technical leadership for chip-free and fast turn-around dicing. CORWIL dices Si, GaAs, Sapphire, SiGe, laminates and many other materials and CORWIL is unsurpassed in IC assembly in ceramic, BGA, flip-chip, and MLF/QFN type packages.

- **High Volume – millions of dice per month.**
- **Automatic High-Speed Pick & Place**
- **Automatic Vision Inspection Systems**
- **Low K, MEMS and Optical/Imaging wafers processed**
- **Experts in Multi-die Type Wafer dicing**
- **Highest Quality and Best Service in the Industry**

Since 1990 CORWIL has built its reputation providing customers with:

Excellent Quality and Superior Service

Phone 408-321-6404 • Fax 408-321-6407

www.corwil.com

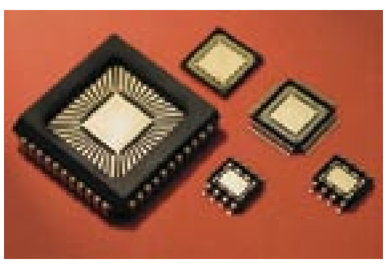
ELLE TECHNOLOGY

Elle Technology is a focused provider of niche Semiconductor Products and Services.

- Assembly & Test: PDIP, SOIC, SSOP, TSSOP, QFN
- Package Assembly: PQFP, BGA, COB, SiP, MCM, WLP
- Test Programming & Development, Load board and DUT Board Design
- Open Cavity Packages for Quik Proto-types in Plastic or Ceramic.
- BGA & SiP Substrate Design, Simulation & PCB Design
- Used Assembly Equipment – Wafer Saw, Wire Bonders, D/A, Ovens, etc.

For further information call our Silicon Valley Office at (408) 582-3531.

info@ellecorp.com



Off-the-Shelf Package Solutions for Quick-Turn Test and Prototyping

Premolded Plastic Packages

- QFN, LQFP, PLCC, and SOIC
- Ideal for RF, MEMS, and Sensors
- Custom molding services available

Ceramic/Hermetic Packages

- Sidebraze/DIP's, PGA's, CQFP's, LCC's, SMD's and matching lids
- Extensive Technical Data Online

916-853-9300

www.icpackages.com

HANA Microelectronics

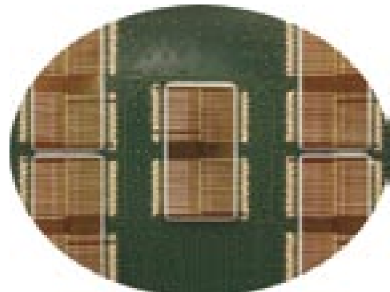
Servicing the Semiconductor Industry for over 25 years with manufacturing locations in Thailand and China.

- Specializing in Low Pin count Plastic Packages
- Ceramic and Laminate LGA's
- Standard and Custom QFN's
- Custom Package Development for Sensor Applications.
- Full service Semiconductor processing including; Back Grinding, Wafer Saw, Packaging, Test and Drop Shipment coordination
- Lead Free, Green and RoHS compliant Packages available
- QS9000, TS16949, and ISO14001 Certified

For more information visit our website or call Bruce Stromstad at **408-467-0911**.

www.Hanagroup.com

U.S. BASED IC ASSEMBLY For BGA-CSP-LGA PACKAGES



ENGINEERING - PROTOTYPE - PRODUCTION

Hestia Technologies, Inc.: If your packaging requirements call for an organic substrate package with a single or multiple die, contact Hestia for its innovative and refreshing approach to packaging. Hestia can provide just the packaging service or provide a complete turnkey package from design through engineering, prototype and production volume packages from our Santa Clara, California facility.

Contact Hal Shoemaker at (408) 844-8675 for more information about our services.

www.hestiatechnologies.com

TEMPERATURE DATA RECORDERS

Marathon Products, Inc. headquartered in Oakland, CA. is a global supplier of investigative temperature recording devices used to validate shipments of epoxies, laminates and other critical materials used in the manufacture of integrated circuits. Temperature operating ranges: -80˚C to 72˚C. Our devices are programmed in English, Japanese, French, German, Spanish, Mandarin, and Portuguese to support globalization. Make C\TEMP your last QC gate for product validation prior to acceptance of critically-sensitive materials for manufacture.

Don't ship without us®

866-848-8002

www.marathonproducts.com

NAMICS

Underfill for Your Current and Future Requirements

- **Low K Die**
- **Lead Free Bumps**
- **Fine Pitch**

Namics Corporation is a leading source for high technology underfills, encapsulants, coatings and specialty adhesives for use by the producers of semiconductor devices. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe and China, the company serves its worldwide customers with enabling products for leading edge applications and superior technical support.

For more information visit our website or call **408-907-8430**.

www.namics.co.jp

Challenge Your Assumptions! It's a QFN World NOW.

In its day – 1944 – the Electronic Numerical Integrator and Computer (ENIAC) was a marvel of science.

But today's QFN format from NSEB delivers packages with these attributes:

- Faster, lighter
- Lower thermal resistance
- Larger die in same footprint
- No bent leads
- Production available in several thicknesses (0.85mm, 0.75mm and 0.50mm nominal)
- MSL level 1 @ 260°C up to 12×12 (green and lead-free)
- Test and probe services available
- World-class quality and cycle time

If you're ready to develop advanced packages using our reliable sawn QFN package format, contact NS Electronics (USA) at (408) 749-9155, Email: jkirby@nseb.com.

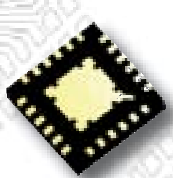
www.nseb.com

LEAD FREE SOLDER SPHERES

Profound Material Technology Co. Ltd. is a producer of high quality solder spheres for BGA and CSP packages and other interconnect applications. Our solder spheres are available in alloys from eutectic to lead free, in a variety of diameters to meet your requirements and applications. Our flexible approach enables us to meet your solder sphere requirements by supplying a high quality product with low oxidation, highly accurate sphere diameter and sphericity, better oxidation resistant along with quick delivery. Our factory is ISO 9001, ISO 14001 and QS 9000 certified. Visit our website or contact Hal Shoemaker at (408) 969-9918 for more information.

www.profound-material.com

COST EFFECTIVE ALTERNATIVE TO CERAMIC PACKAGING



SEMPAC, Inc. designs and manufactures Pre-Molded, Open Cavity Plastic Packages. Our focus is on developing standard air cavity packages that meet JEDEC outline and footprint standards that are easily customized. SEMPAC's products provide an ideal choice for IC Die qualification, Prototype & Test applications, and device packaging for MEMS, Optoelectronic, RF, Sensor and Telecommunication devices.

Phone: **408-400-9002**
Fax: **408-400-9006**
Email: **sales@sempac.com**

www.sempac.com

AuroStan H

Gold-Tin Alloy Plating Process

AuroStan H plating solution is formulated to deposit semi-bright to bright eutectic Gold Tin alloy.

Features & Benefits

- AuroStan H deposits eutectic or near eutectic alloy from 5 to 7.5 ASF.
- Excellent electrolyte stability
- Excellent solderability characteristics
- Compatible with most photoresist systems
- Reflow Target Temperature 280C° - 320C°

www.technic.com
info@technic.com
(714) 632-0200

Best in Class Dummies

TopLine® is the original one-stop-shop for mechanical samples (AKA Dummies). Dummy packages are used during set up for evaluation and calibration of board-level assembly and soldering equipment. TopLine has delivered 500 million dummy packages to 6000 customers in 40 countries during the past 16 years. TopLine out-sources fabrication to MEPTEC member companies.

Thank you MEPTEC!

(800) 776-9888

www.topline.tv

ON-SHORE ADVANCED ELECTRONICS SERVICES FOR ENTREPRENEURS, GOVERNMENT APPLICATIONS, AND LOW VOLUME PROPRIETARY CUSTOMERS

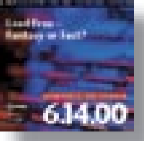
- Design, engineering, prototyping, and production of Tessera μBGA™ chip scale packages (CSP), chip stacking, MCM, and SiP
- Design, engineering, prototyping and production of dense, miniaturized electronic Systems
- Legacy system upgrades
- Sensor networks
- Cold climate qualification
- R&D, consulting, training

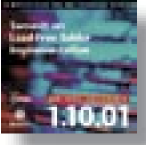
e-mail: p.karulkar@uaf.edu, karulkar@ieee.org, or fyoem@uaf.edu
or call (907) 455-2008 or 455-2000

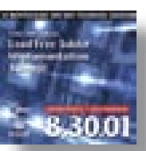
NOW AVAILABLE

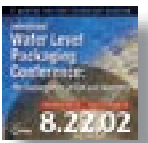
MEPTEC Symposium Proceedings on CD

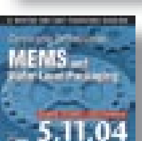
MicroElectronics Packaging and Test Engineering Council

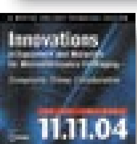












Symposium titles include: *Lead Free- Fantasy or Fact? / Summit on Lead-Free Solder Implementation / From Micro-P to Opto-E ... / Lead-Free Solder Implementation Summit / 2002 – The Year of the Ultra-Thin Wafer / The Opto-Mystic Industry - Packaging, Assembly & Test in OptoElectronics/ International Wafer Level Packaging Conference / Package Systems - Substrate Trends and Challenges / Packaging, Assembly and Testing in RF Technology / MEMS and Advanced Packaging Technologies / Where the Component Meets the Board - Package Reliability Issues / Packaging Industry Roadmaps / SIPs or SOCs? - The Multi-Million Dollar Question / Converging Technologies - MEMS and Wafer Level Packaging ... and more!!*

Visit www.meptec.org for more information and to Order Today!

APRIL 2006

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
2 **DAYLIGHT SAVINGS TIME BEGINS**	3	4	5	6	7	8
9	10	11	12	13	14	15
16 **EASTER**	17	18	19 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley	20 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	21	22
23	24	25	26 **2006 DEL MAR ELECTRONICS SHOW** April 26 - 28 Del Mar Fairgrounds, San Diego, CA	27	28	29

MAY 2006

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
30	1	2	3	4	5	6
7	8	9	10	11	12	13
14 **MOTHER'S DAY**	15	16	17 **MEPTEC MEMS PACKAGING TRENDS SYMPOSIUM** Hyatt San Jose, San Jose, CA	18	19	20
21	22	23	24	25	26	27
28	29 **MEMORIAL DAY**	30 **ECTC 2006 - THE 56TH ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE** May 30 - June 2 Sheraton San Diego Hotel & Marina, San Diego, CA	31	1	2	3

JUNE 2006

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
4	5	6	7	8	9	10
11	12	13	14 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley	15 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	16	17
18 **FATHER'S DAY**	19	20	21	22	23	24
25	26	27	28	29	30	

Industry and Academic Partnership

Dan Neinhauser, Director of MacroTechnology Works
Arizona State University

You might be asking yourself, why is an academic administrator contributing to this report for MEPTEC? I would imagine that a number of you, upon glancing at the byline, are leaning towards a quick closure of this Q1 report. Understandable. The world of academia does not typically have the best record of contributions to the "real" or industrial world. But that is something we wish to change. If we have any hope of continuing to lead globally, we must forge strong relationships between academia and industry.

A handful of institutions define the current gold standard for research universities. Some fortunately are now proposing that a retooling of the traditional static organizational paradigm of the research university is needed. How will universities best evolve to respond to scientific discoveries, technological innovations and the societal challenges that confront us? At Arizona State University (ASU), we are building a solution-focused university that is linked to its community and the needs of the world outside our classrooms and labs.

How does this apply to you? Let me first discuss some of the changes that we see happening in the marketplace(s). We are witnessing a rapid convergence of disciplines, markets and competition that has never before transpired in a single generation. Traditional "industry" lines are blurring – "nano" is sneaking into everything without a particular home, electronics and packaging are becoming a major issue in the medical arena and wireless communications and sensing devices are enhancing an unlimited number of products and services. All this convergence will undoubtedly usher in new, and sometimes complex, questions and problems.

Global competition is occurring at breakneck speed rapidly changing… again and again… in almost every facet of our daily lives. We put the fiber optics under the oceans and drove many aspects of the internet revolution that is now the superhighway for globalization. In Asia, government-industry-academic consortiums are frequently synchronized, and financed, around specific answers to problems. The number of engineering graduates annually coming out of India and China are staggering (combined more than 400,000 in '04)... and by 2025 if not sooner their universities and students are going to begin to challenge many of our academic institutions.

So, what are the problems you need solved? What are your customer's needs? How is the solution best translated to a product or platform? These questions are not common in today's university research lab. For a new American University there should still be traditional, disciplinary specific research – but excitingly, especially for industry, there should also be answers to questions and problems. The bottom line: academics and industry professionals working to deliver specific answers for specific problems.

If we have any hope of continuing to lead globally, we must forge strong relationships between academia and industry.

Universities need your involvement, your counsel, your customer "needs", your problems, your quality systems demands, your manufacturing scale expectations. Some universities may not want it, but that doesn't mean they don't need it, at least some of it. A side benefit? Better trained and brained graduates that have what it takes to fuel innovation in your industries.

Obviously, most of your challenges are being solved internally, or with your vendors and partners. But as we move to a world with medical devices that include electronics, sensing, wireless communications and some bio component, and might be implantable; is your infrastructure and knowledge base going to suffice? As the competition with electronics and wireless and sensing companies, or goverment-univiversity-industry consortiums in Asia heat up, is it going to be enough to "go it on our own"? When transistors on malleable plastic and flexible displays become scalable and affordable, how will your design and production requirements be impacted?

By exchanging ideas, scientists, product developers, project managers, and engineers – into and out of applied academic environments with industrial ones – "we" will be better able to solve problems and answer questions. We will even be able to anticipate new questions and challenges that we never even contemplated.

Innovation is most applicable through the recombination of existing technologies and knowledge. A medical bladder inserted into a shoe and voila, a new "pump" product line. Symbiotic opportunities exist for universities and industry, to conduct research and nurture education in ways that we would have never thought of – by recombining your knowledge and insights into how we act. And industry stands to gain by leveraging both the infrastructure and know-how that our neutral playing field has to offer, as well as fresh student insight and answers to improve "their" world.

There are positive signs at the university level. MIT Media Lab just recently hired an entrepreneur, with 25 years of industrial experience, as its new Director. The Biodesign Institute at ASU, under the leadership of a visionary with 25 years of industrial and 10+ years academic experience is advancing innovation in life sciences with collaborative multidisciplinary partnerships in the (Phoenix) Valley – merging science and engineering to design critical technology solutions with an equally diverse cross-section of industrial partners.

A brave new world of innovation is on the horizon. Are we ready? We have the tools – we just need the strategy. ◆

Dan Neinhauser is currently Director of MacroTechnology Works (MTW) at Arizona State University, having recently moved to AZ from NY. Incorporating a global perspective, MTW undertakes and advances complex applied research for the benefit of society through collaborative engagement of private and public enterprises. Dan believes that by bringing a customer voice and processes with rigor into the research lab, academics will succeed (with industry) at building innovative products and platforms. MTW which was launched by ASU with a $100+ M investment, together with the US Army, in a state-of-the art Flexible Display Center (FDC, an electronics development and fabrication facility). The FDC is a university-industry-government collaborative venture designed to advance full color flexible display technology and flexible display manufacturing to the brink of commercialization. For more information visit http://mtw.asu.edu or email mtw@asu.edu.

Magazines and Carriers for Process Handling Solutions

Film Frames

Film Frame Magazines

Film Frame Shippers

Grip Rings

Grip Ring Magazines

Grip Ring Shippers

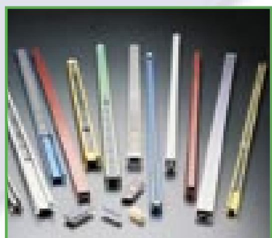
Lead Frame Magazines - F.O.L./E.O.L.

Stack Magazines - E.O.L.

Process Carriers (Boats)

Boat Magazines

I. C. Trays - Multi-Channel


I. C. Tubes and Rails

Miscellaneous Magazines

Substrate Carrier Magazines

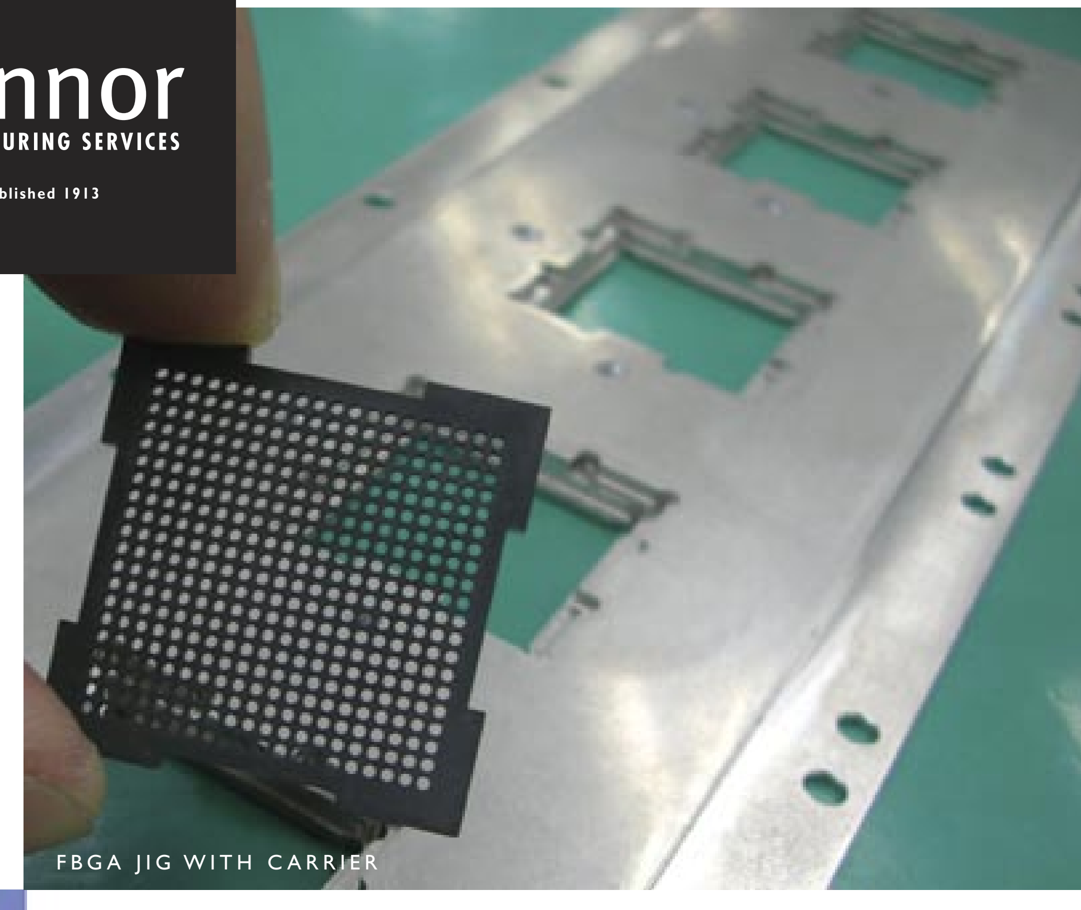
TO Tapes & Magazines

Wafer Carriers

Accept Nothing Less.

Perfection Products Inc.
1320 S. Indianapolis Ave. • Lebanon, IN 46052
Phone: (765) 482-7786 • Fax: (765) 482-7792
Check out our Website: www.perfection-products.com
Email: sales@perfection-products.com

Connor is a manufacturing company that provides customized precision formed metal parts and integrated assemblies for the Semiconductor, Electronics, and Heavy Truck industries. We serve these markets with wholly owned factories in the United States, Mexico, Singapore, and China.



FBGA JIG WITH CARRIER

MEDIA HANDLING AND PROCESS AIDES

HIGH TEMP BRIDGE CLAMPS

WAFER RINGS

CONNOR CLIP
(CATALOG AVAILABLE)

MANUFACTURING SITES

PORTLAND, OREGON
Phone: 503-256-0230
Phone: 800-968-7078

SINGAPORE
Connor Manufacturing Services, Pte. Ltd.
Phone: 65-6854-1661

TIJUANA, MEXICO

SHANGHAI, CHINA

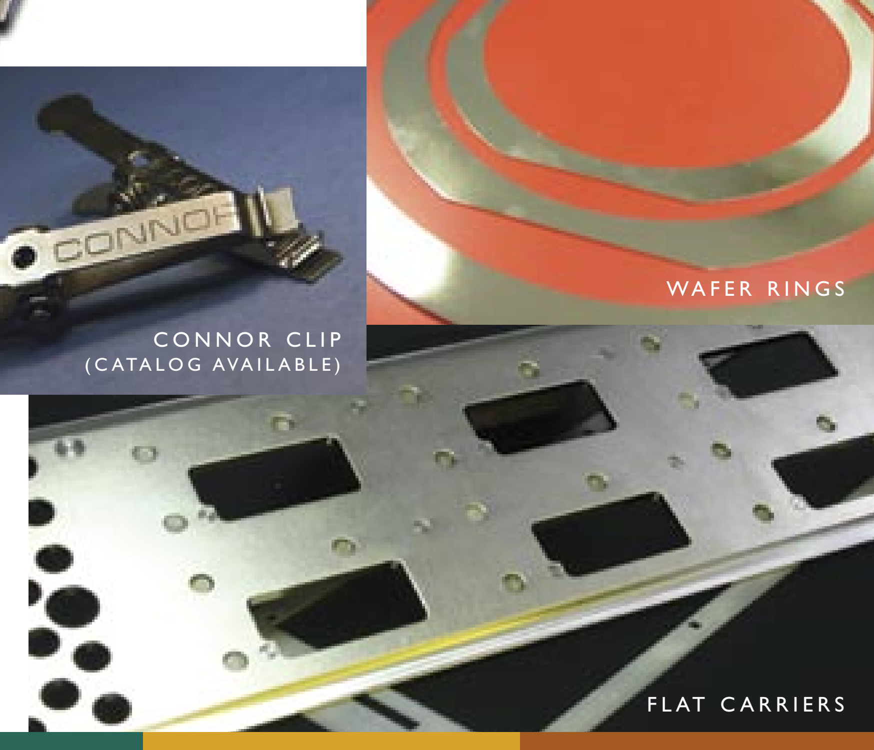
SALES & TECHNICAL SUPPORT

PHOENIX, ARIZONA

SAN FRANCISCO, CALIFORNIA

PHILIPPINES

Contact Us At: **Visit Us At:**
sales@connorms.com



FLAT CARRIERS

UNITED STATES | MEXICO | SINGAPORE | CHINA