MEPTEC report

Volume 10, Number 2

QUARTER TWO 2006

A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Kulicke & Soffa Industries has relocated its corporate headquarters. *page 16*

SUSS MicroTec AG has installed the latest 300 mm technology in wafer probe systems at the nanoelectronics research center IMEC in Leuven, Belgium. *page 16*

Advanced Interconnect Technologies (AIT) has announced that it is expanding its world-class assembly and test factory in Batam, Indonesia. *page 16*

March Plasma Systems has established direct operations in Shanghai, China, that include an Advanced Applications and Demonstration Laboratory. *page 17*

PacTech GmbH announced that **Nagase and Co.**, a major trading company in Japan, acquired a 60% share of **Pac Tech GmbH** in February for an undisclosed amount. *page 17*

STATS ChipPAC has expanded its Quad Flat No-lead (QFN) packaging portfolio. *page 18*

According to final results reported by **Gartner, Inc.**, worldwide semiconductor revenue totaled $235 billion in 2005, a 5.7 percent increase from 2004. 2005 revenue surpassed the semiconductor industry's previous record of $223 billion set in 2000. *page 19*

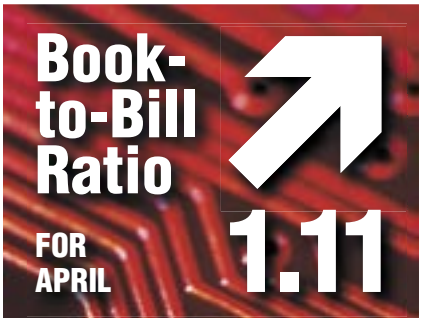
SEMICON West returns to Moscone Center in San Francisco July 10 though 14. *page 21*

MEMBER COMPANY PROFILE

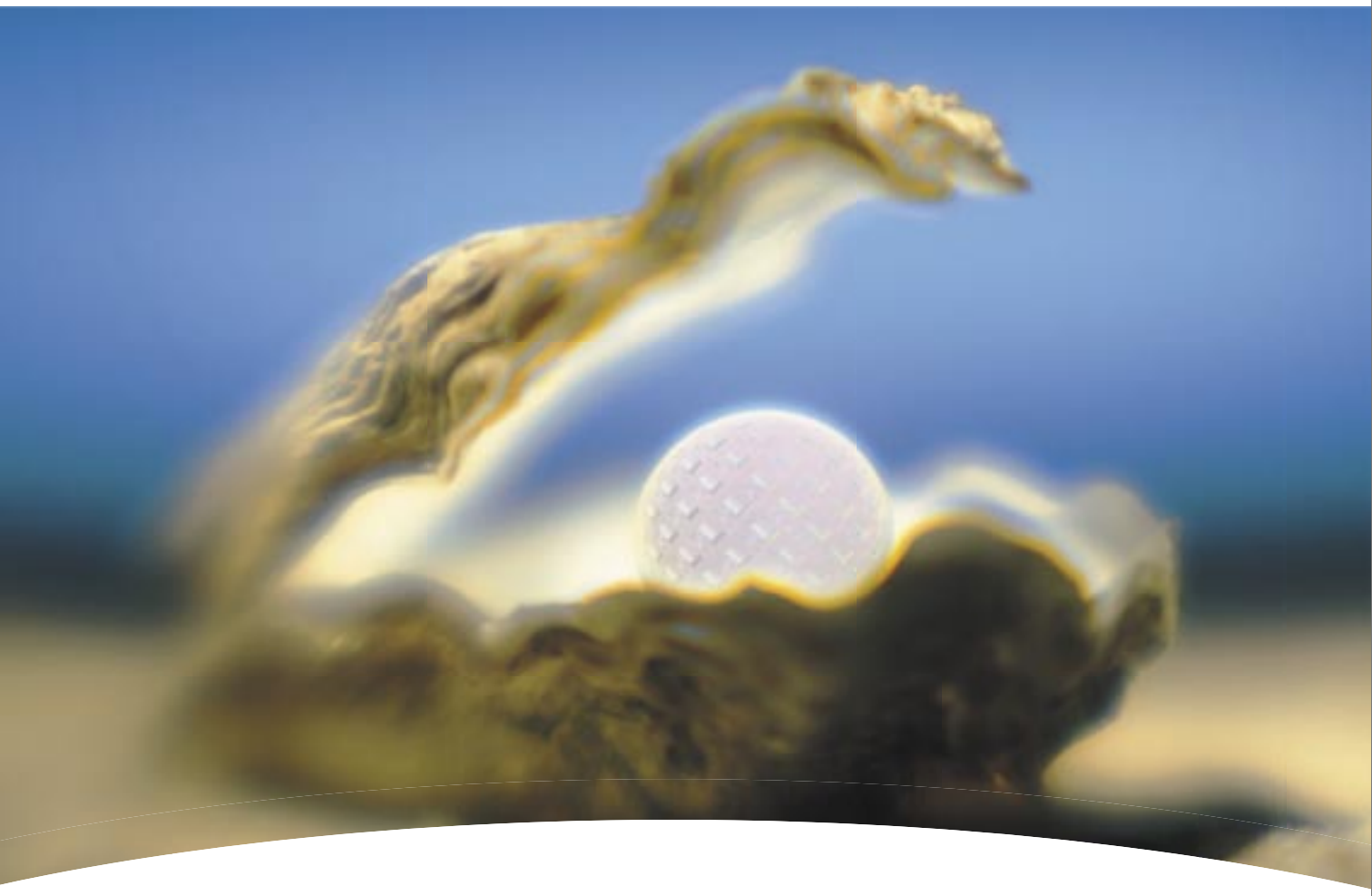
Rose Street Laboratories, the parent company of FlipChip International, was founded in 2003 with a roadmap of providing leadership in product and service support to the electronics industry. RSL has been very active in the life sciences, renewable energy and homeland security markets.

FlipChip International's acquisition of Kulicke and Soffa's Flip Chip Division (K&S FCD) in Phoenix, Arizona, in February of 2004, enabled FCI with bumping technology services that are well known in the industry. This acquisition included standard flip chip and UltraCSP® as bumping offerings and is now FCI's Bumping Division. Since the acquisition, a specialized polymer process named Spheron® has been commercialized and is gaining popularity as a high performance solution for high speed applications such as Radio on Chip. *page 22*

Semiconductor equipment bookings increase 60% over April 2005 level. *page 20*



unique value



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MEPTEC report

Council Update

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It's that time again...summertime, and that of course means **Semicon West**, when thousands in the industry converge on Northern California to see the latest and greatest technology in the semiconductor industry. This year is the second since **SEMI** moved the entire show to San Francisco, integrating the *Final Manufacturing* segment of the show into the rest of the event.

We're pleased this year to be a part of Semicon West, as a technical session contributor to their **TechXPOT** (pronounced "Tech Spot"). According to a press release on the special sessions (see page 19), SEMI is building on the "show-within-a-show" concept, and the *Test, Assembly and Packaging* portion will focus on innovations in test, assembly and packaging, with exhibits, displays and technical presentations. There will be two **MEPTEC** sessions during TechXPOT: *The Packaging Roadmaps* session will be held on Tuesday, July 11 from 11:00 am to 12:20 pm, and *Materials for Packaging* session will be held on Wednesday, July 12 from 11:00 am to 12:20 pm, and will be held in the Test, Assembly and Packaging hall, right on the show floor. The SEMI press release mentioned above offers details of speakers and topics. Other organizations contributing are **FSA, ITC** and **iNEMI**. We hope you'll stop in to see these information sessions

We're pleased to announce another new MEPTEC Advisory Board member: **Bhavesh Muni** of **Henkel Corporation**. Bhavesh is currently their Director, Global Semiconductor Material Business and is responsible for development and execution of global business strategy for Henkel's semiconductor packaging material business. Welcome Bhavesh!

Our next event will be held on Thursday, September 21 and will be a divergence from our usual Bay Area venue: we've been invited to hold it on the **Tempe campus** of **Arizona State University**, in the beautiful Old Main building. The event, called *"Medical Electronics – Integrating Technologies: Merging the Microelectronic, Bioscience and Medical Industries"* will be co-sponsored by **ASU** and the **MacroTechnology Works**. The symposium will be co-chaired by MEPTEC member **David Ruben** of **Medtronics** and MEPTEC Advisory Board member **Nick Leonardi** of **CMC Interconnect Technologies**. See page 5 for further information.

We also offer a follow-up look on a couple of past symposiums. These follow-ups are regular features in each issue. For each event, **Jody Mahaffey** of **JDM Resources** writes a pre-symposium article wherein she previews the program, interviews participants, and summarizes in an article which gets distributed to the trade magazines and on-line publications. After the symposium she updates and finalizes the article, and that is what you will see here. In this case the event was our special 2-day symposium on May 17-18 called *"MEMS Packaging Trends: From Production to Market"*. This event included a **SEMI** workshop on *MEMS Packaging Standards*, as well as an *academic session* where we heard about some of the leading-edge research in MEMS technology. In addition, **Julia Goldstein**, editor at **Advanced Packaging magazine**, follows up with a review of our February event on *"2nd Annual The Heat is On: Thermal Management Solutions in Semiconductor Packaging"*. See page 6 for both of these summaries. CDs of the proceedings for both of these events will soon be available on the MEPTEC website at www.meptec.org, or call Bette Cooper at the MEPTEC office to order today – 650-714-1570.

One of the feature articles this issue is con-

Issue Highlights

tributed by a new MEPTEC Corporate member company, **Hymite**. **Dr. Jochen Kuhmann** and **Andreas Hase** write about *"Low Cost, High Performance Silicon Packages"*. This is a very interesting look at how silicon as a packaging material offers exceptional thermal and electrical performance. We were pleased to have Hymite as a speaker on the same topic at our 2005 MEMS Packaging event; we'll see if we can get them to come back in 2007 and give us an update. See page 24 for this informative piece.

Our other feature article is an informative look at *"Materials Declaration for Everyone"*. **Dr. N. Nagaraj** of **Papros, Inc.** offers a discussion on exchanging material content data in the form of Material Composition Declarations. Sometimes the practical management issues in our industry are overshadowed by the cutting-edge technology, so we're pleased Dr. Nagaraj has taken the time to explain this important element of data management. It really is a best practice for supply chain management.

Our regular Thermal Management contributor and MEPTEC Corporate member company, **Advanced Thermal Solutions (ATS)**, writes about *"Airflow Optimization for Enhanced Cooling"*, and can be found on page 32. **Norman Quesnel** discusses why airflow characteristics are so important to device manufacturing. We appreciate their continued contributions on this important topic.

Our Editorial this issue is contributed by new MEPTEC Advisory Board member, and frequent speaker at various MEPTEC symposiums, **Tom Clifford** of **Lockheed Martin**. Tom offers himself up as our "Technology Reporter", and takes a very interesting and introspective look at future technology, and what future community will be responsible for coming up with this new technology. He researched trade magazines, newspaper sources, and even high school and junior high school Science Fair programs to find out if our kids are focusing on more than what he calls "fashionable" technology, such as cool music gadgets, video games, etc. I think you'll find his comments and findings fascinating…see page 38. If you've ever met Tom you'll know that he's a very smart, inquisitive and reflective guy; we'll see if we can get him to contribute more "Technology Reporter" pieces in future issues!

Our Industry Analysis coverage this issue is contributed by **Bob Johnson, Klaus Rinnen, Jim Walker** and **Mary Olsson** of **Gartner Dataquest** (Jim and Mary are also long-time MEPTEC Advisory Board members). This article takes a look at the impact on the semiconductor equipment segment of the industry, and how historically the equipment industry responded to changing technology by succumbing to semiconductor financial pressures. They are suggesting that things are changing; see page 10 for their article titled *"The Evolving Changes for the Semiconductor Equipment Industry"*.

Our Member Company Profile this issue is MEPTEC Corporate member **Flip Chip International**. Theirs is a really interesting success story: it tells the tale of two visionaries, **Bob Forcier**, President/CEO and **Dr. Joan Vrtis**, CTO of **Rose Street Laboratories (RSL)**. They wanted to provide flip chip and wafer level packaging services in packaging, operate globally to support worldwide marketplaces, incorporate new IP into products and services, and form a team to make this happen, and **FCI** was born. You'll see that every February since 2004 FCI has hit a major milestone, and the question is asked, "Will we have to wait until next February to hear what's next?". Find out by reading their story on page 22.

Our "University News" section this issue is not really about a classic academic institution, but it is about a similar type of research institution that works with academia and industry alike on electronics research. This is also our first coverage of an institution outside the U.S. It is **IMEC**, and is located in Leuven, Belgium. IMEC is Europe's largest independent research center on nanoelectronics and nanotechnology. They have developed a powerful network of over 500 partners including IC manufacturers, equipment and material suppliers, universities, research institutes, etc. Coincidentally, we received a news release recently from SUSS MicroTec about their collaboration with IMEC by installing their latest 300mm technology in wafer probe systems at the nanoelectronics part of the research center. They will continue their alliance with IMEC in the following years on technology enhancements. See their story on page 13.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at the Semicon West show, or another of the many events where we'll be distributing this issue, we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC Welcomes New Advisory Board Member

Bhavesh Muni
Director, Global Semiconductor Material Business
Henkel Corporation

Bhavesh Muni has more than 18 years of experience in various materials for electronics assembly & semiconductor packaging. His experience ranges from hands on R&D Chemist to technical/application services and leading up to sales & marketing aspects of electronics material business. Bhavesh is currently Director, Global Semiconductor Material Business at Henkel Corporation, responsible for development and execution of global business strategy for Henkel's semiconductor packaging material business. Prior to Henkel Bhavesh held positions at Thermoset, Lord Corporation; Emerson & Cuming/Ablestik; Olin Hunt Conductive Materials; and Pacific Polytech/Namics. Bhavesh holds an MS in Polymer Science from the University of Detroit, Detroit, MI; a BE in Chemical Engineering, REC, Srinagar, India. He has published several technical papers on Interpenetrating Polymer Networks (IPNs).◆

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MEMS Packaging – The Saga Continues

Jody Mahaffey
JDM Resources

According to market research company YOLE Développement, the MEMS market reached $5.1 Billion in 2005 and is expected to reach $9.7 Billion in 2010, representing a compound annual growth rate of almost 15%. For the fourth year in a row, MEPTEC, the MicroElectronics Packaging and Test Engineering Council, brought together leading experts in the MEMS field to discuss the topic as it relates to packaging in its technical symposium "*MEMS Packaging Trends: From Production to Market*" held on May 17 & 18th, 2006 in San Jose, CA. Some of the speakers at this conference offered insights into the changing and challenging world of MEMS.

Most analysts agree that MEMS based products are forecasted to grow significantly in the next ten years. We asked our experts what they thought the driving factors are for that growth. Most agree that one of the largest reasons for this growth will be new applications.

Tom Clifford of **Lockheed Martin Space Systems** was a speaker in the *End User Applications* session of the symposium. He believes that, "MEMS growth depends on the product and the corresponding process. There are scores of current and potential MEMS applications of all sorts. Success depends on the profoundly new capabilities that well-designed and positioned MEMS products will provide."

Mathieu Potin is a Market Analyst for **YOLE Développement** out of Lyon, France and presented in the *Industry and Market Overview* session of the symposium. Potin believes growth of the MEMS market goes beyond just new applications. "The development of the MEMS markets will of course be related to new applications," explained Potin, "but the primary market growth would depend on the ability of MEMS manufacturers to supply from the component to the module." Potin's definition of a module is a MEMS product which can provide a function instead of just a sensor (component) alone. Potin believes that device manufacturers will be pushing a module offer (compared to a component offer) in order to attract added value.

Many MEMS based products such as DLP, accelerometers, pressure sensors and printers, can already be found in the general marketplace. With the introduction of so many new applications we should expect to see many other products in the near future.

"MEMS microphones are a major growth area for applications such as hearing aids and cell phones," according to **John Heck** of **Intel**. "RF MEMS switches are entering the marketplace, starting in test and measurement equipment, and we may expect to see them in handheld wireless devices within the next few years. Also a wide variety of medical devices will be seen in the near future." Heck was the Session Chair for the *Enabling Technologies* session.

Mark Crockett of **Applied Materials** said that people should expect to see MEMS sensors and actuators in more "user-centric" devices like set top boxes that sense viewer's emotions and adapt accordingly. "We may also begin to see wearable devices to optimize worker productivity and effectiveness," said Crockett, who presented in the *SEMI Standards Workshop* on the second day of the symposium.

Potin added that, "Micro fuel cells are at a key development stage in Japan with companies like NEC, Fujitsu, and Toshiba, and are likely to enter the cell phone market in 2007-2008. Several service providers including NTT and KDDI have already presented mobile phone models with integrated micro fuel cells. Europe and the US are also engaged in such development through companies such as STM and Infineon."

Alvin Barlian, of **Stanford University**, believes that as the MEMS field matures, more development of MEMS products will be driven by academic and industrial labs. According to Barlian, relatively newer applications may include biological and chemical sensing for military and homeland security as well as transportation infrastructure systems, structural health, and environmental monitoring. The rebirth of aerospace and telecommunication industries will also increase the demand for more advanced MEMS products. In addition, advances in material science play a major role in the growth of MEMS by enabling innovative unconventional fabrication processes. Barlian was a speaker in the *Academic Workshop* which was part of the second day of the symposium.

Other than new applications, cost reduction and increased reliability still remain critical drivers for growth in the MEMS industry. Heck feels that significant competition in the foundry business, as well as common availability of MEMS-specific tools such as wafer bonders and deep silicon etchers are key to lowering costs.

"Lower costs and improved reliability will encourage the expansion of MEMS into new markets," added **John Crane**. "As improved assembly processes yield lower costs and better reliability, new markets will proliferate." Crane represents **Boschman Technology** who presented in the *Advanced MEMS Packaging Trends* session.

Ken Yang of **Honeywell** believes the growth will be driven, not only by lower cost and better performance, but also by ease of manufacturing and government policy requirements. Yang was a speaker in the *Advanced MEMS Packaging Trends* session.

Clifford agreed that cost and reliability aren't the only issues, saying that, "Most MEMS concepts must confront and control particulate and molecular contamination. Furthermore, specific challenges include CTE mismatch and thermal management; pass-thru of optics/gases/liquids/signals; vacuum packaging; and subtle but crucial materials compatibilities. "

For people who have been watching the MEMS market for many years, it seems that changes have come slowly. However, some significant changes have occurred over the past year according to our experts. Heck explained, "MEMS foundry consolidation has started to occur, and this trend will likely continue. Also, many groups are at the cusp of commercializing in-situ, or self-packaging methods for MEMS, where the mechanical elements are self-sealed during the fabrication process. This enables the MEMS die to be treated much like a standard IC throughout the packaging process, thereby reducing packaging cost significantly."

Clifford believes many things are chang-

ing for MEMS. "Certainly one enabler is maturing design software keyed to multi-physics solutions and to the particular fab process," explained Clifford. "Another is growing materials expertise, riding on nano-lab developments. Another enabler might be turn-key development services structured to ease and accelerate the painful transition from concept to manufacturable prototype. Another bright light is the emergence of 'packaging' in academia, as a respected and pivotal skill-set."

As new MEMS devices are developed, the packaging industry will continue to struggle with the question of whether to use existing technology or develop new technology. This question becomes even more important when getting MEMS products into high volume. Many people are divided on this. Heck believes that current packaging solutions will continue to evolve and drive down cost, but also new packaging methods will begin to arrive in commercially-available products in the near future. "In order to get to high volume production," explained Heck, "ultra-low cost packaging methods are needed, both in the form of cost reduction on existing methods (such as glass frit wafer bonding), and the advent of new self-sealed MEMS devices, which will enable significant cost reduction."

Clifford agreed that both existing and new technology will be needed depending on the product. "Some, including hermitic fluidics, optics, integrated sensors, etc. might currently be package-limited. Others might work fine in tailored conventional or vacuum-finessed packages. In every case, the package is a major challenge."

But many people, like **Chris Lee** of **Quantum Leap Packaging**, feel that existing packaging must be made to work in order to keep costs low. To this end, according to Lee, companies like Quantum Leap are combining existing packaging technology with new material sets such as QLP's Quantech™ high performance polymer material to meet the changing demands. "As MEMS devices become more complex," explained Lee, "devices are much more stress sensitive and prone to lower performance yields. Managing the device stress is a key in packaging in high volume." Quantum Leap Packaging presented in the Enabling Technologies session.

Crane added, "As MEMS products have migrated from ceramic packages to BGA and/or QFN package types, the ability to move to high volume production has become easier and easier."

One of the biggest questions for packaging MEMS has always been and continues to be, where is the packaging done, in the front-end or the back-end? Both sectors are working on new packaging technology which will enable the proliferation of MEMS.

"In-situ packaging is beginning to pay off," according to Heck. "This technology comes directly from the front-end fabrication side."

Yang agreed that wafer level packaging and wafer level vacuum packaging done at the front-end are critical to move MEMS forward.

Crane believes that the ability to successfully mold exposed die MEMS, such as finger print sensors or optical sensors, using transfer molding and film assisted molding, has allowed for significant assembly cost savings and improved capability. Film assisted molded products are free of mold compound flash and bleed. Lower cost and a reliable process at the back-end have enabled such MEMS devices to proliferate.

There are other areas of concern for MEMS beyond packaging. One of these is Intellectual Property. With the increasing trend toward overseas manufacturing in the past few years, IP has become a critical issue in all semiconductor areas and perhaps more so for MEMS products. Clifford believes IP is a bigger problem for MEMS. He explained, "IP resides in and must accommodate the one fact that characterizes all MEMS products: the inseparable linkage of design / process / material / fab tooling / test methodologies / process techniques / etc. Any IP and business arrangement (licensing, scale-up, product proliferation, supply-chain expansion, etc.) must deal with that."

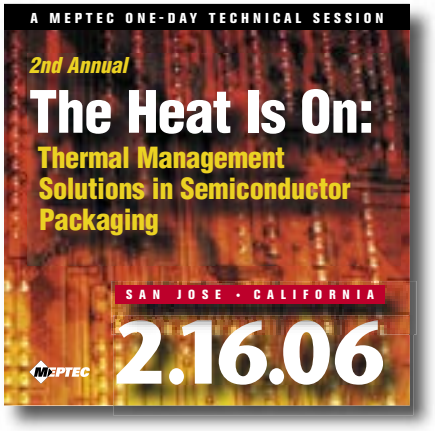
Heck agreed saying, "MEMS devices are so much more process-dependent than IC's – you can easily port a new CMOS design from one foundry to another. But the IP inherent in a MEMS device is in both the design AND the process. Therefore foundries and companies may possess key differentiators based on processes they develop."

Another area of concern for MEMS is standardization. This year's MEPTEC conference was extended to two days to include a half-day workshop, in conjunction with **SEMI**, to discuss standardization for MEMS. MEMS offers a unique challenge when it comes to standardization because so many of the devices are applications specific. "Applications that are customized, generally require greater up front cost to achieve economies of scale," explained Crockett. "Standardization and level of difficulty will be driven by a variety of market forces. Unique applications will only leverage standardized solutions if the standards exist. Today, such standards for MEMS are not an option. As individual solutions proliferate, advantages in standardized solutions grow. For example, if five products perform the same function to a customer and only one of those products offers features in compatibility and lower cost of ownership through standardization, then the decision of which product to buy is simple. Establishing this differentiation is critical in newly shaped markets."

Heck believes that because MEMS devices are all made for different purposes and in different markets, standardization will only work at a very basic level. "We already have several relatively standard process modules for MEMS. For example, glass frit wafer bonding is so common these days that it may be considered a standard; this is in part due to the availability of wafer bonding and screen printing tools. I don't think we will ever see full processes that are standard in the sense that many devices with different functions can be made with a single MEMS process."

Though it may be difficult, standardization is still important, even with application specific MEMS products, according to Yang. "At least individual processes should be standardized so that you can use any subset of them to apply to your specific process set. It can then enable the foundry to group similar processes together to make a volume production from various products."

With or without standardization, the MEMS market continues to grow. According to **Marlene Bourne** of **Bourne Research**, funding of MEMS start-ups exceeded $500 million in 2005, with the average funding received per round at approximately $13 million. **Bance Hom** of **Consultech International** and Symposium Co-Chair said, "MEMS start-ups today are more market driven rather than technology driven…more direct application now, rather than pie in the sky fantasy we may have seen in the past." One thing is for certain, even with all the issues and challenges facing MEMS, the technology is here to stay and getting stronger every day. ◆



Julia Goldstein
Advanced Packaging Magazine

Thermal management continues to be a "hot" area, and MEPTEC's second annual "The Heat is On" symposium on February 16 packed the hall despite the plethora of events covering the topic. Keynote speaker **Herman Chu** of **Cisco** divided cooling into two categories – heat transport and heat transfer – and explained that efficient heat transfer is critical

for data centers. Customers aim to achieve sufficient cooling using traditional technologies, preferring to avoid liquid cooling and other technologies that require infrastructure change. Reliability, availability and serviceability, as well as cost, are all hurdles for new technology. Chu suggested that the push to minimize energy usage could drive future data centers to be rated on efficiency, similar to the "Energy Star" ratings on home appliances.

Professor Van Carey from **UC Berkeley** discussed the relationship between the theoretical maximum heat flux removal rate for a vaporization process and heat flux achieved in mini and micro heat pumps. The ratio between the actual and maximum heat flux is one measure of the efficiency, which can be increased by optimizing the coolant pressure and selecting a mixture of coolants, for example water and alcohol.

Debendra Malik of **Intel** discussed the *2005 International Technology Roadmap for Semiconductors (ITRS)* and stated that the ITRS recognizes that packaging is a limiting factor toward improving cost and performance, and that thermal management is given significant attention in the Assembly and Packaging chapter. The focus is hot spot mitigation using heat spreaders or thermo-electric cooling. Thermal interface materials (TIMs), spreader design and cooling technology are listed as areas for improvement.

While ITRS is just now recognizing the need to focus on thermal management, heat dissipation has been addressed for decades. **Sandra Winkler** of **Electronic Trend Publications** described solutions from the 1950s that used metal screws and thermal grease to conduct heat away from power transistors. Winkler gave an overview of current thermal management materials as well, including TIMs, fans, heat pipes, and cold plates. She described substrates containing metal layers specifically designed to act as heat spreaders.

Devesh Mathur of **Honeywell** discussed the connection between the surface condition of heat spreaders (flatness, roughness, plating) and TIM performance by showing thermal resistance tests of TIMs using various test blocks. Mathur also described new TIMs, including polymer solder hybrids filled with a high conductivity filler and low melting solder. During processing, the solder melts and surrounds the filler, providing a direct thermal path through the thickness of the TIM. **Scott Allen** of **Henkel** described a two-part adhesive TIM applied in separate beads, which then mix when the components (a package and a heat sink, for example) are assembled. Since these TIMs are solid materials they tend to perform better than chemically activated TIMs on ceramic packages, presumably since the solvent in activated materials can absorb into the ceramic, reducing TIM effectiveness. Heat-cured TIMs are another solution for ceramic packages.

The thermal performance of heat sink base plates can be improved by using a vapor chamber instead of solid copper or by increasing the thickness of the base plate, as **Kaveh Azar** of **Advanced Thermal Solutions** explained. He discussed the difficulty in achieving sufficient flow rate in micro-pumps and proposed an alternative solution, a BGA with a built-in, water-cooled heat spreader.

Hot spot mitigation was a recurring theme, and **Nanda Gopal** of **Gradient Design Automation** warned package designers to consider the chip as a dynamic device with variable temperature distribution rather than a simple heat source in their models. Gopal described the benefits of 3D thermal design incorporating input from both chip and package designers.

James Forster of **Wells-CTI** described a solution that actively controls the temperature and voltage applied to individual socketed packages during burn-in, holding them at the desired burn-in temperature and turning them off individually if they fail, while maintaining the burn-in oven at a lower temperature. This technology works for low power devices, but higher power devices can require passive or active cooling during test. **Jerry Tustaniwskyj** of **Unisys** discussed incorporating both heating and cooling capability into test sockets. ◆

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DPC

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The Evolving Changes for the Semiconductor Equipment Industry

Bob Johnson, Klaus Rinnen, Jim Walker and Mary Olsson
Gartner Dataquest

The steady and relentless advancement of semiconductor manufacturing technology provides the foundation for the long-term growth of the industry. As summarized by Moore's Law in its various forms, the cost to produce a single function, whether it be a bit of memory or a single gate on a logic chip, has decreased by about 50 percent every two years since the dawn of the integrated circuit age in the 1960s, and there is every expectation that this will continue.

This progress in design and manufacturing technology was neither easy nor inexpensive. Over the years, the industry created a methodical approach to new technology development that has served it well. Basic research in advanced semiconductor manufacturing technology is carried out by the leading integrated device manufacturers (IDMs) (Intel, Samsung, TI, Infineon Technologies, Renesas Technology, Toshiba and others) or through industry technology development alliances (for example, the IBM alliance with AMD, Chartered Semiconductor Manufacturing, Samsung, Sony and Infineon). This research is turned into plans for future technology development at the detailed process level. In a parallel effort, the major semiconductor manufacturers from around the world, working through International Sematech, develop and publish the International Technology Roadmap for Semiconductors, which delineates industry consensus regarding the directions and new processes needed for future semiconductor production.

Although the semiconductor manufacturers develop the overall process flows at the fab level – and may even develop specific processes in their labs – it is generally the equipment companies that turn these recommendations into production-worthy equipment when it is needed. This model worked reasonably well as long as the majority of the advances needed for the next technology node required scaling existing technology. In most cases, the technology risks were few, and equipment manufacturers could meet most of the demands of the next process generation with upgrades to existing products.

This model frequently broke down if new technologies or major changes in materials were needed. In such cases, equipment R&D efforts must begin years before production process development at the semiconductor manufacturers. Initial schedules are developed with milestones for evaluation tools but with no guarantee of market adoption. The introduction of new technologies was often delayed for years beyond initial expectations because new life was found for existing methods. Some prime examples of this were in the lithography field. For example, 248-nanometer (nm) deep ultraviolet lithography was initially developed for implementation in the late 1980s, but it didn't make the mainstream until almost 10 years later. X-ray lithography was once touted to be the next technology after 248 nm, but that never happened. Originally, 193-nm lithography was considered a requirement for 0.18-micron production, but the industry waited four more years until 90 nm started production. Once viewed as essential for 65-nm production, 157-nm lithography dropped off the road map entirely. On the materials side, low-k dielectrics, tungsten, high-k gate materials and others have all seen their deployment slip from initial projections by years.

Although each of these developments involved a limited portion of the industry, the move to 300-millimeter (mm) wafers strained the resources of the entire equipment industry. Originally scheduled for initial widespread use in 1997 or 1998, it wasn't until 2003 and 2004 that the first large 300-mm fabs ramped up fully. As a result of this slip and the continued large R&D investment required – with no returns for an extended period – the return on investment (ROI) in 300-mm technology development for equipment companies plummeted.

Looking forward, the need for the development of new processes and new materials increases with each new technology node. Although lithography appears to have settled at the 193-nm technology node for another couple of generations, new materials will be needed for each node as the industry progresses. But there is no definitive list of necessary new processes. Each new development undertaken by the equipment companies faces the risk that its ultimate acceptance by the industry will be either delayed or indefinitely postponed.

These financial risks are becoming significant and are increasing at a time when the industry is facing lower growth rates and tighter margins. Lower profitability breeds risk aversion and creates an environment in which equipment companies will be hesitant to make the necessary investments in process R&D without some reasonable guarantee of a decent ROI on the project.

Thus, the question of whether the industry can keep on the path dictated by Moore's Law for the next decade or so depends not as much on whether we can develop the necessary technology, but on whether it can be done profitably with reasonable and manageable financial risks.

Gartner Dataquest Perspective

A number of significant market and structural trends facing the industry will lead to a rethinking of traditional business models for developing new technology. Each of these trends leads to a market demonstrating many of the characteristics of a mature industry: slower growth, tighter margins and fewer players. Gartner Dataquest has developed a series of Strategic Planning Assumptions as listed below that can help guide long-range planning efforts of industry participants.

1. The growth rate for the wafer fab equipment (WFE) market will parallel that of the semiconductor market through 2014.

During the past few years, the overall growth of the semiconductor market has slowed as it moved from a high-growth emerging market segment to a more mature, but still dynamic, industry. Present forecasts show that the long-term growth of the semiconductor industry has

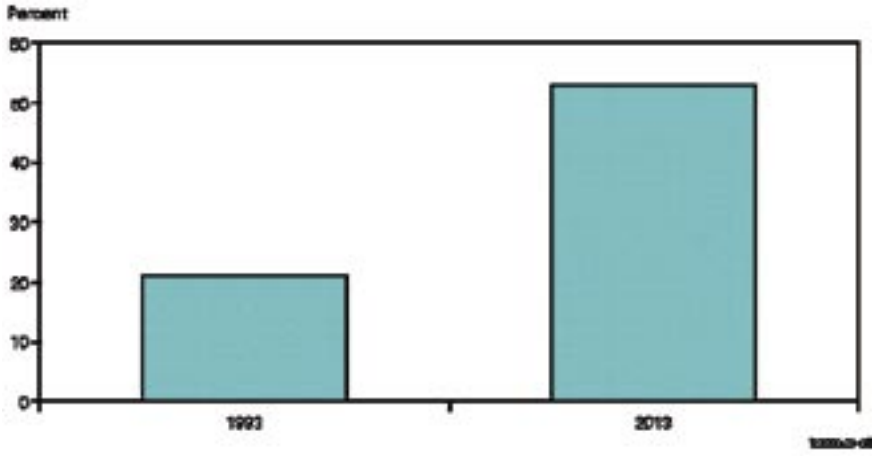


Figure 1. Consumer Percentage of Semiconductor Market

slowed to a per-year projected average of about 9 to 10 percent for the near future. The slowing growth rates will also affect the semiconductor equipment industry, because the demands for additional capacity and capital investment to support that growth will also decrease.

2. By 2014, greater than 50 percent of chip sales will be for equipment markets targeted at consumers.

As shown in Figure 1, consumer applications have been gaining an increasing share of the semiconductor market, and they will likely eclipse business and commercial applications in the next decade. The implications of this shift on the industry are profound. The consumer market is extremely price-sensitive, putting downward pressure on profit margins. Product lifetimes are shorter than for commercial products, and the timing of market introduction is more critical. These markets are driven by fashion, features and fad; productivity and function have less intrinsic value than in commercial markets. Much of the value for consumer products lies in the software, which creates brand differentiation and brand loyalty.

3. During the next 10 years, the key differentiation for semiconductor vendors will shift more strongly from silicon manufacturing to IP and design.

With the advent of foundries providing leading-edge capabilities, silicon manufacturing is becoming more of a commodity, and the primary differentiation for devices will shift from manufacturing to chip design, software and other forms of non-manufacturing IP. Although manufacturing technology will always be considered a key core competency for the largest IDMs, many of the leading semiconductor designs will base their market position on product factors other than manufacturability. With manufacturing drifting more and more toward a commodity status for much of the industry, the margins it once commanded will also experience pressure. For materials and equipment suppliers, enabling a commodity and not a key differentiator will lead to continuous price pressures and reduced margins.

4. By 2014, fewer than 25 manufacturers will be building new fabs.

As any industry matures, consolidation becomes inevitable. This is happening in the semiconductor industry and will continue as the present industry leaders become the only ones that can afford to build new fabs. Many of the smaller manufacturers that are currently running their own fabs will move out of manufacturing and become fables companies, relying on the major foundries for their manufacturing. This consolidation reduces the number of potential customers for equipment manufacturers and makes establishing successful long-term relations critical.

5. By 2014, fewer than 10 equipment suppliers will satisfy 80 percent or more of semiconductor manufacturing equipment demand.

As shown in Figure 2, the equipment industry has already progressed significantly along the path to consolidation and is likely to continue to do so. As industry growth rates slow and margin pressures increase, only larger equipment companies can afford to make the R&D investments necessary to remain competitive. In addition, as critical equipment markets coalesce to two or three key suppliers, equipment companies can have the market presence to resist profitability-destroying pressures from the major semiconductor manufacturers.

The direct result of these trends leads to the following new rules for manufacturing:

- Only the paranoid will survive - Caution prevails in upturns; manage capacity and investment carefully.
- Big manufacturers can ignore business cycles and invest counter-cyclically to strategically prepare for upcycles.
- Focus on core competencies - Outsource when possible but only if it does not affect core competencies.
- Think bigger - Alliances, mergers and acquisitions can provide increased financial leverage.
- Timetables are collapsing, but being there first reaps profits.
- Time to anything" assumes paramount importance.
- Enabling time savings leads to higher profits and ROIs.
- Don't slow the pace of innovation.

The industry has been facing increasing pressures on its profitability since

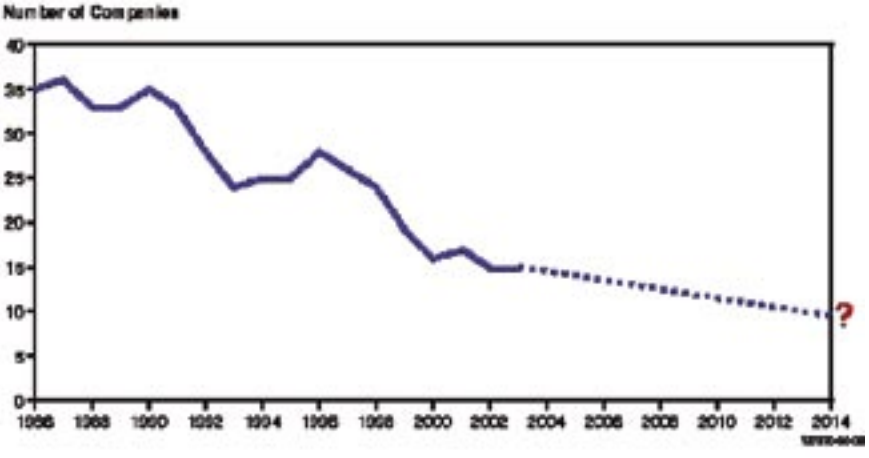


Figure 2. Equipment Companies Generating 80 Percent of Total WFE Revenue

the mid-1990s, when the long-term revenue trend turned downward. Although the initial impact of this was obscured by the wild gyrations of the dot-com boom-and-bust cycle, the results have been the same: increased efforts to be more cost-efficient across the board. This approach is evidenced by the increasing importance of cost of ownership on equipment suppliers in the late 1990s and by the industry dictating increased capital and materials efficiency for 300-mm equipment. Many of the major semiconductor manufacturers have formed technology alliances to alleviate the costs of leading-edge research. The pressure to develop new process and new equipment is still directly on the equipment manufacturers, which are expected to develop new processes on demand, with little or no guarantee of an acceptable return on their R&D investment or even assurances that the newly developed technology will be selected for production. The current practice is to encourage multiple equipment suppliers to solicit competitive parallel developments and then stage a winner-take-all, best-of-breed competition for the production business. Although this approach may lead to slightly superior processes in the short run, the long-term effect is an inefficient use of scarce R&D resources on an industry-wide level.

As the relentless march of new technology continues, these financial pressures will continue to weigh on even the largest equipment companies. This factor leads to the final Strategic Planning Assumption…….

6. By 2014, the existing R&D model will have to change drastically; equipment companies will not be able to afford product development with no guaranteed ROI.

A number of possibilities will provide acceptable ROIs for equipment company R&D in the near term:

- Consider equipment company process development alliances and mergers similar to the technology development alliances in the semiconductor arena.
- Demand a firm purchase commitment before agreeing to develop specialized processes. Don't agree to an open-ended development project that has no guarantee of an acceptable ROI. Consider a nonrecurring engineering model to fund development of unique processes. Make the semiconductor manufacturers share the financial risk.
- Create joint technology development consortia between semiconductor manufacturers and semiconductor equipment manufacturers. Shift the focus from competitive best-of-breed tool evaluation to competitive equipment supplier evaluation so that participation in joint development efforts guarantees equipment purchases. Some consortia, such as IMEC in Europe and Albany Nanotech, are already involving major equipment companies.

Summary

Historically, the industry has relied on the big semiconductor manufacturers putting pressure on the smaller equipment suppliers to meet their technology and cost objectives, with little or no consideration of the consequences. The equipment industry responded by succumbing to semiconductor financial pressures. The stakes for the entire industry are too great for this modus operandi to continue. More than ever, future industry growth depends on achieving the cost and performance goals of Moore's Law, but it is getting increasingly difficult to do so. The industry's lifeblood is its manufacturing technology, and it must develop new and more-effective ways to maximize returns from an increasingly scarce R&D dollar. ◆

IMEC – Research Center on Nanoelectronics and Nanotechnology

Three to ten years ahead of industrial needs

Katrien Marent
Corporate Communication Manager
IMEC

IMEC's ultra modern research facility is continuously expanding.

As Europe's largest independent research center on nanoelectronics and nanotechnology, IMEC has over 1,450 people from all over the world working together in this institute with headquarters in Leuven, Belgium. They develop design methodologies, IC process and packaging technologies and enabling technologies for the electronic systems of the future. IMEC's research bridges the gap between fundamental research at universities and technology development in industry. Its unique balance of processing and system know-how, intellectual property portfolio, state-of-the-art infrastructure and its strong network of companies, universities and research institutes worldwide position IMEC as a key partner for shaping technologies for future systems.

A Broad Range of Research Activities: IMEC's Strategic Research Programs

IMEC's know-how on this broad range of research topics is gathered in several strategic research programs. First, to cope with the ever continuing scaling of transistor dimensions, IMEC has set up a centralized research platform. Here, leading IC-manufacturers, together with renowned equipment and material suppliers collaborate to find innovating solutions for the **sub-45nm technology** nodes. The platform includes technology programs on lithography, substrate modules, gate stack, interconnects, ultra-clean processing, emerging devices, germanium devices and others. Next to these 'core' programs, technologies to add extra functionalities to the chip are being developed. Meanwhile, IMEC looks further into the future. New technologies like carbon nanotubes, semiconducting wires and spintronics shall be needed within ten to fifteen years to explore the possibilities of semiconductor applications. The fundamental knowledge for these innovations is already studied at IMEC.

IMEC's portfolio also contains **polymer-based electronics**, a promising technology for flexible, light and cheap microelectronic systems. While first applications already hit the market – displays based on organic light-emitting diodes (OLED) – future applications include advanced memories, smart clothing, radio-frequency identification (RFID) tags, chemical sensors, **solar cells** and biosensors. IMEC studies different applications of organic electronics, including transistors, diodes, memories, solar cells and biosensors. In the field of renewable energy sources, IMEC improves the technology for solar cells based on crystalline silicon and organic materials and also high-efficiency photovoltaic stacks for space applications. Moreover, adaptation of the electricity grid architecture and the implementation of energy storage devices are examined.

In IMEC's 300mm cleanroom, solutions for the sub-45nm technology nodes are being investigated.

IMEC has also set up a strategic research program 'efficient power' that focuses on developing **high-efficiency/ high-power systems**, beyond the silicon limits, enabled by GaN technology. The program addresses three application domains: RF power amplification, switching devices for power conversion and, to a lower extent, optoelectronics.

In the coming years, microsystems will have an increasing impact on our daily lives and wellbeing. Microsystems integrate multiple technology domains into small autonomous sensors with a variety of functions like detection, data processing and wireless communication. These miniaturized systems can create a network that communicates with the environment. Application domains include healthcare, industrial processing, food-quality control and the manufacturing of intelligent clothing. IMEC develops basic technologies for these **autonomous sensor networks** and therefore bundles its expertise in low-

power data processing, wireless communication, interconnection and packaging, alternative energy sources and sensors. This research is conducted in the Holst Centre in Eindhoven, The Netherlands, established in 2005 as an initiative of IMEC and the Dutch research institute TNO. The Holst Centre has to develop into an internationally recognized research institute for the future generation of wireless autonomous transducer solutions and systems-on-foil.

In its M4 program, IMEC develops the necessary building blocks to create the future **multi-mode multimedia terminal**. This terminal will offer ubiquitous broadband multimedia access, served through broadband wireless communication. To realize this, several technological roadblocks have to be overcome, such as increased multimedia encoder/decoder complexity, seamless switching mode across different communication standards, increasing device cost and power consumption due to increased functionality and fast time-to-market.

IMEC's Advanced Packaging and Interconnect Center (APIC)

IMEC's strategic program on advanced packaging and interconnection technologies focuses on bridging the so-called 'interconnect gap' between circuit and system, heterogeneous integration of RF components and thermal management in high-density devices. The extreme miniaturization of transistors has a large impact on packaging and interconnection technologies. While the size of the chip is being reduced, the amount of input-output control pads does exactly the opposite. Assembly on for example printed circuit boards therefore becomes increasingly difficult. To solve this problem, IMEC develops a multilayer thin-film technology, which consists of multiple thin layers of metal and dielectric materials. The same technology can be used to protect vulnerable structures like MEMS in the early stages of packaging. When applied on active wafers, the technology is considered a wafer-level packaging (WLP) technology. Thin-film WLP technology can be used to realize on-chip flip-chip redistribution layers, for on-chip digital transmission lines, and for integration of high-quality RF passives. When thin-film technology is applied on an intermediate glass or high-resistivity Si substrate, it is considered a thin-film system-in-a-package (SiP) technology or MCM-D.

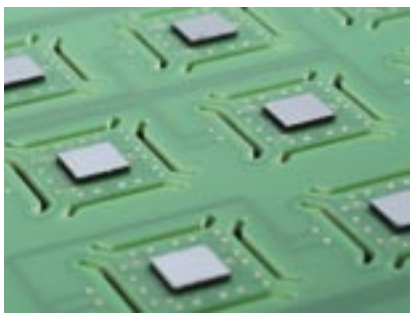
To make even smaller systems with increased functionality, IMEC has several activities on 3D-integration and (ultra-thin) chip stacking. First of all, 3D-SiPs are developed which are complete systems-in-a-package stacked on top of each other. This approach ensures a high yield since each sub-SiP can be tested individually ensuring that only 'good' SiPs are used in the 3D stack. A second approach makes use of WLP techniques where 3D interconnects are created in a post-IC passivation process. A variant of this approach, called ultra-thin chip stacking (UTCS), uses thinned chips, which are embedded in thin-film interconnect layers. A third approach, called 3D-stacked IC (SIC), makes the connections between the different chips during IC processing. Within its strategic program, IMEC additionally focuses on the thermal characterization of packages and the development of advanced cooling systems.

3D-stacked chips assembled on a printed circuit test board using leadfree solder joints.

Collaboration and Training Opportunities

Collaboration in Flanders, Europe and the rest of the world is of the uppermost importance for the success of the IC industry and the growth of the knowledge economy. This is why IMEC has set up a large network of partners (over 500), including IC manufacturers, equipment and material suppliers, universities, research institutes, etc. Through a unique collaboration model, based upon sharing of knowledge, talent, costs, risk and intellectual property, industrial researchers are integrated in IMEC's research teams. As a result, they gather their forces to tackle technological challenges the IC industry is facing. This strategy has become the only right one to survive in a world of technological challenges, million-dollar investments and fierce competition.

In the field of nano-electronics, managers, engineers and researchers must also be kept abreast of the latest technological developments. IMEC's microelectronics training center (MTC) therefore organizes courses and workshops for a variety of target groups. A broad scope of issues is addressed, ranging from IC process technology, chip- and system design to basic knowledge on IC technology, biology and multimedia. IMEC also supports teachers of Flemish schools and universities. Moreover, IMEC offers an international platform called 'Center for Advanced Learning in Information Technologies (CALIT)' where CEOs, policy makers and scientists can meet and exchange ideas. ◆



Wafer-to-wafer bonding tool.

IMEC is headquartered in Leuven, Belgium, and has representatives in the US, China and Japan. Its staff of more than 1450 people includes more than 500 industrial residents and guest researchers. In 2005, its revenue was EUR 197 million. For further information on IMEC visit www.imec.be or contact info@imec.be.

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K&S Relocates Corporate Headquarters

FORT WASHINGTON, PA – Kulicke & Soffa Industries has relocated its corporate headquarters to a new building in Fort Washington, Pennsylvania. The company will maintain its current telephone numbers and email addresses.

Please ensure that all of your business correspondence is directed to their new corporate address at Kulicke and Soffa Industries, Inc., 1005 Virginia Drive, Fort Washington, PA 19034

SUSS and IMEC to Develop Measurement Tools for Latest Technologies

MUNICH, GERMANY – SUSS MicroTec AG has installed the latest 300 mm technology in wafer probe systems at the nanoelectronics research center IMEC in Leuven, Belgium. Both PA300PS ProbeShield® semiautomatic probe systems with ReAlign™ and ContactView™ technology and PA300 probe systems for RF-noise and S-parameter measurements have been installed. An agreement has been made for further collaboration on enhancing 300 mm probe systems in the following years.

"We are very pleased to sign this agreement with IMEC, Europe's leading independent nanoelectronics research center," said Dr. Claus Dietrich, Managing Director of the Test Systems division at SUSS MicroTec. "This collaboration proves SUSS MicroTec is offering the latest technology for advanced wafer probing, like the unique ReAlign and ContactView solutions. Furthermore, it shows that we continue to set standards in excellent electrical performance, such as noise and leakage levels, with our cutting-edge hardware and software solutions."

In another development, SUSS MicroTec will deliver a second vacuum probe system to IMEC. The manual system will compliment the existing semiautomatic vacuum system, which is currently being used to test the reliability of MEMS devices at wafer level. These unique systems allow the user to place the device under test in ultra-high vacuum environments that simulate actual operating conditions. Therefore the device can be tested before the packaging process, which decreases feedback time for R&D and saves costs.

IMEC's technologies and devices are on the front line of technology development, and therefore new measurement challenges arise continuously. Close collaboration with SUSS MicroTec will ensure early feedback on possible future needs for wafer-level testing, and IMEC will explore solutions and future enhancements together with SUSS.

Ultrasonic Coating Module Debuts at Semicon West

HAVERHILL, MA – Ultrasonic Systems, Inc. will introduce their new Ultrasonic Coating Module at the Semicon West Show, Booth 8007. This new modular system design is perfect for integration into robotic work cells or semiconductor integrated processing systems.

This Ultrasonic Coating Module features the CAT 35 ILDS (Integrated Liquid Delivery System) Coating Head, micro-valve control, and PLC controller for integration into work cell software. This coating head provides a superior alternative to conventional spin coating, dispensing and other coating technologies.

Ultrasonic Systems, Inc. manufactures the world's most advanced spray coating systems. Headquarters are located at 135 Ward Hill Ave, Haverhill, MA 01835 USA; Tel: (978) 521-0095; Fax: (978) 521-7023; e-mail: sales@ultraspray.com; web: www.ultraspray.com.

Maxtek Earns ISO 14001:2004 Certification

BEAVERTON, OR – Maxtek Components Corporation, a Tektronix, Inc. company and a custom microelectronics assembly and test service provider, has announced that it has achieved ISO 14001:2004 certification. ISO is the International Organization for Standardization, and ISO 14001 is a globally accepted standard that pertains to creating and managing environmental management systems.

"We view the ISO 14001: 2004 certification as a key element of our company-wide quality initiative, which is designed to enable our customers' most advanced microelectronic technologies while minimizing their development risks," said Tom Buzak, President, Maxtek Components Corporation. "The ISO 14001:2004 certification sets Maxtek apart from many of its competitors and positions the company to better serve its customers striving to comply with environmental programs in their own industries and regions."

Maxtek, a Tektronix company, is a proven custom microelectronics company providing a complete range of design, assembly and test services to equipment manufacturers. With 35 years of experience serving the measurement, military and medical markets, Maxtek works as an extension of their customers' product teams to resolve the most demanding packaging challenges. Headquartered in Beaverton, Oregon, Maxtek can be found on the web at www.maxtek.com.

AIT Expands Batam Factory

SINGAPORE – Advanced Interconnect Technologies (AIT) has announced that it is expanding its world-class assembly and test factory in Batam, Indonesia, to 400,000 square feet by September of this year – adding more than 30,000 square feet. This expansion will be developed on AIT's existing property in the Batamindo Industrial Park.

With the expansion of the Batam factory, AIT will be able to enlarge its floor space dedicated to final test which will allow them to meet the growing demand in the industry and from its existing customers for full turnkey assembly and test services. Faced with continued pressure to streamline time-to-market and improve profit-ability, many semiconductor manufacturers are using outsourcing as a key business strategy. While outsourcing wafer production has become commonplace in the industry, now both test and assembly functions are also being outsourced by fabless manufacturers and integrated device manufacturers (IDMs) alike.

For more information about the company, its products and services please visit their website at www.aithome.com..

Kyocera Creates Department of Continuous Improvement

SAN DIEGO, CA – Kyocera America, Inc. has announced the creation of a Department of Continuous Improvement. This department will consist of Kyocera America's trained and dedicated "Black Belt" Specialists in Lean Six Sigma tools.

"The Department of Continuous Improvement will help support our initiative of better

serving our customers by facilitating improvement projects in production, sales and support areas throughout the company" said Bob Whisler, President of Kyocera America, Inc.

Lisa Hamel, formerly Engineering Manager in the Metallized Division, will lead the department as Manager of Continuous Improvement.

Hymite Awarded ISO 9001 Certification

COPENHAGEN and BERLIN – Hymite announces that it has been awarded the ISO 9001 certificate. Hymite develops, manufactures and markets innovative packaging solutions for semiconductor devices that allow better performance and optimized manufacturing.

"Our packaging technology is based on silicon – this enables us to increase the level of functional integration and to use highly automated manufacturing technologies developed by the semiconductor industry. The ISO 9000 certification is for us another step that demonstrates our dedication to obtain best-in-class quality and give the support to our customers to achieve their cost and performance goals", says Jochen Kuhmann, CTO and founder of Hymite. "Today we are engaged in several customer projects within high growth markets such as mobile phones, consumer applications and communications products. The certification process has helped us to tune our manufacturing and management processes so that we are ready to ramp up to volume production."

March Plasma Systems Opens Direct Offices in Shanghai, China

CONCORD, CA – Building on over 20 years of continuous plasma technology innovation, March Plasma Systems has announced that it has established direct operations in Shanghai, China. The new March offices are located at 828 Xin Jin Qiao Road, Pudong, Shanghai 201206, China. The office telephone number is +86 -21-5854-2345, and the facsimile number is +86-21-5854-9150.

To manage March's China operations, March has appointed Mr. David Pang as Regional Sales Manager and named Mr. Michael Zhang as Applications Field Service Engineer. Other recent activities include the appointment of new distributors for the semiconductor and PCB markets, and the formation of strategic alliances with key e-zquipment partners within the Chinese market.

The China facilities are equipped with an advanced Applications and Demonstration Laboratory containing a variety of March plasma processing systems for local customer training, demonstrations and applications support.

Contact March Plasma Systems directly or see the March web site for more details: www.marchplasma.com.

Nagase Acquires 60% Share of Pac Tech GmbH

NAUEN, GERMANY – Pac Tech GmbH has announced that Nagase and Co., a major trading company in Japan, has acquired a 60% share of Pac Tech GmbH, for an undisclosed amount. The acquisition was completed on February 10, 2006.

Pac Tech GmbH focuses on bumping and packaging based on advanced electroless metallization. It also provides advanced laser bonding and bumping equipment worldwide. Pac Tech GmbH doubled its sales worldwide in 2005 to roughly 14 million Euros.

Nagase began selling Pac Tech GmbH equipment and technology licenses in Japan in 2000. According to Nagase Director Executive Officer Mr. Kazuo Nagashima, "Through the addition of Pac Tech's technology and its market penetra-

tion in Japan and China, we intend to double our overall sales of back-end equipment and materials over the next three years from approximately 6 billion JPY in 2005."

Pac Tech GmbH equipment offers semiconductor manufacturers several distinct advantages over other conventional methods. There is virtually no damage to substrates using their patented contactless method of applying solder-balls to fine and thin materials such as those used in hard disk drive head applications. The electroless wafer bumping method has a strong advantage in achieving short lead-time and low-cost compared to existing electroplating methods. As semiconductor geometries become smaller and smaller, the need for very fine-pitch solder-ball placement and wafer level packaging will become even more critical.

Visit the Pac Tech website at www.pactech.de.

STATS ChipPAC Expands QFN Portfolio for Wireless Applications

U.S. & SINGAPORE – STATS ChipPAC Ltd. has announced that it has expanded its Quad Flat No-lead (QFN) packaging portfolio with technology advancements in both single mold cavity format and molded array format for applications requiring a higher number of input/output (I/O) terminal pads and lower package profile and weight.

QFN is a leadframe based, plastic encapsulated, chip scale package in either single mold cavity format (punch singulated) or molded array format (saw singulated). An exposed die pad combined with extremely low RLC (resistance, inductance, and capacitance) provides excellent electrical and thermal performance enhancement which is ideal for high frequency and high power applications, particularly wireless and handheld portable applications such as mobile phones. STATS ChipPAC offers multiple configurations in each of these package types.

The saw singulated version, or QFNs, is a leadframe based molded package in land grid array format with square or rectangular body sizes. The QFNs is available in 0.40mm, 0.50mm, 0.65mm and 0.80mm lead pitch, with standard package profile heights of nominal 0.75mm or 0.90mm. STATS ChipPAC now offers an extremely thin version of the QFNs, called XQFNs, which features a nominal package height of 0.45mm. Advanced molding technology, wafer thinning technology, and ultra low loop wire bonding are key to achieving the extremely low profile height of the XQFNs.

For customers who require devices with higher I/O terminal pads in a smaller footprint, the dual row punch singulated (QFNp) package design, called VQFNp-dr, can accommodate greater than 50% more terminals than a single row QFN pad design in the same body size. The VQFNp-dr features two rows of staggered I/O terminal pads in a 0.50mm lead pitch with an exposed die pad for die grounding and improved thermal performance. With its higher number of terminals pads and small profile, VQFNp-dr also enables higher functional integration in a package by means of die stacking. VQFNp-dr is available in body sizes up to 12mm x 12mm with up to 156 pins.

QFN packages are available in various body sizes and thicknesses, offered in standard and green/lead-free bill of materials, and can be processed by conventional SMT equipment, benefiting surface mount operations downstream.

Further information is available at www.statschippac.com.

Gartner's Final Semiconductor Market Share Results Show Industry Grew 5.7 Percent in 2005

STAMFORD, CT – Worldwide semiconductor revenue totaled $235 billion in 2005, a 5.7 percent increase from 2004, according to final results by Gartner, Inc. 2005 revenue surpassed the semiconductor industry's previous record of $223 billion set in 2000.

"Personal computers and cellular telephones remain the largest drivers for semiconductor business," said Richard Gordon, research vice president at Gartner. "The popularity of MP3 players, however, accounted for dramatic growth among flash memory vendors in 2005."

High PC demand helped Intel retain its position as the No. 1 semiconductor supplier in 2005. Intel's revenue grew 12.6 percent, twice the market average. Commodity memory demand bolstered the fortunes of Samsung Electronics, who now dominates most areas of the memory market, and Hynix Semiconductor, who moved into the top 10 for the first time in 2005.

Samsung held the No. 1 position in DRAM, SRAM and the fast-growing NAND flash market in 2005. Hynix's NAND flash revenue reached $1.5 billion, up from $212 million in 2004, an increase of more than 600 percent. Over all, this company grew 23 percent – the fastest growth among the top 10 semiconductor suppliers.

The entire NAND flash memory segment grew 71 percent between 2004 and 2005. Other fast growth markets included CMOS image sensors (28 percent), and consumer ASICs (14 percent). The wireless ASIC segment, where Texas Instruments was the market leader, grew 9 percent last year.

The regional trend of sales moving towards Asia/Pacific continued in 2005. The Asia/Pacific region, which includes China, Taiwan, Korea and Singapore, accounted for 44.5 percent of worldwide semiconductor revenue, and the region experienced the strongest growth in 2005 – 11 percent. The Europe, Middle East and Africa (EMEA) region saw the next strongest revenue growth with 4 percent. The Americas had 1 percent growth in 2005 and Japan was flat with revenue increasing 0.2 percent.

Additional information on specific market segments and devices is available in the Gartner report "Market Share: Semiconductor Revenue, Worldwide, 2005." This report provides rankings among vendors of microprocessors and memory, DSPs, ASICs, Application-Specific Standard Products (ASSPs), analog ICs, discretes and many other semiconductor products. The revenues of top suppliers are identified in specific markets such as automotive, consumer products, wireless and wired communication, computers, com-puter peripherals and industrial controls. Regional market share results are also available for the Americas, EMEA, Asia/Pacific and Japan. The report is available on Gartner's web site at www.gartner.com/DisplayDocument?doc_cd=120719.

Semicon West 2006 TechXPOT Offers Special Focus on Test, Assembly and Packaging Technologies

SAN JOSE, CA – SEMI has announced additional details for its upcoming Test, Assembly and Packaging TechXPOT, located in West Hall Level 2 of the Moscone Center during SEMICON West 2006, July 11-13 in San Francisco. Building on the "show-within-a-show" concept, the Test, Assembly and Packaging TechXPOT is a special area focusing on innovations in test, assembly and packaging, with exhibits, dis-

plays and exhibitor presentations on the topic. In addition, the Test, Assembly and Packaging TechXPOT will feature presentations from select winners of the fourth annual Technology Innovation Showcase (TIS), as well as two detailed roadmap sessions.

In a continuous effort to build a stronger and higher quality curriculum, SEMI has partnered with leading industry associations and companies including FSA, the International Electronic Manufacturing Initiative (iNEMI), the Microelectronics Packaging and Test Engineering Council (MEPTEC) and TechSearch International to create the Test, Assembly and Packaging TechXPOT at SEMICON West 2006.

A dedicated display area will feature examples of the latest packaging technologies. Additionally, the TechXPOT will house a stage for TIS winners and select exhibitors to present technical content and solutions. Sessions include: test roadmaps and design for test, organized by SEMI; user packaging roadmaps, organized by MEPTEC; fabless roadmaps, organized by FSA; and a lead-free seminar, organized by iNEMI and TechSearch International. Additionally, buses from SEMI headquarters located in San Jose will be available for attendees who would like to attend SEMICON West. The shuttle is free, however registration will be required.

Topics for the first of the two Test, Assembly and Packaging sessions include: Drivers and Challenges for Packaging of Next Generation FPGAs, featuring Tarun Verma, director of packaging technology at Altera; ASICs Packaging Roadmap, featuring Maniam Alagaratnam, vice president of package development at LSI Logic; and Critical Package Requirements for Advanced Manufacturing Flow, featuring Bo Chang, packaging engineering director at Cypress.

The second Test, Assembly and Packaging session will cover: Modeling for Material Sets in Semiconductor Packaging Assembly, featuring Jack Zhang, Ph.D., materials scientist at Henkel Corporation; Impact of Application Surface on the Development of TIMs, featuring Devesh Mathur, director of global technology at Honeywell; Electronic Packaging Materials, featuring Jonathan Harris, president of CMC Interconnect Technologies; and a Global Semiconductor Packaging Materials Outlook, featuring Dan Tracy, senior director of industry research & statistics at SEMI.

For more information about the Test, Assembly and Packaging TechXPOT, and SEMICON West 2006, please visit www.semi.org/semiconwest. ◆

North American Semiconductor Equipment Industry Posts April 2006 Book-To-Bill Ratio of 1.11

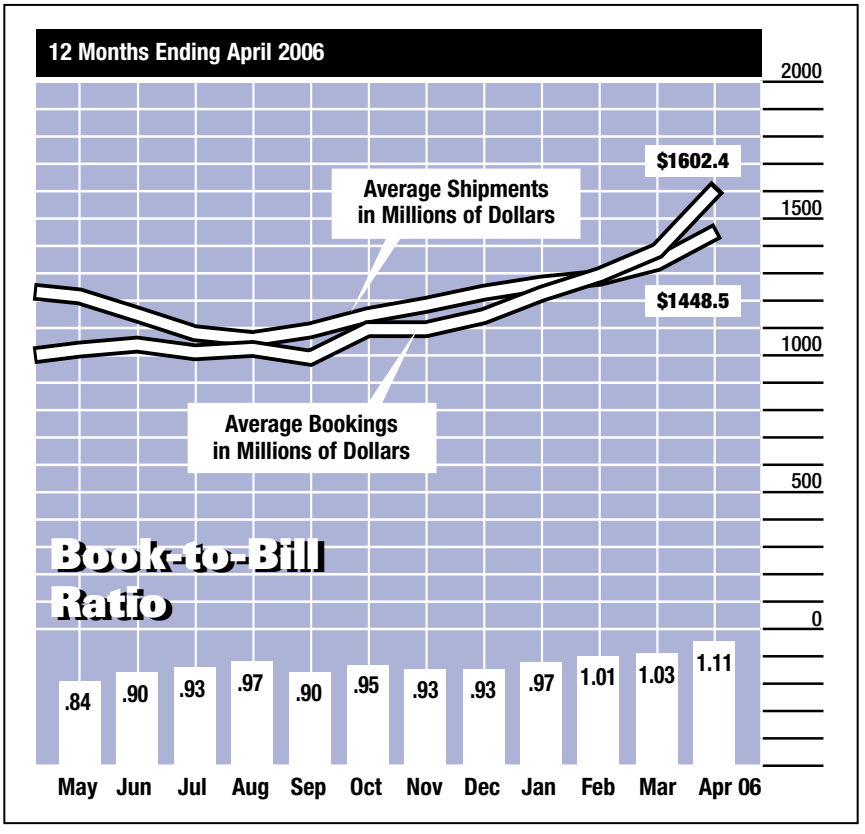
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.60 billion in orders in April 2006 (three-month average basis) and a book-to-bill ratio of 1.11 according to the April 2006 Book-to-Bill Report published today by SEMI. A book-to-bill of 1.11 means that $111 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in April 2006 was $1.60 billion. The bookings figure is almost 16 percent higher than the final March 2006 level of $1.39 billion and over 60 percent higher than the $999 million in orders posted in April 2005.

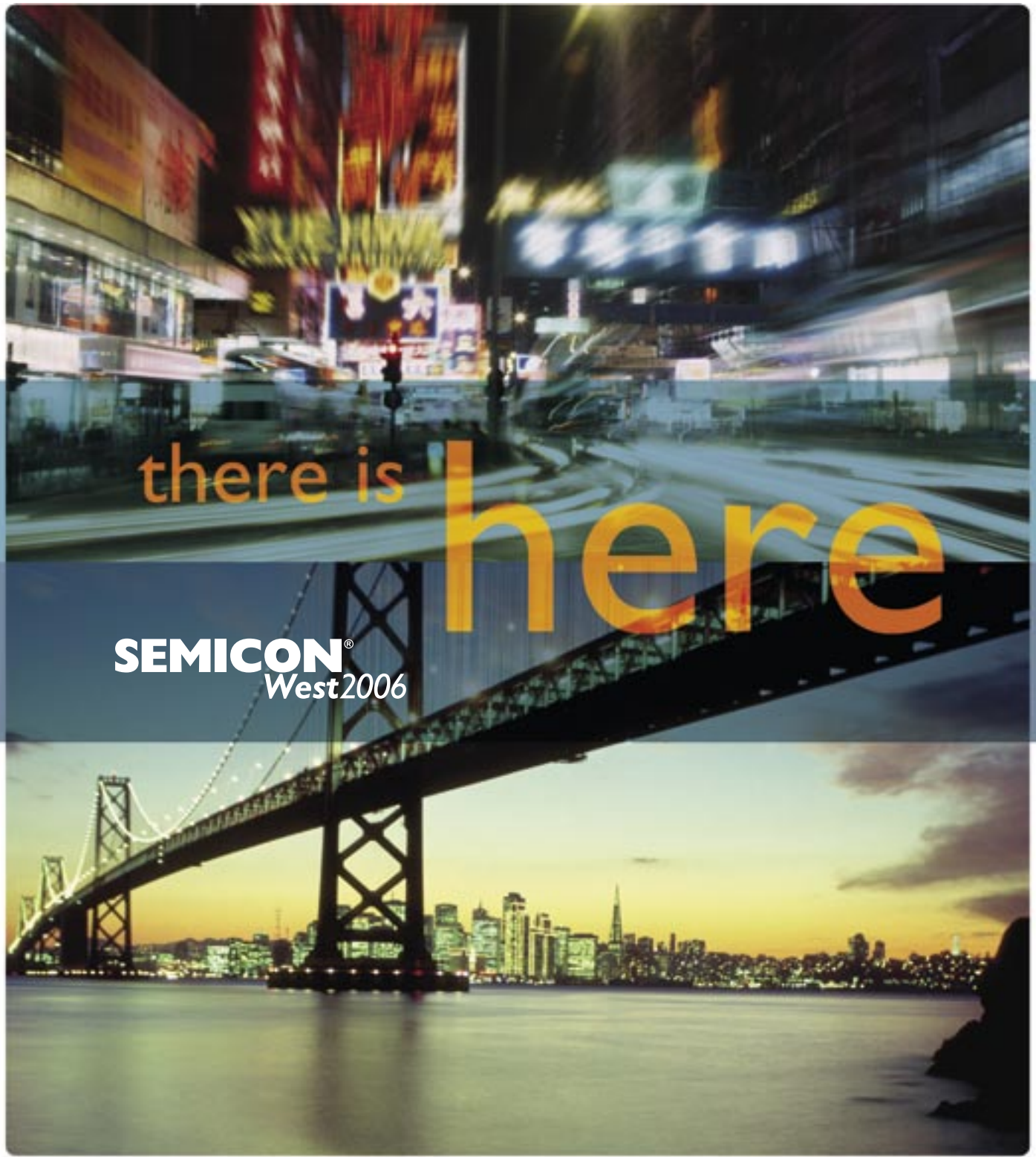
The three-month average of worldwide billings in April 2006 was $1.45 billion. The billings figure is eight percent above the final March 2006 level of $1.34 billion and almost 17 percent above the April 2005 billings level of $1.24 billion.

"The book-to-bill continues into its fifth consecutive month of growth, and third over parity," said Stanley T. Myers, president and CEO of SEMI. "This continued trend points to increasing confidence in the market and a healthy year over year billings growth in 2006."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.



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FlipChip International

New Services, New Look

Attending the FCMS ground breaking in Shanghai were (from left) HK Foo (Executive Vice President and GM of MMS), Tom Strothmann (Vice President of New Business Development at FCI), Bob Forcier (President and CEO of RSL), and Vic Tee (President and CEO of Millennium MicroTech).

Bob Forcier, President/CEO and Dr. Joan Vrtis, CTO of Rose Street Laboratories (RSL) had a vision. They wanted to 1) provide flip chip and wafer level packaging services in the number one growth area in packaging, 2) operate internationally to support North American, European and Asian marketplaces, 3) incorporate new IP into products and services and 4) form the team to make this vision successful. With these goals in mind, Forcier and Vrtis initiated actions to secure FCI's future.

Rose Street Laboratories, the parent company of FlipChip International, was founded in 2003 with a roadmap of providing leadership in product and service support to the electronics industry. RSL has been very active in the life sciences, renewable energy and homeland security markets and has gathered rights to over forty patents and patent applications during these initial years.

RSL opened its first basic research laboratory for commercialization of products in 2005. The lab was designed for advanced polymer and bio chemical research. Another lab will be opened in 2006 designed for commercialization of advanced solar cell packaging and next generation flip chip products. RSL currently has two product incubations preparing for commercialization and spin out – a Full Spectrum Photovoltaic product and a Metabolic Breath Analyzer product. RSL and its wholly owned subsidiaries now employ over 250 people, including a substantial group of engineers and scientists. RSL is privately held as an LLC incorporated in Delaware.

FCI's joint venture with Millennium MicroTech in China - FCMS.

In ***February, 2004***, the acquisition of Kulicke and Soffa's Flip Chip Division (K&S FCD) in Phoenix, Arizona enabled FCI with bumping technology services that are well known in the industry. This acquisition included standard flip chip and UltraCSP® as bumping offerings and is now FCI's Bumping Division. Since the acquisition, a specialized polymer process named Spheron® has been commercialized and is gaining popularity as a high performance solution for high speed applications such as Radio on Chip. An Electroless Ni/Au - bumping process has been added as well. Electroless plating - bumping compliments other bumping processes at FCI with a low cost solution to the industry. Other new processes that have been implemented at FCI are backside coat, laser mark and enhanced automated optical inspection.

FCI's innovations include the design and manufacture of custom robotic-controlled, automated wafer processing equipment to support advanced processes requiring stringent process control.

Some of the largest manufacturing subcontractors have chosen FlipChip International processes and license the processing today. ASE, SPIL, Amkor, and STATS/ChipPac are currently active as licensees.

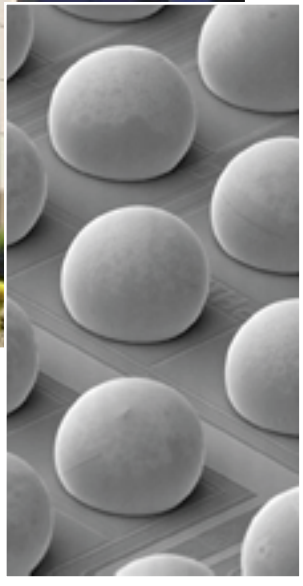
When FCI acquired K&S FCD, there were 103 employees. Now, FCI employs over 200 people at the Bumping Division on a 24/7 shift coverage basis. The Bumping Division continues to grow and FCI is currently adding personnel and capital to meet increased market demand. Wafer output will grow 50% in 2006 and another 50% in 2007.

FCI's Bumping Division is currently supporting over 90 customers in markets such as telecom and medical.

Next, was the acquisition of IC Services in Minnesota with operations primarily in Tempe, AZ in ***February, 2005***. This acquisition is now FCI's Die Sales Division (DSD) and further enables FCI with back end processing capability that compliments the Bumping Division. DSD encompasses processes including backgrinding, saw, automated optical inspection and tape/reel, tray, film frame end use packaging.

The Die Sales Division employs approximately 50 people also on a 24/7 shift basis. DSD is also adding personnel

FlipChip International's corporate headquarters, located in Phoenix, Arizona.



The acquisition of K&S's Arizona Flip Chip Division enabled FCI with bumping technology services that are well known in the industry.

and capital to meet increased demand. Current output is 600,000 die per week – growing to 1.5M die per week this year.

FCI's Die Sales Division is currently supporting over 40 customers in markets such as automotive, medical and consumer.

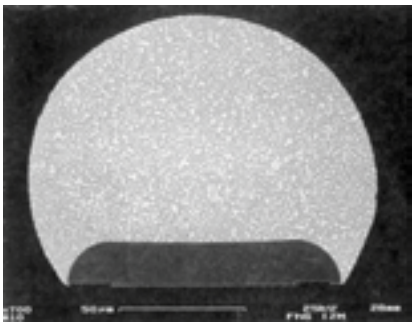
Another major event for FCI, again in February, was the venture into the Asian market and to make the company's namesake. In ***February, 2006***, FCI announced the joint venture with Millennium MicroTech Shanghai, China. This joint venture initiates bump and back end process manufacturing support in the Asian market. Phase 1 is underway in the Pudong area with a new Electroless Ni/Au - bumping line being implemented. Several phases are planned to develop and implement more bumping and back end processing in Shanghai for future expansion.

FCI has attracted several industry veterans that are now involved in the success at FCI. Dr. Joan Vrtis is CTO. Bruce Bowers is V.P. Business Development. Fred Hickman is V.P. Sales and Marketing. Jay Grover is V.P. Operations. Ted Tessier is V.P. Engineering. Terry Lubsen is V.P. Quality. Tom Strothmann is V.P. New Business Development (China).

Wafer Level Electrical Test (WLET) has been developed at FCI through alliances with test service companies. Three test service companies are now qualified to cover an array of test platforms. FCI provides program management for test program development, hardware design/fabrication, product characterization, correlation/qualification and production volume testing. By providing WLET, FCI provides turn key support covering every flip chip/WLP process step from wafer fabrication through direct shipment.

Will we have to wait until next February to hear what's next ??

"Probably not" says Forcier. "We have some more exciting developments on the way that further expands our process/product offering. Look for more technical and geographical growth at FlipChip International."



Cross-section of electroless UBM and solder.

How do you feel about the goals you set at the outset of your business ventures?

Forcier's response. "Very, very good – especially when we review the health of the company. We have been profitable every single quarter."

"We have doubled our headcount in Phoenix to meet our customer demands and continue to break performance indices month to month. We have dedicated employees that care about FCI."

"Our revenue continues to grow and with expansion in both our core business and new business endeavors, we are excited about our future."

" Our operation in China is off to a good start with a great partner."

"We have shored up our offerings, made continuous improvements and are underway to make even more dramatic improvements with investments in people and equipment." says Forcier.

Inquiries can be made via FlipChip International's website at www.flipchip.com or visit their booth at Semicon West in the West Hall – booth number 8246.◆

Low Cost, High Performance Silicon Packages

Vertical µ-via enabled silicon wafer level packaging for hermetic sealing, stacking and SiP applications

Dr. Jochen Kuhmann, CTO, Andreas Hase, Product Manager
Hymite A/S, Denmark, Hymite GmbH, Germany

The fast growing market of handheld devices drives the miniaturization of components and subsystems. In addition to performance, package size and assembly strategy have become key parameters. Chip scale packages begin to replace traditional leadframe packages and device integration in subsystems is strongly emerging supported by wafer level packaging technology.

Using silicon as a packaging material has advantages in thermal performance to support power dissipation of devices in high density assemblies, it matches the coefficient of thermal expansion (CTE) of silicon based devices like electronic ICs or micro-electro-mechanical systems (MEMS) and thus reduces thermo-mechanical stress and increases reliability.

In this article we describe the use of micro-machined silicon with vertical through wafer μ-vias as a packaging platform. Vertical feed-throughs in silicon play a pivotal role to meet the stringent requirements of handheld applications with respect to cost, size and manufacturability. In addition monolithic integration of passives and precise mechanical manufacturing together with accurate alignment during wafer to wafer assembly allows for ultra small and low profile silicon packages.

Package Requirements

To enable low cost, high volume packaging the complete manufacturing flow of components and systems has to be considered. Size constrains of final products require subsystems with small footprint and low profile while the board level interface and the design rules defined by standard IC assembly processes constrain the I/O density of electrical interconnects. Device integration in one package reduces the number of I/Os to board and enables complete subsystems.

System designers prefer the use of completely tested sub systems encouraging the development of systems in a package (SiP). Board level assembly requires surface mount technology, and the packages need to interface with solder land pads or solder bumped pads.

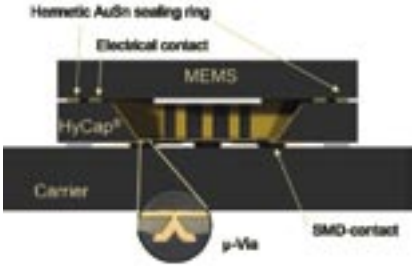


Figure 1: Schematic of MEMS packaging by HyCap®. HyCap® provides sealing and electrical connection to MEMS in a one step assembly. Electrical µ-vias enable smaller MEMS and SMT mounting to a carrier or PCB board. Insert: microscope picture of a cross sectioning through a µ-via.

Conventional packages use die level handling with complex, and costly processes. For MEMS devices the particle generation during assembly can result in failure of the device and 2nd level packaging contributes to the large device size. A significant portion of up to 70% of the final device cost originates in the packaging of the component.

The advantage of wafer level packaging compared to individual die handling explains the increasing popularity of this process. This includes chip to wafer assembly of active and passive components and sealing caps on wafer level by the use of pick and place equipment. In addition wafer to wafer sealing or stacking of two or more wafers has become an enabling technology. The wafer level processes completely changes the cost structure of the final package by reducing die handling, shortened alignment cycles and decreased bill of material.

Hermetic sealing of devices is an additional requirement mainly known from the MEMS world. Different sealing methods are available and care must be taken that the selected process is compatible with the MEMS device.

Surface to surface bonding, like anodic or fusion bonding, involves high temperatures and require a flat surface. An alternative sometimes used is surface activation at low temperature. Like the methods previously outlines, this has the disadvantage that it does not provide electrical connection to the device. Commonly used in the MEMS industry is glass frit sealing. This insulating interlayer needs a wide sealing ring to provide reliable sealing and lateral electrical feed-throughs increase the space requirement on the MEMS device. A metallic interlayer on the other hand allows for narrow sealing rings and small footprint when vertical electrical feed-throughs are available.

HyCap® - The Silicon Packaging Solution

Hymite has developed and manufactures silicon packages utilizing vertical, hermetic feed-throughs. A representative package is shown schematically in Figure 1 with a MEMS device hermetically sealed

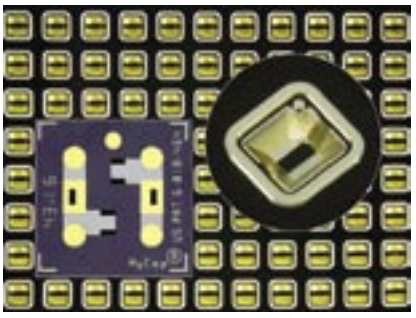


Figure 2: HyCap®S wafer with enlarged pictures of the sealing ring side and the SMT side. Electroplated AuSn solder on the electrical connection and sealing ring metallization defines the interface to MEMS device. The deep cavity of up to 500 µm gives headroom for devices. The SMT side shows pads for solder deposition by stencil printing separated by a solder dam.

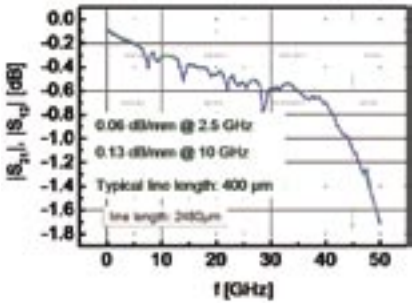


Figure 3: RF transmission line measurements for an impedance matched coplanar line along sidewalls, cavities and through µ-vias of a HyCap®.

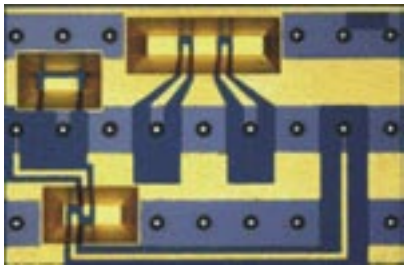


Figure 4: SMT solder bumped backside of a HyCap® for a RF application. Tapered coplanar lines for impedance matching are running into the cavities and connect to the frontside through µ-vias.

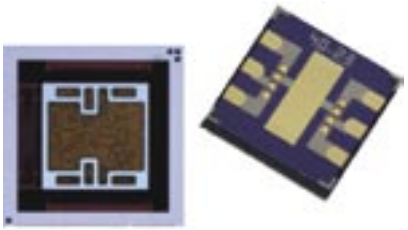


Figure 5: General purpose SON/QFN-style package (front and backside). Components can be placed into the cavity. Slanted sidewalls can act as reflectors as light reflectors for optical emitter applications. SMT metallization is continued up slanted outer edges for solder filleting.

by a HyCap®. In a one step assembly to the MEMS device the silicon cap forms the electrical contact and the hermetic sealing by the AuSn metallic interlayer. The sealed volume has a controlled atmosphere or vacuum. Sealing with the HyCap® transforms the MEMS into a surface mountable device which can now be mounted to a carrier or PCB board without the need of wire bonding.

The HyCap® is processed using standard silicon wafer micro-machining processes. The wafer processes are currently implemented at 6 inch, but can be scaled to 8 inch for cost reduction and volume purposes. A cavity is formed by wet isotropic etching providing headroom for the MEMS. In the membrane formed by the cavity vertical μ-vias are etched and a thermal oxide acts as passivation for the subsequently deposited metallization. Using 3D lithography and electroplating of metal the vias are filled and sealed. The electrical connection from the SMT side of the HyCap® to the solder pads is formed along the slanted sidewalls. The solder pads in turn connect to the MEMS. The insert in Figure 1 shows a microscope image of a cross section through a μ-via filled with electroplated metal. The electrical contacts and the sealing ring are electroplated with AuSn solder for soldering to the MEMS (Figure 2).

Compared to dry etched through wafer vias this low cost batch process ensures perfect isolation (thermal SiO2), avoids sharp edges and defines a uniform metal layer without void formation. In addition, using coplanar waveguide design, the HyCap® is well suited for RF applications with low attenuation up to 40 GHz (Figure 3). Typical line length on a HyCap® are in the range of 400 μm with a loss of 0.13 dB/mm at 10 GHz. Figure 4 shows an implementation of two coplanar waveguide lines from the SMT pads into a feed-through cavity to the sealing side. Due to the wafer topology the lines are tapered to maintain the impedance from the board up to the sealed device.

For high power applications the vias can be designed for high current loads of up to 2 A.

The SMT interface strongly depends on the final application and can be in the form of solder bumped arrayed pads (Figure 4) or in SON/QFN style (Figure 5) to meet the requirements of standard assembly lines. The SMT pad metallization on the SON/QFN style package has visible slanted edges for post board assembly inspection.

Beside the benefits of wafer level packaging the vertical μ-vias allow for smaller MEMS die, reducing MEMS cost by increasing the number of dies on a wafer.

For wafer level testing, all contacts to the device are on one level and accessible via the HyCap®.

Figure 6 shows different HyCap® configurations for device integration. In these the HyCap® is used as a bench to mount devices either by soldering or epoxy attachment. Wire bonding or flip-chip attach may be used to electrically contact the device (Figure 7). Careful selection of epoxy allows for subsequent sealing if required. The complete assembly can be performed chip to wafer reducing handling and testing costs.

Availability of small e.g. 01005 SMD passive components is limited and handling is difficult, therefore, monolithic integration of passives like resistors, inductors and capacitors opens the path for further cost and size reduction. Figure 8 shows integrated thin film resistors on cavity sidewalls for RF applications.

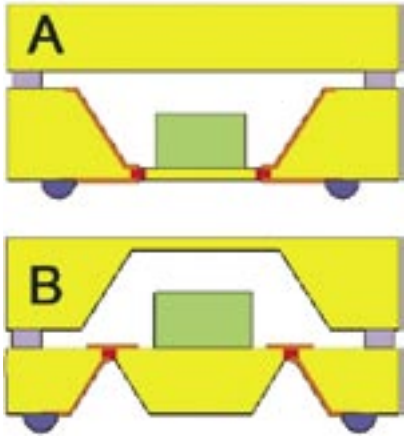


Figure 6: HyCap® configurations for device integration. Lid sealing is optional and depends on device requirements A) Placing the device into the cavity gives best access for thermal management in case of high power applications. Metallization on cavity sidewalls improves shielding and can act as a reflector for light emitting devices. B) Silicon interposer configuration.

Figure 7: Active and passive device integration on HyCap®.

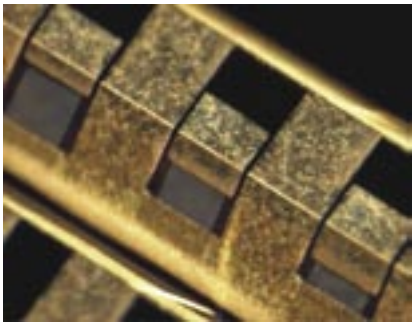


Figure 8: Integrated thin film resistors on cavity sidewalls for RF applications.

The low silicon thermal resistivity enables new approaches for high power device packaging. A thermal model using finite element analysis (Figure 9) shows the performance for a flip chip assembly of a high power device in the cavity. Electroplated solder is provided in the cavity of the HyCap®. The thermal resistivity is below 5° C/W. This packaging concept sets

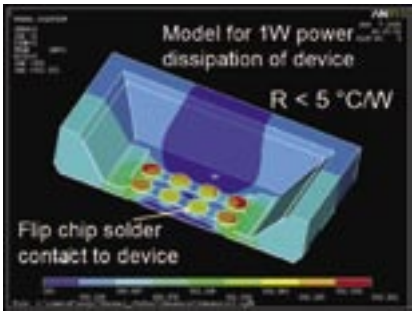


Figure 9: Low thermal resistivity of silicon package. Thermal modeling of power dissipation for flip chip mounted device.

Figure 10: HyCap®U pad metallization on SMT side. Solder bumping is performed on wafer level by stencil printing.

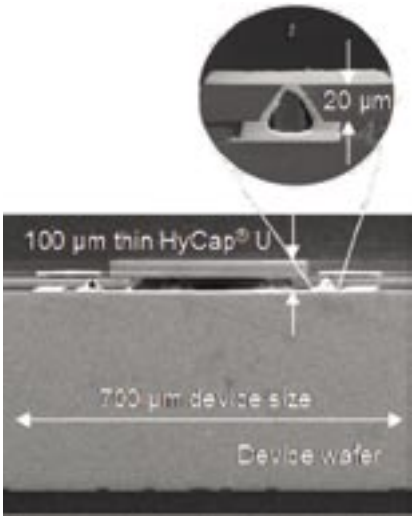


Figure 11: Cross section of low profile HyCap®U package. Insert shows detail of µ-via through thin membrane.

new standards in terms of size and thermal performance.

The silicon packaging solutions described up to now were based on wafer thicknesses in the order of 400 μm, giving large headroom for devices. These packages go under the product name HyCap®S and they may be assembled as chip to wafer or as wafer to wafer.

At this years *Electronic Component and Technology Conference, ECTC*, Hymite introduced an ultra low profile silicon cap called HyCap®U. The hermetic cap only adds 100 μm to the device height and encompasses wafer level assembly and backgrinding. Hermetic packages as small as 700x700 μm can be manufactured with I/O counts of 4-6 (depending on bump size requirements for SMD, see Figure 10). A cross section SEM picture (Figure 11) illustrates the manufacturing process. As a first step, the one side processed HyCap®U wafer is bonded to the device wafer. The wafer bonding seals and protects the device, before the final grinding and SMT pad definition. The vias are formed in thin membranes with very little lateral space consumption. Optionally the cap can be manufactured with a shallow headroom of up to 60 μm.

In the following we like to introduce some standardized HyCap® solutions for hermetic sealing. These designs are implemented in the new release of the Coventor MEMS software CoventorWare 2006 as a package library and cover DC and RF implementations.

HyCap®S - Deep Cavity Silicon Package

Figure 12 shows HyCap®S chip size packages for DC and RF applications. The cavity depth is chosen to be 350 μm resulting in a smallest package for the a 6 contact DC applications of 1760 x 1600 μm. One GND contact connects to the sealing ring. The RF design uses impedance matched coplanar waveguides for the two RF ports. Two control lines are arranged perpendicular to the RF ports. The sealing ring is grounded to avoid electrical coupling. Smallest design: 2200 x 2000 μm.

In addition to the solder bumped SMT interfaces demonstrated, all HyCap®S designs are also available as SON/QFN style packages.

HyCap®U – Ultra Low Profile Silicon Package

Depending on the actual device size the low profile 6 contact DC HyCap®U can be smaller than 1000 x 1000 μm. The DC design included in Figure 13 has a headroom area of 650 x 430 μm. Again one contact grounds the sealing ring.

The corresponding RF design uses a coplanar waveguide arrangement of the ports. Two control lines are arranged perpendicular to the RF ports. The short line length, small footprint and low profile make this package attractive for handheld RF applications. The number of RF ports can easily be increased.

Conclusion

Silicon as a packaging material offers excellent thermal and electrical performance. HyCap® products address the need of a hermetic, SMT compliant, chip sized package with an easy to design interface. HyCap® provides enabling solutions for emerging markets like MEMS and SiP and shorten the development cycles of device manufacturers.

The use of standard silicon micromachining for manufacturing of silicon housings and reliable vertical μ-vias in HyCap® products allow very small formfactors in packaging and a high cost reduction potential for device sealing. ◆

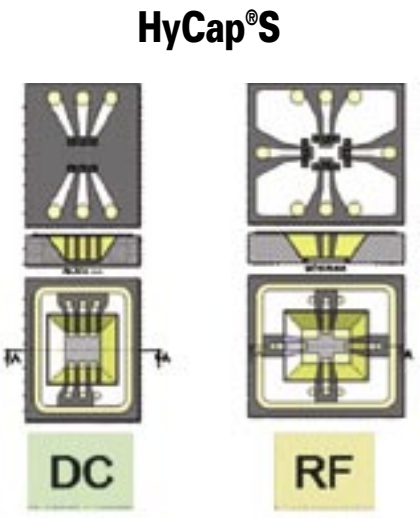


Figure 12: DC and RF HyCap®S designs for hermetic sealing.

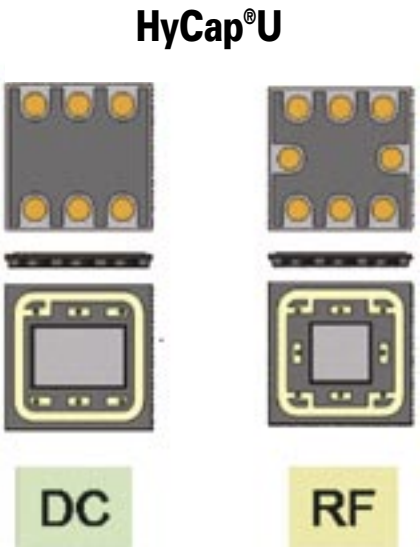


Figure 13: DC and RF HyCap®U designs for hermetic sealing.

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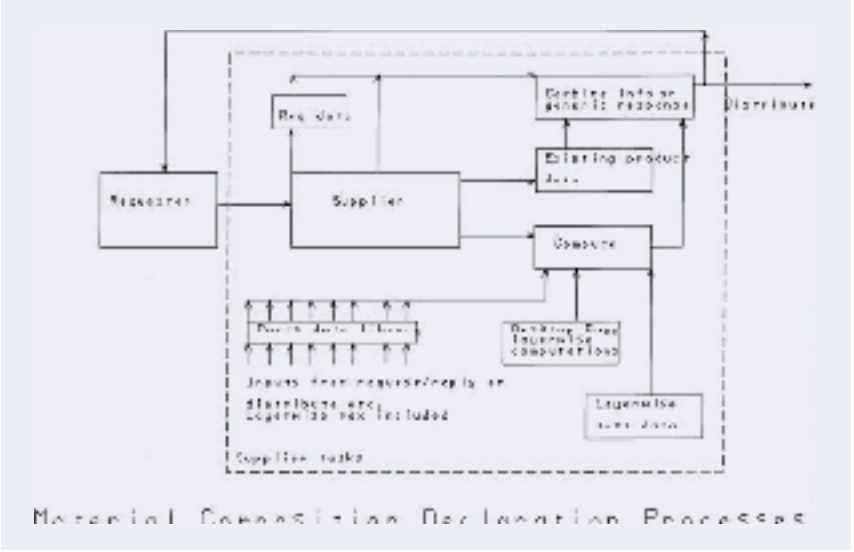
Materials Declarations for Everyone

N. Nagaraj, PhD, PE
Papros Inc.



Current and potential future regulations have brought about a need for a uniform and consistent method for encapturing, expressing and exchanging material content data in the form of Material Composition Declarations. Materials Declarations may be exchanged in a variety of means. These can be distributed on secure websites, exchanged securely such as by using the IPC forms 1752 or by traditional less secure email, flash drives or other modes of storage. Supply chain data requires high degrees of security, and thus reduces the choices frequently to distribution on secure websites or for exchange of the IPC 1752 forms. The need for exchange of IPC 1752 form information requires companies to generate accurate material composition information that the users can rely on to generate their own MCDs.

Discussion

Users of Material Declarations for parts and/or products can obtain MCDs downloaded from a secure website if they are distributed as such. Typically, Material Declarations exchanges can occur by a Requester sending a request in an IPC form electronically to a Supplier. This Supplier captures the requester information including any custom declarations and/or other details and collates it with requested information and sends it back in the IPC 1752 electronic form. In the context of the diagram, the term Supplier is used to mean either the Supplier who is collecting Product information for the manufacturer or the manufacturer who is supplying all of the product information. The manufacturer him/herself could in other contexts be a requester when requesting MCDs for parts procured. In fact in the figure, that is one of the methods that the Supplier collects information such as shown in the bottom left of the "Supplier tasks" box. The Supplier/Manufacturer should be able to read in easily parts data from IPC 1752 forms, do a BOM merge, account for parts not in BOM (solder, wire, cable etc, if any), add in desktop engineering calculations that are permitted by the industry standards on a layerwise basis, test all other parts layerwise and do a final merge of all of this for any product material declaration.

The following figure shows the potential flow of data associated with requests for, replies to, compilation of, and distribution of material composition information. This information flow can extend from any point in the supply chain to any other. Small manufacturers can request parts information from major manufacturers that they use for making their own products. Similarly, large manufacturers can request this information from small or medium manufacturers for compilation of products comprised of many small assemblies. The point of interest is that using the IPC 1752 form creates a platform that can satisfy the needs for all of these exchanges in a smooth, seamless and speedy manner. The underlying xml schema associated with the IPC 1752 form is enables exchange of information using the open format for data interchange, the xml (Extensible Markup Language) format. The xml format, in addition to being non-proprietary, also enables data to be stored fairly efficiently in a manner that several applications can access it.

It is important to recognize that material information must be calculated on a part-level basis and also at the homogeneous layer level. The latter need is to satisfy the RoHS standards.

Desktop engineering calculations allowed by the standards must be entered as information on a layerwise basis. This is true for test data also. These must be automated to read from text or spreadsheet files to reduce input errors Typically, desktop engineering data and test data are both entered in a speciated form (each substance referenced by its CAS). However, MCDs in the IPC 1752 forms will be listed in categories. The supplier/manufacturer must be able to integrate all of this information as well as BOM information for each of these parts in the computing process. The Supplier/Manufacturer obviously does not do this for every request, but has a library where such information is stored once the MCD is computed the first time. From here the Supplier/Manufacturer merges this with Requester information captured just earlier, and can any time reply with full product information.

The Supplier/Manufacturer can also just directly distribute or respond to requester using a standard distribution form. He/She can also send requester a standard email to discourage spam activities, if situation necessitates this.

The libraries of the Supplier/Manufacturer, in addition to being used to distribute material information, must also account for parts information inequities. Pre-RoHS and post-RoHS parts might in common cases, contain the same part number. Also, the same part supplied by a different supplier might often possess a different MCD. Easy access for such information necessitates associating this with the proper file for the part MCD. All this information can be easily stored in the form of a name for the file that the information is stored in. For example a part of part number xyz, when suffixed a supplier id, which could be a real id, or in the case of pre-RoHS and post RoHS part sharing the same part number, an id that references this, becomes ***xyz-1.xml.***

The suffix 1 could refer to the supplier ID or a reference to distinguish parts having shared part numbers. This enables data to be thus kept natively in xml and accessed only as needed. This enables easy exchange of data with external applications, if need be.

Parts information, which is read from engineering calculations or test data, could also be kept in such form after appropriate aggregation of individual layer information. Obviously, such aggregation includes summation of all substance masses in the category and

also identification of the layer containing the maximum concentration and the value of the maximum concentration for RoHS purposes.

In keeping parts data simply as xml files in an IPC 1752 format can have several other advantages. Typically, each xml file may be of only 20 kilobytes in size. Without the need for any database to store in, xml files for a million parts, comprising approximately less than 25 gigabytes, can be quite easily kept on a single desktop computer, with proper backups and archival as needed. As each xml file is accessed only as needed, there will be minimal slowdown of the program even if data is accessed in typically hierarchical data access applications such as spreadsheets as opposed to using relational databases (and, if any, IT or personnel overhead associated with that). Such an approach maintains the robustness associated with high-end applications, while at the same time it allows for economical implementation of the MCD process and its associated tasks. Management and maintenance of data is also thus easier because the requirements for personnel to maintain data and systems are less stringent, requiring only spreadsheet level expertise. This means that that the only expertise required for personnel to operate such a system would be related to materials, parts and inventories.

Other preferable options in developing MCDs are that the user should be able to view all compositions, maximum concentrations and the associated layer information for the layer containing the maximum concentration prior to creating the IPC 1752 form. This is because the user may want to add additional identifying or explanatory information relating to the layer or the material used. Typical spreadsheet applications could also be color coded to identify non-compliant layers thus enabling the user to reject such parts at an early stage.

Training and personnel related issues also play a part in the MCD process. Turnover of personnel is quite common in the electronic manufacturing sector. So the MCD process should be enabled to allow for easy transition of new personnel, who should be able to adapt to the job easily. This will keep the process of developing and exchanging of MCDs smooth and without kinks that can upset critical factors such as time-to-market.

Adapting to Engineering Change Orders (ECO) will also be easy in such an approach. With MCDs being able to be generated easily, ECO implementation will be made easier. Alternate parts information from different suppliers capable of fulfilling the ECO can be easily evaluated by quickly preparing MCDs and evaluating compliance. This will enable the ECO to be implemented with lesser cost overheads and maximize profits for companies.

Summary

These best management practices for supply chain data using the IPC form 1752 enable a smooth, uniform and consistent exchange of data at any point or layer or link of the supply chain. ◆

Stress Free Modeling

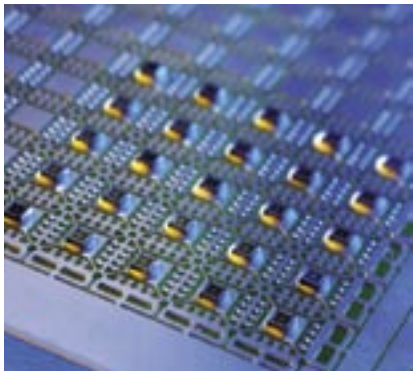
Jack Zhang, Ph.D., Electronics Group
Henkel

It's no coincidence that when the phrase "stress free" is used here, a dual meaning is absolutely intended: a stress free package and a stress free product development experience.

As IC packages become increasingly complex, designing and building a cost-effective, robust product in a shrinking time-to-market window is, arguably, one of the biggest challenges facing packaging specialists today. Everyone is competing for the same piece of the pie, so getting product to market first is essential. But, being the first to introduce a new device isn't enough on its own: the product must be proven reliable, robust and manufactured at the lowest cost possible. In most cases, today's packaging OEMs take on an incredible amount of risk and investment resources when they put something into prototype production.

It is quite common that companies designing and building IC packages today have their own modeling capabilities, whereby they analyze the mechanical properties and related stresses on varying package types. And, while this analysis is absolutely critical, often too much emphasis is placed on the mechanical design and there is not enough understanding of the consequences of materials variations or interactions to get a complete picture of package viability. For example, even the slightest modification to the design and dimensions of a die attach material can alter the stress on a mold compound. It is precisely these types of package design issues that are not discovered during mechanical-only modeling routines and will only be revealed once the device is put into production and significant manufacturing investment has already been made. Consequently, costs rise and the product's market-viability window shrinks.

But, it doesn't have to be that way. By partnering with an expert in materials and mechanical device engineering early in the design phase, several of these issues – and costs – can be avoided. Henkel is one of the only materials suppliers in the market today that can alleviate these unnecessary expenses by delivering proven device modeling and prototyping services. The company's expert technical staff can adapt an IC package design to ensure optimum performance between substrates and packaging and assembly materials. Through innovative modeling and simulation software, along with testing and analysis performed by the industry's leading experts in packaging device materials science, Henkel evaluates synergies and identifies potential problems between specified substrates and various materials. This technology ensures minimal risk with maximum return for guaranteed stress-free packages.



Die Attach on lead frame.

Henkel's work in this area has uncovered some critical package design issues which are significantly impacted by both the choice of materials used and variations in materials properties. While there are countless examples of Henkel's work and subsequent efficiencies realized through the company's modeling and prototyping technology, two recent examples of QFN (Quad Flat No-Lead) package analysis bear mentioning. In the first instance, the package manufacturer wanted to evaluate moving from a lead-frame to a laminate, stacked MCM package. By modeling both package types, device stress variation and warpage was evaluated from a mechanical point of view and from a materials perspective, analyzing die attach and mold compound materials. Through detailed analysis, it was determined that moving from a lead-frame package to a laminated, stacked package should not introduce higher failure rates on the die attach materials because there were little variation in stresses. The laminated packages also showed lower stress on the mold compound and lower package warpage. The manufacturer now has the confidence to move forward with this design change and the assurance that its materials choices are solid.

In the second scenario, Henkel evaluated warpage of three different QFN package sizes: 3mm, 5mm and 10mm. In the 10mm package, the effects of die size and pad size were also evaluated. In a typical array package, warpage is seen in either a "crying face" (ends of the package bowing downward) or a "smiling face" (ends of the package bowing upwards) presentation. What needed to be analyzed, though, is why and how this occurs and the associated materials implications. This detailed modeling analysis revealed that array package warpage is determined by die size, pad size and mold compound properties. Bigger die sizes tends to warp the package in the "crying face" direction, whereas smaller die sizes show a tendency to warp the package in the "smiling face" direction. But, both of these problems can be addressed by altering the mold compound properties. By using a high CTE (coefficient of thermal expansion), high modulus mold compound, the "crying face" warpage can be corrected. Conversely, by incorporating a low CTE, low modulus mold compound, the "smiling face" warpage associated with smaller die sizes can be amended. Again, a solution uncovered by the materials experts at Henkel.

By utilizing Henkel's unique understanding of both mechanical and materials design constraints, packaging specialists are enjoying the benefits of robust IC package design and reduced manufacturing costs. Don't let designing a stress-free device make your job stress-filled. Partnering with Henkel can alleviate anxieties, reduce risk and ensure the design of a stress-free package.

For more information on Henkel's modeling and prototyping capabilities, log onto www.electronics.henkel.com or send an e-mail to electronics@us.henkel.com. ◆

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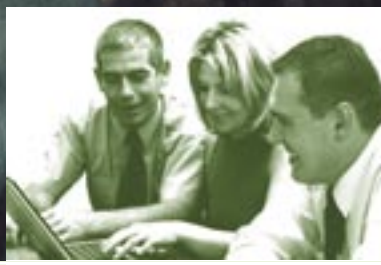

"So much to do, so little time" is a common dilemma for today's manufacturers. But, it need not be this way. Henkel's material sets will save you time for more pressing concerns.

Can you really afford to spend the time necessary to qualify, test and guarantee compatible products? If not, mistakes are inevitable. Fortunately, Henkel's Material Sets solve this dilemma by delivering proven package performance - stress reduction, compatible chemistry and material interface designs. Using the cross-qualified Hysol mold compounds, QMI die attach adhesive and underfills, this complete solution saves you up front design time and reduces overall maintenance time and costs. And you get the support of a world-renowned electronics specialist – Henkel is the Single material solutions provider you've been waiting for.

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Airflow Optimization for Enhanced Cooling

Norman Quesnel
Advanced Thermal Solutions, Inc.

Increased miniaturization means that devices must provide greater functionality in higher density and lower profile spaces. The combination of open channel and large component protrusions, e.g. BGAs, PQFPs, creates varied pressure distributions that contribute to complex airflows. Common airflow characteristics include laminar (parallel), turbulent, pulsatile (pulsating), and unsteady, along with coexisting flow reversals.

Why are airflow characteristics important? All devices in an air-cooled system must be kept within their operating temperature limits, i.e., inside their maximum allowed device junction temperature. Device manufacturers provide these specs for the user to perform thermal analyses, along with such data as power dissipation and package thermal characteristics.

Taking the Air's Temperature and Velocity

The key for determining a system's airflow requirement is to find the temperature and velocity of the approach air for each given device. For rack-based enclosures, critical factors for this analysis range from the physical architecture, to power dissipation, to fan placements. Other elements are venting, spacing from adjacent systems, and environmental issues. The objective is to develop an understanding of the volumetric flow of air within the system and where the hotspots are found.

Airflow occurs only when there is a difference between pressures. Air follows the path of least resistance and will flow from a region of high pressure to one of low pressure – the bigger the difference, the faster the flow. An uneven distribution of airflow passageways can deprive devices from the benefits of convective cooling.

In Figure 1, a water tunnel containing dyed fluid reveals flow reversal when the first component encountered is twice the size of the other parts downstream.

A clear picture of airflow distribution across a PCB can be achieved using experimental and computational techniques. Computational fluid dynamics, CFD, is ideal in the conceptual design phase for avoiding potential airflow (and other) problems.

Figure 1: Water-based visualization of flow in an electronic board with the first component being twice the size of the others down-stream.

Direct Numerical Simulation, DNS, can provide a more accurate picture at all levels of a design if experimental tools are not readily available, e.g., flow sensors or air or water tunnels for flow visualization.

In Figure 2, a direct numerical simulation model shows a board with both straight and disked fin heat sinks. The air travels in an uneven flow pattern and there is premature egress of the flow from the fin field in both types of heat sinks.

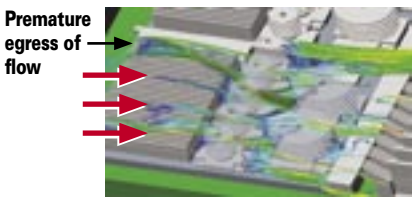

Figure 2: Computational Fluid Dynamics (CFD) simulation of PCB with straight and disked fin heat sinks.

Where these complex and unpredictable flows present problems is when it comes to determining the channel temperature rise or a device's junction temperature. Because most analysis tools fail to accurately predict such complicated flows, it's necessary to take actual airflow measurements. The key is to take enough measurements to be able to pinpoint the problem regions. Some of these spots are not readily detectable, but can be discovered with non- to least-intrusive devices such as thin, low-profile sensors that won't alter the airflow characteristics.

With a good understanding of the airflow profile, individual components should be reviewed for their thermal condition. Problem components can often be addressed by optimizing the fan system or by adding an off-the-shelf heat sink. In severe cases a high performance, custom sink is needed to work with the available airflow, but this will cost less than redesigning board layouts.

Measuring Fluid Velocity

There are many techniques for measuring airflow. Here are some of the methods that are well-suited for use in electronic systems:

- Hot-film and hot-wire anemometry (most common). Measures fluid temperature based on heat transfer. This technique is further described below.
- Pitot tube velocimetry (not accurate for low flows). Uses the Bernoulli equation to relate the pressure difference to the velocity
- Laser Doppler velocimetry (LDV). Requires optical access and seeding of the flow. Measures the speed of micron-sized seeding particles that flow through a pair focused beams.
- Particle image velocimetry (PIV). Requires optical access and seeding of the flow. It is basically LDV in a plane.

NOTE: LDV and PIV, though accurate, require line of sight and do not measure air temperature.

Hot Wire Anemometry (HWA)

Hot wire anemometry (HWA) is by far the most suitable method for electronics cooling applications. By maintaining the wire temperature at a constant level, i.e. between 150-250°C, you can correlate the rate of heat loss to the air velocity passing across the sensor. To accurately measure the air velocity, it is necessary to know the temperature of the air approaching the sensor, where the velocity sensor is located, and the temperature of the sensor itself.

There are two basic sensor types: single and dual. See Figures 3 and 4. Single sensors measure both air temperature and air velocity at the same location. Dual models include a second sensor for measuring the approach air temperature, but at a distance away from the velocity sensor.

While physically less invasive, dual sensors have certain features that may become sources of error. The following are the most common issues.

Figure 3: Single sensor technology.
(Product of Advanced Thermal Solutions, Inc.)

Figure 4: Dual sensor technology.

Fluid Temperature Gradient

Due to the non-isothermal nature of airflow in electronic enclosures, dual sensors used for measuring temperature and air velocity at two different points can cause significant errors, particularly as values increase.

Radiated Heat Transfer

Dual sensors contain both hot (velocity) and cold (temperature) areas. Radiation coupling between the two will cause the temperature sensor to report a Ta value that is substantially larger than the actual. As a result, the measurement system will produce significant errors in air velocity magnitude.

Lack of Calibration at Elevated Temperature

Because HWA is a heat transfer sensor, and is exposed to high temperature air during actual testing, calibration must include the impact of air temperature at different levels. Not having such calibration, there will be measurement errors.

Sensor Size and Its Support Body

Good measurement practices mandate that the best sensor is the one that introduces the least disturbance in the flow field. Large blocks alter the flow dramatically and cause errors in measurement.

Conclusion

A variety of thermal management issues can be solved using multipoint air velocity measurements. Typical uses include evaluating the performance of fans and heat sinks. Another use is to verify CFD software modeling. Multipoint measurements have been used to profile printed circuit boards to determine critical component placement and to monitor quality. The best place to address thermal problems is in the concept stage where they are relatively cheap to fix. Otherwise, the cost for failing the eventual thermal tests will be much higher in terms of price and time. ◆

	SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
JULY 2006	2	3	4 INDEPENDENCE DAY	5	6	7	8
	9	10	11	12	13	14	15
	16	17	18	19	20	21	22
	23	24	25	26	27	28	29
AUGUST 2006	30	31	1	2	3	4	5
	6	7	8	9	10	11	12
	13	14	15	16	17	18	19
	20	21	22	23	24	25	26
	27	28	29	30	31	1	2
SEPTEMBER 2006	3	4 LABOR DAY	5	6	7	8	9
	10	11	12	13	14	15	16
	17	18	19	20	21	22	23
	24	25	26	27	28	29	30

SEMICON WEST 2006
July 10 - 14
Moscone Center, San Francisco, California

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SUNNYVALE MEPTEC LUNCHEON
Ramada Silicon Valley

SOUTHWEST MEPTEC LUNCHEON
Dobson Ranch Inn
Mesa, AZ

MEPTEC MEDICAL ELECTRONICS CONFERENCE
Arizona State University
Tempe, AZ

2006 SMTA INTERNATIONAL / ASSEMBLY TECHNOLOGY EXPO
September 24 - 28
Donald Stephens Convention Center, Rosemont, Illinois

What is this "technology" they speak of? Who is doing it ... and why?

Tom Clifford, Advanced Electronics Packaging Group Leader
Lockheed Martin Space Systems Company

We hear great things about "technology". And what is that, precisely? We quickly realize the buzz continues to be about convenient TV-watching, video-gossip gadgets, cool games with your buddies, how best to sort your digital photos, or neat ways your tennis shoes can track your stride. Your favorite "Technology Reporter" on the radio speaks of tunes and games.

We and our kids like gadgets; but will that matter, a couple short decades from now? We look around the landscape, at the next generation of potential technology-creators, and we see a huge population of youngsters who are superbly capable of using these gadgets, but painfully, the vast majority have no clue how these things really work, deep inside. To be fair, we don't know much about internal combustion stoichiometry, yet we drive cars pretty well. Certainly these youngsters are capable of deciding, in their aggregate market pressure, what minor spin-offs might be fashionable next year, and thus can claim to drive "technology"..... but that thrust has profound limits: gadgets are fun but they don't remove salt from sea-water. Demographics, worldwide, points to declining numbers of youngsters desperate for entertainment, and to an increasing and aging population locked into a finite and fragile resource base (we call it Earth), needing survival and quality-of-life solutions. These solutions will not be streaming-video jewelry, but serious hard technology providing proper food and health.

Examples of serious, useful technologies are evident in every direction ..... not only from the usual "Scientific American" and "MIT Technology Review" sources, but from today's morning paper and popular business magazines. The San Jose Mercury last week ran a piece on the top 1Q 2006 Venture Capital actions. Of the 222 items, ~22% were purely consumer entertainment, ~28% offered business and communications solutions and applications, but ~48% were advanced material, process, and hardware start-ups. Lots of fluff (sorry, not "fluff" but applications sure to be interesting for at least a year or two); but even more solid engineering technology.

The medical products magazines this month ran their usual clips on profoundly important technologies: bio-compatible prostheses; intelligent drug-delivery systems, shape-shifting stent wires, nano-coatings for specific deliveries and property-optimization, implantable wireless sensor systems, etc. That's what this reporter calls real technology.

From "Business 2.0" magazine in June, the hottest 50 stocks, from a review of 2000 "tech" stocks, featured ~44% companies that offered solid technologies, the balance were involved with commercial and consumer applications. That magazine also reported on emerging globally-significant startups: nano-tech fabrics that fight infection, skin-repair enzyme-based topicals to fight skin-cancer and aging effects; biomembranes to carpet/seal the desert soil surface to aid plant growth, reduce moisture loss, and minimize CO2 emissions. Clearly many folks agree that tunes-on-demand is not the metaphor for the technology that the next couple generations really need.

Who will create these real technology solutions ?

Here's one clue. High School and Junior High School Science Fairs offer a clear view into our next-gen skills-and-interest resources. This reporter skimmed some reports on examples of recent science-fair winners: a) analysis of water-quality trends in several Utah rivers, heretofore considered "clean", documenting increases in biological and chemical pollutants and toxins, using methodologies recognized as beyond-EPA accuracy; identifying human-activity sourcing and recommending monitoring and mitigation protocols .... and this from a sophomore, b) novel mathematical proofs, enabling enhanced pattern-recognition and search optimization, with possible applications for global weather modeling, c) studies identifying molecular mechanisms associated with arterial plaque-buildup, with obvious health applications, d) characterization of the brain's processing of simultaneous visual and auditory stimuli, identifying locations and neural pathways, with implications for damage-diagnostics, as well as for training and real-time displays, e) demonstrations and interpretation of chemical reactions involving "inert" gases and noble non-reactive metals, leading to new understanding of molecular and elemental reaction kinetics and mechanics, f) effects of intense UVA and UVB radiation on certain microorganisms, leading to possible diagnostic and therapeutic treatments, g) utilization of selected classes of marine bacteria, to metabolize and bio-degrade crude-oil spills, suggesting soil remediation and eco-recovery solutions, h) review of non-toxic, naturally-occurring micro-organisms, to control human-harmful and agricultural pests, i) identification of pre-cancerous conditions, using "taught" image-pattern-recognition algorithms applied to a growing data-base of X-Ray and MDI imagery, with profound future heathcare diagnostic and treatment implications, j) protocols for destruction of pseudomous aeruginosa, a major contributor to fatal secondary infections of burn, AIDs, and cancer patients. k) review, classification and recommendations for emergency and survival shelters, keyed to third-world resources and cultures, ... and these are junior high and high school youngsters. And this report chronicles only a tiny fraction of bright youngsters at a pivotal point in their lives and potential contributions.

What can we do? We in the microelectronic packaging industry are superbly positioned to understand and to create enabling technologies. We are also parents and global citizens and voters, and also are pretty bright folks. We must encourage educational opportunities for every youngster, our kids and the neighbors kids, of all races and levels of privilege, starting early. That means math and science curricula, well-equipped schools and resources. Special encouragement, internships, and opportunities must be provided for the best and brightest. That means on-shore, local jobs in development and manufacturing which must be high-paid to attract career-pathing towards creating real technologies, not just tunes-and-gossip. We must focus on these domestic jobs to pull the youngsters in the direction of real technology. We must maintain our domestic intellectual edge, or we will surely lose out to global competition in the next decade or two. Further, we must act wisely, in our personal consumptions and in our influence on global events, to ensure a continuing domestic technology base. That "technology" must not be equated to fashion accessories that peep and flicker and distract, but the less familiar but far more important technology which offers soil remediation, or infection-free healing, or CO2 emission-control, or efficient solar-energy-cells.

We have the obligation to direct trends in technology appropriately. We know there are high-school and college kids available to develop and deploy it. ◆

Magazines and Carriers for Process Handling Solutions


Film Frames


Film Frame Magazines


Film Frame Shippers


Grip Rings


Grip Ring Magazines

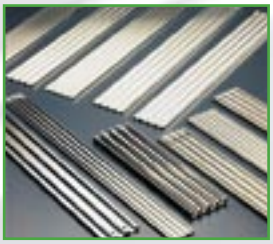

Grip Ring Shippers

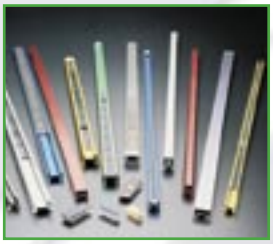

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.

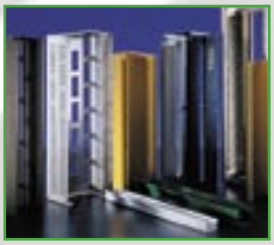

Process Carriers (Boats)


Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines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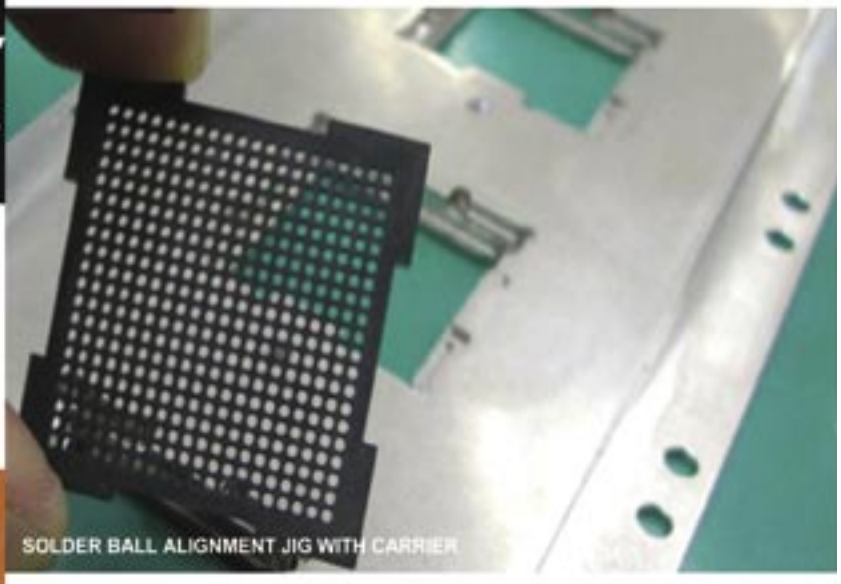
SOLDER BALL ALIGNMENT JIG WITH CARRIER


BOARD LEVEL EMI SHIELDS

Small Enough To Know You
Big Enough To Serve You Worldwide

BEZEL

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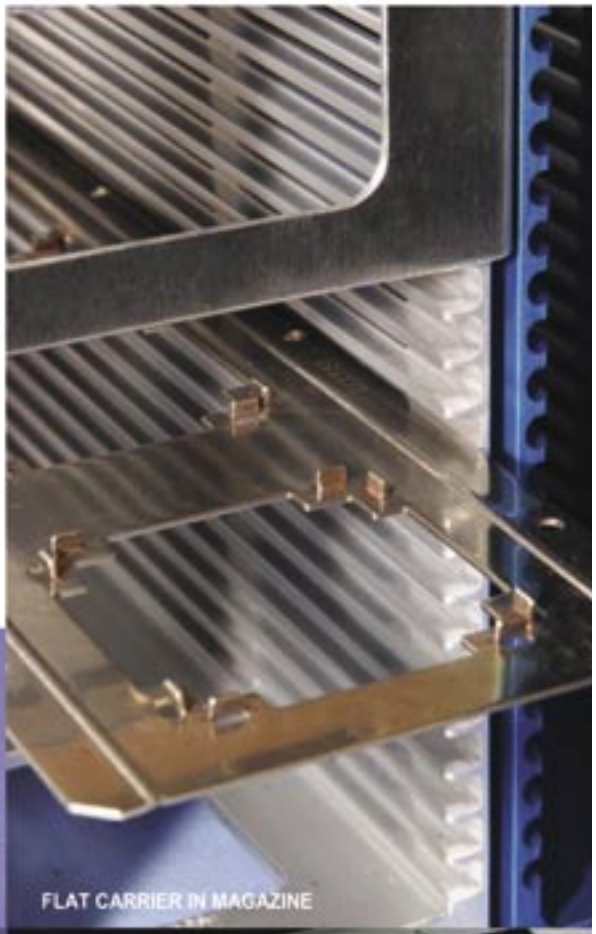
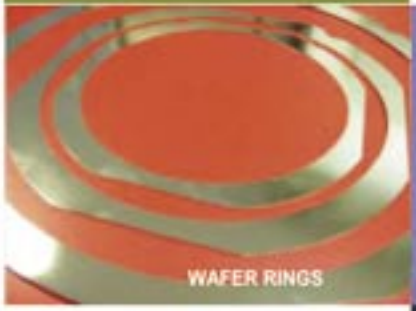
TIJUANA, MEXICO
SHANGHAI, CHINA


FLAT CARRIER IN MAGAZINE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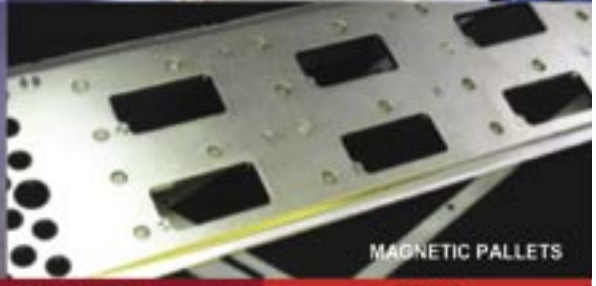
MAGNETIC PALLETS

UNITED STATES | MEXICO | SINGAPORE | CHINA