MEPTEC report
Volume 10, Number 3
QUARTER THREE 2006
A Publication of The MicroElectronics Packaging & Test Engineering Council

IC Packaging & Test Roadmaps:

Device Trends Impact on Package & Test Technology and Supply Chain

One Day Technical Symposium Coming to San Jose November 16th ... page 5

INDUSTRY NEWS

STATS ChipPAC has announced it has established a dedicated Turnkey Solutions Management team as part of a comprehensive program to streamline supply chain logistics for wafer bump, wafer sort, package assembly, and final test customers. *page 14*

Balazs Analytical Services announces quantitative techniques that provide parts per quadrillion (ppq) trace analysis. Analysis at ppq levels, where 1 ppq is equivalent to 1 in a million billions, becomes critical as technology nodes decrease to 90nm and below. *page 15*

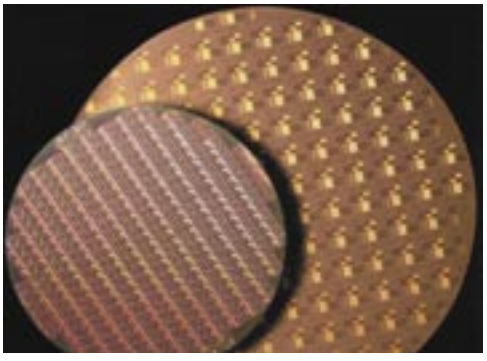
Palomar Technologies has received the Semiconductor International magazine Editors' Choice Best Product Award for its Model 3500-II Automatic Component Placement Cell. *page 16*

UMC has reported the progress of its 65nm production ramp up. The leading-edge process is seeing strong demand and interest from a variety of customers whose products span a wide range of semiconductor applications. *page 16*

CMC Interconnect Technologies continues to expand their capabilities for Ceramic Substrate, Module and Package Rework. *page 17*

RTI's Technology Venture Forum 2006 comes to the San Francisco Airport Marriott in Burlingame, CA October 31 - November 2. *page 25*

MEMBER COMPANY PROFILE



Surfect was founded in December 2000 for the purpose of developing automated electroplating tools for wafer-scale deposition, processes to apply metal deposits at the wafer level, and high performance interconnect technologies designed to address the challenges facing the electronics component fabrication and semiconductor assembly industry.

Surfect Technologies, Inc. product development team of industry veterans and technical experts work closely with customer leaders and industry research groups to understand internal and industry development roadmaps and create the necessary processes. The team, located in Albuquerque, New Mexico, is focused on technology required for initial tool and process entry as well as technology developments that will ensure that the Surfect products will also meet emerging requirements. This process requires a tight interaction with both customers and key universities. *page 20*

Semiconductor equipment bookings increase 73% over July 2005 level. *page 18*

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Council Update

Welcome to our Q3 issue, and to the official end of summer. As always, **MEPTEC** kicked off its luncheon presentation series in September after a two month summer hiatus. **Gartner-Dataquest** has presented on the state-of-the-industry at these kick-off luncheons for many years, and this year is no different. On September 13 in Sunnyvale and September 14 in Phoenix, Gartner-Dataquest's **Jim Walker** (and MEPTEC Advisory Board member) spoke on *"Semiconductor Manufacturing Services: Increased Value in Outsourcing?"*. If you're interested in getting a copy of this presentation please contact the MEPTEC office.

Mary Olsson of **Gartner-Dataquest** is also an active MEPTEC Board member. She wrote our Industry Analyst piece for this issue on *"The Evolving Landscape: The Influence on Future Designs"*. Mary postulates that "the next generations of 32nm/22nm process technology and 450mm fabs are inevitable, but they will come at the expense of an industry wide effort." See page 8 for this interesting analysis. We appreciate Gartner-Dataquest's continued support over the years.

This issue is being distributed at our *"Medical Electronics: Integrating Technologies – Merging the Microelectronic, Bioscience and Medical Industries"* symposium. Our first symposium outside Silicon Valley's borders, this event is being held in association with **Arizona State University** and **Macro-Technology Works at ASU**. ASU hosted the event at the historic Old Main building on the Tempe campus, and a reception was held the evening before for speakers, sponsors and other participants at the **Biodesign Institute**, also on the Tempe campus. We'd like to thank ASU for their great support in putting this event together. We hope to be back in 2007 with *"The 2nd Annual Medical Electronics"* symposium.

If you're a regular reader of the *MEPTEC Report* you know that we've been covering Universities and research institutions for about five years. One of our first profiles was **Arizona State University**. With the growth of ASU in the last few years, and with our recent collaboration with them on our Medical Electronics event, we decided to take a look at them again. There have been many changes there; for example in 2003 the engineering school received a $50 million endowment and was named the Ira A. Fulton School of Engineering in honor of its benefactor. See their story on page 11.

The theme of "Integrating Technologies" is carried even further with our editorial this issue called *"Integrating Technology with the MEPTEC Mythology"*. Written by long-time Advisory Board member **Nick Leonardi**, VP of Sales & Marketing at **CMC Interconnect Technologies**, Nick points out that to put on an event such as this there are important similarities in the integration and cooperation

Issue Highlights

of industries in technology to the way that technologists get together in a manner of open sharing and cooperation. If you missed the event, our Q4 issue will contain a follow-up of the symposium, and a CD of the presentations will be available – just contact MEPTEC for information on ordering.

Our next one-day technical event will be held on November 16, 2006 at the Hyatt San Jose hotel in San Jose, California. The event is entitled *"IC Packaging and Test Roadmaps: Device Trends Impact on Package & Test Technology and Supply Chain"*. This event is the third in a series of "roadmap" related events that we offer at our annual symposium in Q4. See page 5 for information on attending, exhibiting or sponsoring.

As usual, in each issue we also offer a follow-up look on a past symposium. In May we held our *4th Annual MEMS Packaging symposium*. This event was a departure from our usual one-day format in that we expanded to two-days. A couple of new programs were added to this annual event in 2006 to support the second day. One was presentations by university graduate students and professors in a special "University Workshop". The other was a special **MEMS Standards meeting** cooperatively developed by **MEPTEC** and **SEMI**. **Julia Goldstein**, Contributing Editor of **Advanced Packaging** magazine and MEPTEC Advisory Board member, summarizes the two days on pages 6 and 7. Plans for the *5th Annual MEMS Packaging* event are underway; we'll keep you posted on that.

Our feature article this issue is from long-time Corporate MEPTEC member **STATSChipPAC**. Called *"Test Cost Reduction"*, this article explores the opportunity of reducing test cost through hardware optimization and software advancements, and is authored by **Goh Swee Heng** and **Toh Ser Chye**. See page 24 for this informative piece.

The subject of our other feature article is a look at a topic that is on many semiconductor companies's radar screen these days: The European RoHS (Restriction on Hazardous Substances) directive which will ban the use of specific materials in electronics products. New MEPTEC member company **Air Liquide - Balazs Analytical Services**, **Hugh Gotts** and **Fuhe Li** discuss an alternative screening method for the detection of RoHS substances. See page 26 for this timely and informative piece.

MEPTEC is fortunate to have many different types of companies as our members. Our Member Company Profile this issue is **Surfect Technologies, Inc.** located in Albuquerque, New Mexico. Founded in late 2000, Surfect's mission is to bring cost-effective electroplating tools and reliable multi-layer processes to semiconductor back-end assembly. Surfect has supported MEPTEC over the last few years at various events as presenters and exhibitors, and we appreciate their support. See their story on page 20.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

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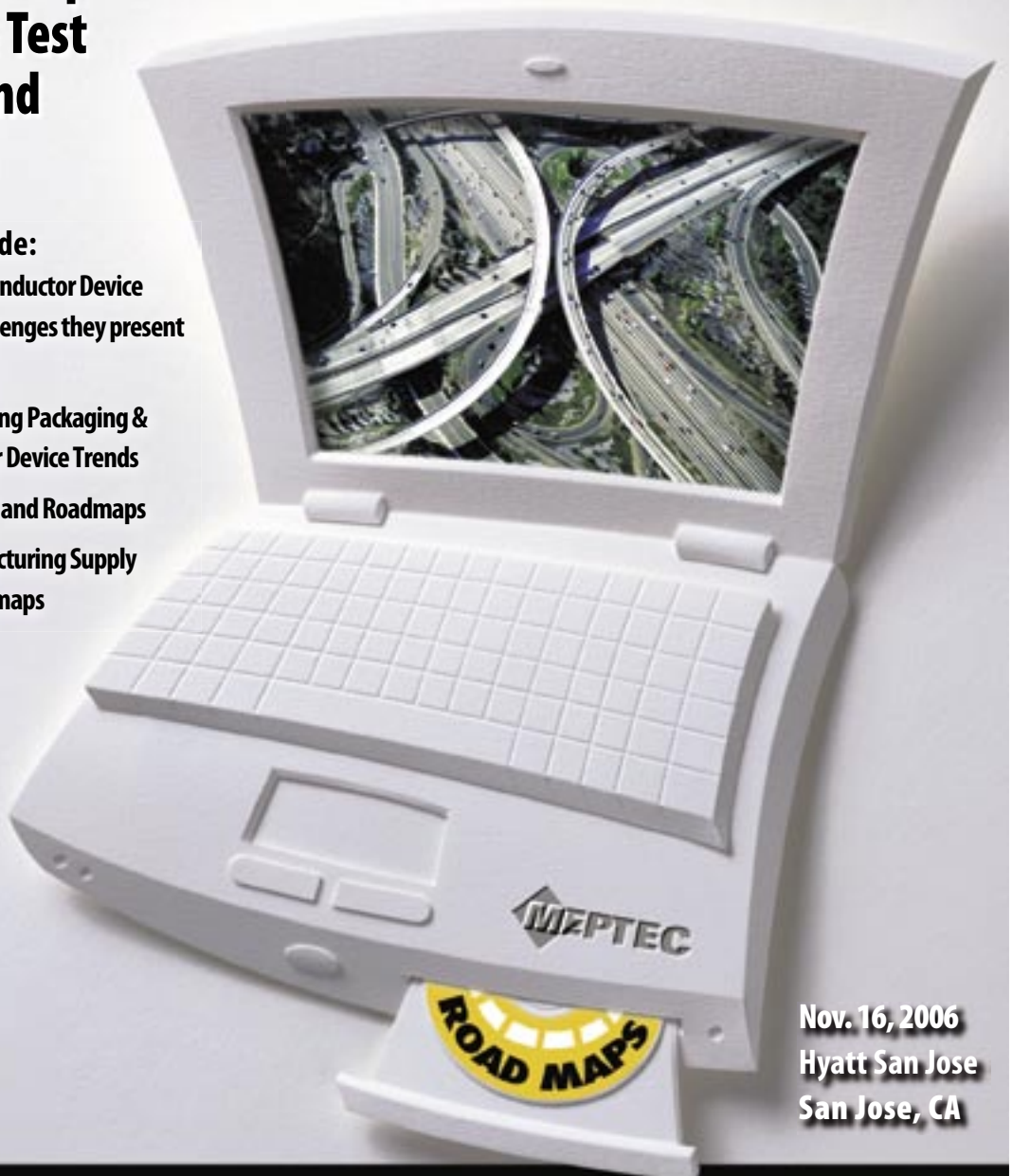

Sessions will include:

- Overview of Key Semiconductor Device Segments and the Challenges they present to Packaging & Test
- Converging and Diverging Packaging & Assembly Roadmaps for Device Trends
- Test Challenges, Trends and Roadmaps
- Semiconductor Manufacturing Supply Chain Trends and Roadmaps

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MEMS Packaging Trends:
From Production to Market

Julia Goldstein
Advanced Packaging Magazine

Bance Hom and her team of session chairs (Janusz Bryzek, Sean Cahill, John Heck and Joseph Mallon) brought in experts from industry and academia for MEPTEC's 4th Annual MEMS Packaging symposium, expanded to two days to include a market overview, packaging trends, new technology and applications, as well as the latest academic research and a standards workshop with SEMI (see separate article). Bryzek, CEO of LV Sensors, listed in-vitro diagnostics, gyroscopes, chemical sensors, optical switches and RF devices as the fastest growing MEMS applications. Portable spectrometers that could analyze various solids, liquids and gases for applications covering environmental, security, industrial, medical and consumer markets are a potentially huge market. According to Bryzek, a one-dollar spectrometer on a chip could be feasible if the volumes were high enough.

Mathieu Potin of Yole Developpment presented an analysis of the MEMS market, listing growth drivers as increased performance and integration, as well as anticipated decrease in prices as volume manufacturing becomes more prevalent. Potin explained two major trends: migration from MEMS devices to MEMS-based modules, including integration of MEMS and ICs; and increased penetration of MEMS into the consumer market. New companies like MemsIC, Invensense and Kionix are leading the way into cell phone, MP3 and optical projection applications, partially because differing cost structure and design requirements make it difficult for established MEMS companies to move from the automotive to the consumer markets. Automotive and aerospace markets are likely to continue to demand custom packaging, while standardization efforts will be focused on the consumer market, where there is more incentive to "break the MEMS law" of "one product, one process."

There is definitely interest in leveraging IC packaging for MEMS devices. As Elizabeth Logan of LV Sensors pointed out, technologies such as chip scale and wafer level packaging are well-suited to MEMS – MEMS devices sealed between two wafers need only a layer of interconnect to be ready to mount to a PCB. The most popular package types for MEMS include cavity packages, molded plastic packages and chip on board or chip on flex. SiP is also a huge opportunity for incorporating MEMS devices.

Paven Gupta of SiTime gave an example where a MEMS resonator, a freestanding silicon structure within a CMOS wafer, is included within a standard QFN package. While a silicon resonator does not naturally exhibit frequency stability, as does a quartz resonator, results show sufficient stability over a wide range of temperatures, demonstrating that package stress has not negatively impacted performance.

To address the problem of package stress transferring to a sensor, researchers at Arizona State University decided it was easier to redesign the sensor than the package. Professor Gary O'Brien described a lateral accelerometer design that includes a solid outer frame, folded beam springs and overtravel stops in x, y and z directions, as well as an angular accelerometer with similar features. These designs are less susceptible to package stress than standard z-axis or x-axis accelerometers.

In some cases, new package materials are being developed for MEMS devices. One example, presented by Mike Zimmerman of Quantum Leap Packaging, is an air cavity package made from a new liquid crystal polymer material. The material can withstand high temperature assembly, is moisture-resistant (hermeticity is similar to that of ceramic packages), and CTE and dielectric constant can be tailored to the application.

For MEMS gyroscopes, which require vacuum to function properly, vacuum sealing at the wafer level provides flexibility in the final packaging since the die is already protected from the environment. As Ken Yang of Honeywell explained, the silicon wafer is bonded to a Pyrex wafer that has cavities etched in it and includes a deposited getter material to maintain low vacuum pressure over the lifetime of the device. The sealed device can then be used in a variety of standard plastic or ceramic packages.

Professor Junseok Chae of Arizona State University discussed the use of vertical rather than lateral feedthroughs in a thinned glass substrate as part of a vacuum-sealed package to save die real estate and reduce leakage. The package also contains a micro-Pirani gauge that can monitor vacuum pressure, temperature or other parameters within the vacuum-sealed cavity.

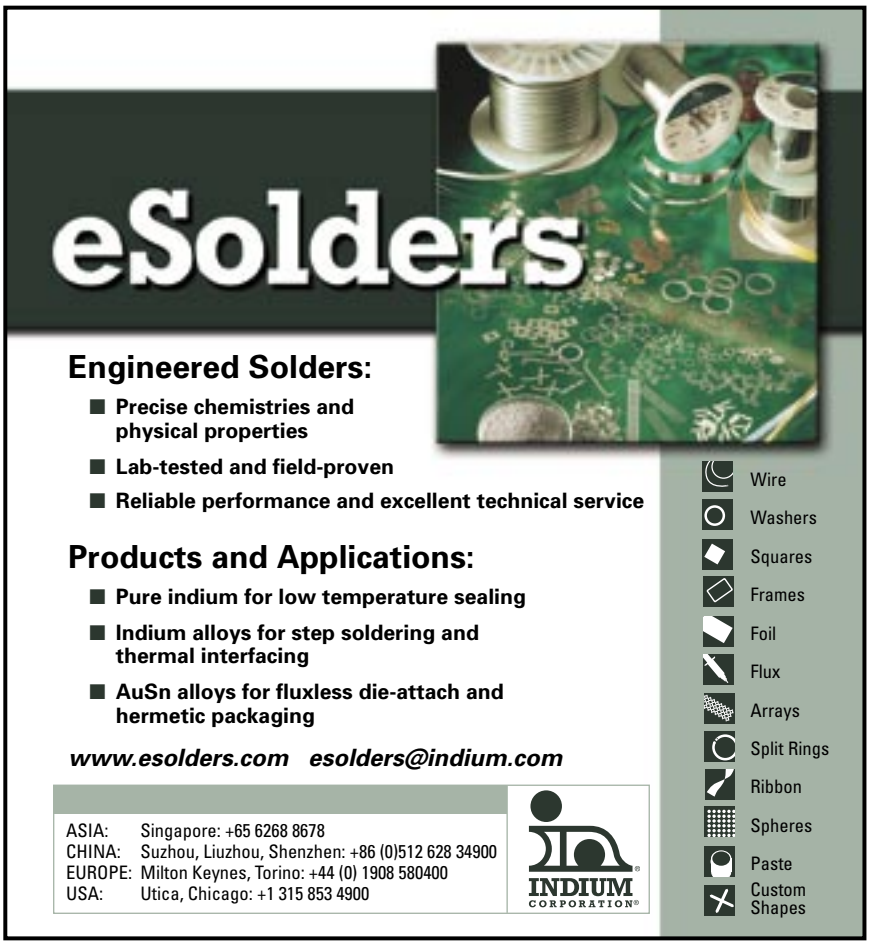
SEMI Holds Meeting on MEMS Packaging Standards

If you're like most of the people who responded to SEMI's April survey on MEMS packaging standards, you're not aware that SEMI has published three MEMS-related standards. Existing standards cover the areas of microscale fluidic systems, termi-

nology and wafer bonding. SEMI's MEMS technical committee has identified MEMS packaging as a task force area, and standardization efforts are just beginning. Survey respondents listed cost, reliability, hermeticity and standardization as the top current challenges in MEMS packaging. They rated hermeticity, reliability, external connections and package dimensions and material specifications as the areas most in need of standardization.

A group of over a dozen attendees of MEPTEC's May 17-18 MEMS packaging symposium in San Jose met with SEMI staff at the end of the symposium to discuss hermeticity standards. Issues include how to define a hermetic seal – it may be necessary to specify fully hermetic and pseudo-hermetic packages – and specifying test methodology and structures, starting with existing standards and adopting them to MEMS packages. Measuring hermeticity is difficult for very small package volumes, and existing standards are limited to packages over a certain size. Another issue is defining when hermeticity is necessary for a device to function (for example, the Q factor of gyroscopes is affected by vacuum pressure) and when a product can still function but hermeticity is specified to enhance assumed reliability. Two categories of hermetic sealing need to be addressed separately: hermetic sealing of devices, for example by wafer bonding, and hermetic packages where the MEMS device is exposed to the environment within the package. The group emphasized the importance of not over-specifying test standards, listing desired results rather than restricting test methods because it may be impossible to get industry-wide agreements on test methods.

The plan for development of hermeticity standards within the MEMS packaging working group is for the group to first develop hermeticity definitions, categorization and scope of the standards. The next step will be to review existing hermeticity-related standards and survey the MEMS industry. The working group was scheduled to have a teleconference in June and meet during SEMICON West (July 10-14 in San Francisco). Anyone interested in learning more or being part of this standardization effort is encouraged to contact group leader Ron Foster (foster@arisetek.com, 479-571-2592) or SEMI's Susan Turner (sturner@semi.org,408-943-7019). ◆



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During the second quarter of 2006, semiconductor IDMs and foundry suppliers reported that capacity utilization remained in the mid-80 percent range. Foundry suppliers were adding 90-nanometer device capacity to keep pace with increased demand. The first 65-nanometer processes were also being announced; but suppliers indicated that 65-nanometer would not be a significant factor in the foundry capacity picture during 2006.

By the third quarter of 2006, a moderate increase in demand spurred capacity additions that are expected to drive capacity utilization to around 90 percent by the end of the year. We expect this trend to continue into 2007, as foundry capacity utilization drives into the 90 percent range following a slight seasonal dip in the first quarter of 2007.

During the third quarter, chip, system and board designers attending the 2006 DAC (Design Automation Conference) Conference in San Francisco, and representing the EDA (Electronic Design Automation) world, were already discussing the current challenges of 65nm/45nm designs, Design For Manufacturing (DFM) strategies for 2007 through 2009, and scaling issues for 32nm/22nm processes for 2010. In reality, the EDA vendors are leading the semiconductor chip industry in technology process design and development by 2 to 4 years. As noted in Figure 1, the semiconductor landscape is just now ramping up production of 90nm. This will be the dominant process node for the next few years, after which time the 65nm production will begin to ramp up in volume.

From a leading edge supplier perspective, Broadcom won't have any 65nm process node in mass production until 2007. Qualcomm has a 65nm cell phone chip sampling at the end of this year, and Nvidia is just coming out with an 80nm solution for production in year end 2006. In a recent survey, Gartner Dataquest discovered that only 3 percent of ASIC designs will be at 65nm process technology this year.

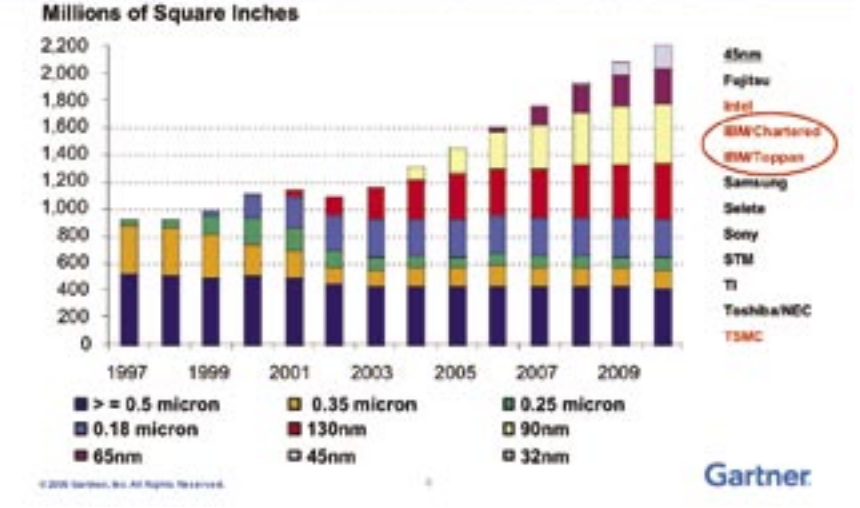
During interviews with both startup and established EDA companies at the DAC show, many stressed that they were already working with Intel and NVIDIA on future 45nm process node designs. But these designs would not be introduced until late 2007. Leading chip vendors listed in Figure 1, are taking different paths to transistor formation using new materials at 45nm process nodes, but their bread and butter products are only shipping out at 130nm and 90nm. Even TSMC is only getting 17% of its revenue from production of 90nm devices. Companies like IBM have found that design tools that worked for 45nm designs will not work for 32nm and thus they have employed a less flexible, but more efficient design path using their Restricted Design Rules (RDR) set of rules for next generation deep submicron development.

Design versus Production in 2006

If you're a silicon supplier today, you saw 300mm wafers that were originally forecasted to enter the market in 1998, actually not ramp up until 2005 as shown in Figure 2. Even now, Intel is pushing the industry to build 450mm fabs; but the earliest expectations for 450mm silicon is 2014. By that time we expect that fewer than 25 manufacturers will be building new fabs, because the new fab cost estimates have already reached $3.8 to $5 billion dollars per fab. In addition, the lack of tools for design, as well as scaling challenges and unreliable silicon issues for 32nm/22nm chips, are possible barriers of entry for design and fabless startups and foundry suppliers.

If you were an OEM developing hardware during the last 20 years, your revenue growth would have been driven by compute and consumer applications,

Figure 1
Capacity By Feature Size



while DRAM and MPU chip technology drove supplier revenues (see Figure 2). With the entrance of the fabless and foundry business in 1995, wireless/wired communications systems, SOC designs and submicron manufacturing, the number of design houses quadrupled, and product life cycles dropped from 3 to 5 years, down to 18 months.

While a few companies have talked about 45nm reaching production in 2007, notable capacity is not expected to ramp until 2009. Of the leading IDMs and fabless companies, as shown in Figure 3, actual production by process node activities centers on the 90nm range in 2006. While there is a lot of hoopla about announcements and introduction of bleeding edge technology, the majority of product shipped in 2006 remains at 90nm and above. Although chip vendors love to talk about their latest product advancements, their bills are being paid by parts designed 7 to 10 years ago, that hit production 5 years ago. Although vendors of DRAMs, Flash, and advanced MPUs do drive silicon, chip and system technology, it should be noted that 1/3rd of the industry's silicon is for device production at or above 150mm.

We definitely believe that the next major design challenges at 32nm/22nm process node technology will be a high impact technology for designers, tool suppliers and manufacturers. After discussions with companies like IBM, AMD, Intel, SRC, University of Michigan, Mentor Graphics and Synopsis, the new silicon materials, EDA tools, and design changes made at 90nm, 65nm and 45nm will work for device production through the 2012 time frame. However, the transition to increased complexity at 32nm/22nm processes will come at significant costs and investments, and many companies and universities have already started building their R&D strategy. The current estimates to develop manufacturing technology for today's leading edge device production are $500M/year. In addition, increased integration of SOC design and manufacturing, coupled with more advanced package and test is increasing costs and also challenging the traditional boundaries between design and manufacturing.

At this time, evaluations by IBM of their RDR set of rules, and the SRC/University of Michigan efforts on "Self Healing Chips", indicate that if successful, these developments could provide alternative methods that will once again extend Moore's Law. If successful, their alternative design technology could also disrupt the EDA industry's current focus on DFM tools and strategies.

As companies and universities finds ways around the challenging issues of 45nm and 32 nm processing, designers could also benefit from access to less expensive layout tools, and possibly decrease their investment in analysis tools.

Development of 45nm and 32nm process nodes will be a high impact process for the EDA and chip vendors. There will be new opportunities for EDA designers, as ESL will still be needed. However, the number of IDMs will decline, or transition to fabless vendors, as not all will be able to support high cost of R&D for new materials, new tools and new process equipment. We expect to see more consolidation of large fabless and foundry companies, as they will have to share the higher cost of production with equipment manufacturers or drop from the market. The smaller design and fabless companies will have to build stronger IP relationships, and partner to share increased costs of design and software tools. The next generations of 32nm/22nm process

Figure 2
The Industry Today

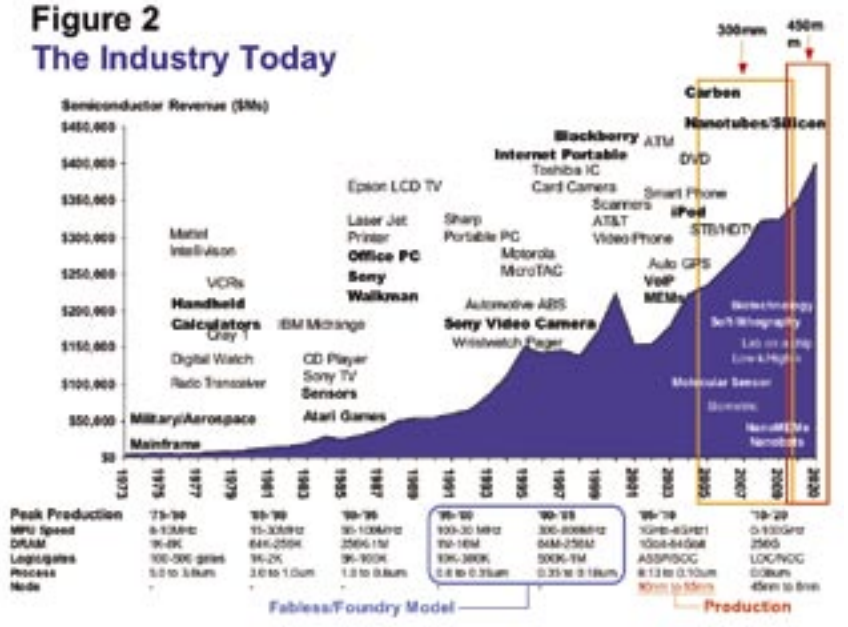


Figure 3
Future Design Directions for IDMs/Fabless

Estimated Percent of Production by Process Node by Year End 2006

Top 10 IDMs	≥ 130nm	90nm	65nm	45NM	32NM	Total
Intel	34	66	10	0 2007	0 2009	100
Samsung	15	75	10	0	0	100
Texas Instruments	40	55	5	0	0	100
Toshiba	25	70	5	0	0	100
STMicroelectronics	40	55	5	0	0	100
Renesas	40	55	5	0	0	100
Infineon	40	55	5	0	0	100
Philips	45	50	5	0	0	100
Hynix	5	95	0	0	0	100
NEC	30	65	5	0	0	100
Top 10 Fabless	**≥ 130nm**	**90nm**	**65nm**	**45NM**	**32NM**	**Total**
Qualcomm	35	60	5	0	0	100
Broadcom	55	45	0	0	0	100
NVIDIA	40	55	5	0	0	100
Marvell	55	45	0	0	0	100
ATI Technology	45	55	0	0	0	100
Xilinx	30	60	10	0	0	100
Mediatek	50	48	2	0	0	100
Altera	35	55	10	0	0	100
Conexant	35	60	5	0	0	100
Novatek	48	50	2	0	0	100

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ASU is a university of many places. In addition to the historic Tempe campus, a college town in the midst of a dynamic metropolitan region, the university comprises three newer campuses: ASU West campus in northwest Phoenix, ASU Polytechnic campus in Mesa, and the most recently launched ASU Downtown Phoenix campus. This newest addition, which eventually will serve as many as 15,000 students, will help provide an active 24/7 downtown environment as part of a larger plan to redevelop and revitalize the city's urban core.

ASU's Tempe campus has the nation's largest enrollment on a single campus – 51,612 students – and is home to the Ira A. Fulton School of Engineering.

In 2003, the engineering school received an endowment of $50 million and was named the Ira A. Fulton School of Engineering in honor of its benefactor. The gift and Mr. Fulton's ongoing involvement continue to reflect confidence in the school's accomplishments and its ability to become one of the finest engineering schools in the nation.

The U.S. News and World Report's 2007 editions of "America's Best Colleges" and "America's Best Graduate Schools" rank the Fulton School among the top 50 engineering programs in the nation, with five graduate specialties ranking in the top 30. Approximately 7,000 undergraduate and graduate students and 200-plus faculty members make up the Fulton School's emerging, vibrant learning community. Flexible interdisciplinary curriculum, engaged professors and innovative research programs produce creative students who can work in multiple fields, effectively contribute to society and compete in the global economy.

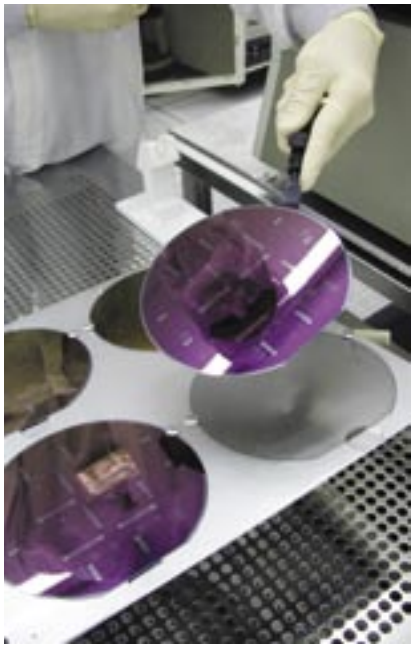
MacroTechnology Works was launched with a $100 million investment in a state-of-the-art display research and fabrication facility.

The Fulton School offers undergraduate, master and Ph.D. degrees in engineering fields such as aerospace, civil and environmental, chemical, electrical, industrial and mechanical engineering, as well as bioengineering and construction management. Newly formed units and collaborative efforts – Arts, Media and Engineering, School of Computing and Informatics, School of Materials, and School of Earth and Space Exploration – offer academic opportunities in areas such as computer engineering, computer science, biomedical informatics, materials science, and Earth and planetary studies.

Continuing education plays a large role in the Fulton School's program portfolio. The Center for Professional Development has been delivering distance education for more than 20 years. In 2000 the center expanded to offer online courses, and by 2003 complete online graduate engineering programs were available. Now more than 2,500 professionals take advantage of 150 engineering courses offered annually in 13 programs. In addition, customized programs are developed for corporations such as Intel, Motorola and Target.

ASU is "academically, a rising star in the world of research," says Princeton Review's 2006 edition of "The Best 361 Colleges." With more than 20 centers plus academic unit-driven research, the Fulton School is playing a critical role in the applied research mission of the university. The school of engineering focuses on several central research themes that reflect its core competencies, support collaborative research, and encourage continued engagement among the faculty and students outside the classroom. Signature themes include wireless communications, nanotechnology, sustainability, human health, and computing and informatics.

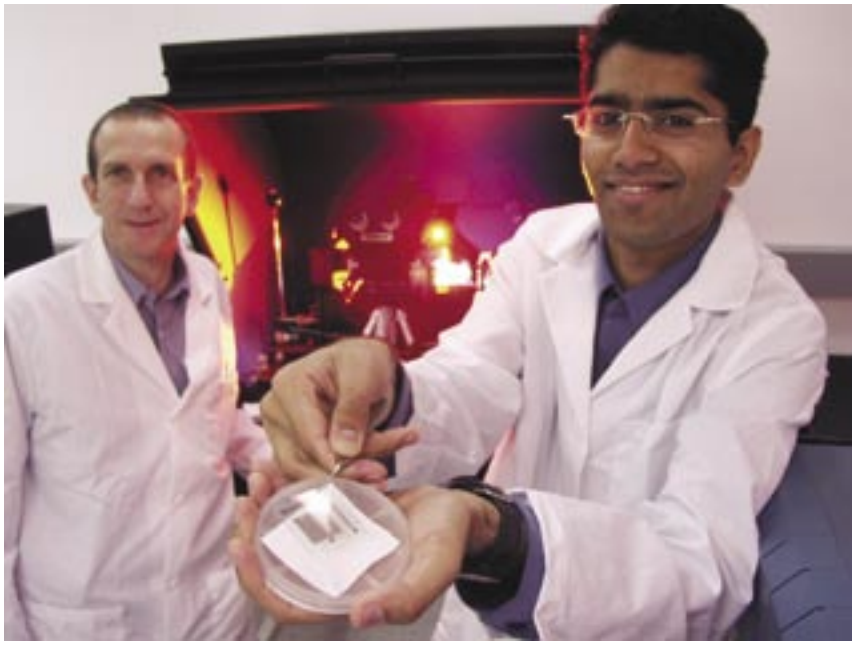
The university's research mission to develop new technology platforms and products useful to society drove the recent



Six-inch wafers with thin film transistor (TFT) arrays fabricated on FDC's 6-inch Pilot Line.

creation of MacroTechnology Works (MTW) at ASU. This enterprise brings consumer input, market trends and the rigor of business process into the academic laboratory to define research activities and validate results.

MTW was launched with a $100 million investment in a state-of-the-art display research and fabrication facility. The Flexible Display Center (FDC) combines the resources, talents and technologies of the federal government, university and industry partners to provide an unparalleled core capability and innovation potential in flexible display technology creation. The Fulton School is a primary FDC collaborator as chemical, electrical and materials engineering faculty researchers comprise the key leadership of the center. The FDC is currently developing low-power, rugged, light-weight military devices with 16 industrial partners for the U.S. Army.



FDC engineers Ed Bawolek and Sameer Venugopal conduct transistor performance measurements on flexible arrays used to drive displays.

MTW employs scientists and experts with significant industry experience and background in project management, quality systems and product commercialization to educate ASU faculty, researchers and students on customer needs definition and new product design and development. These practitioners also keep industry informed about ASU's technology developments and research direction to stimulate partnerships and collaborative research initiatives.

The MTW and FDC are productive, innovative examples of the continuing evolution and success of ASU and the Fulton School of Engineering – enhancing the university's entrepreneurial prowess through market-driven research and product success. ◆

For more information visit ASU on the web: ASU's Ira A. School of Engineering at fulton.asu.edu; MacroTechnology Works at mtw.asu.edu; Flexible Display Center at fdc.asu.edu.

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Advanced Applied Adhesives Announces its Board Of Directors

SAN DIEGO, CA – Advanced Applied Adhesives (AAA) has announced its newly appointed Board of Directors, whose five members consist of high-level executives from the electronics industry.

The Board of Directors are: Ron Benham, former President of Dexter Corporation's Electronic Materials division, has over 40 years of experience in electronic materials. Benham worked for Dexter/Hysol his entire career in Marketing and Executive Management throughout locations in the US, Japan, and Germany.

John Boruch, former President of Amkor Technology, has 40 years experience in the electronics industry. Boruch retired after 22 years with Amkor, which he joined as Corporate Vice President of Worldwide Sales in 1984.

William Dawson, former President of AVX Materials Division, has 25 years experience in electronic materials. Dawson's previous executive roles include Vice President and General Manager of AVX's hi-reliability capacitor facility, President of AVX's European manufacturing facility, and Vice President of Worldwide Sales and Marketing.

Frank Husson, President and CEO of AAA, has over 30 years experience in the international electronic materials industry. Husson was the Founder of and held Executive Management positions at AVX Materials Division and Quantum Materials, Inc.

John Thompson is the Senior Vice President of Corporate Development for Invitrogen Corporation. Of the 11 years experience in Corporate Development, Thompson has served 9 years in the electronic materials industry.

Advanced Applied Adhesives was founded in 2002 by Frank Husson to manufacture and market die attach adhesives and specialty materials for the microelectronics industry. The company occupies a 32,000 square foot facility in San Diego that had previously been Honeywell Incorporated's Advanced Polymer Operation. The building has Class 1,000-10,000 clean rooms and production areas and extensive production and analytical equipment for volume manufacturing of precious metal powders, proprietary polymers and specialty adhesives.

Editors' Choice Best Product Award Presented to K&S for Semiconductor Manufacturing Excellence

WILLOW GROVE, PA – In developing a product that is truly making a difference in semiconductor manufacturing, Kulicke & Soffa Industries received the prestigious Editors' Choice Best Product Award, presented annually by Semiconductor International magazine, for its Maxum Ultra Wire Bonder.

Engineered for higher productivity, the Maxum Ultra is capable of processing today's most complex packaging applications including stacked die, multi-tier packages, low-k dielectric materials and ultra-fine pitch and long/low shapes. Incorporating numerous technology advancements, this high-performance wire bonder processes devices 10% faster than its predecessor – the industry-leading Maxumplus – as well as market competition. Engineered for customers who want greater throughput and finer pitch down to 35 microns, the wire bonder offers bond placement accuracy of + 2.5 μm accuracy at 3 sigma. Wire cycle time is 60 msec for a standard loop, based on 2.5 mm wire length, 0.25 mm loop height and 10 msec first and second bond times.

For more information on the Maxum Ultra Wire Bonder, visit www.kns.com.

STATS ChipPAC Streamlines Supply Chain Logistics

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. has announced it has established a dedicated Turnkey Solutions Management team as part of a comprehensive program to streamline supply chain logistics for wafer bump, wafer sort, package assembly, and final test customers.

As semiconductor companies utilize more complex and collaborative supply chain models to meet ever increasing market pressure for fast time to market at the lowest possible cost, the entire outsourced assembly and test supply chain management process from material procurement to final order fulfillment becomes more complicated and multifaceted. The number of suppliers involved in the supply chain has increased and they are often in multiple geographies. The management of materials and information throughout the supply chain must evolve to provide fast and efficient feedback to stakeholders up and down the supply chain and facilitate rapid response to changes in the demand profile.

Over the last several years, STATS ChipPAC has built its packaging and test portfolio around fully integrated turnkey solutions which encompass wafer sort, wafer bump, assembly, test, and drop shipment. STATS ChipPAC is expanding the standard supply chain management services it provides customers with a specialized team dedicated to Turnkey Solutions Management. This team serves as a resource to customers in working through complex supply chain issues from material management to final shipment of product. They will assist customers in working through transportation and logistics issues so customers can efficiently have a single product manufactured in multiple geographies while meeting cost targets and aggressive cycle times.

With a centralized capacity planning and logistics management process, the Turnkey Solutions Management team examines customer requirements on a global level and determines the optimum factory and geography for products to be built based on the technology requirements, current and future capacity demands, and optimized time to market goals. The Turnkey Solutions Management team works to ensure that the appropriate supply chain is in place and optimized for the specific countries in which the customer's products are to be manufactured.

With advanced process technology capabilities and a global manufacturing presence spanning Singapore, South Korea, China, Malaysia and Taiwan, STATS ChipPAC has a reputation for providing dependable, high quality test and packaging solutions.

Further information is available at www.statschippac.com.

Flex-Circuit Based Chip-to-Chip Interconnection Concept Validated by Intel Team

SAN JOSE, CA – The performance potential of high speed, copper based, direct interconnections between IC packages by means of a flexible circuit has been proven again, this time by Intel Corporation.

The results were discussed in a paper at the IEEE CPMT Society's Electronic Component and Technology Conference (ECTC) conference, July 2006, in San Diego in a paper titled: *"Flex-Circuit Chip-to-Chip Interconnects"*. The paper was authored by team of scientists and engineers from facilities in Hillsborough, OR, Santa Clara, CA and Chandler, AZ. In the data rich paper, the authors concluded that "20Gbps signaling on channels of relevant lengths is possible", however the authors also noted that "we are not ready to introduce flex I/O into any mainstream products." Even so, they did conclude also that "the possibility of a chip-to-chip interconnect with minimal discontinuities and propagation loss is a strong attractor and corresponding high-speed solutions will be in demand".

"We are delighted with both the quality of the Intel team's research and their reported results" noted SiliconPipe CEO and co-founder Joseph Fjelstad, "These results (20Gbps over extended distance) add significant credibility to SiliconPipe's concepts and validate the results SiliconPipe has presented to the electronics industry over the last few years, most recently in February at DesignCon West in Santa Clara, CA in a paper coauthored with Aglient, Aleuros and Gigatest."

SiliconPipe OTT technology (an acronym for Off-the-Top or Over-the-Top) is viewed, by many pundits of the electronics industry, as an important enabling technology not only for meeting high-speed data requirements as reported but also for low power potential. "In our demonstration vehicle, code named "Sidewinder", Fjelstad noted "our team showed it possible to send signals at 10Gbps over distances up to 30-inches through two connectors and do so using less than 2% of the anticipated transmission power while maintaining a 60% timing margin."

"However," Fjelstad continued, "there is still more benefit to mine and extract in this area and SiliconPipe is continuing to develop and evaluate new copper based interconnection solutions to meet the cost performance needs of future electronics and the Stair Step Package (SSP) it appears will be an important element of that future."

For more information about SiliconPipe visit their website at www.siliconpipe.com.

Air Liquide's Balazs Analytical Services Announces a New Breakthrough

FREMONT, CA – Balazs Analytical Services announces quantitative techniques that provide parts per quadrillion (ppq) trace analysis. Analysis at ppq levels, where 1 ppq is equivalent to 1 in a million billions, becomes critical as technology nodes decrease to 90nm and below.

As semiconductor technology advances, increased attention to the purity of manufacturing material is required. To more accurately quantify trace concentrations of contaminants, Balazs Analytical Services, a division of Air Liquide Electronics U.S. LP, has introduced PPQ Analysis, a new analytical technique for accurate quantification of ultra-trace metal concentrations in water and process chemicals down to part per quadrillion (ppq) levels.

The ability to provide accurate and routine PPQ Analysis results from a multi-year R&D effort to develop and incorporate ultra-clean processes throughout the sample lifetime. Special care begins at initial sampling and sample preparation and continues through the final blank and sample analysis by Inductively Coupled Plasma Mass Spectrometry (ICP-MS).

Balazs' PPQ Analysis has been validated by the leading semiconductor industry organization and is currently used in production by several industry leaders.

Balazs Analytical Services, a division of Air Liquide Electronics U.S. LP, operates ISO

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For further information visit www.airliquide.com.

SiliconPipe Announces First Full Technology License

SAN JOSE, CA – SiliconPipe has announced that the company has secured a use license agreement with an unnamed company. For business reasons, the licensee prefers to remain anonymous for the present time

"We are extremely pleased that we were able to strike this first use agreement and we at SiliconPipe are looking forward playing a small role in the future of success of this pioneering company by way of their use of SiliconPipe technology." stated company co-founder and CEO Joseph Fjelstad. "We have previously licensed certain manufacturers, most notably the advanced assembly foundry, NexGen Electronics (San Diego, CA) to build products for user evaluation", he continued, "but this represents the first company seeking to explore use and deployment of certain of SiliconPipe's diverse technology.

Under the terms of the license agreement, the new licensee will have access to SiliconPipe's full technology portfolio which includes innovations in interconnections, substrates, IC packages, connectors, sockets, embedded passives, test and ESD protection as well as novel memory architecture that the company believes will allow for standard DDR2 memory to operate at 12.8Gbps and beyond.

For additional information visit www.siliconpipe.com.

UMC's 65nm Process Sees Widespread Acceptance

SUNNYVALE, CA – UMC has reported the progress of its 65nm production ramp up. The leading-edge process is seeing strong demand and interest from a variety of customers whose products span a wide range of semiconductor applications. Two customers have already qualified their designs and are in production for various 65nm products at the foundry, with eight other customers engaged and 11 product tape-outs expected by the end of summer 2006. Designers are leveraging the foundry's established DFM solutions, most recently at 90nm (see www.umc.com/English/news/20060301.asp), to minimize design-in risk and uncertainty and realize the power and performance benefits offered by 65nm technology.

The DFM challenges faced by today's SoC designers can vary and are unique with every chip design. As such, instead of a single, generic DFM solution, UMC provides optimized DFM resources that customers can easily incorporate into their existing design environments. In addition to this customized approach, UMC's DFM solution includes DFM-compliant IP that embraces the intricacies of the fabrication process. The foundry also performs post-tapeout services for each customer, including OPC, LRC, dummy metal fill, slotting, and others.

UMC's robust DFM solution includes Lithography Process Check (LPC), Critical Area Analysis (CAA), Litho and Chemical Metal Polishing (CMP) variation aware extraction, Thermal impact analysis and Static Statistical Timing Analysis (SSTA), etc. To develop its comprehensive 65nm offering, UMC partnered with every major EDA vendors, and newer DFM companies that provide specialized DFM solutions.

UMC's 65nm process is currently ramping to volume production at its 300mm fabs in Taiwan and Singapore.

Visit UMC on the web at www.umc.com.

Palomar Receives Semiconductor International's Editors' Choice

CARLSBAD, CA – Palomar Technologies, leader in precision automation equipment and process development for microelectronic assembly, has received the Editors' Choice Best Product Award for its Model 3500-II Automatic Component Placement Cell. Presented annually by Semiconductor International magazine, the award honors products that are making a difference in semiconductor manufacturing. This is the second consecutive year, and the third time, that Palomar has won this award.

The Model 3500-II is designed for fully automatic, high accuracy, precision microelectronics assembly. The flexible, computer-controlled work cell performs adhesive dispense, component placement, die attach, and flip chip operations over a spacious 720 square inch (0.46 square meter) work area. Using look-up and look-down cameras for flip chip applications and relative-to referencing for linear micro-strip line placement, the 3500-II sub-micron axis resolution yields typical placement accuracies of better than ±12 micron (0.5 mil), 3 sigma. Applications include flip chip, stacked die, chip-on-board, fine pitch surface mount, multi-chip modules, microwave modules, and hybrid microcircuits.

Palomar's team, including some of its most experienced engineers, consistently improves this multi-functional, multi-dimensional, flexible tool to push the limits on speed and accuracy. The Model 3500-II represents the latest develop-

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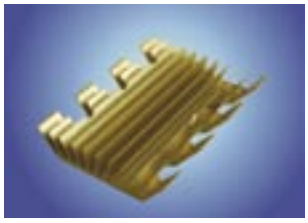
ment in Palomar's long history of manufacturing automatic placement systems.

For more information, visit www.PalomarTechnologies.com or call 760-931-3600.

Heat Sinks Cool BGAs in Low Air Flow Conditions



NORWOOD, MA – Advanced Thermal Solutions, Inc. (ATS) has introduced a low profile, high performance heat sink designed for cooling hot BGA components in low airflow velocity conditions. The EX2 heat sink is only 9 mm in height, which allows its use inside enclosures where space is limited. Its case-to-ambient thermal resistance is 1.8°C/W within an air velocity of 600 ft/min.

EX2 heat sinks weight just 16 grams and can be securely attached to a component with double-sided, thermally conductive adhesive tape. With no mechanical hardware needed, weight and assembly time are reduced and valuable board space is conserved.

More information on these sinks can be found on the Advanced Thermal Solutions web site, www.qats.com, or by calling 1-781-769-2800.

CMC Expands Ceramic Substrate Rework

TEMPE, AZ – CMC Interconnect Technologies, a provider of Technology Services to the Electronic Interconnect and Advanced Materials Industries, continues to expand their capabilities for Ceramic Substrate, Module and Package Rework. With focus on complex and high dollar value ceramic products, rework is the refurbishing of material for reuse in production. Reworked ceramic substrates will meet the same quality standards and product reliability specifications as new incoming substrates, with a significantly lower material cost.

"Reduction in overall product cost, without sacrificing product quality, is a major factor in the increase in rework projects," stated Nick Leonardi, CMC VP of Sales and Marketing, adding, "In many cases, clients were unaware of the successful option to rework ceramic materials".

Other technology services offered by CMC include failure analysis and consulting; material and process characterization; deconstruction or reverse engineering; and technical market studies.

"Reclaim projects take full advantage of CMC's experience with the wide range of electronic materials and processing technologies," noted Bob Tesch, CMC Engineering VP. "Our capabilities and in-house analytical and deconstruction expertise compliment these types of rework projects".

CMC Interconnect Technologies is a Technology Services Business focused on Electronic Interconnect and Advanced Materials. CMC's unique business model combines high level materials characterization and failure analysis with consulting and technical market studies to provide a complete resource to solve process or product issues and implement solutions. CMC has experience with Advanced Interconnect Materials and Interconnect Assembly Processes at the Device, Package, Board and System Level for a range of industries.

Please visit the CMC web site at www.cmcinterconnect.com for more information.

SUSS MicroTec Develops Wafer Bonder for High Vacuum

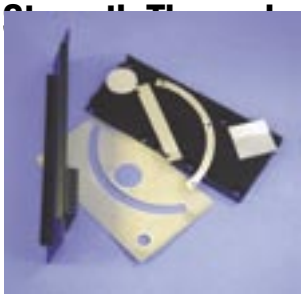
Applications

MUNICH – SUSS MicroTec, a leading supplier of precision manufacturing and test equipment for the semiconductor and emerging markets showed at Semicon West for the first time a unique wafer bonding system designed for high vacuum applications. The system will be available in the third quarter of 2006. An industry-first, this field upgradeable load locked wafer bonding system was developed by SUSS MicroTec for advanced MEMS devices that require ultra clean, low moisture and low contamination vacuum bonding.

In addition the new product offering, named "M-Lock," is well suited for MEMS devices with on-chip getters such as silicon gyros and other advanced MEMS products.

For more information please visit www.suss.com.

New High Bond



MAHWAH, NJ – MH&W International has introduced KoolBond™ material for providing a thermally conductive interface while firmly attaching heat sinks to hot PCB components. KoolBond interface material consists of a fine woven, nickel-coated copper fiber matrix with a high-strength pressure sensitive adhesive (PSA) on the outside. The woven copper closely conforms to irregular mounting surfaces on components and heat sinks to enhance thermal transfer and cooling performance.

KoolBond material's double-sided PSA provides a high strength bond that eliminates the costs of screws, clips, or other hardware for mounting sinks to IC's, transistors, mosfets, op amps, and other hot-running circuit board components.

Complete information is available at www.mhw-thermal.com or www.koolbond.com.

AGEM Changes Name to AGC Electronic Materials

HILLSBORO, OR - Asahi Glass Electronic Materials, known in the Electronics indus-

North American Semiconductor Equipment Industry Posts July 2006 Book-To-Bill Ratio of 1.06

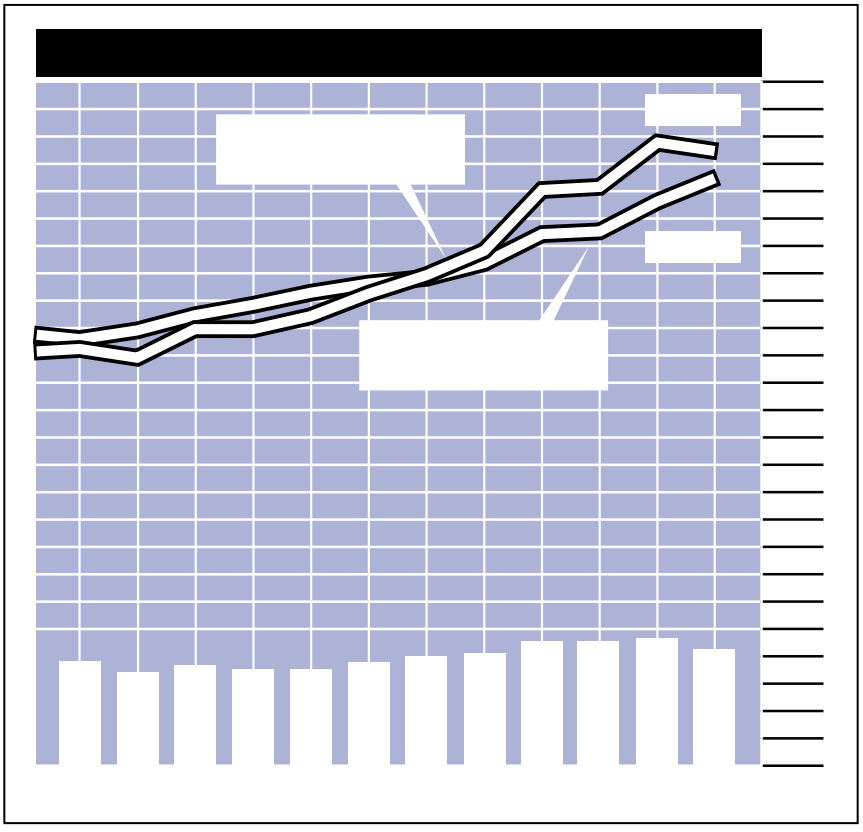
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.75 billion in orders in July 2006 (three-month average basis) and a book-to-bill ratio of 1.06 according to the July 2006 Book-to-Bill Report published today by SEMI. A book-to-bill of 1.06 means that $106 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in July 2006 was $1.75 billion. The bookings figure is about two percent lower than the final June 2006 level of $1.78 billion and over 73 percent higher than the $1.01 billion in orders posted in July 2005.

The three-month average of worldwide billings in July 2006 was $1.65 billion. The billings figure is almost six percent above the final June 2006 level of $1.56 billion and almost 53 percent above the July 2005 billings level of $1.08 billion.

"Billings for North American equipment manufacturers are at their highest level since April of 2001, while bookings decreased slightly," said Stanley T. Myers, president and CEO of SEMI. "Even with a slight bookings slowdown, the worldwide equipment market is still on track to grow about 20 percent in 2006."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



try as "AGEM", has formally changed its name to AGC Electronic Materials as of April 1, 2006.

Founded in 1996, AGEM is a manufacturer and supplier of Silicon Carbide furnace components, and is a certified-approved supplier to wafer fabs and OEM furnace manufacturers throughout North America and Europe.

"AGEM is no longer just a silicon carbide company. We're gaining market share in both North America and Europe with our synthetic quartz and glass product lines that already have large established market shares in Asia," explains Jeff Schmitt, General Manager of AGEM, of their new product lines from Asahi Glass.

"Our new company name, AGC Electronic Materials, will align us closer to Asahi Glass (known globally as "AGC") and better reflect our new product line-up of glass materials for photonics, MEMS and other leading-edge next-generation applications," Schmitt explained.

AGEM has also launched a new website to include their full product line up and their new branding - www.agcem.com

More information about Asahi Glass can be found at www.agc.co.jp.

SUSS MicroTec Introduces SussCal® Professional

MUNICH – SUSS MicroTec AG has announced the release of the newest version of its renowned wafer-level, high-frequency calibration software. SussCal Professional simplifies the wafer-level calibration process and significantly increases the accuracy of on-wafer measurements.

SussCal Professional is the cornerstone of accurate, on-wafer measurements, guaranteeing excellent wafer-level calibration time after time. The VNA, cables and wafer probes are calibrated using a set of well-defined standards to eliminate systematic error, moving the reference plane of the measurement to the device under test (DUT). SussCal Professional simplifies this calibration by using an intuitive, top-down process to guide the user through the entire set-up, from system settings to standard assignment. It also includes powerful features like the Port-Mapping™ technology for easy set-up of complicated multiport calibration.

For more information, please visit www.suss.com.

F&K Delvotec

F&K Delvotec presented its new Heavy Ribbon Bonder 66000 G5 at the SMT/Hybrid/Packaging fair 2006 in Nuremberg. This specialized version of the successful Heavy Wire Bonder is easily converted from the standard version to process aluminium ribbon for power applications.

This technology has gained popularity in the last few years for a number of power applications because it features higher current carrying power on a smaller contact area while simultaneously increasing bonding productivity. Nonetheless the bond process remains robust and reliable and the patented Bond Process Control BPC can be employed to improve process quality.

F&K Delvotec's goal is to deliver highest quality bond processes based on state of the art bonding equipment as well as service and support to the industry.

F&K Delvotec offers the widest range of wire bonders and bond test and inspection systems available in the market for the production of discrete devices, ICs, hybrid systems and sensors, as well as multi-chip modules (MCM), chip-on-board (COB) applications and MEMS.

For more information visit www.fkdelvotec.com.

STATS ChipPAC Enters Strategic Joint Venture with China Resources Logic Limited

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. and China Resources Logic Limited have announced the signing of a definitive agreement for the companies to enter into a strategic joint venture for the assembly and test of select products in Wuxi, China.

Under the agreement, CR Logic's indirect wholly-owned subsidiary Wuxi CR Micro-Assembly Technology Ltd. will purchase more than 1,000 sets of key assembly and test equipment from STATS ChipPAC for US$35 million, to be settled in cash installments over a four year period until 2010. STATS ChipPAC will continue to provide sales and technical support to its existing customers on specific low lead count packages until December 31, 2009 with customer purchase orders being placed directly with ANST. ANST, in return, will pay STATS ChipPAC a commission on the aggregate amount of revenues generated from such orders on a quarterly basis in 2007, 2008 and 2009. In addition, STATS ChipPAC will receive a 25% ownership stake in ANST for a cash consideration of US$10 million with CR Logic owning a 75% interest.

ANST has been in business for over 25 years and currently provides IC assembly and testing foundry services to fabless design houses and integrated device manufacturers ("IDMs") in the People's Republic of China. Located in Wuxi, China, ANST specializes in assembly and test services for various leadframe based IC packages.

Further information is available at www.statschippac.com.

Gartner Says Worldwide Semiconductor IP Revenue on Track for 25 Percent Increase in 2006

STAMFORD, CT — Demand for semiconductor intellectual property (IP) is growing, and the demand is shifting from simple IP to complex IP, according to Gartner, Inc. Worldwide IP revenue is projected to total $1.8 billion in 2006, a 24.9 percent increase from 2005 revenue of $1.4 billion. By 2010, worldwide semiconductor IP is forecast to surpass $2.7 billion.

Gartner defines semiconductor IP as predesigned blocks of circuits for use in making complete semiconductor devices. Its definition of the semiconductor IP market only includes revenue from IP sold on the open market. Captive IP, which is IP designed and used by one organization alone, is excluded.

Complex IP products have the potential to generate large revenue streams. However, they require customization, which means they will face the same problems as design services, such as being hard to scale.

Gartner analysts expect a significant number of complex IP solutions to be supplied by fabless semiconductor companies to complement their chip revenue. With their application expertise and their chip businesses to keep engineers busy during periods when licensing sales are slow, these companies will have a big advantage.

Additional information is available in the Gartner Dataquest report *"Forecast: Semiconductor Intellectual Property,*

The Surface of Chip Scale Packaging

SURFECT TECHNOLOGIES, INC.

Steve Anderson
CEO

Doug Welter
COO

Mark Eichhorn
VP Sales & Marketing

Surfect was founded in December 2000 for the purpose of developing automated electroplating tools for wafer-scale deposition, processes to apply metal deposits at the wafer level, and high performance interconnect technologies designed to address the challenges facing the electronics component fabrication and semiconductor assembly industry. Since its creation, Surfect has developed and patented:

- Automated electroplating tools for wafer-scale deposition
- A unique process to apply combinatorial metal deposits at the wafer level
- Proprietary solder material and lead-free technologies

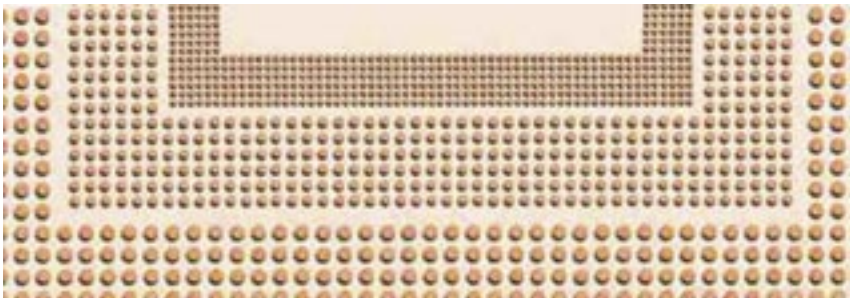
These developments capitalize on a widespread industry imperative for back-end interconnect technology to catch up and follow Moore's law for the millions of transistors that are produced each year and must be interconnected. The Company's current focus is on completing research and product development, ramping up sales and marketing activities, and providing local customer factory support for its new tools for the Asian market.

Surfect believes that two of the three biggest obstacles to wide spread use of flip chip production are fading fast: the availability of cost-effective equipment and the higher costs to produce flip chips in volume. The third obstacle, finding a lead-free and high performance wafer scale metal deposition solution, is much more complicated. As flip chip technology expands, so, too does the demand for new tools, improved materials and bulletproof process. The company's focus on creating a true process plating computer using quick change chemistry tanks is designed to provide customers more flexibility with multiple metal processing requirements and higher uptime. Surfect's mission is to bring cost-effective electroplating tools and reliable multi-layer processes to semiconductor back-end assembly.

Surfect is addressing the growth of flip chip with development of a compact electroplating deposition process tool that provides the electronics industry with a more cost effective way to fabricate high performance, low cost interconnects. Availability of very cost-effective deposition tools to provide this key metal path between the IC die and the PCB or package is critical for continued growth of high density electronic products. Surfect believes that the large growth in consumer and wireless products drives a demand for miniaturization that can only be satisfied with reduction in interconnect paths and materials offered by flip chip and wafer technology. Utilizing a unique single-wafer, multi-metal process cell enables manufacturing of very compact tools with real-time feedback for plating process conditions and provides major operation advantages over its competitors single-metal process cells requiring much more space and maintenance.

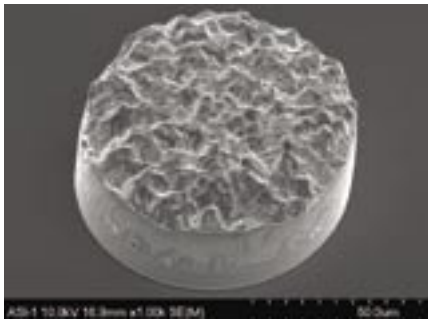
Surfect is also taking the difficult electroplating process knowledge and working to embed it within software/hardware enabling widespread introduction and purchase of much simpler and productive bumping capability. This 'plating computer' should enable most companies that want to develop and implement flip chip and wafer CSP to do so internally, as well at merchant suppliers with recipe portability. Combining improved process technology with a novel closed-cell tool, reduces the difficulty of introducing and supporting flip chip bumping technology in production. Surfect's compact plating computer not only enables multi-metal capability in a continuous and repeatable manner but replaces the traditional cell-to-cell and tank-to-tank wafer transfer with a more powerful single-cell plating computer concept. Utilizing this concept, Surfect has eliminated the need to move the wafer through various plating chemistries reducing the need for robotics and therefore reducing machine cost, footprint and improving machine utilization rates. This single-cell approach expedites and improves production by minimizing wafer handling and, more importantly, enabling a wide range of lead-free solders to be applied.

Through this technology, Surfect's focus is providing customers with a more cost-effective, single-cell tool which fits their incremental capacity needs better and provides the more rapid conversion to the range of leaded and lead-free solders. Growing consumer markets demand more cost-effective process technology with closed-loop plating monitoring, multiple



Current and next two generations of bump pitches: Outer four rows - 250 micron pitch, 120 micron opening; Middle six rows - 180 micron pitch at 82 micron opening; Inside rows - 100 micron pitch at 50 micron opening.

metal deposition, enhanced ion agitation, and lower-cost metrology. Larger wafer diameters often require smaller process lot sizes and they are better addressed with the individual wafer plating cell approach. The addition of bumping capacity in smaller capacity increments enables more cost-effective operation and faster return on capital. The recipe driven, single wafer process eliminates timely setup, increases yield, provides repeatability and reduces the need for dedicated plating expertise at each company. This ease of use is key for wider adoption of flip chip technology at wider base of customer locations and applications.



Enlarged view of 300mm wafer in single wafer processing chamber.

In addition to its tools, Surfect is developing processes for encapsulated powders and solder bumps that would be used in conjunction with these tools. Additional work continues to develop high performance bumps and interconnect which is expected to improve thermal and electrical conductivity in copper as well as solder alloys. This will address the key high performance computing and handheld processor market segment that is demanding more thermal conductivity interconnect.

Development of these tool and process platforms are aimed at the rapidly growing market for both independent device manufacturers (IDM's) as well as merchant suppliers who provide contract wafer bumping services and support. Surfect's believes that its compact and cost effective tool will provide its customers with a definite competitive advantage by enabling them to migrate to flip chip and wafer scale technology more rapidly. Market researchers have stated that the large growth in consumer products such as the iPod is fueling an insatiable demand for miniaturization in silicon ICs that will be served by wafer bumping and flip chip technology. The growing pricing pressures for traditional gold wiring and petroleum-based epoxy mold compounds are accelerating these pressures.

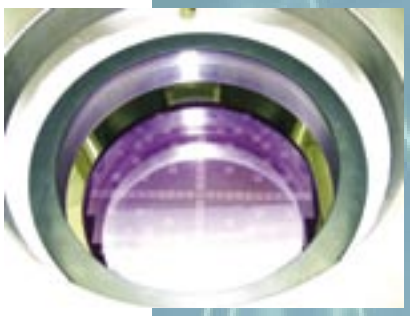
Surfect is led by Steve Anderson, CEO, and a semiconductor industry veteran. Mr. Anderson brings a unique business value and technology set to the company and he is leading Surfect Technologies to new and emerging markets. Steve's depth and history in the semiconductor market at TI and Amkor Technology has attracted a senior management team with significant experience in operations, technology, semiconductor industry management and sales, business development and financial oversight. Doug Welter, COO, is a 28 year Philips and Motorola executive. Yixiang Xie, PhD is CTO and has over 24 years experience in semiconductor and electronics development. Mark W. Eichhorn is head of Sales & Marketing and a 28 year veteran in the semiconductor capitol equipment sector with Kulicke & Soffa Industries. The company has attracted leading engineers for process and software development.

Surfect's product development team is located in Albuquerque, New Mexico. This team of industry veterans and technical experts work closely with customer leaders and industry research groups to understand internal and industry development roadmaps and create the necessary processes. The team is focused on technology required for initial tool and process entry as well as technology developments that will ensure that the Surfect products will also meet emerging requirements. This process requires a tight interaction with both customers and key universities. Their close proximity to the National Labs such as Sandia National Labs and Los Alamos enables tight interaction with some of the leading chemical and nano-material technology which gives Surfect both expert confirmations on its approaches as well as excellent testing facilities.

While the trend toward miniaturization and advanced packaging continues, Surfect believes its tools, materials and wafer-scale processes will enable device engineers to breakthrough performance limits set by current packaging techniques. Surfect's technologies are compatible with existing fabrication processes and procedures, easing adoption of such technologies.

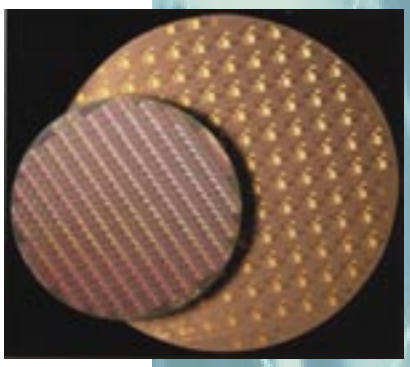
Surfect is poised to pioneer the market for affordable flip chip packaging. The company's mission is to transition current FAB based bumping to the package assembly business model that will reduce costs at the wafer level. In addition, Surfect Technologies unique machine and process structure will allow the industry to reduce capital decision from millions to thousands.

Surfect Technologies, Inc., is located at 12000-G Candelaria NE, Albuquerque, NM 87112 USA, Phone: 505-294-6354, Fax: 505-294-6311, E-mail: info@surfect.com, Web: www.surfect.com. ◆



View of 300mm wafer in single wafer processing chamber.

Array of copper bumps capped with solder.



200mm and 300mm wafer level bumping and interconnect growth accelerated using new multi-metal process tool.

SURFECT TECHNOLOGIES, INC.

Test Cost Reduction

Goh Swee Heng and Toh Ser Chye, Staff Engineers
STATS ChipPAC Ltd

With advancements in packaging technology and increasing complexity in IC components, the challenge is to perform more complex test algorithms for multiple components in a single package and minimize the unit test cost.

This article explores the possibility of reducing test cost through hardware optimization and software innovation. This would include providing flexibility among different tester platforms, innovative uses of existing tester/handler resources to support high volume manufacturing and optimal test time reduction.

Introduction

With the advancement in technology, more functionality is being integrated into a chip, either through system-on-chip (SOC) designs or by assembly process improvements to achieve system-in-package (SiP) solutions where more chips are packed into a single package. The increasing complexity of today's integrated circuit has made testing a challenging task, particularly under the context of maintaining high quality while ensuring a low cost of test.

Built-in Self-Test (BIST) and Design-for-Test (DFT)

The concept of BIST involves the design of test circuitry inside a device that automatically performs the device testing by applying certain test stimulus and observes the corresponding system response. As the testing is done from within the chip, testing can be completed in a much faster and more efficient way than it can be tested using external instruments.

Though BIST testing has a higher design cost and is mainly used for digital testing, it is able to achieve a high fault coverage and helps to reduce the test list significantly. To activate the BIST test would require just a couple of simple ATE (Automated Test Equipment) resources to initiate test and interpret the results. With BIST incorporated into the device, there is a significant test saving. The saving could be realized in the form of capital avoidance as well as reduction in test cost. Not only the test time can be reduced due to the shorter test list, it can also allow testing of a complex device on ATE systems with standard resources.

Design-for-test is a concept of placing certain features in a chip design during the design process to ensure testability of the chip. It enhances the test coverage of the chip and at the same time makes electrical testing simpler. With DFT, a test engineer can access each individual, functional block of the chip in a shorter period of time by utilizing direct access mode (special test mode) through DFT design in the chip, hence reducing the test time.

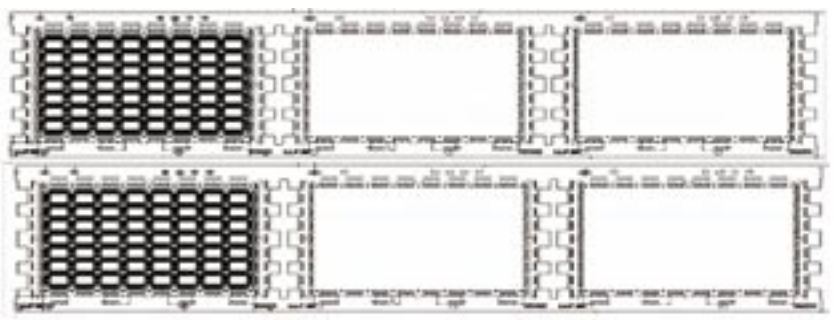
With DFT and BIST design in the chip, instead of using a high cost tester, a low cost tester would be sufficient to test a complex device with the aid of the BIST circuitry. This is especially true for SOC and possibly on SiP as well, where increased circuitry complexity would require high cost tester to test the multi-million gate deep sub-micron ICs.

Strip Testing

Strip testing is another method to reduce the cost of test. Strip testing refers to the process where the devices are tested while they are still in their leadframe strips/panel. Figure 1 shows a device in test panel format. A strip test handler's index time is typically much faster than that of a singulation handler. The increase in throughput will be more significant for devices with short test time where index time could as high as 40% of total test time (index + pure test time) when tested in a singulated unit. Strip testing with its higher parallelism also benefits devices with long test times. Strip testing also allows for a higher level of parallelism testing as the handler does not have the limitation on the number of sites it can handle. Rather, the number of sites available is constrained by the ATE resources available and/or device interface board (DIB) space. In addition, since the handler will be handling the devices in strip/panel format instead of singulated units, it will help to lower or even eliminate downtime due to jamming. This minimizes any manual intervention, thereby improving tester efficiency. With higher parallelism and improved tester efficiency, production throughput will increase significantly in tandem with reduced test cycle time. Strip testing is also able to provide better contact ability because it uses visual alignment. This helps to reduce failures due to bad contacts, thereby reducing the retest rate. The test flow for strip testing and the conventional test flow are shown in Figure 2a and Figure 2b respectively.

On Board Circuitry

Another method to reduce test cost is through the use of onboard circuitry on DIB. For example, one problem often encountered during multi-site development is insufficient tester resources. Instead of upgrading or buying new



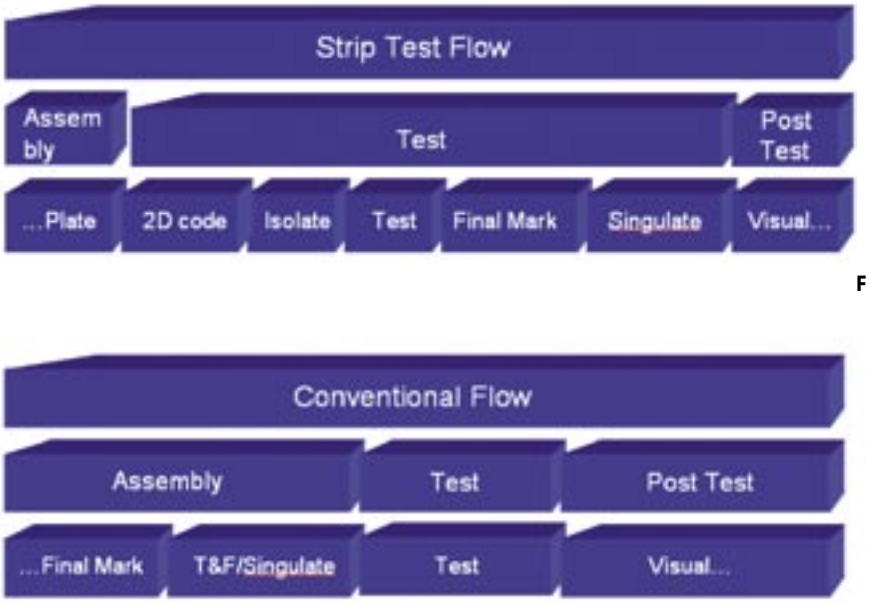


Fig-

instruments for the tester to support testing requirements, extra test circuitry could be designed on DIB at a small fraction of the test instrument cost to overcome the resource constraint. Onboard circuitry could be designed to allow sharing of tester resources across all sites. This provides the ability to test a higher number of sites than was initially limited by the tester resource. However, care must be taken to ensure that the sharing of the resource does not result in serial mode testing, otherwise the test cost saving would be diminished.

Test Time Reduction

Different techniques have been used to reduce test time in an effort to reduce cost of test. One of the most common techniques to keep test times low is parallel testing. Parallel testing could involve multi-site testing and multi-core testing for SOC devices. Multi-site testing is testing multiple units simultaneously whereas multi-core testing involves testing different functional blocks of the device concurrently. This can reduce unit test time and thereby increase tester throughput rate.

Another technique is to eliminate redundant tests from the test program. Redundant tests are termed as tests which do not produce any unit failure. The failure history can be obtained from production test data collected over a period of time and/or for a pre-determined volume of lots. However, this could result in reduced test coverage at final test. To address this, the tests which were removed could be inserted in the quality assurance (QA) test list. In addition, lot sampling could be performed where some lots are sent through the original full test list in order to validate that the tests which were removed do not produce unit failures.

Test time reduction can also be achieved through test program optimization. In this case, the test coverage of the device would remain unchanged since no test would be removed using this technique. Typically test program optimization involves re-sequencing the test flow to eliminate any duplicate setup procedures. Test procedures may also be optimized for faster execution through more efficient test methodology. For example, by using a larger resolution bandwidth to perform digitizing of the waveform, the capture time could be reduced. Programming of the instrument to a fixed measurement range rather than using auto-ranging mode would also help to shorten the instrument's setup time.

For some devices, tri-temperature (hot/cold/ambient) testing is required. An evaluation could be completed to eliminate tri-temperature testing. Normally, a test result from hot and cold temperature can be correlated back to ambient temperature. With hot and cold temperature testing eliminated, significant cost savings can be achieved from a reduction in the device test cycle time and a reduced number of test insertions.

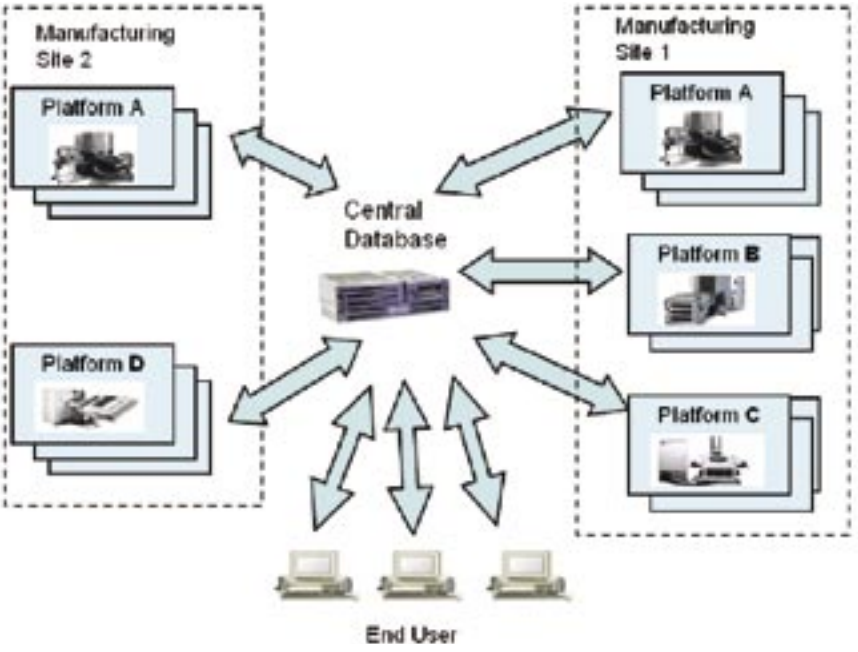


Fig-

Tester Cost

The depreciating cost of the ATE testers is usually the dominant factor that affects the cost of test. In today's testing industry, increasing device complexities and test requirements have shortened the useful life of many ATE testers. In this context, it is crucial that extra effort should be given to the tester selection during the initial test development stage. Scalability is the ease with which

a system or instrument can be tailored to meet different requirements. In the context of ATEs, a tester with scalable architecture would mean that one could re-configure the tester according to the device test requirements. With scalability, the tester platform is architected for change and as device mix changes over time, the tester configurations can be changed to adapt to the device test requirement without the need to purchase new instruments/testers. This broad test capability would help reduce new capital investments and at the same time expand the useful life of existing ATE testers, thereby providing a lower cost of test.

Recoding the test program for migration to other tester platforms may help to provide the flexibility required in today's highly competitive industry. Tester migration helps to utilize different test platforms to support volatile production volumes and provide maximum return on investments (ROI) for the tester purchase. In addition, it also helps to extend the asset life of older tester platforms. The savings will be tremendous if the device can be tested on older tester platforms of which the tester costs have been fully depreciated.

Central Database and Automated Scheduling

Tester utilization also plays an important part in determining the cost of test. Having a higher tester utilization rate will translate to a lower test cost. A centralized tester configuration database can provide information on the tester configuration to aid capacity planning and is one of the ways to improve utilization rates. With a central database, an appropriate test strategy can be developed to optimize the usage of available tester platforms.

Another option to minimize cost and maximize utilization is to create a common tester configuration for digital, mixed signal, radio frequency (RF) and SOC devices. Future test development should be based on this configuration set. This would allow test programs to be ported to any of the testers within the same standard base configuration. Figure 3 show a diagram of a central database.

With an increasing mix of devices, automated scheduling would help to improve tester utilization by determining the appropriate time to the next step and allocating the appropriate tester to the device. This would help to reduce tester idle time, thereby improving utilization and reducing test cost. Such systems can be modeled on the basis of process optimization. In addition, the system is also able to provide feedback on the tester usage.

Conclusion

To achieve the optimum results, various test time reduction techniques such as test program optimization and parallel testing should be employed together with the appropriate test strategy to maximize the utilization and enhance tester efficiency.

Test strategies such as tester migration will help to extend the useful lifespan of older test platforms. Investing in a new tester offers a higher level of parallelism testing and/or scalability with a broad base of testing capability.

A central database and automated scheduling software present opportunities to achieve better synergy among people, machines and processes to improve efficiency and reduce the cost of test. ◆

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An Alternative Screening Method for the Detection of RoHS Substances

Hugh Gotts and Fuhe Li
Air Liquide – Balazs Analytical Services

Alternative screening methods which are rapid and accurate have been sought by the electronics and semiconductor industries to ensure compliance with the European Union Directive 2002/95/EC. The European RoHS (Restriction on Hazardous Substances) directive bans the use of certain materials such as lead, mercury and cadmium, in electronics products built anywhere in the world and sold on the EU market beginning July 1, 2006. Currently accepted methods for analysis include wet chemical processing techniques which, although accurate, can be time consuming and labor intensive. Quick screening methods such as X-Ray Fluorescence (XRF) have taken center stage due to their ease of use and sensitivity at the risk of lower accuracy as compared to wet chemical methods.

Alternative Method

An alternative method which is being developed makes use of Laser Ablation Inductively Coupled Plasma Mass Spectroscopy (LA-ICP-MS or SARIS™). This technique relies on a high power UV laser to instantaneously volatilize the sample surface. The volatilized material is carried in an inert gas stream and introduced into the plasma of the ICP-MS system for subsequent detection of elemental species. One advantage of this technique is that the time consuming sample preparation technique is eliminated allowing rapid sample analysis. Another advantage of SARIS is its ability to control depth of the analysis by varying the laser power density or performing additional ablation of the area of interest, permitting the determination of changing elemental concentration with depth (depth profiles) as deep as 100 mm.

Metals	**Solder Balls**
Alloys	**Bonding Wires**
Polymers	**Inks**
Adhesives	**Package Leads**
Natural Products	**Packaging Material**
Laminates	**Insulators and Ceramics**

SARIS™ also retains the benefits of ICP-MS to accurately quantify elements at the required specification limits through the use of NIST traceable standards, and even to a 10 to 1 ppm range for the method detection limit. A bonus of this analysis is that the concentration of any filler compounds or additives may be monitored as a by-product of the RoHS analysis. Analyses may be performed on any variety of solid materials, as shown in Figure 1. The lateral dimensions of the analysis area may be varied from as large as several millimeters to spots as small as 10 mm.

Case Study

SARIS™ analyses of the solder mask samples from two different vendors were performed to determine the elemental constituents present and whether the materials were RoHS compliant. The blue solder mask was found to be compliant due to the absence of any RoHS substance. The green mask, on the other hand, indicated the presence of bromine. Depending on the concentration of bromine, additional wet chemical analysis may need to be performed to determine if the compounds present were members of the banned PBB or PBDE materials. The graphs in Figure 2 show the bromine peak in the green mask, and the noticeable absence of RoHS banned elements (lead, cadmium, mercury and chromium) in both graphs.◆

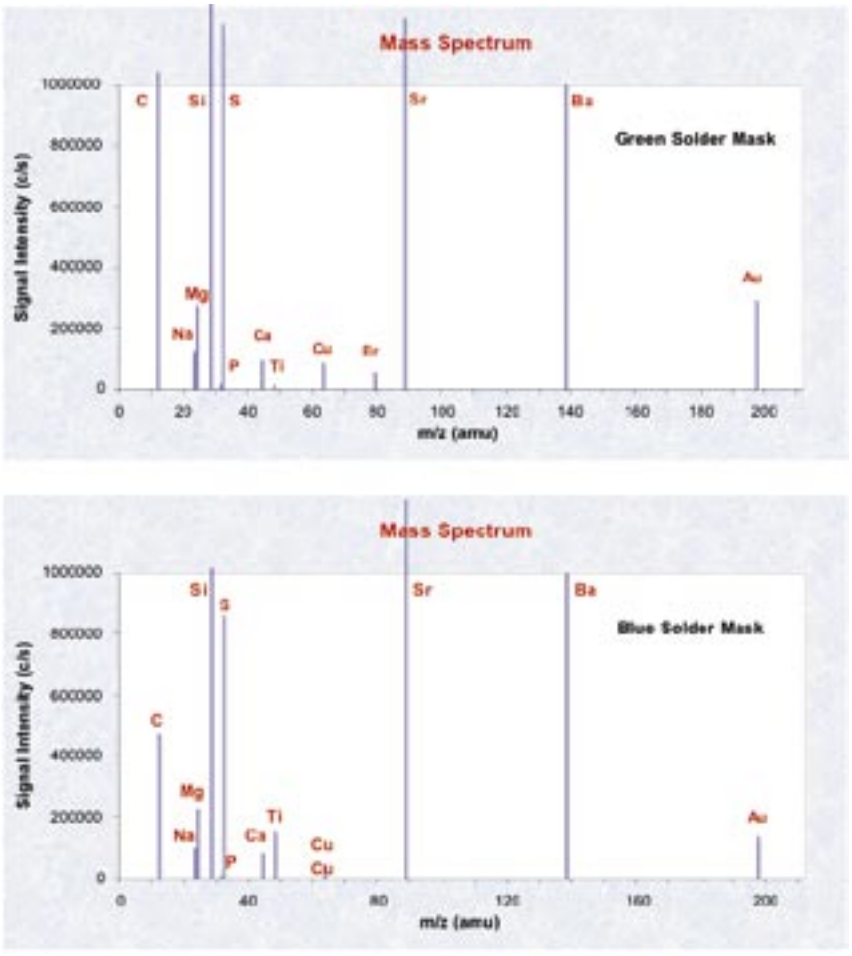

Figure 2: Comparison of PWB Solder Mask Thin Films from Different Vendors.

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Guillermo Velazquez
SMT Manufacturing Engineering Department Head
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Henkel News

Raising the Bar for Materials Development and Analysis
September 2006

Henkel

Raising the Bar for Materials Development and Analysis

George Carson, Ph.D., Electronics Group
Henkel

Formulating and developing advanced electronics materials is a complex process which requires experienced chemical scientists, the know-how of engineers and, let's face it, a fair dose of ingenuity as well. Almost as important as the minds behind the products are the tools used to develop, process and analyze the materials that will be incorporated into sophisticated and, often, mission-critical electronics products.

Recognizing that the most advanced equipment and analysis tools are necessary for research and development of modern materials, Henkel has invested millions of dollars in a state-of-the-art facility that houses next-generation assembly and semiconductor processing equipment, sophisticated analysis tools and, of course, today's top minds in materials science. Henkel's Irvine, California –based Research and Applications Lab is, undoubtedly, the most well-equipped facility of its kind, taking the possibilities for materials development, research and evaluation to a level heretofore unavailable. This unique set-up enables not only product prototyping for customers that minimizes cost and quickens time to market, but also allows for streamlined and accelerated development of advanced assembly and semiconductor materials and material sets for the marketplace at large.

Loaded with Capability

From complete SMT assembly to leaded package and stacked die CSP production and test capabilities and everything in between, Henkel's advanced research and development facilities are unrivalled. State-of-the-art equipment and analysis tools are readily available for customer prototype and development work and package and materials testing. With this equipment literally at their fingertips, engineers and applications specialists research and formulate new materials on a daily basis.

With three complete assembly lines – one for advanced SMT assembly, one for wire bond and one for flip-chip – the experts at Henkel are able to build all types of advanced components and then assemble those devices onto a PCB. This unmatched capability enables scientists and applications engineers to study, in detail, materials behavior, performance and reliability. Also part of the well-equipped facility are encapsulation and molding capabilities, a 5,000 square foot, Class 10,000 clean room and reliability, electrical and gate leakage testing tools.

Product-Oriented Development Teams

And, of course, the teams utilizing these tools and analysis systems are composed of renowned materials experts whose talents and skill sets are utilized with a very unique approach. Unlike other materials suppliers who focus on the development of materials from a myopic materials-only approach, Henkel development teams focus on package-specific (SOIC, StackedCSP, QFN, SIP, etc.) material issues and testing to ensure optimized, compatible material sets for the chosen package style. To the customer, this means that the package is thoroughly analyzed at all materials levels – from die attach to mold compounds to thermal interface materials all the way through to board assembly. Materials often behave differently in different packages. This package-specific development approach to materials formulation ensures optimum performance and reliability.

Proof's in the Products

With expert product teams and advanced production tools all now centrally located in Irvine, California, the electronics group of Henkel has seen the results of this unified materials development approach with the introduction of several new award-winning materials and material sets. In the lead-free arena, Henkel has developed and launched Multicore® LF318, which has become the market's premiere lead-free solder paste. But, solder paste is not the only consideration for lead-free and the materials leader has also formulated and made available Loctite® 3629 Chipbonder®, a remarkable low-temperature cure adhesive that can withstand the elevated processing temperatures of lead free and Loctite 3549 CSP Underfill, which minimizes device stress incurred during shock, drop and vibration.

On the semiconductor packaging side, there have been several lead-free mold compound – die attach material sets developed for a variety of packages including SCSPs, TSOPs, TSSOPs, TQFPs and SOICs, just to name a few. Henkel's material set methodology ensures that all of these materials are tested and compatible – an approach that reduces costs for device manufacturers and speeds time to market.

These products and material sets are truly ground-breaking, but are just a few of the many new materials that have been introduced and those that are under development. This is just the tip of the iceberg. The most industry-changing materials have yet to be seen. Stay tuned, because in the months to come, Henkel is set to introduce some products that will completely revolutionize electronics manufacturing!

For more information about how Henkel's approach is raising the bar for materials development, send an e-mail to electronics@us.henkel.com or call the electronics group's headquarters at 949-789-2500. ◆

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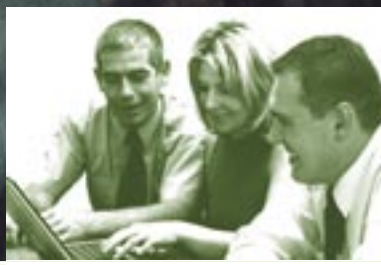

"So much to do, so little time" is a common dilemma for today's manufacturers. But, it need not be this way. Henkel's material sets will save you time for more pressing concerns.

Can you really afford to spend the time necessary to qualify, test and guarantee compatible products? If not, mistakes are inevitable. Fortunately, Henkel's Material Sets solve this dilemma by delivering proven package performance - stress reduction, compatible chemistry and material interface designs. Using the cross-qualified Hysol mold compounds, QMI die attach adhesive and underfills, this complete solution saves you up front design time and reduces overall maintenance time and costs. And you get the support of a world-renowned electronics specialist – Henkel is the Single material solutions provider you've been waiting for.

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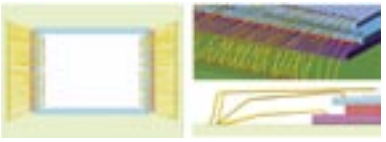

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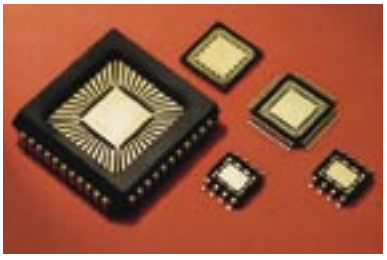

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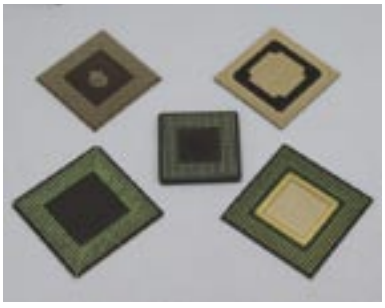

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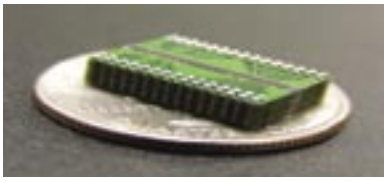

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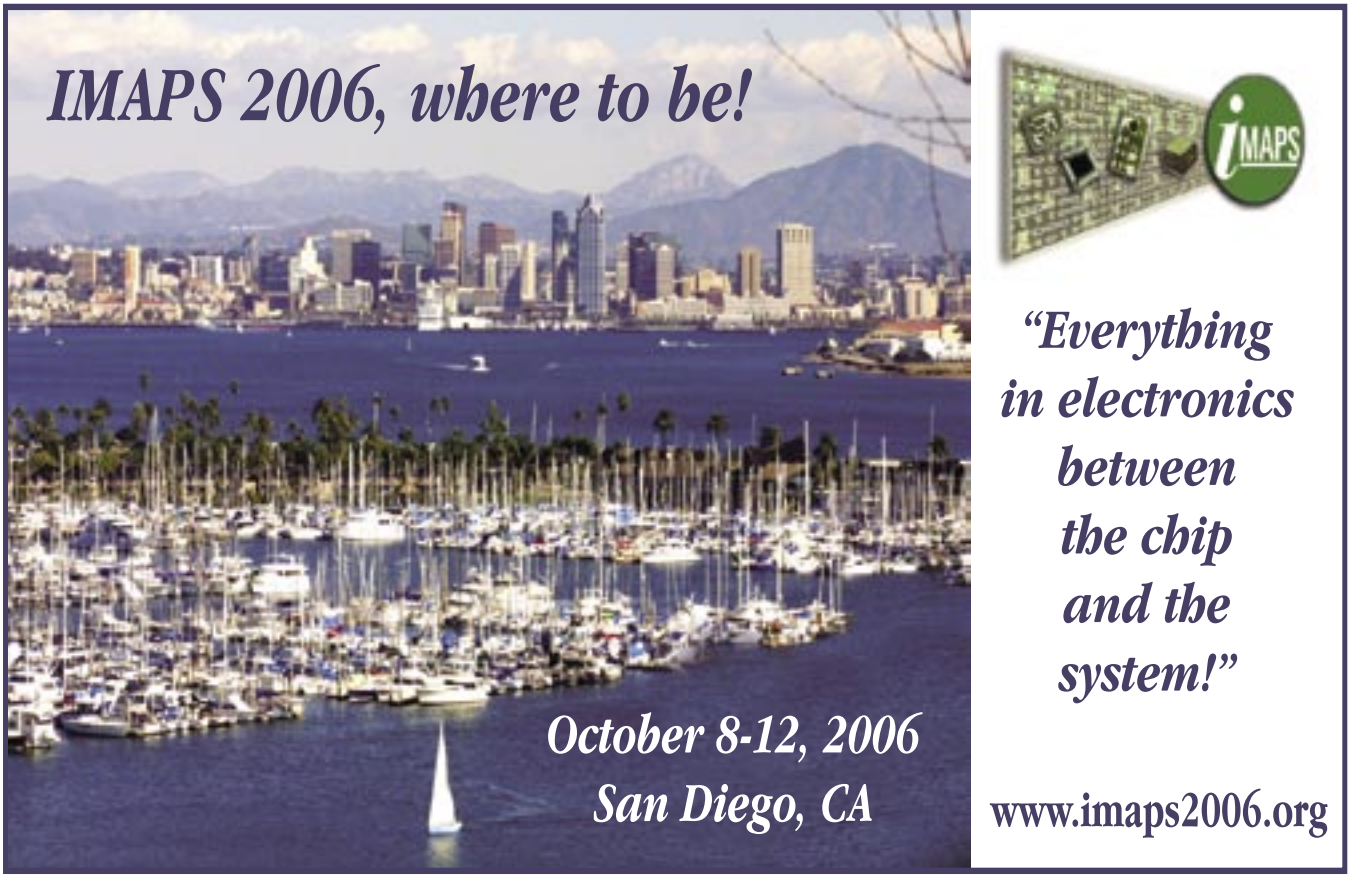

	SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
OCTOBER 2006	1	2	3	4	5	6	7
	8	9 COLUMBUS DAY	10	11 SUNNYVALE MEPTEC LUNCHEON Ramada Silicon Valley	12 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	13	14
	15	16	17	18	19	20	21
	22	23	24	25	26	27	28
NOVEMBER 2006	29 DAYLIGHT SAVING TIME ENDS	30	31	1 2006 TECHNOLOGY VENTURE FORUM October 31 - November 2 San Francisco Airport Marriott, Burlingame, CA	2 INTERNATIONAL WAFER-LEVEL PACKAGING CONFERENCE November 1 - 3 Wyndham Hotel, San Jose, California	3	4
	5	6	7	8	9	10	11 VETERAN'S DAY
	12	13	14	15	16 MEPTEC IC PACKAGING & TEST ROADMAPS SYMPOSIUM	17	18
	19	20	21	22	23 THANKSGIVING	24	25
	26	27	28	29	30	1	2
DECEMBER 2006	3	4	5	6	7	8	9
	10	11	12	13 SUNNYVALE MEPTEC LUNCHEON Ramada Silicon Valley	14	15	16 HANUKKAH
	17	18	19 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	20	21	22	23
	24 31	25 CHRISTMAS	26	27	28	29	30

The MEPTEC Medical Electronics Symposium

Integrating Technology with the MEPTEC Methodology

Nicholas Leonardi, Vice President Sales & Marketing
CMC Interconnect Technologies

This issue of the *MEPTEC Report* will be distributed at the first *MEPTEC Medical Electronics Symposium*; therefore, if you are reading it at the event, I would like to welcome all those in attendance and thank all the members of the symposium committee and speakers for their support in preparation for the event. This symposium was unique for many reasons, both for the veterans in the MEPTEC organization as well as those recently introduced to this microelectronics industry group. In bringing together attendees from three industries, Microelectronics, Medical and Bioscience, it is worthwhile to understand the challenges that were addressed and the methodologies that were duplicated in organizing this major technical event. From my perspective, the success of this symposium is not in the total number of attendees; however, it is measured by the high level of interest in the format of this event and ability to bring together (integrate) technologists from these three key areas of technology, giving them the opportunity to meet face-to-face, learn and exchange ideas.

The developments in the area of medical electronics have allowed for improvements in the quality of life for many people. The overall objective of this event, and my personal mission, was to integrate the "technologists", which to me is synonymous with integrating the "technologies" to build the business relationships and partnerships that will lead to the next generation of new medical electronic product development. Over the past three years with CMC Interconnect Technologies, I have seen firsthand the positive impact these types of collaborations have had in making projects, programs and companies a success. CMC Management brings decades of microelectronics experience to the table and in fact enhanced our technology service offerings by adding capability with experienced staff from the medical electronics industry. There is no question a company is integrating "technologies" when it is actively integrating "technologists" into the staff. On a larger scale, we continue see the acquisition of entire companies by larger companies seeking immediate presence in an industry. As is evident from the speakers and attendees at the Medical Symposium, there are many real-life scenarios in which a technology expert, let's say a bio-scientist, is recruited into a medical electronics company for product development.

I would like to outline key factors which led to organizing the Medical symposium. For the record, the MEPTEC organization has 20+ symposium events under its belt, with the current schedule of four symposiums per year linked to a quarterly publication of the *MEPTEC Report*. Prior to this event, all of the symposiums were held in San Jose, California, the location of the ongoing MEPTEC technical luncheon meetings initiated some 25 years ago. Defined by the industry interest, the schedule and symposiums are as follows: Q1 on Thermal Management in Electronics, Q2 on MEMS Technologies, Q3 now in Phoenix on Medical Electronics and Q4 on Microelectronics Roadmaps. Having chaired prior symposiums and the ongoing chairmanship in Thermal Management, I have been involved with the unique MEPTEC symposium format in which presenting companies are specifically invited, rather than selected from a call for papers.

Selection of the topic and presenting companies allows for an organized agenda and transition of topics covering the scope of technology. The medical electronics symposium agenda offered its own challenge in selecting topics that would be good "representatives" for the background and technical capabilities in not one but three technology areas. Symposium committees are always open to feedback and suggestions on the agenda and types of topic presentations to add value.

From the standpoint of the symposium topic, Medical Electronics has been in discussion for well over a year within the MEPTEC organization and it was simply a matter of timing for it all to fall into place. With the growth of projects and programs at CMC, specifically in the medical electronics areas, it has been interesting to follow the technology trends from the companies I had been involved with previously on the computer electronics side, such as GE, Phillips, and Siemens to name a few. If Thermal Management is a "Very Hot Industry" then Medical Electronics is a "Very Healthy Industry" and one that has become mainstream with everyone from investors to the end-use general public. Recently, an elderly neighbor of mine, the one who refuses to own a cell phone or plug in the old laptop received from a grandchild, asked me for advice on purchasing a portable defibrillator that she saw in an airline magazine. For those of you in "Microelectronics", please be aware of symptoms that you are moving into mainstream medicine and bioscience: your graph on growth in China is for heart monitors - not cell phones; the DeviceLink web site is tops on your favorites; you are getting automatic FDA updates by email; more MD's than Ph.D.'s are in the business meetings, and your manager is sending you to the next MD&M 2007. There is likely a scientist somewhere right now writing an editorial for Bioscience Journal on the impact of the medical and microelectronics industries on the bioscience technology.

Medical electronics are the bridge between Microelectronics and Biosciences as they are tasked with utilizing microelectronics technology for applications in varied bioscience areas. Likely one of the best know medical electronic devices is the "pacemaker", based upon the electronic technologies, the manufacturer must also be versed in the medical biosciences to be able to properly design and manufacture a product that will function properly and under a full range of requirements. From another perspective, medical electronics related companies are well positioned to bring the computing power of microelectronics to bioscience applications. The medical imaging industry and technologies could be a symposium in itself, and again this is an excellent example, as technology has moved from a single photo x-ray to complete scans of the body in real-time and in "living color". Integration of technologies will continue to lead to advances and innovation in medical electronics, with disruptive technologies – those that will significantly enhance or completely replace existing technologies, a focus for many companies.

If you are present at the first *MEPTEC Medical Electronics Symposium* and reading this today, we hope you enjoy it. If you couldn't attend, please contact MEPTEC for a copy of the proceedings, and check the MEPTEC calendar periodically for the second annual Medical Electronics symposium in 2007! ◆

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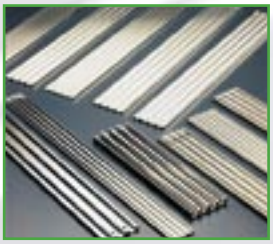
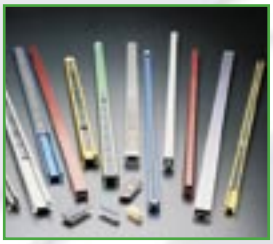
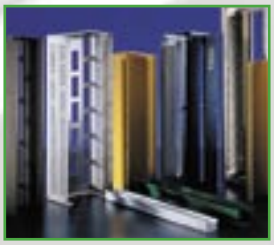
Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines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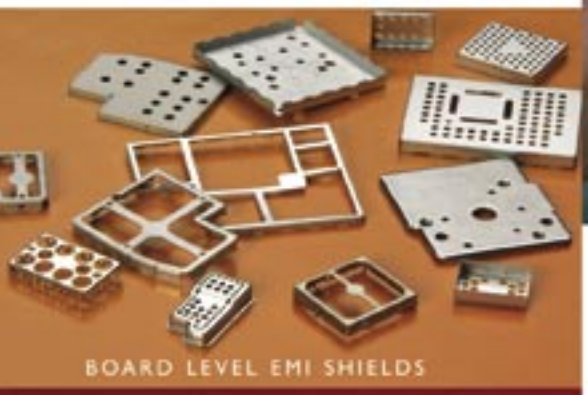

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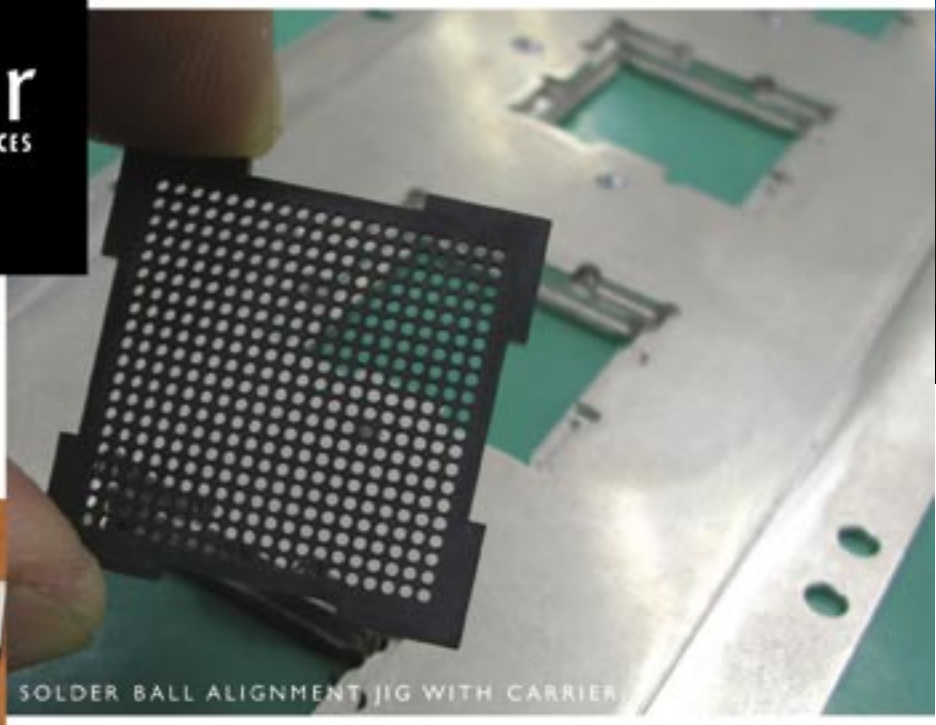

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