MEPTEC report
Volume 10, Number 4
QUARTER FOUR 2006
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

MTBSolutions

AMD has licensed Ultra-Flat Package Technology from **MTBSolutions** (MTBS). *page 14*

Kulicke & Soffa Industries, Inc. has closed the previously announced purchase of **Alphasem**, a leading supplier of die bonder equipment, from **Dover Technologies International, Inc.** *page 15*

Quik-Pak™
IC Packages, Assembly & Prototype Services

Quik-Pak, a division of **Delphon Industries**, has installed a new 200mmm Disco Automatic Wafer Dicing Saw in it's recently expanded facilities in San Diego. *page 15*

Tessera Technologies, Inc. has announced that it has signed a new wafer-level assembly technology licensing agreement with **Flextronics International Ltd.**, the world's largest manufacturer of camera modules. *page 16*

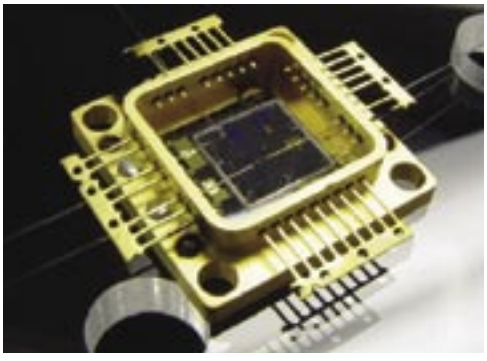
TechSearch International's new study projects a compound growth rate of more than 24 percent for combined solder flip chip and WLP between 2005 and 2010. *page 19*

CAD Design Software has released the latest version of their advanced layout tools. Version 7.5 is the culmination of extensive collaborative relationships with many industry leaders in the U.S., Japan, and Asia in the Semiconductor Packaging, Hybrid/MCM, IC Test, and RF/Microwave fields. *page 19*

IPC PRINTED CIRCUITS EXPO® SMEMA COUNCIL APEX® and the DESIGNERS SUMMIT

APEX 2007 Expo & Conference, co-located with the IPC Printed Circuits Expo, will be held February 20th-22nd at the Los Angeles Convention Center. *page 13*

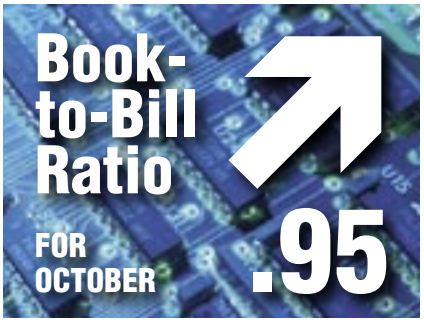
MEMBER COMPANY PROFILE



BMC provides engineering expertise and tools to assist companies in developing new products, including packaging, without having to go through the expense of production line development and equipment purchase. Through this value added component of R&D work, BMC's business model provides assurance that the new product can be assembled and tested.

Nestled in one of the most beautiful areas in the U.S. for fall foliage, one finds the high tech **Bennington Microtechnology Center** (BMC). Begun only three years ago, it boasts yearly revenue currently at approximately $2M and state-of-the-art capability from its clean rooms to its customized MEMS design and production offerings for packaging and microassembly. BMC offers U.S. industry the rare advantage of an off site prototype and low volume production facility to test new product lines, new assembly techniques, and state-of-the-art advancements at a low risk. *page 20*

Semiconductor equipment bookings increase 37% over October 2005 level. *page 18*



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Council Update

In this last issue of 2006, with much recent worldwide focus on the environment, global warning, and a looming energy crisis, we decided to take a departure from our usual packaging-related technical articles; you'll notice that one article in this issue isn't semiconductor related at all, but we felt it was important to run it. One of our member companies, **Asahi Glass**, provides electronic materials and devices, but they also develop energy and environmentally related technologies, materials and devices to, according to their website, "secure a clean environment which are crucial for sustaining growth of future generations of human society". We asked **Vern Stygar** of **Asahi Glass** to give us an update on one of their very important technologies, fuel cells. As stated in the article, "we are now looking at the exhaustion of fossil fuel oil in less than a century". That's a sobering thought. It's great to see technology advancements that are beneficial to the greater good of the society are being developed by some of "our own". We hope you enjoy reading it as much as we did.

As always, we also offer a couple of MEPTEC event follow ups. On September 21 at **Arizona State University** we held our first **Medical Electronics symposium**, with the main theme being *"Integrating Technologies"*. MEPTEC Advisory Board member **Jeff Demmin** of **Tessera**, and contributing editor to A**dvanced Packaging magazine**, gives a thorough summary of the event. Another MEPTEC Advisory Board member and Advanced Packaging editor, **Julia Goldstein**, gives a detailed synopsis of MEPTEC's November 16 *"IC Packaging and Test Roadmaps"* symposium. We appreciate their succinct reporting of all of our events. Remember, all past MEPTEC symposium proceedings are available for purchase on CD through the MEPTEC website.

We'll kick off our 2007 symposium series on February 15, 2007 at the Holiday Inn San Jose (formerly the Hyatt San Jose) in San Jose, California. We're continuing our annual *"The Heat is On"* event series on thermal management issues. We'll once again focus on issues surrounding this "hot" topic. We're pleased that **Tom Tarter** of **NeoPhotonics** will be Symposium Technical Chair, with Advisory Board member **Nick Leonardi** of **CMC Interconnect Technologies** acting as General Chair. See page 5 for information on this exciting event, and visit our website for continued program updates.

Jeff Demmin contributed further to this issue by continuing with the topic of Thermal Management in his editorial on page 34, called *"The Heat Really IS On"*. Jeff talks about the fact that thermal issues are not just a technology issue anymore, they really affect the consumer as well. We like the way he concludes his article: "You can almost use the global warming analogy – if we all do our

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part, we just might solve something". Good point!

In our Industry Analysis this issue we again turn to industry expert and MEPTEC member **Jan Vardaman** of **TechSearch International, Inc.** Jan writes about *"Flip Chip and Wafer Level Packaging: Strong Growth Ahead"*. She compares flip chip vs. wafer level packages, drivers for adoption, trends and expansion. See page 8 for this informative piece.

Our University profile and Member Company profile covered in this issue are synergetic. The **Automation & Robotics Research Institute** at the **University of Texas at Arlington** offers supporting research of packaging and design for the next generation of technical applications (see page 11). Teaming up with partner **Bennington Microtechnology Center (BMC)** in Vermont, together they offer continuous state-of-the-art design from research conceptualization through low volume production. Corporate MEPTEC member **BMC** is the brainchild of **Dr. Harry Stephanou** while he was Director of **Rensselaer Polytechnic Institute Center for Automation Technologies** and was created to fill a niche between university research and corporate application development. Seems like a match made in heaven, and we're glad to have the chance to profile them. See the BMC story on page 20.

We look forward to 2007 as we continue to bring you our high quality services which include our popular technical programs, as well as many networking and marketing opportunities.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC Welcomes New Advisory Board Member

Rich Rice
Senior Vice President of Sales, North America
ASE (U.S.) Inc.

Rich Rice is Senior Vice President of Sales for ASE (U.S.) Inc., with responsibility for the North American region. Appointed in 2003, Mr. Rice oversees field sales and engineering support teams. Prior to joining ASE, Mr. Rice spent over ten years at Amkor Technology, where he held various management roles, including Vice President of Sales and Vice President of Business Development. Previously, Mr. Rice performed engineering roles at Nara Technologies and National Semiconductor Corporation. Mr. Rice holds a BS degree in Agricultural Engineering from the University of Illinois. ◆

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Medical Electronics: Integrating Technologies

Jeffrey C. Demmin, Tessera, Inc.
MEPTEC Advisory Board Member
Contributing Editor, Advanced Packaging Magazine

Making connections – both human and electronic – were key themes throughout MEPTEC's technical symposium ***"Medical Electronics: Integrating Technologies"*** held on September 21, 2006 at Arizona State University. MEPTEC's one-day event, the first outside the San Jose area, was presented in association with the **MacroTechnology Works**, a center at **Arizona State** that focuses on transforming scientific discoveries into real applications. Symposium co-chairs **Nick Leonardi** of **CMC Interconnect** and **David Ruben** of **Medtronic** led the excellent program and lively discussions during an informative day.

The human angle on medical electronics was highlighted in the first talk, a keynote speech by **Gianfranco Zaccai** of **Continuum**, a product development and design firm. He started by noting that 48,000 deaths a year result from mistakes, including such simple human factors as people stopping taking their medicine and the stereotypical but very real problem of a pharmacist reading a doctor's handwriting. Many solutions can be found in electronics, but this can be done to enhance the personal contact that people want with their doctors, rather than replacing it. For example, a networked health monitoring systems – a "Health ATM" as he called it – would allow patients to take vital signs themselves, and a doctor could monitor the results remotely but much more often than when office appointments are needed. This increases the doctor's understanding of the patients situation, and it also frees up time for the doctor to spend meaningful time with patients, rather than consuming it with routine activities.

The first session, an industry overview chaired by **Dan Nienhauser** of **ASU's MacroTechnology Works**, included a review of outsourcing trends and some insightful information on how to work with the FDA. **Charles Wade** of **Technology Forecasters** covered the outsourcing topic, noting that outsourcing of medical electronics manufacturing is growing at 13% annually, significantly more than the 8% growth seen by the medical electronics industry as a whole. A big driver of this, according to Wade, is the unique set of needs in the medical industry, including regulatory, quality, reporting, and tracking system requirements. This led right into the next talk, *"Innovation and Consumer Protection: Working with the FDA,"* presented by **Dr. Ellen Feigal** of **The Critical Path Institute**. She reviewed some surprisingly interesting history of the FDA, including numerous success stories of unsafe products and practices that were stopped. The scope of the FDA has increased over the years, with medical devices being added in 1976, for example. Another interesting talk in this session was given by **Celeste Null** of **Intel**. She noted that there is a "perfect storm" for medical products, given the issues of an aging, increasingly overweight society. One effort that she highlighted is the **Continua Alliance**, which is working to create standards for networking sensors in the medical field.

The second session, *Industry Trends & Integration of Technologies*, focused more on some of the nuts and bolts of medical electronics. Session chair **John Crane** started his session with **Chuck Richardson** of **iNEMI** giving an overview of the roadmap process and some specifics on the medical sector portion of it. Richardson described the medical product emulator group, whose job is to devise categories of products and the associated traits and requirements. One outcome of that is a medical grade component specification project, analogous to the military grade specifications from decades ago. **Tessera**'s presentation on miniaturization followed, with a key conclusion being that miniaturization is critical for many medical products – presenter **Jeff Demmin** was one of at least four speakers to mention the "pill-cam" as an example of that. However, for some mainstream products, human interfaces and ergonomics prevent further miniaturization, while product user-friendliness requirements prevent further integration of capability that miniaturization would allow. **Randolph Leising** of **Greatbatch, Inc.** discussed the technology of power sources for implantable electronics. The need for low-power electronics was one theme that came up repeatedly during the event. In the last talk of the session, **Clinton Powell** of **Freescale** discussed the ZigBee wireless standards and its application to medical and sports biometrics.

More enabling technologies were discussed in the third session, led by **Roger Emigh** of **STATS ChipPAC**. **Ganesh Moorthy** of **MicroChip Technology** led it off with an interesting analogy showing what a heart transplant would be like if that technology had advanced as quickly as the semiconductor industry over the last 20 years. The audience agreed that it was probably a good thing that heart transplants have not followed the same path, since few of us would be comfortable with an out-patient transplant procedure that cost only $17. Moorthy highlighted low power technologies, including processing, device design, and active power management, as critical enablers. He also focused on the increasing need for connected medical devices. **Jeffrey Jordon** of **NanoDynamics** reviewed a wide range of nanotechnology with applications in the medical field. Many of these, such as silver platelets, are in the materials field. The next presentation was by **Angad Singh** of **CardioMEMS**, who reviewed many materials and design issues of a MEMS-based biomedical sensor. The final talk in that session was given by **Randall Nelson** of **ASU** on a high-throughput mass spectrometer system for protein analysis. This talk was an excellent example of the nature of the program – even if the specific topic was not pertinent to your current business, it was well-presented, interesting, and thought-provoking to anyone with an interest in medical technology.

Finally, as a good way to wrap up the day, some leading medical product companies discussed their products and technology in a session chaired by **Bruce Bowers** of **Flip Chip International**. **Thomas Burns** of **Starkey Laboratories** and **Glen**

Vaughn of **Medtronic** both gave spirited presentations about their companies' backgrounds and current technologies. An interesting tidbit from Starkey was that their business tripled when they were shown fitting President Reagan for a hearing aid. Again, the human factor is a huge influence in the medical device business. They also discussed in some detail their electronics manufacturing capability, including stacked die, flip-chip technology, and vertical interconnect. Also, and typical of larger medical device companies, they do chip design and wafer fab, as well as packaging and assembly. The medical sector is one where the uniqueness of the product and proprietary issues encourages vertical integration. Medtronic's recent packaging roadmap as related by Vaughn illustrated the proprietary nature of the field well. The packaging technology in 2000 was BGA, in 2003 it was thinned stacked die and SiP, and in 2006 it is "secret".

The feedback on MEPTEC's first medical electronics event has been very positive thus far, and the industry – another year older – should be even more interested in another installment next year. ◆

Julia Goldstein
MEPTEC Advisory Board Member
Contributing Editor,
Advanced Packaging Magazine

Do roadmaps make a difference? According to **Dr. Bill Bottoms**, keynote speaker at MEPTEC's recent ***"IC Packaging and Test Roadmaps"*** symposium and chair of the Assembly and Packaging working group of the **International Technology Roadmap for Semiconductors (ITRS)**, the answer is yes. Bottoms explained how the semiconductor industry's desire to look to the ITRS publications for guidance but try to be a step ahead continues to drive progress. The first industry roadmap for semiconductors, Moore's Law, has been driving innovation for over three decades. The "red brick wall" beyond which further device scaling is made impossible by the laws of physics has "never showed up where it should have" so far, but we have now reached a point where packaging has become the limiting element, opening up an opportunity for innovation in assembly and packaging.

Bottoms noted that while the ITRS aims to be extremely accurate in its assessment of requirements five years out, this doesn't always happen. For example, while the 2003 Assembly and Packaging chapter addressed wafer thinning, it didn't predict that 50 μm wafers would be commonplace two years later. Revisions to the tables from the 2005 ITRS will be published in December, including significant updates to wafer thinning and wafer level packaging. ITRS is also publishing a special white paper titled *"The next step in Assembly and Packaging: Systems Level Integration"* to address advances and new technology trends for SiP. Increasing digital content through SoC while diversifying non-digital content with more integrated SiP provides innovation that is "More than Moore."

Of stacked packages with multiple wire-bonded die, Bottoms said, "every time I look at that I think there's got to be a better way," such as through-silicon vias that can improve high frequency performance by eliminating the affect of each wire bond acting as an antenna. Other speakers at the symposium also mentioned through-silicon vias. The technology can enable thinner packages, which is critical as packaging houses are "fighting for every micron of thickness reduction," according to **Amkor**'s **Chris Scanlan**.

Scanlan discussed advances that are reducing package thickness: vacuum molding and compression, low loop wire bonding, film rather than paste die attach and wafer thinning. Package on package (PoP) is the fastest growing segment in 3-D packaging, and Scanlan noted that thin PoP solutions exist that can meet the height limitations for cell phones.

John Hunt of **ASE** discussed how wafer level chip scale packaging (WLCSP) is going "back to 1962," with ball drop technology replacing solder printing as the wafer bumping method of choice. As Hunt explained, it is very difficult to print sufficiently large balls on 400 μm or finer pitch. Future directions for WLCSP include more integration of passive devices, as well as applications that are not truly CSPs. With die shrinks increasing the interconnect density beyond the limits of ball pitch, semiconductor chips may be embedded in a polymer wafer, using a fan-out WLP design that allows the balls to be spread out over an area larger than the die itself.

"Emerging Trends in Electronic Test" include test functions move closer to the die itself. **Dr. Burnell West** described how advances in built-in self test (BIST) and built-on self test, where testing is done by board-mounted modules, are turning testers into merely data handling machines. Test modules within an SiP, for example, can perform boundary scans and test interaction between various devices in the SiP. West explained that for microprocessors with extremely fast clocks, the tester can't drive the circuit to maximum speed, causing test responsibility to migrate into the device. BIST can be important in WLP, where variations in device behavior across a wafer can be tracked and test limits adapted to wafer-level variation.

Kevin Fetterly of **Apria** pointed out that testers are not yet obsolete since mixed signal devices, for example, still need external test instrumentation and presumably will for some time. Fetterly discussed the work of the semiconductor test consortium toward standardizing test interfaces and software so that instruments can be integrated into multiple testers and ATE vendors do not need to create all their own instrumentation for specialty applications.

The symposium concluded with a panel discussion on supply chain management moderated by **Chip Greely** of **Qualcomm**. Panelist **Mike Coleman** of **Qualcomm** talked about their approach to reducing product lead times by holding a die bank of multipurpose die from several suppliers that can be quickly assembled when orders arrive. **Moshe Bunyan** of **STATS ChipPac** provided the SATS perspective and discussed the challenge of integrating multiple die from multiple sources into an SiP. For PoP, obtaining compatible packages for a stack is an issue.

Both Bunyan and **Dongkai Shangguan** of **Flextronics** alluded to the blurring of boundaries between SATS and EMS providers as both seek to broaden their offerings. While EMS companies are performing processes such as wafer dicing and EMS providers are assembling PCB-like SiPs, the two panelists agreed that the overlap is relatively small and is not a problem. Greely noted that it may become more of a problem in the future with the expansion of SiP.

Dan Hamling of **Teradyne** gave a perspective on managing test capacity, noting the importance of accurate modeling to optimize utilization rates. Equipment that can be reconfigured in days eliminates long lead times resulting from shifts in demand. Hamling acknowledged that open test standards will also help, but that implementing them will take years. ◆

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Flip Chip and Wafer Level Packaging: *Strong Growth Ahead*

E. Jan Vardaman
TechSearch International, Inc.

The area of flip chip and wafer level packaging is one of the most dynamic and fastest growing sectors in first level interconnect arena and has a compound growth rate of more than 28% between 2004 and 2009.

Flip Chip versus Wafer Level Packages

Wafer level packages (WLPs) are fully packaged before dicing and include bumped die that are not packaged or underfilled due to thermal stress management concerns. Typically the ball or bump is a larger diameter and has a larger pitch than found in flip chip bump applications. Often the WLP uses a preformed solder ball.

Flip chip is a first level interconnection that typically takes the form of a solder or gold bump. The bumps can be formed by a variety of methods. The flip chip device can be mounted inside a package to form a flip chip in package (FCIP) or directly on a board to form a flip chip on board (FCOB). Examples of FCIP include microprocessors for PC applications and many ASICs. When an organic substrate is used, an underfill material is typically required for mechanical reliability to control the thermal coefficient of expansion (TCE) mismatch between the silicon (TCE = 3.5) and the laminate substrate (TCE = 15-17). Table 1 compares a typical WLP with a flip chip bumped device.

Drivers for Flip Chip and WLP Adoption

The drivers for flip chip continue to be performance, on-chip power distribution, pad limited designs, and form factor requirements. High performance logic suppliers such as ASIC, field programmable gate array (FPGA), DSPs, chipset, graphics, and microprocessor makers are expanding their use of flip chip in package (FCIP). Applications such as watch modules and automotive electronics use flip chip on board (FCOB) packaging solutions. An increasing number of devices, from diodes to DRAMs, are packaged at the wafer level. WLPs are also growing in volume for a variety of low lead count (≤100 I/O) applications – including analog devices such as power amplifiers, battery management devices, controllers, memory, and integrated passives. Most of these devices are relatively small in size, and thousands can be fabricated on a single wafer. While the shift to flip chip and WLP did not materialize in high volume for DDR2 DRAM, performance requirements will necessitate a shift in interconnect methods from wire bond to bumps (flip chip or wafer level package) for DDR3. Gold bump demand continues to be dominated by LCD driver ICs, but an increasing number of gold stud bumped devices are also shipping.

Flip Chip Trends

The expansion of flip chip technology continues to spark innovation and new developments. The assembly of bumped silicon fabricated with low-k dielectric materials resulted in a host of issues requiring changes to the materials and the assembly process. New bumping technologies continue to be introduced for the flip chip market, including a process developed by IBM with Suss MicroTec equipment and new copper pillar technology. These developments were driven in part by European legislation banning lead from electronic assemblies, and some companies continue to qualify Pb-free bumping solutions despite the exemption for flip chip bumping. Legislation in Europe banning Pb and other materials deemed harmful to the environment by 2006 currently provides an exemption for high-lead flip chip bumps, however a number of companies are moving to adopt Pb-free bump compositions. Demand for 300mm bumping is expected to expand with increased production of devices on 300mm wafers.

Solder bumping prices continue to fall and are not considered an issue in the move to flip chip. Flip chip growth has been limited by organic laminate substrate shortages, longer delivery times, and high substrate prices. Normally, a price decline of 10 to 15 percent would be expected for flip chip substrates as the technology matures and volumes increase, but instead prices stayed the same or increased slightly and delivery times for some companies increased in 2005, due to increased demand by chipset and graphics makers and the decreased capacity resulting from the May 2005 ASE fire. Substrate prices are the major component in the price of

Characteristic	Flip chip	WLP
Die size (mm)	< 24 x 24	< 5 x 5
I/O count	8 to 1,000s	4 to 100
Minimum I/O pitch (µm)	> 150	400
Bump diameter (µm)	< 150	250 – 500
Bump height (µm)	100	180 – 400
Package height (mm)	0.4 – 0.75	0.5 – 1.2
Underfilled for stress relief	Yes	No
Requires high accuracy placement equipment	Yes	No
All packaging is done in wafer level format	n/a	Yes

Table 1. WLP versus Flip Chip. Source: TechSearch International, Inc., adapted from Amkor.

the flip chip PBGA assembly, representing at least 50 percent of the cost, with some estimates placing it as high as 70 percent. However, recent capacity expansions have making this less of a barrier and prices are expected to decline in 2007.

WLP Expansion

Shipments of WLPs have exceeded expectations, both in the number of units shipping and size and complexity of the devices. Once relegated to the few I/O range, wafer level packages are routinely shipping with more than 100 I/Os. They type of devices shipping in WLPs are expanding from integrated passives and analog devices, to a variety of integrated circuits including RF and memory. While many of the early parts were on 6-inch wafers, companies are migrating from 8-inch to 12-inch wafers and some are expecting to use WLPs for devices fabricated with low-k dielectrics.

Conclusions

More than two dozen companies offer flip chip assembly – both FCIP and FCOB. Almost 30 companies offer flip chip bonders or pick and place equipment, each suited for a particular application. Bump inspection systems from at least eight companies are available. Improvements in equipment for flip chip assembly have enabled the technology by allowing the user to select the equipment that provides the required trade-off in accuracy and speed.

Growth in the flip chip market continues as a result of performance and form factor drivers coupled with infrastructure developments. As the demand for greater functionality in portable products continues, the need for WLPs will increase. The future for flip chip and wafer level packaging is bright. ◆

TechSearch International, Inc., founded in 1987, is a technology licensing and consulting company specializing in microelectronics packaging and assembly technologies. Single and multi-client services encompass technology licensing, strategic planning, and market and technology analysis. Research topics include optoelectronic packaging, flip chip interconnects, CSPs, BGAs, high-density flex circuits, microvia substrates, multichip (MCP) and system in packages (SiP), and lead-free and environmentally friendly manufacturing. TechSearch International professionals have an extensive network of more than 12,000 contacts in North America, Asia, and Europe. For more information, contact TechSearch at tel: 512-372-8887, fax: 512-372-8889, or http//www.techsearchinc.com.

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About the Semico Summit

March 11-13, 2007

The Semico Summit is hosted by Semico Research, a worldwide leader in semiconductor market analysis, research, and custom consulting. This annual event, now in its tenth year, is one of the most anticipated gatherings of semiconductor industry executives and is attended by Presidents, CEOs and Vice-Presidents from across the full spectrum of the semiconductor supply chain.

The Semico Summit is characterized by a series of engaging keynote presentations followed by discussions focused on the most pressing business and technology issues facing semiconductor industry executives. The presenters are a select group of the upper echelon of executives at leading technology companies who have demonstrated vision, leadership and a track record of success.

Keynote Speakers

- **Brian Halla, CEO, National Semiconductor**
- **Wally Rhines, CEO, Mentor Graphics**
- **Chia Song Hwee, CEO, Chartered**
- **Abhi Talwalkar, CEO, LSI**
- **Dan Donabedian, Pres & CEO, Elpida Memory USA**
- **Behrooz Abdi, Sr VP & GM, QUALCOMM**
- **Shawn DuBravac, Chief Economist, Consumer Electronic Asso.**
- **Kin Wah Loh, CEO, Qimonda**
- **John East, CEO, Actel**
- **Mike Fister, CEO, Cadence**
- **Jack Harding, CEO, eSilicon**
- **Rick Cassidy, President, TSMC NA**
- **Bill McFarland, CTO, Atheros**
- **Jim Feldhan, President, Semico Research Corp.**

Topics

The Tenth Annual Semico Summit will feature keynote addresses from this list of visionaries. Each of the speakers will share their insight into the future, highlighting the challenges and opportunities that face the industry over the next few years.

The Setting

The Marriott Camelback Inn Resort and Spa has been welcoming guests to its award-winning desert hideaway for more than 60 years and is the home of the 2007 Semico Summit. It provides an excellent opportunity to relax at a world class resort while simultaneously networking with peers. A southwestern hacienda situated on 125 acres of tropical desert, the Camelback Inn also features 36 holes of championship golf, tennis, restaurants, shops and a 27,000 square foot spa.

Semiconductor Data, Analysis, Knowledge

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The Automation & Robotics Research Institute

The University of Texas at Arlington

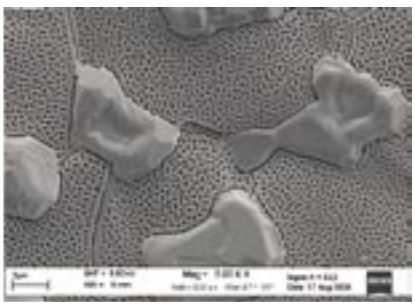
Cynthia Kalina-Kaminsky
Commercialization Manager
Automation & Robotics Research Institute
The University of Texas at Arlington

The interplay of packaging and design requires that both be developed together to gain the best supporting research for next generation technical applications. Research at the Automation & Robotics Research Institute (ARRI) does just that, and so much more. With a research staff that is familiar with the world of industry, ARRI does research with a purpose. In the miniaturization area, ARRI combines the glamorous with the practical, the packaging with the design, and the breakthrough manufacturing techniques with the breakthrough research by offering continuous state-of-the-art design from research conceptualization through low volume production with its partner, the Bennington Microtechnology Center.

What's in Your Structures?

One of the most telling areas of how packaging and design are melding is in the area of materials. Traditionally, a design is created and then packaging is thought of. This afterthought leaves almost 85% of the cost and external integration seemingly up to chance. In some cases, concurrent engineering techniques allow packaging design to begin during the device design stage. Yet the real transformational design work occurs when the device design and the packaging design are not only integrated, but when the packaging is an extension of the device and sometimes of the structure itself. This leads to one of ARRI's major research areas: structural health monitoring.

Typical structural health monitoring is used outside the surface/structural area and tries to get a glimpse of what's going on further off. Since not all critical areas are accessible by external devices, a time lag exists between an occurrence of interest and data collection, occurrences may be missed due to dependence on the predetermined monitoring intervals, and the reliance on maintenance intervals makes it difficult to assure correct and continuous operation. The first part of the solution is to embed the sensors and their accompanying packaging into the structure itself. A better first part of the solution is to embed the sensor-packaging combination into the structure where the sensing-packaging offers material characteristics important to the structural design of the device being monitored. The second part of the solution is to provide real time monitoring of the sensors, which entails the ability to assure that the sensors are integrated into the structure with communication abilities. An additional benefit, these systems provide useful information to help avoid performing unnecessary, and sometimes costly, maintenance. Impedance-based structural health monitoring techniques combined with wave propagation methodology have shown promise in detecting damage in a wide variety of structures as well as in far field communication. Impedance techniques utilize small piezoceramic (PZT) patches attached to a structure to both excite the structure with high-frequency inputs and monitor any changes in structural mechanical impedance.



SEM image of piezo material.

While these systems may cost more initially, the time and money saved over the lifetime of the system can make it more economical in the long-term. ARRI's research capitalizes on miniaturization to embed sensors into materials, to provide real time monitoring over product life, to combine systems into an assembly, to force better knowledge of systems due to reduced bandwidth and to enable monitoring of most critical design aspects.

Built ARRI Tough

Capitalizing on the state-of-the-art materials development is ARRI's research into design devices themselves, such as microsensors, micropumps, microfluidics, biomimetic devices and communication arrays. MEMS fabrication techniques are often exploited to create highly-integrated systems on a single-chip, which can be highly advantageous when integrating the sensor with other components (including other types of sensors). Examples of devices integration with sensors can include communication devices for data transmission or energy harvesting devices for powering the chip. Careful design of embedded sensors is crucial since the materials used to fabricate the sensors are often critical to the sensors' performance and can, simultaneously and significantly affect the degree to which it can be successfully incorporated into the structure with minimal adverse impact on structural integrity. For many composite materials formed under high temperatures or extreme pressures, this fundamental aspect of design is essential. Geometry must also

be considered in the cases of embedded sensors. This limits choices of sensing technologies, but can be somewhat alleviated through skilled design and by creating smaller sensors using microfabrication techniques, smaller components or other similar methods.

Keeping America Running

Another aspect of the research at ARRI-UTA is currently directed towards automated machine maintenance, condition-based maintenance (CBM) and prognostics & health management (PHM). Dynamical models for rotating machinery that include gears, bearings, and other mechanical subsystems and are aimed at detecting tooth wear as well as critical failures are being developed. Experimental measurements were used to study fault progression using statistical and system identification techniques. To monitor the condition of these machines, wireless nodes are used, including accelerometers, temperature, pressure, and strain. ARRI has developed a wireless sensor net for CBM that can be installed in 30 minutes on machinery systems, such as an HVAC room with pumps, compressors, fan motors, and piping. A laptop PC can be quickly configured to sample the sensors and compute the operating condition of each machine. Code is currently being added to allow internet-based monitoring and to send alarms on any out-of-range status to allow CBM monitoring on a PDA.

Changing American Manufacturing

Microassembly is a promising approach to creating heterogeneous microsystems modules that can easily be integrated with various joining technologies such as bonding, soldering, snap-fit assembly, and so on. The key technology in fabricating the microfluidic/microsensor platform is MEMS wafer bonding, which is currently used to create 3D wafer stacks. The main advantage of the above approaches compared to monolithic integration is the ability to integrate fabrication processes and materials that are dissimilar.

Traditionally, manufacturing is performed in a sequential manner which requires large amounts of product movement. ARRI's breakthrough manufacturing techniques utilize multiple scales of robotics, some with only one (1) centimeter of range and nanometer scale resolution, all within one manufacturing cell. The manufacturing is brought to the part instead of the parts to the manufacturing cell. This allows for 3-D manufacturing on chips, large and small assembly needs, as well as vacuum chambers for inert gas use. All of the robots are choreographed to work in a small area that keeps the part secure and in one location. The end product of the cell is a complete assembly, not just one assembly step. This eliminates the requirements for large amounts of manufacturing floor space and provides the flexibility to reprogram the cell for multiple assemblies, thus allowing small manufacturers to capture niche markets in highly knowledge intensive manufacturing environments.

Additionally, gripper-free distributed manipulation is a non-contact manipulation approach for handling of multiple small parts in micromanufacturing. ARRI researchers introduced "semi-distributed manipulation" by using two arrays of nozzles, one fixed, and one movable using shared XY actuation. The combination of pneumatic normal force and linear motion creates a friction force field that can be applied in a round-robin fashion to each of the microparts present in the field. Such a manipulation surface is referred to as an Active Surface Device (ASD). This method can provide several manipulation mechanisms depending on friction conditions, such as vibratory manipulation applied for translation, rotation and any combination of the two. The key to using this device is to generate an appropriate force field in order to displace parts from their initial position to their final configuration. The advantage of a gripper-free, distributed manipulator is its ability to handle many different delicate objects without damaging them.

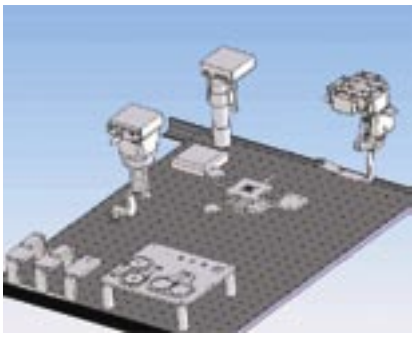


Illustration of ARRI's M3 multiscale precision robotic cell.

Close up of ASD stage with assembly parts.

ARRI has also used similar MEMS arrays in contact microassembly. The throughput of a microassembly system can be greatly increased if multiple parts are assembled in parallel. Examples of parallel manipulation are the simultaneous insertion of multiple pegs in multiple holes, or the parallel transfer and assembly of microparts from one wafer to another. Combined with the multiscale robotic cells, manufacturers enjoy the advantages of speed as well as reduced space requirements for advanced manufacturing capabilities.

A Word About Our Sponsors

Employing interdisciplinary teams, ARRI requires expertise from a wide variety of degree fields. ARRI is a part of the College of Engineering at The University of Texas at Arlington (UTA) which offers degrees in 38 areas of engineering as well as physics, chemistry, and computer science. The campus is physically located about ten miles from ARRI's research area, thus providing an easy commute for the professors who teach at UTA and research at ARRI as well as providing a bit of seclusion for the state-of-the-art research pursued by full time researchers based at ARRI.

While ARRI itself has been in existence for approximately twenty years, with the arrival two years ago of Dr. Harry Stephanou from Rensselaer Polytechnic Institute's Center for Automation Technologies where he was the director, the entire focus and research strategies were redesigned and redirected to enable state-of-the-art research in next generation high tech miniaturization to enable the creation of high worth jobs and spin out companies. ARRI collaborates with other universities around the globe as well as industry in a variety of ways. While the traditional form of breakthrough research sponsored via grant money is present, so now is the untraditional form of breakthrough research sponsored by ARRI to collaborate with emerging tech companies and highly focused industrial consortia intent on producing measurable economic development. With this type of economic impact capability, it is unlikely that the secret of ARRI will remain so for long. ◆

To see if ARRI research could help propel your company into your next generation offerings ahead of your competitors, visit ARRI's website at www.arri.uta.edu or contact ARRI's Commercialization Manager Dr. Cynthia Kalina-Kaminsky at (817) 272-5923, kaminsky@arri.uta.edu.

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Senior Project Manager
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Indium Hires Product Manager for Semiconductor Packaging Materials

Indium Corporation announced the addition of Andy Mackie as Product Manager for Semiconductor Packaging Materials. Andy is based at Indium's Global Headquarters in Clinton, NY, and reports to the Director of Solder Products.

Andy is responsible for the global marketing efforts for all of Indium's Semiconductor Packaging Materials, including solder spheres, ball attach fluxes, wafer bumping fluxes and pastes, and epoxy fluxes.

Andy has over 17 years of experience in new product development, sales, and marketing of electronics assembly and semiconductor packaging. He is an industry expert in solder paste printing, reflow, and atmosphere control in electronics assembly. He received the IPC President's Award in 2001 for his leadership in IPC's Solder Paste Task Force and the Assembly and Joining Materials Subcommittee.

Visit www.indium.com, or email askus@indium.com, for more information about Indium Corporation.

K&S Appoints Boulanger as GM of Switzerland Die Bonder Operations

FORT WASHINGTON, PA – Kulicke & Soffa Industries, Inc. has announced the appointment of Richard Boulanger as General Manager of its Die Bonder operations located in Berg, Switzerland. In this role, Mr. Boulanger will be responsible for overall manufacturing, R&D, product development and business operations for the facility, including the development of a next-generation die bonder platform and expansion into new markets throughout the world.

Mr. Boulanger has extensive experience in semiconductor assembly. Most recently, he served as Vice President of the Advanced Semiconductor Assembly Division of Universal Instruments Corporation, a business unit that provided full solutions for the precision placement of flip chips and bare die. While at Universal, he helped develop a dominant worldwide market share of the flip chip on flexible circuit for the Hard Disk Drive Industry and the emerging package-on-package assembly.

Quantum Leap Packaging Appoints David Grooms as CEO

WILMINGTON, MA – Quantum Leap Packaging, Inc. (QLP) a leading provider of high-performance electronic component packaging utilizing Quantech™ proprietary polymers, is pleased to announce the appointment of David Grooms to Chief Executive Officer.

"QLP is entering a new phase of global expansion where we need to quickly ramp volume manufacturing, develop second sources around the world, and support Sumitomo, our strategic partner in Japan," said Mike Zimmerman, Founder and CTO of Quantum Leap Packaging. "David brings years of expertise in the packaging industry, from the Sales, Marketing and Manufacturing sides. In addition, he has in-depth experience with the Japanese market, which is a core focus for us. We have made tremendous progress already against our goals of transforming semiconductor packaging, and I welcome David's leadership to help continue our momentum and accelerate our global expansion."

In his distinguished career, Grooms has held the top post at several large public and small emerging technology companies to include President of Kyocera America, Inc. and Kyocera Mexicana S.A.de C.V., both based out of San Diego, CA, where he served a twenty year tenure.

For more information please visit www.qlpkg.com.

Pac Tech USA Becomes Primary Contact for ATV Technology

Dr. Thorsten Teutsch, President of Pac Tech USA

NORTH READING, MA – After more than 12 years, the North American sales management for ATV Technology will transition from Concord Technical Sales in North Reading, Massachusetts to Pac Tech USA in the Santa Clara, California. The transition will take place at the end of 2006, with the complete sales function in place with Pac Tech beginning January 1, 2007.

The primary contact for North American Sales of ATV products will be Dr. Thorsten Teutsch of Pac Tech. He will be responsible for directing field services to the various North American regions with sales centralized at the Silicon Valley location. Pac Tech's website is www.pactech.de.

Founded in 1972 in Munich, Germany, ATV Technology, Inc., offers several specialized pieces of equipment supporting the semiconductor industry. These include an Atomic Deposition Systems that can control layer thickness on an atomic scale at low deposition temperatures. ATV's Solder Reflow Ovens are available in rack and table top versions. Their Programmable Process Furnaces provide precision controlled temperatures and clean atmosphere. The Micromanipulator System is a versatile piece that lends itself to a wide range of applications in microelectronics. Visit www.atv-tech.com for more information about ATV.

AMD Licenses MTBSolutions Ultra-Flat Package Technology

SAN JOSE, CA – AMD has licensed Ultra-Flat Package Technology from MTBSolutions (MTBS). "The MTBSolutions Ultra-Flat Package Technology is a potentially enabling technology for technology requirements that include multi-core chip size, high performance, thermal requirements, and high bandwidth I/O that require scalable solutions" said Raj N. Master, AMD Senior Fellow and flip-chip packaging expert.

The Ultra-Flat Package Technology is believed to be both a technical enabler and may also be a cost enabler. It is primarily utilized for large scale flip chip packaging structures where package flatness and the corresponding stress transmitted to the Si chip is of concern.

The Ultra-Flat Package Technology was developed for FC-BGA where the CTE dissimilarities between the silicon chip and the organic substrate result in a package warpage inducing undue stress upon the FC interconnect structure. The technology is designed to:

- Reduce package warpage by 50% over current processes
- Improve flip chip interconnect reliability by a factor of 2X
- Reduce low-K ILD cracking in the silicon chip

Ultra-Flat Package Technology is a series of patents that include both processing and design methodologies designed to reduce stress between the organic package and the silicon die which can be detrimental to the reliability of the flip chip interconnect joint and the silicon chip's inner layer low-K dielectric.

For more information about MTBSolutions visit their website at www.mtbsolutions.com.

Winslow Automation, Inc. Celebrates 20 Years in Business

MILPITAS, CA – Winslow Automation, Inc., an industry leader in lead finish technology equipment and consumables, is celebrating its 20 year anniversary. Soldering technology equipment includes both table top and a freestanding robotic lead tinning machine known as the FlexLine®. Winslow Automation, Inc.'s SolderQuik® Ball Grid Array (BGA) Preform is an economical consumable product which provides a unique BGA reballing solution that eliminates the need for stencils, loose solder balls, and solder paste in the reballing process. In 1998, SolderQuik® was recognized by Surface Mount Technology magazine as a Vision Award Rework and Repair Product of the Year.

As the need for subcontract services grew and outpaced the demand for new equipment, Winslow Automation expanded its operations to include a service division known as S·I·X S·I·G·M·A. Utilizing its own FlexLine® equipment to hot solder dip millions of components annually, S·I·X S·I·G·M·A has become and remains the premier lead finish subcontractor. In 2001, S·I·X S·I·G·M·A, was the recipient of the Advanced Packaging Award for its column attach services technology for ruggedizing COTS components.

For additional information on products and services, call at (408) 262-9004 or visit www.winslowautomation.com

Palomar Receives ISO 9001:2000 Recertification

CARLSBAD, CA – Palomar Technologies, leader in precision automation equipment and process development for microelectronic assembly, announced that it has been recertified as meeting the requirements of ISO 9001/ANSI-ASQ Q9001:2000 and is registered by SGS. Palomar was assessed and certified as meeting the requirements of ISO 9001:2000 for design, manufacturing, sales, servicing, and marketing of automated assembly equipment serving the communications, microwave & RF, semiconductor, optoelectronic, wireless, disk drive, automotive, aerospace & defense, and medical industries.

For more information visit Palomar Technologies website at www.PalomarTechnologies.com or call 760-931-3600.

Kulicke & Soffa Purchases Alphasem

FORT WASHINGTON, PA – Kulicke & Soffa Industries, Inc. closed the previously announced purchase of Alphasem, a leading supplier of die bonder equipment, from Dover Technologies International, Inc., a subsidiary of Dover Corporation. The purchase price was $27.1 million in cash, after a working capital adjustment and subject to further post closing adjustments.

Scott Kulicke, K&S chairman and chief executive officer, commented on the acquisition, "We had identified die bonding equipment as a natural growth path for K&S. The Alphasem purchase is the most attractive way for us to enter that market. Alphasem has good position in the die bonder market, serving a wide range of applications. Their line of products fulfills the market needs for leading edge technology and cost efficient solutions across a variety of package types."

Alphasem is a leading supplier of die bonder equipment. According to the most recent VLSI Research market data report, Alphasem held a 10% share of the $520 million die bonder market in calendar year 2005. Alphasem generated sales of approximately $60 million in calendar 2005 for die bonders, related materials, and services, with 260 employees.

For more information visit the Kulicke & Soffa website at www.kns.com.

Pac Tech Opens New Asian Facility

NAUEN, GERMANY – Pac Tech GmbH, announced the incorporation of Pac Tech Asia, a wholly owned subsidiary of Pac Tech GmbH, and the acquisition of a new 53,512 square foot facility located in Penang, Malaysia. The new facility will provide state-of-the-art wafer bumping and backend processing for semiconductor companies within the Pacific Rim. The building will have up to 40,000 square feet of remodeled production floor space, including cleanroom area. Both will be equipped with the latest generation equipment.

The new Malaysian facility is designed and laid-out to accommodate mass-production. In the initial phase of operation, it will be capable of handling up to 600,000 wafers per year. Pac Tech Asia will provide a variety of special applications designed to enhance and support the Asian semiconductor manufacturing community.

The facility is scheduled to begin operation in June 2007, and is currently accepting process qualification orders.

For more information visit the Pac Tech website at www.pactech.de.

DuPont Signs Joint Development Agreement with Taiyo Ink

RTP, NC – DuPont Electronic Technologies announced it has signed a joint development agreement with Taiyo Ink Manufacturing Company, Ltd. to advance the development of buildup microvia dry films for use in advanced flip chip ball grid array packages for the semiconductor industry. By combining their interests, expertise and technologies, the companies expect to find new ways to meet the growing demand for higher density circuits with superior interconnect reliability. The early target is a material offering with a low coefficient of thermal expansion (CTE), superior adhesion, improved signal integrity and speed.

"Close collaboration and material integration are critical to meeting our customers' needs in the semiconductor industry, and key components of our strategy to expand the DuPont offering in this fast growing area of the market," said David B. Miller, vice president and general manager, DuPont Electronic Technologies. "Combining Taiyo Ink's proprietary resin technology and expertise with DuPont's filler, surface treatments and dispersion technologies will result in some exciting new products available for OEM qualification by early next year.

For more information on DuPont Electronic Technologies, please visit electronics.dupont.com.

Quik-Pak Installs Wafer Dicing Saw

SAN DIEGO, CA – Quik-Pak, a division of Delphon Industries, has announced the installation of a new 200mmm Disco Automatic Wafer Dicing Saw in it's recently expanded facilities in San Diego. The new in-house capability complements

Quik-Pak's existing rapid turn IC assembly service offerings, which include die bonding, gold ball wire bonding, remolding and marking/branding. Quik-Pak is also the largest supplier of open cavity plastic packages, which allow IC designers to insert new die in existing production packages for design verification, testing and customer samples.

The new dicing service can either be utilized as part of Quik-Pak's turn-key packaging and assembly process for fabless semiconductor companies or as a stand-alone service for customers with internal assembly capability.

For further information, contact Quik-Pak at (858) 674-4676, moreinfo@icproto.com.

Flextronics Licenses Tessera's New Wafer-Level Assembly Technology for Image Sensors

SAN JOSE, CA – Tessera Technologies, Inc., a leading provider of miniaturization technologies for the electronics industry, announced it has signed a new wafer-level assembly technology licensing agreement with Flextronics International Ltd., a leading electronics manufacturing services (EMS) provider and the world's largest manufacturer of camera modules. Under the terms of the agreement, Flextronics has access to Tessera's SHELLCASE® CF technology for use across the company's entire camera module line. Introduced in July 2006, SHELLCASE CF is a wafer-level technology that utilizes the manufacturing infrastructure of conventional Chip-on-Board (COB) assembly processes, while resolving the challenges associated with increasing resolution and decreasing pixel size in image sensors. This wafer-level assembly technology is used to assemble optical components integrated into electronic products such as miniaturized cameras in camera phones, digital still cameras and video camcorders.

The newest addition to Tessera's SHELLCASE wafer-level technology family, SHELLCASE CF is ideally suited for CMOS and CCD image sensors used in consumer electronics devices, such as camera phones and digital still cameras. Using a novel encapsulation process, SHELLCASE CF protects the image sensor's active area from contamination from the initial stage of processing and also provides manufacturers the flexibility to perform optical testing at the most favorable point of the assembly flow, as defined by their specific requirements and manufacturing environment. SHELLCASE CF utilizes existing wire-bond assembly infrastructure and processes, minimizing the hurdles to rapid adoption. This helps to ensure high module assembly yields and significant reductions in overall cost.

Visit www.tessera.com for more information.

Osram Selects SUSS Photolithography Solution for Manufacturing of HB-LEDs

MUNICH, GERMANY – SUSS MicroTec continues to prove its dedication to the advancement of the Opto-Semiconductor market. In both the second and third quarter of 2006 Osram Opto Semiconductors, one of the leading suppliers of innovative lighting solutions, placed additional follow-on orders for SUSS LithoFab200 Clusters, which are specifically used in volume production for the manufacturing of High Brightness/ High Power Light Emitting Diodes (LED).

The SUSS LithoFab200 cluster system consists of coat, bake, align, expose and develop cells and has been selected for its superior ability to safely handle fragile substrates as well as for its high productivity and for its high yield at lowest possible cycle times. A new concept of the exposure cell based on the MA200Compact Mask Aligner further optimizes alignment accuracy, thereby widening the process window for a variety of applications. The novel SUSS DirectAlign option allows for an alignment accuracy down to 0.5 micron (3 sigma), the highest performance available for a mask aligner today.

For more information, contact Brigitte Wehrmann, Marketing Communications Manager Lithography Division at Tel: +49 (0)89 32007 237, Email: brigitte.wehrmann@suss.com.

Integrated Sensing Systems (ISSYS) Selects AML Wafer Bonder from OAI for Production

SAN JOSE, CA – ISSYS, a world leader in the manufacture of MEMS devices, has announced the purchase and installation of the AML Bonder from OAI. OAI is a leading manufacturer of precision UV Lithography Equipment for MEMS, Semiconductors, Microfluidics and other emerging markets. In response to increasing customer demand, ISSYS is expanding its production capabilities by purchasing from OAI both its stand-alone wafer bonder and advanced mask aligner system.

The AML bonder is a semi automatic, stand-alone, computer controlled, substrate bonder. It features a rigid vacuum pressure chamber, upper and lower independent heaters, superior post alignment accuracy, and a twin camera system with through-the-lens illumination. With a small foot print, fast throughput, budget friendly pricing and flexible platform, the AML bonder is unique in its versatility to be used with any manufacturer's mask aligner.

OAI is located in the heart of Silicon Valley. It designs and

manufactures standard and specialized precision mask aligners, UV Exposure Systems and custom-engineered systems for over 30 years. Go to www.oainet.com for more information. For more about ISSYS visit www.mems-issys.com.

Asymtek's PreciseCoat Jet Delivers Conformal Coating into Tight Spaces

CARLSBAD, CA – Asymtek, leader in dispensing technology and pioneer in jetting technology, introduces the SC-400 PreciseCoat™ Conformal Coating Jet for applying coating materials to highly selective areas, especially on small substrates or substrates with high-component density where there are tight tolerances between coated and uncoated areas. With PreciseCoat jetting, the need for masking is virtually eliminated because delivery of the coating is so accurately controlled.

Using a needle design with non-contact jetting action and fast pulse-width modulated control, the SC-400 jet delivers conformal coating to areas not accessible by other applicators. Small volumes and precision control of the conformal coating material enable line widths down to 1.2 millimeters (0.05 inch) wide. Film thicknesses of 15 micrometers are achievable when using solvent-based materials. Acrylics, silicones, urethanes, UV-cure, and water-based materials with a viscosity range of 1 to 850 centipoise (cps) can be jetted.

For more information visit www.asymtek.com.

Indium Expands Sales Efforts in France with New Distributor

Indium Corporation announced an expansion of its sales efforts in France with the addition of Accelonix Group, its newest distributor. Accelonix is responsible for selling Indium Corporation's extensive line of Semiconductor Packaging Assembly Materials, Engineered Solders, and Materials for Wafer and Chip Bumping, as well as Solder Pastes, Fluxes, Cored Wire, and Underfills for non-PCB assembly.

Accelonix Group is located in France and has been introducing, selling, and supporting products in the French electronics market since 1984. Their expertise and high-performance technical team have given them the essential support and service strengths required by today's electronics assembly industry.

Indium Corporation is a four-time Frost & Sullivan Award-winning supplier of electronics assembly materials, including solder pastes, solder preforms, fluxes, Pb-Free solder alloys, underfill materials, die-attach materials, and more. Factories are located in the US, United Kingdom, Singapore, and China. Founded in 1934, the company is ISO 9001 registered.

For further information about Indium Corporation visit www.indium.com or email askus@indium.com.

DuPont MCM Celebrates 10 Year Anniversary at EMDD China

DONGGUAN, CHINA – DuPont Microcircuit Materials (MCM), part of DuPont Electronic Technologies, recently celebrated its 10th year of successful operations at the Electronic Materials DuPont Dongguan Ltd. (EMDD) facility in Dongguan, China. DuPont was the first multinational company to establish a production facility for thick film microcircuit materials in China. Since its start-up in 1996, EMDD has been serving the rapidly growing China domestic electronics market for products that support such industries as telecommunications, automotive electronics, passive components, and pho-

tovoltaics. DuPont hosted a special event to mark the occasion with key customers, DuPont local employees and leadership team members.

Since the late 1990s DuPont has expanded the EMDD facility's output by 300 percent, and plans to nearly double production capability again within the next two years, as exports increase to MCM customers globally. The local technical service facility at EMDD is also growing to better support the increasing local customer demands particularly from photovoltaic and passive components industries.

For more information on DuPont Microcircuit Materials visit mcm.dupont.com.

New Kulicke & Soffa Copper Capillary Ensures Greater 2nd Bond Quality for More Stable Mass Production

FORT WASHINGTON, PA – Expanding upon the capabilities of its highly successful copper capillary called CuPRA, Kulicke & Soffa Industries, Inc. has developed the CuPRAplus™ that supports highly consistent and stable fine wire 2nd bonds, while maintaining the quality of the overall wire bonding process. By ensuring both 1st and 2nd bond quality during fine copper wire bonding, the CuPRAplus Copper Capillary offers a more stable mass production process.

CuPRAplus Copper Capillary works together with K&S' iCu Copper wire and bonder kit to provide a complete solution for manufacturers looking

North American Semiconductor Equipment Industry Posts October 2006 Book-To-Bill Ratio of 0.95

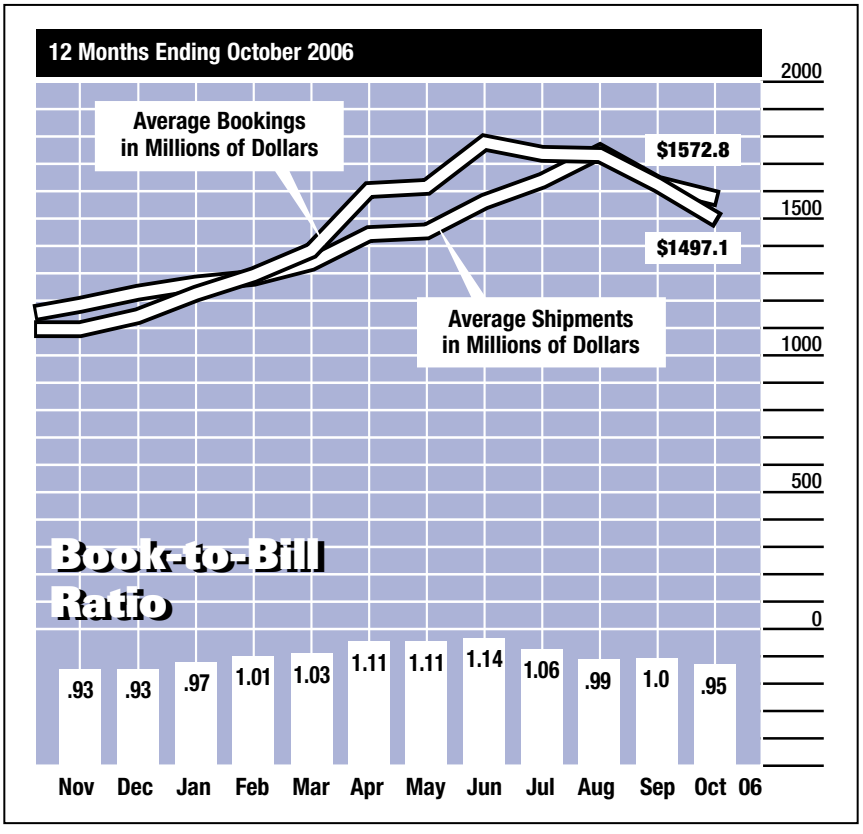
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.5 billion in orders in October on a three-month average basis, and a book-to-bill ratio of 0.95, according to the latest book-to-bill report published by trade group Semiconductor Equipment and Materials International (SEMI).

A book-to-bill of 0.95 means that $95 worth of orders were received for every $100 of product billed for the month. The $1.5 billion bookings figure is almost 9 percent below the final September level of $1.64 billion, and 37 percent above the $1.09 billion in orders posted in October 2005.

The three-month average of worldwide billings in October 2006 was $1.57 billion. The billings figure is 6 percent below the final September level of $1.67 billion, and over 37 percent higher than the October 2005 billings level of $1.15 billion.

"Total orders for semiconductor equipment have declined from the peak levels posted back in June of this year, though they are significantly higher than levels reported one year ago," Stanley Myers, president and CEO of SEMI, said in a statement. "There has been a gradual decline over the past three months, as the industry absorbs new capacity."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



to take advantage of the cost advantages offered by copper wire. While K&S' original CuPRA capillary offered superior bonding performance comparable to gold bonds on various pad materials, the CuPRAplus takes fine copper wire bonding a step forward by ensuring both a quality 1st and 2nd bond for superior process control and productivity.

Visit the K&S website at www.kns.com for more information.

SHELLCASE RT Delivers High Yield and Reliability in a Miniaturized Wafer Level Package

SAN JOSE, CA – Tessera Technologies, Inc. announced SHELLCASE® RT, one of the world's thinnest, wafer-level chip size packaging (WLCSP) technologies developed to provide key benefits to OEMs and others developing advanced electronics which integrate cameras.

Built upon Tessera's foundational wafer-level encapsulation technology, SHELLCASE RT delivers high yields by protecting image sensors and other optical devices from contamination from the initial stage of packaging. In addition, the platform's enhanced reliability is engineered to open up new market opportunities, such as the use of cameras in harsh environments, including automotive electronics. As one of the thinnest WLCSPs available on the market today (at approx. 500microns), SHELLCASE RT also enables very low profile camera modules, providing OEMs greater design flexibility and a powerful tool in developing thinner portable electronics.

SHELLCASE RT is a member of Tessera's industry-leading SHELLCASE® technology family and leverages Tessera's established SHELLCASE® OP and SHELLCASE® OC technologies. According to analyst firm Prismark, in 2006, approximately 225 million image sensors will be packaged in Tessera's SHELLCASE technology, representing an approximate increase of 96% over 2005.

Tessera is currently licensing this technology to interested parties. In addition, Tessera is offering related services, such as technology transfer and training. Prototype samples for evaluation are available. For additional information, please go to www.tessera.com.

TechSearch Intl Study Shows Flip Chip and WLPs Expanding in a Wide Range of Devices

TechSearch International's new study, *Flip Chip and WLP: 2006 Market Update and Technology Developments*, projects a compound growth rate of more than 24 percent for combined solder flip chip and WLP between 2005 and 2010. The report profiles drivers for the demand for gold and solder bumping, as well as for wafer level packaging.

The drivers for flip chip continue to be performance and form factor. Flip chip interconnect is expanding into many device types, ranging from high performance logic to a variety of devices found in wireless products. An increasing number of suppliers of ASICs, field programmable gate arrays (FPGAs), DSPs, chipsets, graphics, and microprocessors are expanding their use of flip chip in package (FCIP).

WLPs have typically been used for low pin count (≤50 I/O) applications, including analog devices such as power amplifiers, battery management devices, MOSFETs, image sensors, controllers, memory, and integrated passives. However, many companies plan to use WLPs for higher pin count applications (≥100 I/O), including analog parts with larger die sizes.

The report provides an updated forecast for the flip chip wafer bumping market by product application, device type, FCIP/FCOB split, number of wafers, and number of die. Also included in this report are projected demand and capacity (merchant and captive), presented by the number of wafers and by bump type. Geographic changes in the location of bumping supply are analyzed. WLP demand is projected by number of die, number of wafers, and device type. Capacity is projected in number of wafers. Bumping, wafer level packaging, and contract assembly service providers are highlighted in terms of capability and experience. Contacts for these companies as well as suppliers of laminate substrates, bonding equipment, and inspection systems are provided.

For more information visit www.techsearchinc.com or call 512-372-8887.

Ultra-Soft Thermal Gap Filler Cools and Protects Hot PCB Components

MAHWAH, NJ – MH&W International has introduced Softtherm® 86/200 material for providing an ultra-soft, thermally conductive gap filling interface between hot PCB components and their heat spreaders. The material can blanket over multiple components of differing height, contours, and planarity. It is especially useful on fragile components sensitive to high pressure, or when only very low mounting pressure is available for attaching a heat spreading device.

Softtherm 86/200 material features a highly elastic, structurally secure silicone filled with ceramic particles. Unlike many gap fillers, it retains its memory after compression which enables the material to be reused. Thermal resistance is just 1.50 K/W, and thermal conductivity is 1.0 W/mK. Gap filler parts made from 86-200 material have strong wet-out and air gap-filling properties. 86/200 is UL rated 94V-0 and has a TML (total mass loss) under 0.40%. It can be used in application temperatures from -60 to 200°C.

MH&W's family of Softtherm gap filler materials provides a wide range of cost-performance choices for different cooling needs. Complete information is available at www.mhw-thermal.com.

CDS Announces the Release of Version 7.5

SAN JOSE, CA – CAD Design Software announces the release of the latest version of their advanced layout tools. Version 7.5 is the culmination of extensive collaborative relationships with many industry leaders in the U.S., Japan, and Asia in the Semiconductor Packaging, Hybrid/MCM, IC Test, and RF/Microwave fields.

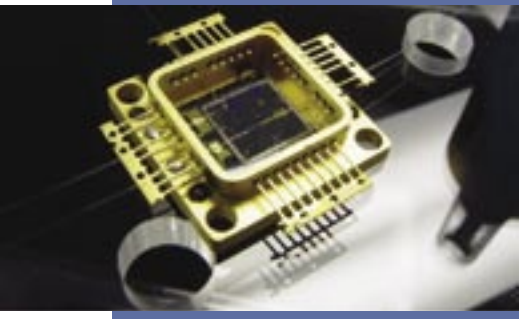
More robust, sophisticated algorithms and new data optimization result in faster processing, and new customer-requested functions improve overall time-to-market, and verifiably improve yields.

CAD Design Software's Version 7.5 is unsurpassed in features, functions, and most of all, flexibility. CAD Design Software leads the EDA industry with the most rapid development and implementation of new tools for emerging high-end new technologies for its customers. This has resulted in many industry firsts, including Stacked Die, 3D design, automated IC package routing, co-development and design-for-manufacture (DFM) platforms.

For more information on CAD Design Software and Version 7.5 call 877-CAD-USER (223-8737), visit the CDS website at www.cad-design.com, or e-mail sales@cad-design.com.◆

μ bennington microtechnology center

Nestled in one of the ten most beautiful areas in the U.S. for fall foliage, one finds the high tech Bennington Microtechnology Center (BMC). Begun only three years ago, it boasts yearly revenue currently at approximately $2M and state-of-the-art capability from its clean rooms to its customized MEMS design and production offerings for packaging and microassembly. BMC offers U.S. industry the rare advantage of an off site prototype and low volume production facility to test new product lines, new assembly techniques, and state-of-the-art advancements in a low risk manner.



Assembled package with fibers.

Helping Make Industry More Competitive

Without having to go through the expense of production line development and equipment purchase, BMC provides engineering expertise and tools to assist companies in developing new products, including packaging, and then testing their viability. Through this value added component of corporate R&D work, BMC's business model provides assurance that the new product can be assembled and tested. Two other economic development activities are embedded: 1) once the design/packaging/assembly and test procedures/equipment have been developed for the product and proven to produce additional profit for the company, BMC makes available the customized procedures and equipment to the company for use in its own factories, or 2) if outsourced production and testing is desired and production requirements support it, BMC can spin off a specialized company to support the sponsor's low volume production and test needs. This model allows not only lower risk product development and manufacturing, but also helps protect the IP from global competitors, thus providing first market mover advantages.

Helping You Increase Your Competitiveness

To get first mover advantage, customers rely on BMC's expertise and equipment offerings. BMC's 12,000 sq. ft. state-of-the-art facility includes: approximately 3,000 sq. ft of certified class 10,000 clean room which in turn includes approximately 600 sq. ft. of clean room area that is reconfigurable to class 1000, a Norcom Optical Leak Tester – only about 40 exist globally, Motoman Robotworld automated microassembly ability, a Wyko Optical Profiler with DMEMS so that one can watch the device being tested as measurements of performance are taken so as to assure operations meet specifications, and a Laurier M9 Flip Chip Bonder to allow stacked chip assembly with solder, epoxy or UV cure. While equipment is important, employee expertise is crucial. Key employees cumulatively have significant experience, thus offering easier integration between corporate R&D areas and BMC's prototype/low volume operations. Engineering skills are available for design of packaging, manufacturing procedures, and in special cases, fully customized manufacturing production lines to be transferred to the customer. Once the designs are ready, customers may choose to ship parts into BMC or have BMC control the parts coming into the assembly area, the second method having proven to produce higher production yields.

Since the MEMS market is fragmented, it is imperative that the prototype and low volume portion of the value chain accommodate all industries for a multitude of applications. Packaging for chemical sensors and opto-mechanical needs are just a few of the applications BMC handles for any industry. Design work is customized to the customer's application needs.

Enhancing the design is BMC's unique production procedure of providing testing after each critical step of assembly. By testing on site (testing which includes mil spec capability for leaks, shear strength, and bond strength as well as hermeticity, wire bond pull strength and optics) potential compo-

BMC – M3 (Macro – Meso – Micro) Assembly System

This versatile assemble system is based on the Motoman's Robotworld platform. It features multiple overhead robotic systems that operate on a layer of air that carry various tools such as vision systems, pneumatic, servo, and vacuum grippers for pick and place of components, lasers, and epoxy dispensing equipment. The system also features micro and nano scale stages for precision alignment of small components such as MEMS dies, fibers, and lenses. Supervisory control of the system is performed by National Instruments Labview. Small to medium scale production can be accomplished.

Norcom – Optical Leak Detector

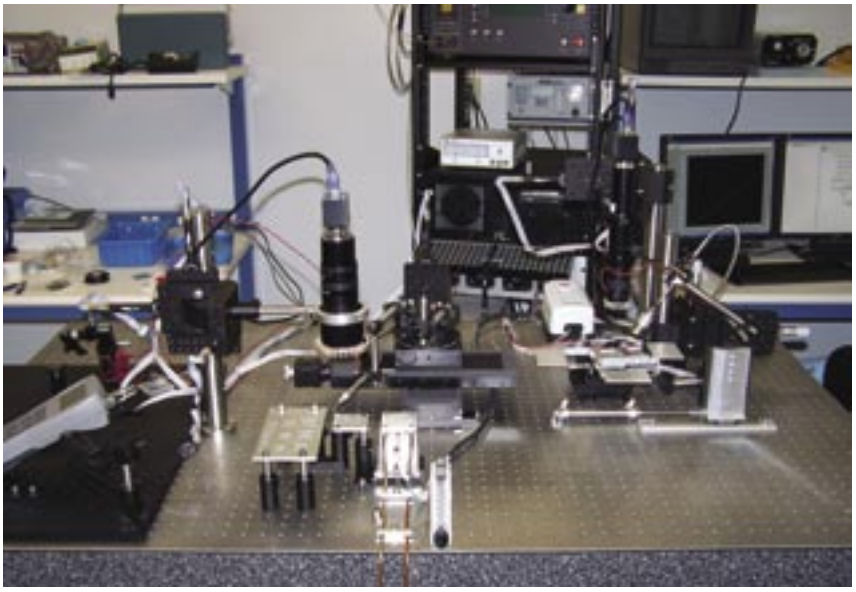
The 2020 single footprint (SF) optical leak test system for hybrid, MEMS, and optoelectronic packages automates leak testing of hermetic electronic packages. The 2020 SF provides simultaneous, full-matrix gross and fine leak testing on up to 200 hermetic devices. Using digital holography, the system measures small changes in package stiffness and leak results as the packages are placed into a helium pressure cell. Optical leak testing is said to exceed conventional helium mass spectroscopy and fluorocarbon bubble testing in repeatability, accuracy, and direct measurement of leak rates (cc-atm/sec. helium).

nent damage is avoided from having to ship to outside test facilities. It also allows BMC to assure tighter control of the manufacturing process. By inserting testing at critical assembly points, changes can be made during the process instead of waiting until the product is fully assembled and then scraping non-conforming parts. This in turn provides a cost advantage to BMC's customers since low yield and high scrap are wasted expense.

So with an emphasis on high yield, low scrap prototype/low volume production, how long does it take to create a viable design? Since each MEMS design is different, packaging design as well as production process design and possible equipment design times vary with complexity. Simple chip packaging with hermetic sealing designs usually are completed in a week's time while more advanced designs, including those requiring development of new technologies through the Automation & Robotics Research Institute (ARRI) arm at The University of Texas at Arlington, take longer. The ability to reach back into the research area allows companies to develop next generation products based on breakthrough technologies developed by ARRI's world class researchers. ARRI's new technology platform development consists of the integration of not only

Semi-Automated Assembly System

This system is a rapid proto-typing station and is used to determine process parameters and produce 1 of a kind devices. The system contains 19 degrees freedom of movement using micro and nano stages, multiple vision systems, global and local heat sources, and a variety of fixtures. Supervisory control of the system is performed by National Instruments Labview.



materials, micro/nanoassembly, and MEMS design, but also the integration of commercial requirements that are then implemented for the customer at BMC.

The benefits of this unique combination are shown in the following example. The packaging shown above was developed for a large customer who required packaging that contained chemical sensors, was hermetically sealed, had a guaranteed shelf life of over 30 years in harsh thermal and environmental conditions – even if the first operation was past the 30 year mark, and utilized precision fiber alignment at the micrometer level. The technologies required to meet the customer's demands were unavailable, so, ARRI developed them knowing that everything had to be easily transferable to BMC for production. Since the development process was integrated with BMC throughout the project, transition and production missteps were avoided and the customer is now being served. This process took approximately one year from the beginning of the research work to production capability.

History

Begun as the brainchild of Dr. Harry Stephanou while he was the Director of Rensselaer Polytechnic Institute Center for Automation Technologies, BMC was created to fill the unique niche between university research and corporate application development. The belief was that by eliminating expensive prototype equipment purchases and production disruptions, collaboration with BMC would allow industry to more quickly adopt new technologies into product design work. This is proving to be the case.

The location of BMC in Vermont was made possible thanks to the sponsorship of Senator Patrick Leahy. So as to stimulate measurable economic development, one of BMC's main objectives was to ramp up to speed and become independent of all support through commercial success. To do this, unique management was required. Management that understood the needs of industry and could avoid the common pitfalls of a growing, small business.

Since BMC's operations allow large companies to become more entrepreneurial and small companies to become more competitive, someone with an entrepreneur's outlook was needed. Hired in July 2006, Executive Director Henry Klim is providing just the right combination of large corporate knowledge (Boeing Aerospace and Digital Equipment Corporation) as well as competitive flexibility common to successful repeat entrepreneurs (founder MST Systems Technology, founder/President of Electronic Test Engineering Company, and founder/President of Eteck Inc.) The combined efforts of Mr. Klim and Dr. Stephanou, who is now the Director of ARRI, offer industry the unique chance to lessen risk while introducing break through technologies to the market.

Unbeatable Parallel Processing with BMC

Working with BMC is possible in many ways. First, a quick call to Mr. Klim at (802) 753-1901 or an email to henry@benningtonmicro.org will start the process, but he asks all potential customers to skip the formalities and call him Henry. Information can be found on the website at www.benningtonmicro.org. A BMC representative can come to your location or, even better, you can let BMC do the work while your company takes a break from the fast paced, sometimes frenetic world of industry by dropping off the negotiated design work, driving the hour and a half to one of the Vermont's beautiful ski resorts, and then receiving the completed design work at the end of your corporate retreat.

BMC looks forward to working with you and to helping provide you with the competitive advantage your company deserves. ◆

(Please see page 3 for an introduction to this article.)

Fuel Cells: The Next Big Technology Wave

Vern Stygar
Product Manager
Asahi Glass Electronic Materials

Where Are We Now?

It has been said that Sam Morey is credited with building the first self propelled vehicle, utilizing an internal combustion engine and a buckboard, in 1826. The story goes, that upon start up, the vehicle lurched forward without him and crashed into a barn across the street. The true car appeared in 1885 when Karl Friedrich Benz came out with first practical car. The car has truly transformed the way we work, socialize and has become an integral part of our lives.

Oil Driven Economy

For more that 150 years, the world was looking for the next model, faster, smoother and more comfortable. Now, the storm clouds have begun to darken our horizon. We are now looking at the exhaustion of our fossil fuel oil in less than a century. According to International Energy Outlook 2006, we currently use 81 million barrels of Fossil fuel oil per day worldwide. Half of this usage is to support transportation. Consider a world without cars. Not just cars, but pharmaceuticals, plastics, and chemicals. Whether we have 30, 60 or 100 years, the fact is that it is not too far in the future; the world will begin to exhaust its source of fossil fuel oil. Currently Energy Information Administration (EIA) released the report on the total World Proven Reserves for Oil which states, that there is approximately 1,292 billion barrels still in the ground. (See table 1.) Based on the 81 million barrels per day we have approximately 31-35 years left of oil.

The thirst for energy is relentless. The world energy consumption will continue to grow at nearly 1.4% per year. Not surprisingly, United States and China will consume the lion's share.

Region	Proved Oil Reserves (Billions of Barrels)
Western Hemisphere	317
Western Europe	16.4
Asia - Pacific	35
Eastern Europe	123
Middle East	743
Africa	102
Total World	1,293

Table 1. Worldwide oil reserves as of January 2006. Source: Energy Information administration, 2006

Type	Description
Phosphoric Acid (PA-FC)	Have been used in applications not sensitive to cost. Electrical generating cost is in the $3500-4000/kW range. Per year production is 40 MW per year, mostly in Canada and US. Additional declines in pricing are not expected due to the limitations of power density.
Alkaline (A-FC)	This type of fuel cell has been proven very reliable in space borne applications for more than 35 years. Electrical generating cost $3000/kW Per year production is 10 MW per year in Germany with prototypes being planned in US and Russia. Alkaline fuel cells suffer from low power density and sensitivity to carbon dioxide.
Proton Exchange Membrane (PEM-FC)	Presently the lead technology for attainment of commercial viability. Conversion efficiencies of 24-40% which have led to installed stationary cost of $4000-10,000/kW. Pricing is expected to drop to $650-1500/kW with further improvement in efficiencies and manufacturing processes by 2008. Per year production is 20 MW per year in US/Canada/Japan. A doubling of this production is expected in the next several years as APU's for the vehicle industry.
Molten Carbonate (MC-FC)	Highest conversion efficiency at 55%. Current cost estimated is $8000/kW. With further improvements in efficiency and manufacturing techniques, costs can be reduced to $1000-1900/kW. Current product capacity is 10 MW in the US & Canada.
Solid Oxide (SO-FC)	SOFC's are achieving 47% conversion efficiencies with planned efficiencies of 67%. Production cost remains problematic and hovers in the $10,000/kW range. With high volume manufacturing, cost is expected to drop to $800-1500/kW.
FC/Turbine Hybrids	Combining conventional technology such as turbines and fuel cells can attain efficiencies of 57-60% with a production cost of $6,000/kw. With continuing improvements, production cost of $1000-1200/kW in 2008 can be achieved.

Table 2. Fuel cell type, readiness and typical pricing.

What is on the Horizon?

Many new fuel technologies are now being investigated for a replacement of fossil fuel oil as the primary source of fuel for cars. There are three engineering issues that need to be addressed with any new fuel source: 1) Portability, can be carried efficiently and safely on the car, 2) Emissions requirements, and 3) Fueling infrastructure. Government agencies don't see the replacement of fossil fuels occurring all at once, but instead over sev-

eral decades. This transition will involve meeting targets for cost, performance, safety and fueling infrastructure.

Some of the current renewable fuels being considered are fuels made from corn and soybean. Both natural gas and corn fuels represent technology that is proven and is used now. Unfortunately, natural gas is a non-renewable energy source and fuel made from corn or soybean would require many hecta-acres of corn (organic fuel) to support current consumption. Moreover, both fuel types suffer from emissions that may not meet future requirements and are subsidized by the government.

Fuel cells can meet the portability and emissions but are still too costly to replace traditional fossil fuels. Fuel Cell reliability and durability in extreme climate conditions need to be established as well as the true fuel efficiency. In order to house the fuel cell and associated fuel, novel packaging concepts for safely storing hydrogen will need to be developed. Engineers will need to determine data and overcome technical barriers for long term storage density, cyclic life, and end of life determination. In addition to the issues facing fuel cells, the hydrogen manufacture, transportation and fueling infrastructure will need to be determined.

In order to become a viable source of energy, several near term problems need to be resolved: 1) Cost, 2) Fueling, 3) Reliability, and 4) Safety. It should be noted that Cost is a function of manufacturing and operation. Unlike solar cells, fuel cells can operate continuously.

Research and Development expenditures are rising with increasing cost of a barrel of oil and the near term desire of countries to become less oil dependent. Fuel sources for hydrogen must be efficiently distributed as and is estimated to cost nearly 12 billion dollars to establish fueling stations and establish safe equipment that can be as easily used as our currently developed fuel distribution system. The largest challenge for fuel cells will remain reliability. Reliability cannot be adequately discussed until we resolve which fuel cell type will be used. There are two types, high temperature and low temperature fuels cells. Most low temperatures fuel cells, also known as PEMS (Polymer Exchange Membranes) utilize a precious metal such as Platinum. Platinum while having excellent catalytic ability, suffers from high cost, nearly $1200 per troy ounce. (See figure 2.) It maybe difficult for PEM's to compete for portable applications.

High temperature fuel cells do not require the precious metal content, as they use temperature to convert Hydrogen to electricity. Fuel cells such as SOFC operate at temperatures between 700-900°C. However because of the high temperature of operation, many technical, reliability and material challenges await the engineers. In order for them to be cost competitive, they must cost no more than $3.00 per gallon equivalent. Table 2 shows a summary of each type of fuel cell, readiness and typical pricing.

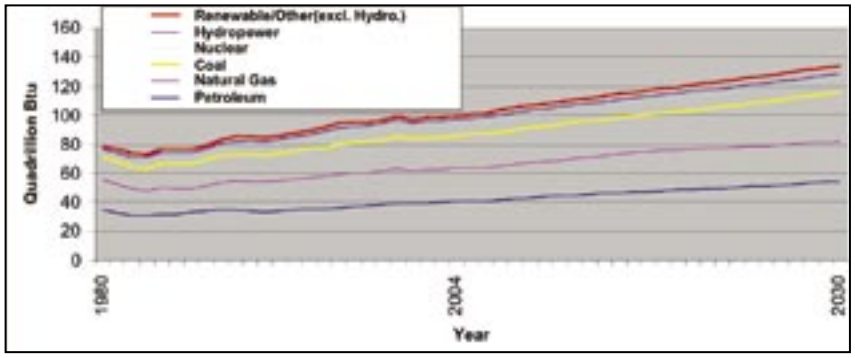


Figure 1. Energy Consumption by Fuel 1980-2030. Source: EIA, Released December 12, 2005

Figure 2. Kitco historic platinum price per troy ounce.

Who is Involved?

Governments around the globe recognize that dependency of nations on foreign oil and its inevitable exhaustion. The degree of engineering resource and monies required in developing the renewable resources warrant government involvement and development partners amongst utilities, companies and manufactures. In the United States, government agencies such as the National Energy Technology Laboratory is coordinating and setting mileposts through the Solid State Energy Conversion Alliance to help focus US resources in improving efficiency and drive down cost while increasing power density.

The Challenge

It is a fact that we are using nonrenewable fossil fuel resources for which there is no viable replacement for the automotive industry. Current technologies will not meet all the needs, emission, portability, density but will provide a bridge to the next generation power sources. These new renewable energy technologies will present engineering challenges that will push the technology envelope. Fuel cells have the potential of meeting the requirements, however, operating at temperatures greater than 750°C will present durability and reliability issues. Engineering teams around the world are coordinated by government agencies, utilities and channel partners to provide the leadership and monies to develop energy source technologies efficiently. The next technology wave for energy will certainly provide for some very exciting times and challenges. ◆

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"Everything in electronics between the chip and the system!"

Hysol LOCTITE Multicore
Henkel News
December 2006
Henkel

Stressed Out by Large Die Flip Chip Applications?

New Underfill Technology Keeps You from Coming Unglued!

Dan Loskot, Dr. Qing Ji and Dr. Renzhe Zhao, Electronics Group Henkel

The benefits of flip chip technology for advanced device applications have been well proven. With advantages such as more efficient electrical interconnections, smaller device footprints and increased I/O counts, flip chip technology has gained favor among package designers and electronic product OEMs in recent years. While the reliability of flip chips in smaller footprint packages such as BGAs, CSPs and the like has been established, large die (20 mm and above) flip chips for applications such as ASICs, video chips and microprocessors are subjected to more stress due to the large die size and, thus, may face processing and reliability challenges not shared by their smaller footprint flip chip counterparts. Newly developed underfill technology, however, addresses these challenges and helps device manufacturers realize all the benefits of flip chip technology without the hurdles often associated with large die flip chip processing.

Today's mainstream flip chip assembly processes generally consist of two steps: the bonding of the flip chip followed by encapsulation or underfill. Once the die is placed with the active side down onto the substrate, the entire device is then sent through a reflow oven to form electrical and mechanical connections. An alternative approach for gold bumped flip chips is the use of thermo-compression bonding. After the connections are formed, the device is then underfilled and cured. The underfill provides chip protection but, even more importantly, enhances the reliability by evenly distributing the stress across the die. As one can imagine, the bigger the die, the larger the stress.

To address the challenges associated with large die flip chip applications, Henkel has developed a new Amine-based underfill system that delivers the robustness and reliability of smaller-die flip chip technology. One common problem with older generation underfills is their limited adhesion to Silicon Nitride (SiN), which is one of the more common die passivations utilized by modern packaging specialists. Many of the traditional underfill materials do not adhere well to SiN, subsequently causing problems – such as shorts and, thus, catastrophic device failure when the devices go through real life cycles. Henkel's next generation Amine underfill system alleviates these issues by delivering excellent adhesion to SiN and polyimide and, when tested against competitive underfills, provided superior performance. These next generation underfill systems are designed to deliver lower stress with the unique combination of thermal mechanical characteristics to prevent delamination, bump fatigue and UBM (Under Bump Metalization) failure. The images shown on page 30 illustrate the effect of higher Tg and lower CTE to prevent UBM failure.

Certainly excellent adhesion is a key property requirement of underfills utilized by advanced device manufacturers, but the materials must deliver other high reliability characteristics as well. Low moisture absorption is also critical, so that as the device goes through the reflow processes – both in package assembly and subsequent PCB assembly – it will remain void-free. Henkel's new Amine-based underfill system delivers these benefits as well as superior fracture toughness. In testing to JEDEC Level 3 plus 1000 cycles TCT, Henkel's underfill system outperformed competitive materials by showing no UBM failure – proving the superiority of the material's long-term integrity. The fracture toughness feature of this Amine underfill technology has gotten the attention of several major device manufacturers – many of whom are now considering incorporating this product into their packages. Since large die flip chips are subjected to more mechanical stress because of the die's larger DNP (distance from neutral point), the underfill material's fracture resistance is crucial.

All of these long-term reliability underfill characteristics – optimal thermal mechanical characteristics, good adhesion, low moisture absorption and fracture toughness – are vital for excellent in-field performance. But, of equal importance is the material's manufacturability. An underfill's flow characteristics, process window and cure properties dictate its ability to perform well – and at relatively fast speeds – within a manufacturing environment. In addition to the reliability characteristics of Henkel's new Amine-based underfill technology, the material also embodies the important manufacturing properties of a wide process window, faster flow and longer gel time, which enables self-filleting and eliminates the need for a seal pass. All of these benefits amount to superior performance, more efficient manufacturing and, ultimately, lower costs and higher reliability.

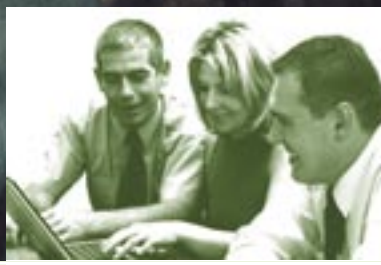
Though this material has been developed to specifically address the

(continued on page 28)

Hysol® LOCTITE® Multicore®

Not enough hours in the day?

Henkel's material sets let you get back to more *'important'* office work.



"So much to do, so little time" is a common dilemma for today's manufacturers. But, it need not be this way. Henkel's material sets will save you time for more pressing concerns.

Can you really afford to spend the time necessary to qualify, test and guarantee compatible products? If not, mistakes are inevitable. Fortunately, Henkel's Material Sets solve this dilemma by delivering proven package performance - stress reduction, compatible chemistry and material interface designs. Using the cross-qualified Hysol mold compounds, QMI die attach adhesive and underfills, this complete solution saves you up front design time and reduces overall maintenance time and costs. And you get the support of a world-renowned electronics specialist – Henkel is the Single material solutions provider you've been waiting for.

Henkel

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electronics.henkel.com

(continued from page 26)

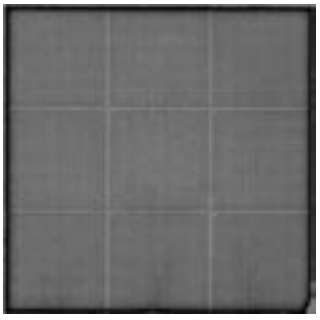
current underfill technology gap for large die flip chip applications, Henkel's new Amine offering will undoubtedly perform well with any die size. And, while the first version of this underfill system will address high lead flip chips, Henkel is currently developing a lead-free compatible version which will soon be commercially available.

Don't flip out over large die applications. Henkel's new Amine-based underfill technology will help keep you and your components stress-free!

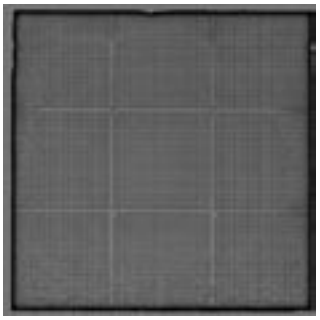
For more information on Henkel's advanced underfill technology, log onto www.electronics.henkel.com or call the company's headquarters at 949-789-2500. ◆

Initial C-SAM Images

Henkel Amine Technology



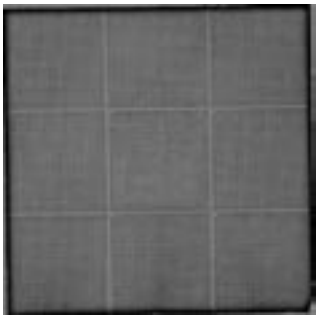
Competitor A



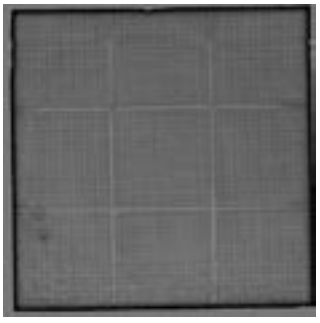
Competitor B

After JEDEC3 260°C

Henkel Amine Technology



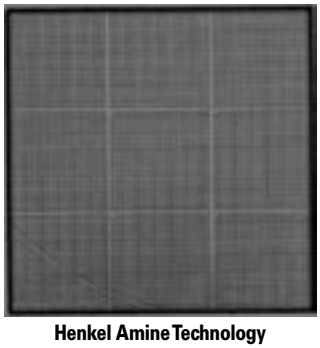
Competitor A



Competitor B

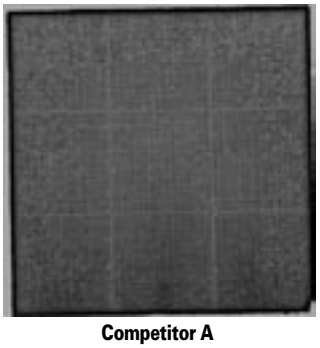
(Higher bump stress — competitive materials begin to show solder fatigue / UBM failure)

After 1,000 Cycles AATC (Air to Air Temperature Cycles)

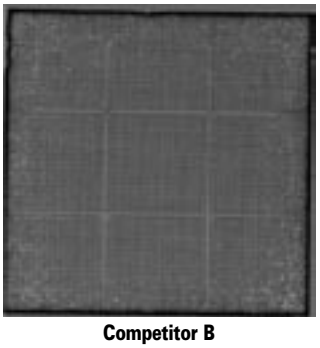


Henkel Amine Technology

Clean

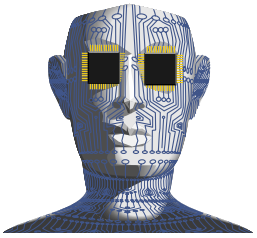


Competitor A



Competitor B

(Significant solder fatigue/UBM failure)



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JANUARY 2007

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1 NEW YEAR'S DAY	2	3	4	5	6
7	8	9	10 SUNNYVALE MEPTEC LUNCHEON Ramada Silicon Valley Sunnyvale, CA	11 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	12	13
14	15 MARTIN LUTHER KING JR. DAY	16	17	18	19	20
21	22	23	24	25	26	27

FEBRUARY 2007

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
28	29 DESIGNCON 2007 January 29 - February 1 Santa Clara Convention Center, Santa Clara, CA	30	31	1	2	3
4	5	6	7	8	9	10
11	12 LINCOLN'S BIRTHDAY	13	14 VALENTINE'S DAY	15 MEPTEC THERMAL MANAGEMENT SYMPOSIUM San Jose, CA	16	17
18 CHINESE NEW YEAR	19 PRESIDENT'S DAY	20 IPC APEX/PRINTED CIRCUIT EXPO February 20-22 Los Angeles Convention Center, Los Angeles, CA	21	22	23	24 FLAG DAY

MARCH 2007

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
25	26	27	28	1	2	3
4	5	6	7	8	9	10
11 DAYLIGHT SAVING TIME BEGINS	12 SEMICO SUMMIT March 11-13 Camelback Inn, Scottsdale, AZ	13	14 SUNNYVALE MEPTEC LUNCHEON Ramada Silicon Valley Sunnyvale, CA	15 SOUTHWEST MEPTEC LUNCHEON Dobson Ranch Inn Mesa, AZ	16	17 ST. PATRICK'S DAY
18	19 IMAPS THIRD ANNUAL INTERNATIONAL DEVICE PACKAGING CONFERENCE & EXPO March 19-22 Double Tree Paradise Valley Resort, Scottsdale, AZ	20	21	22	23	24
25	26	27	28	29	30	31

The Heat Really *IS* On

Jeffrey C. Demmin, Tessera, Inc.
MEPTEC Advisory Board Member

I am tempted to write that thermal management is the hottest issue in the semiconductor industry, but I will try to spare you from the bad puns on this page. Still, the title for MEPTEC's upcoming annual thermal management symposium – ***The Heat Is On*** – is totally appropriate. Thermal issues are more important than ever.

If the laptop that burns your lap isn't enough evidence of the increasing challenges is keeping electronics cool, I have a few other tidbits that show the current focus on that area. For example, I have recently clipped articles on thermal issues in semiconductors from every periodical that I receive … not just at work but at home. This includes two general business magazines, a general news weekly, a major daily newspaper, and a general technology monthly. The newspaper had an article on the cover of its business section titled "Too Hot to Handle" that included a person-in-the-street interview feature on how the average person deals with keeping their computers cool. Everyone had some kind of interesting tale. The article even had pictures of semiconductor thermal testing equipment, which is something that I never thought I would see on my front doorstep in the morning. Anyway, the point is that widespread coverage of thermal management in the mainstream press makes is arguably the most prominent issue in the industry.

Here's another indicator. I did a survey of the advertising appearing in a recent issue of a major weekly publication covering the whole electronics industry. Nine percent of the ads had power reduction or thermal management as the most prominent theme, while thirty-four percent more of the ads mentioned thermal management one way or another. This is in a periodical for a very general electronics audience, so the ads included connectors, software, PCB fab houses, and other such generic things. In the midst of all of that, thermal management still stood out as the biggest topic being addressed by a very broad range of suppliers.

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Perhaps the most telling indicator is the number of conferences covering thermal management these days. I found six noteworthy conferences focused just on thermal management over the course of a year, and these are only the events that I ran across without going out of my way to find them. I don't mind calling attention to events that might be seen as competitors to MEPTEC's thermal symposium, because I see the proliferation of events as confirmation that the industry needs this kind of focus on the topic. Think of it as the "Auto Row" where competing car dealers locate their businesses close to each other for the convenience of the consumer! Some events are more academic, some focus on the details of thermal analysis and design, and others focus on thermal solutions. MEPTEC's approach with ***"The Heat Is On"*** is to provide in one day a view of thermal management from a variety of perspectives with a slate of hand-picked presenters. I imagine that people working in the thermal management field are happy to have numerous events to select from, and we at MEPTEC are glad to host one of the many successful events in the field.

If all of that evidence – conferences, newspaper articles, ads, and an overheated laptop – doesn't tell the story, ask yourself what the warmest room in your house is. For me, it's the room with our computers, by at least a few degrees. Our dogs seem to hang out there during the winter, while we try to keep the utility bill down in the rest of the house.

Anyway, some of my earliest technical work in the industry was thermal analysis, so I have a special interest in this area. Finite element modeling during the Reagan administration was a different beast from what it is now – I remember submitting FEA jobs to "the computer guy" off in some other building – but the goal hasn't changed. In fact, more than ever, we need to do everything we can to address heat transfer. The great thing about the thermal challenge is that everyone in the supply chain can contribute to the solution. It starts with the basic chip technology – what comes after CMOS? – and includes chip design and wafer processes. It covers package design, materials, and heatsinking of course, and continues up through computer architecture and power management strategies. People from all disciplines have part of the solution in their hands. You can almost use the global warming analogy. If we all do our part, we just might solve something. ◆

Magazines and Carriers for Process Handling Solutions


Film Frames


Film Frame Magazines


Film Frame Shippers


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Grip Ring Magazines

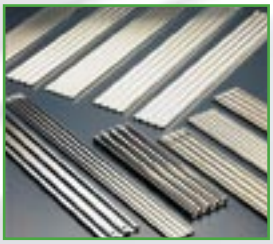

Grip Ring Shippers

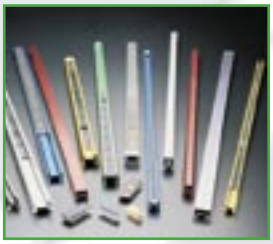

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.

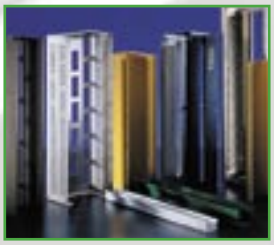

Process Carriers (Boats)


Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines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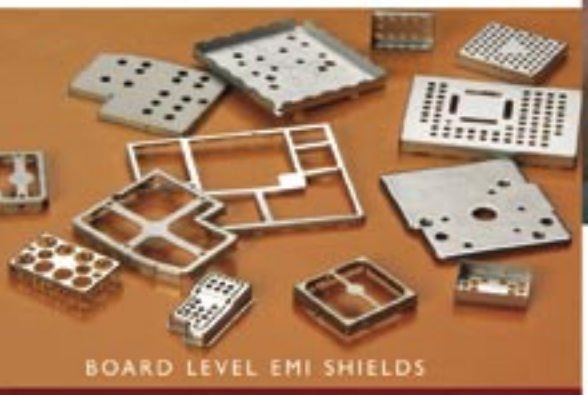
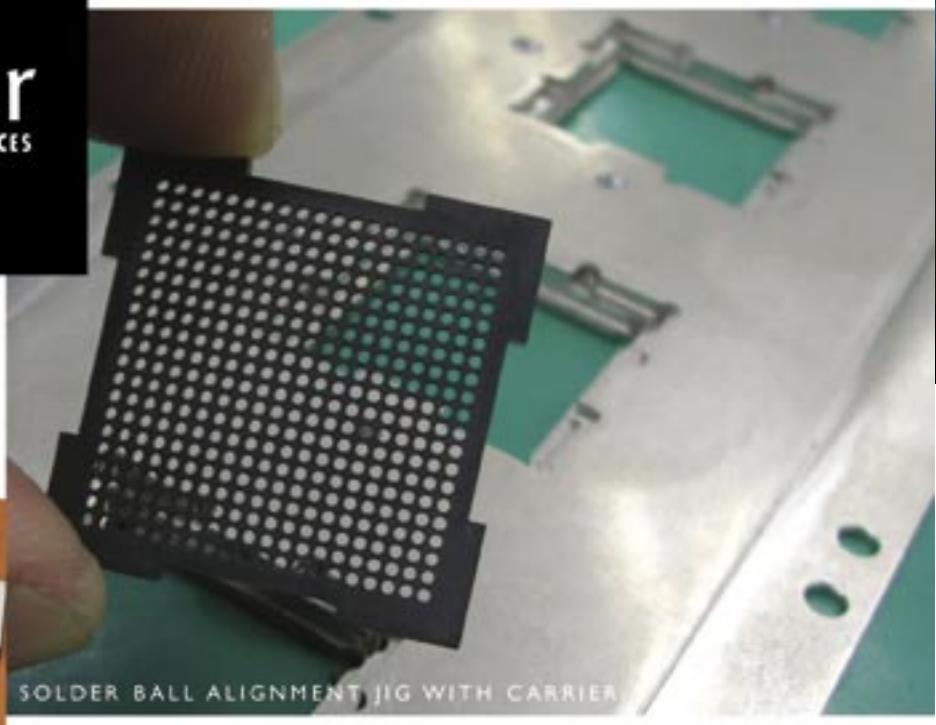


BOARD LEVEL EMI SHIELDS

MICRO STAMPING



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