MEPTEC report

Volume 11, Number 2

QUARTER TWO 2007

A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Dr. Gerald K. "Skip" Fehr has joined the Technical Advisory Board of **Mirror Semiconductor Inc.** *page 14*

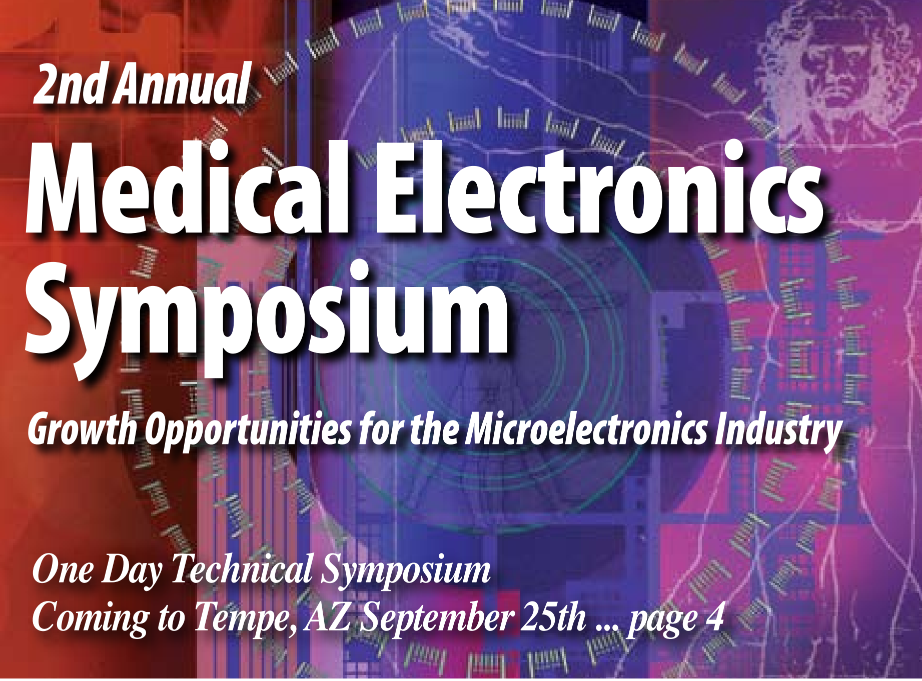
ASAT Holdings Limited has announced the appointment of Gabby Ang as vice president of North American sales. *page 14*

Gel-Pak has announced the launch of its new web-based Product Selection Wizard (PSW), an interactive program that uses a series of targeted questions to recommend the ideal Gel-Pak carrier based on each customer's detailed application. *page 18*

Kulicke & Soffa has introduced the new MaxSoft™ copper bonding wire engineered for a variety of discrete and IC applications. This new copper wire has unique physical properties that reduce IC bond pad stress and significantly improve 2nd bond strengths. *page 19*

Tessera Technologies, Inc. has announced the MicroPILR™ Interconnect platform, a highly innovative technology family that is designed to revolutionize the interconnect within semiconductor packages, substrates, Printed Circuit Boards (PCBs) and other electronic components. *page 19*

SEMICON West returns to Moscone Center in San Francisco July 16 though 20 . *page 7*

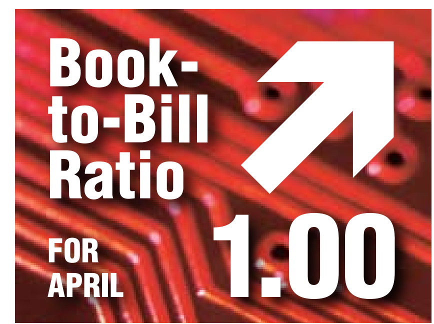


MEMBER COMPANY PROFILE

Since its founding, Pac Tech has received more then 50 patents for products developed in areas relating to semiconductor interconnection, including wafer bumping, flip-chip, chip-scale packaging and laser bonding technologies. Pac Tech has also formed alliances with companies in the U.S., Europe and Asia for licensing, equipment sales, and contract wafer bumping services.

Pac Tech Asia Sdn. Bhd., a wholly owned subsidiary of Pac Tech GmbH, purchased its new 53,500 square foot contract wafer bumping facility in Penang, Malaysia in December 2006. 40,000 square feet of the facility floor space will be dedicated to manufacturing, much of it in a clean room environment. When completed, the facility will be equipped with the latest generation of equipment aimed at supporting semiconductor market requirements for low-cost wafer bumping and backend processing. *page 21*

Semiconductor equipment bookings increase 12% over March 2007 level. *page 20*



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Council Update

It's hard to believe summer is upon us again, and in our industry that means time for **SEMICON West**, when thousands in the industry converge on Northern California to see the latest and greatest technology in the semiconductor industry. This year is the third since SEMI moved the entire show to San Francisco, integrating the Final Manufacturing segment of the show into the rest of the event, and it seems as if most of the kinks have been worked out. We're pleased this year to again be a part of SEMICON West as a technical partner contributing to their **TechXPOT** (pronounced "Tech Spot"). The **Advanced Packaging Trends** and **MEMS** session will be held on Tuesday, July 17 from 10:30 am to 1:00 pm, in the Test, Assembly and Packaging hall, right on the show floor. Several presenters from past **MEPTEC** technical symposiums will be speaking. We hope you'll take some time to stop in to listen to these informative presentations.

Our next event will take place on Tuesday, September 25 and once again we'll be holding it on the Tempe campus of **Arizona State University**, in the beautiful Old Main building. The event, called *"2nd Annual MEPTEC Medical Electronics – Growth Opportunities for the Microelectronics Industry"* will be co-sponsored by **ASU** and the **MacroTechnology Works**. The event will cover business and technology overviews, medical microelectronics packaging, impact of the enabling technologies, and medical electronic product applications. See page 4 for further information.

We also offer a follow-up of our most recent symposium, the *"5th Annual MEPTEC MEMS Symposium: MEMS in the Mainstream: $50 Billion and Growing"* which was held on May 16-17. **Debra Vogler**, Senior Technical Editor of **Solid State Technology** and **WaferNews**, attended the event and provided this summary for us. Debra focuses on one specific topic presented at the event, and a very critical aspect of the exploding MEMS industry: the need for world-class pure MEMS foundries. The topic, presented by MEPTEC MEMS event committee member **Janusz Bryzek**, CTO and Chairman of **LV Sensors, Inc.**, is going to be one which MEPTEC will be exploring in more depth in the future. The event also included an academic session where we heard about some of the leading-edge research in MEMS technology. CDs of the proceedings are available on the MEPTEC website at www.meptec.org.

One of the feature articles this issue is contributed by MEPTEC member company **Bridge Semiconductor Corporation** on *"Frame Level Packaging: Performance Gain with Less Pain"*. **Dr. Charles Lin** and **Jerry Tan** describe in depth an innovative technology called Frame Level Packaging, which uses a copper frame as the platform to manufacture advanced packages, with enhanced performance. See page 25 for this very thorough and informative piece.

Our other feature article is from **Ed Pausa**, a former semiconductor executive and a real veteran – more than 40 years of industry experience. He is a now a Director at **PricewaterhouseCoopers Technology Center**. Ed takes a look at *"Understanding China's Impact on the Semiconductor Industry"* which is a summary of PWC's 2006 report of the same name. Ed discusses trends on packaging and testing, IC manufacturing, and challenges and opportunities in China. Ed has presented the China updates for the last couple of years for MEPTEC; we look forward to the 2007 report. See his article on page 29.

Our Editorial this issue is contributed by new MEPTEC Advisory Board member, and frequent speaker at various MEPTEC symposiums, **Rich Rice** of **ASE (U.S.) Inc.** In his commentary on *"Can Package Substrate Technologies Continue to Bridge the Gap?"*, Rich addresses that topic, as well as many other questions he hears from his customers – queries he feels that are very straightforward, but not so simple to answer. Rich

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and fellow MEPTEC advisory board member **Joel Camarda** of **Sipex** will be chairing MEPTEC's Q4 technical symposium in November called *"Substrates: The Foundation Packaging"*. Stay tuned for more details on that event, and make sure to read Rich's thought-provoking piece on page 38.

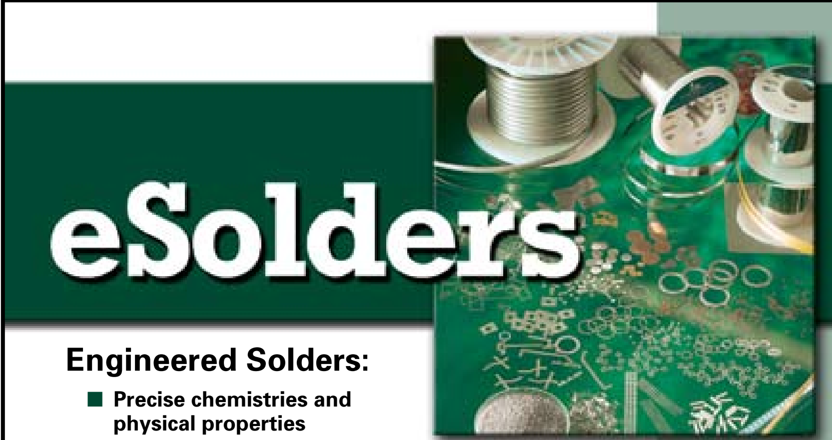
Our Industry Analysis coverage this issue is contributed by **Morry Marshall** of **Semico**. *"Choosing the Right Semiconductor Packaging Partner"* (page 8) takes a look at how critical it is for a semiconductor manufacturer to choose the right packaging subcontractor. Morry looks at comparing the five year forecast from 2006-2011 for shipments of advanced IC packages vs. shipments of mature IC packages, and explains in depth the trends that will evolve. Morry is a frequent contributor to MEPTEC, in both our newsletter and speaking at our events. We'd like to thank him for his continued support.

Our Member Company Profile this issue is from long-time MEPTEC Corporate member and supporter, **Pac Tech Packaging Technologies**. Pac Tech, among many other things, is a world leader in providing advanced wafer bumping, packaging and solder-ball placement equipment. Their quality policy sums it up; in part, their primary objective is "the complete understanding of all customer requirements in accordance to the company philosophy of being a supplier of highly specialized innovative services for the forward looking IC packaging technology market". Read their story on page 21.

Our University Profile this issue is straight from the heartland – Ames, Iowa. We'd like to thank MEPTEC Advisory Board member **Skip Fehr** for putting us in touch with his alma mater, **Iowa State University (ISU)**. We all tend to assume that the semiconductor industry is very Silicon Valley centric, but the profiles of the various universities nationwide and even globally that MEPTEC has done over the past years prove that technology R&D is much more wide spread. The research being done in the Materials Science and Engineering department at ISU is very cutting edge and is specifically relevant to the semiconductor packaging industry. One of the most intriguing things about ISU is that they have the highest resolution virtual reality visualization chamber in the world… see the rest of their story on page 11.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at the Semicon West show, or another of the many events where we'll be distributing this issue, we hope you enjoy it.

Thanks for joining us! ◆



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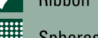
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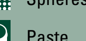
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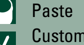
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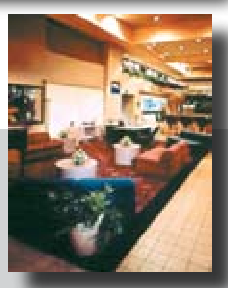

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Prescription for Pure-Play MEMS Foundries Outlined at MEPTEC Event

Debra Vogler, Senior Technical Editor
Solid State Technology / WaferNews

Seeking to accelerate the growth of the MEMS device market, CTO and chairman of LV Sensors Inc. (LVSI), Janusz Bryzek, called for the formation of a world-class pure MEMS foundry business with customizable standard unit processes at the recent MEPTEC conference May 16 and 17 in San Jose, California. These unit processes, characterized and modeled over a broad range of settings, would be enabled by state-of-the-art high-volume processing equipment with first pass process yields similar to what is achievable in CMOS manufacturing.

That such standardization would shorten the current development cycle time and speed time-to-market is apparent given that custom processes represent ~100% of the commercial MEMS market, Bryzek observed. He cited Sandia and MemsCap/MCNC as being among the few that have standardized MEMS processes. But pursuing standardized processes would also restrict device designers – a familiar lament heard even by designers of bleeding edge advanced CMOS logic and memory devices. Bryzek pointed out to the conference attendees that venture capitalists are already pushing for start-ups to go fabless. Furthermore, he added that many of the objections being raised for MEMS standardized processes were the same ones heard in the CMOS sector before the rise of the fabless model.

However, accomplishing Bryzek's goal, at least for newer MEMS devices, will require overcoming significant process IP protection. Competitors who hold key IP portfolios view the status quo as a way to ensure higher barriers to entry and standardization would challenge their leverage he said. And while the IC industry continues to push the envelope with respect to manufacturing in China (with Intel seeking a new 300mm fab, backend facility expansions from Micron, Qimonda, and NXP/ASE, and even Silicon Valley VC stalwart Kleiner Perkins Caufield & Byers extending roots), Bryzek told the audience that the country's lax enforcement of IP protection is an impediment to the establishment of MEMS foundries there.

Reviewing the market potential for MEMS, Bryzek cited market projections from Yole Développement (see table), but added that his own estimate places the 2005 MEMS device market at $8 billion with growth at 17%/yr, but that's because Yole classifies some MEMS-based devices as systems.

GLOBAL MEMS MARKET, 2005-2010

	2005 (US $B)	2010 (US $B)	CAGR (%/year)
Systems	48.0	95.0	15
Devices	5.2	9.9	13
Equipment	0.6	0.9	6
Materials	0.4	0.8	15

WaferNews Source: Global MEMS/Microsystems Markets and Opportunities, Yole Développement.

Realizing a viable MEMS foundry business model, according to Bryzek, must include a number of elements:

- A focus on 200mm fab equipment, along with building on CMOS processes;
- Training programs to teach new customers how to design devices in standard processes that are already offered;
- MEMS device reference cells using public domain MEMS IP;
- Modeling tools that enable the prediction of yield/performance with customized settings; and
- A standardized set of programmable MEMS unit processes in concert with customers.

One conference attendee, Henry Klim, executive director of the Bennington Microtechnology Center, characterized Bryzek's suggestions as providing the "activation energy" required to promote a change. "Historically, it was thought that MEMS fabrication was simply based on using existing semiconductor foundry infrastructure, because foundries saw MEMS as a way to provide "filler" in lines operating below maximum capacity," Klim told WaferNEWS. With the exception of pressure sensors and, to an extent, accelerometers, "It became clear that this was not the case, and we began to see a noticeable slowdown in product commercialization." Klim called Bryzek's analysis a compelling argument for foundries to being investing in pure-play MEMS lines. ◆

MEPTEC conference speaker Benedetto Vigna, GM of STMicroelectronics' MEMS product division, told WaferNEWS that the company's objective of becoming the leader in MEMS motion sensors for the consumer market will be its entry point into the automotive MEMS market. Already a manufacturer of ICs for games, laptops, and mobile phones, as well as automotive applications, Vigna said that the company will leverage its manufacturing capabilities and suppliers to achieve the goal. "We are riding the wave of the consumerization of the MEMS market," said Vigna.

A big part of this "wave riding" is the company's state-of-the-art 200mm MEMS production line in Agrate Brianza (near Milan), Italy, which was inaugurated in Nov. 2006. The company invested ~$40 million to transform the former 150mm facility into a dedicated 200mm MEMS production line. ST says it has already started pilot production of its first-generation MEMS gyroscopes, and has agreed to incorporate SAES Getters' PageWafer getter thin-film technology in next-generation MEMS gyros, with an expected volume ramp sometime in 1H08.

The company's success in MEMS manufacturing is evident in Wicht Technologie Consulting's (WTC) rankings of the top 30 MEMS manufacturers in 2006 by revenue, presented by conference speaker, Janusz Bryzek, CTO and chairman of LV Sensors Inc. (LVSI). According to the WTC ranking, STMicroelectronics took in US$257 million in 2006, making it No.7 behind (in ranked order) TI, HP, Canon, Robert Bosch, Panasonic, Lexmark, and Seiko Epson. WTC further cited STMicroelectronics for its strategic relationship with HP for the production of printhead wafers. – D.V.

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Choosing the Right Semiconductor Packaging Partner

Morry Marshall, Partner - Strategic Technologies
Semiconductor Partners LLC

Semiconductor vendors need to consider their requirements very carefully when choosing a semiconductor packaging subcontractor. Semiconductor packaging subcontractors can be divided into roughly three tiers. Companies in all three tiers can assemble mature packages. First tier companies, however, also have the capability to assemble advanced packages and to design, develop and assemble complex, leading-edge packages. Second tier companies can assemble advanced packages, but they have a limited capability for designing and developing new, leading-edge packages. Third tier companies concentrate on the assembly of mature packages.

If price is the most important consideration, continuity of supply is not a critical issue and a company's semiconductors are all in mature packages, then a third tier subcontractor may be the right choice. If the capability of assembling mature packages and advanced packages is the requirement, then a second tier packaging subcontractor may be a good choice. If the capability of assembling mature packages and advanced packages is needed; but there is also a need to develop leading-edge packages, then a first tier supplier is the only choice. Even if a semiconductor manufacturer doing packaging in-house should consider a strategic partnership with a first-tier packaging subcontractor to develop new packages. The increasing costs of developing new packages make that consideration a must.

The costs for designing and bringing to production a next-generation semiconductor package type are becoming enormous, running into tens of millions of dollars. Those costs are too high for all but three or four of the largest semiconductor manufacturers. Even those companies need to consider whether or not they have the engineering capability or the financial means to design and develop a next generation package type. They would most likely be better served by choosing a partner, a first tier semiconductor packaging subcontractor who can spread the costs across many customers, amortizing the NRE (Non-Recurring Engineering) charges into the piece price.

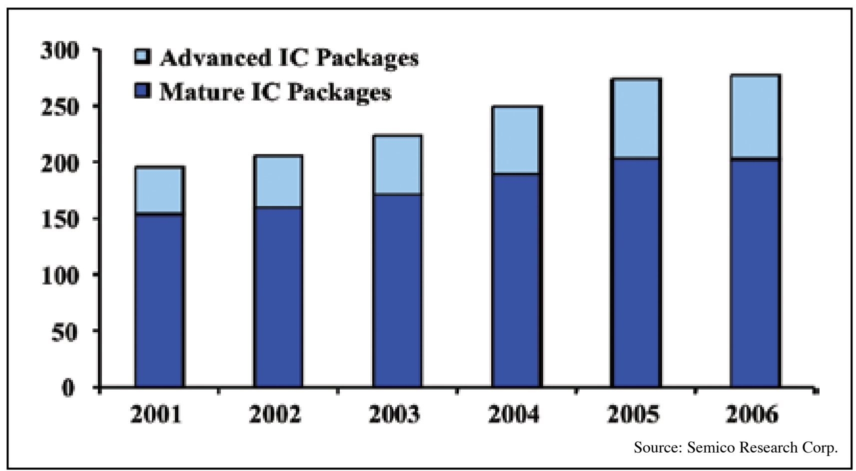
The chart shown at right compares the five-year forecast (2006 to 2011) for shipments of advanced IC packages versus shipments of mature IC packages. Discretes are not included, but optoelectronic devices and sensors are. For the purposes of this chart leaded IC packages are defined as mature IC packages. Non-leaded IC packages, typically BGA packages, are defined as advanced packages. There are exceptions. Leaded MCU packages are obviously advanced packages.

From 2006 through 2011 the growth in advanced IC packages will be more than double the growth of mature packages. The CAGR for advanced IC packages for that time period will be 12.2% while the CAGR for mature IC packages will be only 5.7%. The primary reason is that ICs are reaching higher levels of density and integration, particularly in consumer products. Higher levels of density or integration lead to higher pin counts than leaded packages can provide and so advanced packages are required.

The trend towards higher levels of density and integration will continue, eventually leading to the need for a next-generation package that will either be able to provide higher pin counts or provide interconnects that will lower the number of final I/O pins. These packages will be expensive and their development costs will be high. The selection of a suitable first-tier partner to aid with the design and development of these next generation parts will be critical.

There is always an exception to the rule. Although Freescale Semiconductor is not one of the top three or four semiconductor vendors by revenue, Freescale has developed a package, the RCP (Redistributed Chip Package), which has the potential to become the next generation of semiconductor packaging. Although the process is proprietary, RCPs use standard CMOS processes and materials to provide insulating and wiring redistribution patterns between stacked layers of ICs. The RCP process offers the potential to reduce costs for packaging complex ICs and to reduce the I/O pin count.

Choosing the right semiconductor packaging contractor is critical to a semiconductor manufacturer's success. In mature semiconductor markets where mature, leaded packages are used, a third tier subcontractor may be the best choice. For other companies, which have a mixture of mature and advanced packaging needs, a second tier subcontractor may be the correct choice. For a company with mostly advanced packages and the need to develop next generation packages, a first tier subcontractor is the only choice, remembering that first tier packaging subcontractors also assemble mature packages. In addition, it will pay to keep an eye open for revolutionary packaging technologies such as the Freescale RCP process. ◆



IC Shipments Forecast, Advanced IC Packages versus Mature Packages (units in billions).

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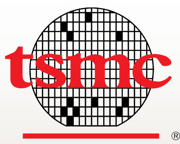

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From creating new materials to formulating innovative approaches to materials development and characterization, the Department of Materials Science and Engineering (MSE) at Iowa State University demonstrates daily how top-rank engineers can be educated in an environment of high-level research.

The department's research and teaching have a direct impact on the microelectronics packaging industry. Areas of research focus such as electroceramics, functional polymeric nanocomposites, and solidification and crystal-melt interfaces are just a few examples of how faculty are pursuing answers to the most pressing questions in the microelectronics field.

This research is coupled with teaching in a way that produces immediate, relevant results for industry partners. MSE interacts with 30 companies and laboratories to solve materials problems and develop new products. These partners leverage MSE's faculty expertise, equipment, and students in a relationship that benefits all parties.

Industries who partner with MSE also gain access to multidisciplinary resources and centers at Iowa State, ranging from the Microelectronics Research Center to the U.S. Department of Energy's Ames Laboratory. The world-class intellectual and physical resources contributing to these and other on-campus groups generate ideas and innovations that find global application.

Such resources make possible notable advances in materials development. The lead-free solder developed by MSE Adjunct Professor and Ames Laboratory researcher Iver Anderson is quickly becoming an industry standard. More than 50 companies have signed licensing agreements for the alloy, which was patented in 1996, and interest is peaking in Europe, where the use of leaded solder in electronic circuitry is limited by law.

The story of Anderson's lead-free solder is one of long-term, painstaking materials development that followed traditional methodologies based on classical metallurgical training. Anderson was able to

Tin-silver-copper-based solder alloys developed by Iver Anderson's research group are replacing lead-based solders for many electronic joining operations.

apply his thesis work while formulating the tin-silver-copper alloy and has spent the past 10 years refining it to achieve increased reliability.

A new four-component formulation that uses zinc now allows the solder to "form the best possible microstructure at

Materials Science and Engineering is housed in Hoover Hall, a $27 million facility dedicated in 2003 on the Iowa State campus.

the start of its lifetime," Anderson says. And yet another "fourth element" is being tested as Anderson designs an alloy that works well with high-power electronics.

Lead-based solders cause performance limitations and environmental problems, and these factors motivate Anderson's solder research. Such factors often drive materials development and characterization, but they become even more compelling as issues of nanoscale manufacturing raise new challenges.

Iowa State has responded by developing new methodologies. Materials informatics is a methodology that holds great promise as the microelectronics industry surges toward the design limits of existing materials. Informatics extracts patterns from vast amounts of data by applying well-established principles of mathematics and physics in novel ways. The methodology is far more than data mining and is not merely some software trick—instead, it is an advanced tool for describing complex systems, and it may well be the future of materials science.

MSE Professor Krishna Rajan, with an extensive background in microelectronics, is leading the materials informatics effort. "As you make things smaller, the design issues become more challenging," he says. "Microelectronics is an area where I think people are now willing to seriously look at new materials. But we don't have 20 or 30 years to come up with a solution."

To address that need, Rajan's group at Iowa State, supported by funding from the Defense Advanced Research Projects Agency (DARPA), has teamed with Stanford University and the University of California-Berkeley to take MEMS development to a new level. "MEMS are being used in sensors and actuators in more extreme environments," says Rajan, "so we can't make them with the same materials any more." The resulting Center on Interfacial Engineering for Microelectromechanical Systems (CIEMS) is a premier example of collaborative research. Through the use of informatics, Iowa State's role is to suggest, predict, and identify new materials for MEMS.

Established and emerging methodologies both depend on access to advanced tools and equipment, and three recent acquisitions make MSE uniquely well equipped. An atom probe microscope, one of only four such instruments in American academic institutions, was dedicated on May 30 as the centerpiece of the new W. M. Keck Laboratory for High Throughput Atom-Scale Analysis.

Just one month earlier, an upgraded C6 – operated by Iowa State's Virtual Reality Applications Center – became the highest-resolution virtual reality room in the world. The six-sided, total immersion room was enhanced by a Hewlett-Packard computer cluster featuring 96 graphics processing units, 24 Sony digital projectors, an eight-channel audio system and ultrasonic motion tracking technology.

The third piece, and one which is capable of tying all three into a powerful array, is the IBM BlueGene/L, a 1024 node supercomputer with 11TB of file storage. The machine went on line in January 2006 and is already proving itself to be a valuable on-campus resource.

Such resources are enhanced by expanding collaborations with other major Midwest research universities. This spring, Iowa State joined the University of Iowa, the University of Minnesota, and the University of Wisconsin-Madison to create BOREAS-Net (the Broadband Optical Research, Education and Sciences Network). The network will help Rajan, for example, share the imaging data produced by the atom probe microscope with researchers around the world.

With elite faculty, industry partnerships, advanced tools, access to on-campus research groups, and global links to outside researchers, the Department of Materials Science at Iowa State is well-positioned to play a leading role in materials development and characterization while mentoring the engineering students who will produce the next generation of advances. ◆

The atom probe microscope is capable not only of rendering the atomic structure of samples in three dimensions, but also of fully characterizing all of the elements comprising the sample, atom by atom.

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Dr. Gerald Fehr Joins Mirror Semiconductor's Technical Advisory Board

IRVINE, CA – Dr. Gerald K. "Skip" Fehr, an internationally known and respected expert in semiconductor packaging and interconnection, has joined the Technical Advisory Board of Mirror Semiconductor Inc.

Dr. Fehr, now an industry consultant in San Jose, brings many decades of experience in semiconductor packaging operations and management to the Mirror Board. He has served in the top packaging jobs at Fairchild Semiconductor, Intel, LSI Logic and Texas Instruments – all among the largest and best-known semiconductor makers in the world.

He was also co-founder of IPAC, a semiconductor assembly and packaging company in San Jose, in 1993, where he was chief technology officer and vice president. He earned a doctorate in material science and engineering from Iowa State University.

The company, which is newly incorporated in California, will provide semiconductor packaging with an exclusive and recently developed technology known as the "Mirrored Pinout."

The Mirrored Pinout concept (patent pending) is based on the use of packages that are wire bonded in the clockwise direction. Traditionally, semiconductor package pinouts have been wire bonded counter-clockwise.

Key benefits of this new packaging method include superior performance over standard forms of interconnection. When a semiconductor package with a "mirrored" pinout is mounted on a printed circuit board with a standard package, the circuit routing may be up to 80 percent shorter to connect the two. The result is superior circuit speed performance.

Primary applications for the Mirrored Pinout include parallel data bus circuits, buss buffers, power management circuits, power control systems, analog and logic products.

Because the Mirrored Pinout, with its shorter circuit routing, improves circuit speed, it will be particularly useful in microcontrollers, memory controllers, graphics accelerators and digital signal processing.

The Mirrored Pinout can be employed with most types of package formats, including BGA, LGA QFN, QFP, SOP, SOT, TSOP and most chip-scale packages.

Mirror Semiconductor Inc., which will produce, sell, and license the technology by agreement with Liberty University, Lynchburg, Va., plans to locate in a facility in Irvine, Calif.

Mirror Semiconductor's President Martin Hart is a three-decade veteran of the semiconductor industry and is founder and president of TopLine, Garden Grove, Calif.

Mirror Semiconductor Inc. maintains a web site at www.mirrorsemi.com.

ASAT Holdings Limited Appoints Semiconductor Industry Veteran Gabby Ang As VP Of North American Sales

HONG KONG and MILPITAS, CA – ASAT Holdings Limited has announced the appointment of Gabby Ang as vice president of North American sales, effective immediately. Mr. Ang will be based in Milpitas, California, and report to Joe Martin, executive vice president of sales and marketing of ASAT Holdings.

Mr. Ang brings nearly 30 years of senior level sales experience in the assembly and test industry to ASAT Holdings. From 2004 to 2006, Mr. Ang served as vice president of sales for Advanced Semiconductor Engineering (ASE). He held a similar position with ASE from 1986 to 1991. Prior to his most recent employment with ASE, Mr. Ang served in key sales positions at Advanced Interconnect Technologies between 1991 and 2004, most recently as executive vice president of worldwide sales. Mr. Ang has also worked in sales positions with Amkor and Interlek/Dynamics.

Mr. Ang holds a Master's in International Management from the American Graduate School of International Management, and a Bachelor's of Science in Mechanical Engineering from Tri-State University.

For more information, visit www.asat.com.

Royce Names Director of Sales

NAPA, CA – Royce Instruments, Inc. has appointed Julie Adams as Director of Sales.

Julie Adams (previously Julie Houghten) brings over 15 years of global semiconductor assembly sales & engineering experience to Royce Instruments.

Diane Cox, President of Royce Instruments, cited Adams' rich experience in strategic sales and development of semiconductor packaging technologies and manufacturing equipment as critical to this position.

Adams has held senior engineering positions at Motorola and Amkor and spent several years as Director of Worldwide Sales and Service for RVSI Vanguard, a manufacturer of automated BGA ball placement systems.

Julie Adams can be contacted at jadams@royceinstruments.com, Office: +1 707 255-9078, Mobile:+1 707 975-2846.

JCET and JCAP Establish North American Operations

FREMONT, CA – Jiangsu Changdian Electronics Technology Co. (JCET) and its subsidiary, Jiangsu Changdian Advanced Packaging Co. (JCAP) has announced the establishment of North America Operations in Fremont, California, USA on May 10, 2007. The new operation is headed by Dr. Weiping (Bill) Li as the General Manager and is primarily responsible for the sales and marketing activities in the North American market. In this move, JCET/JCAP is able to provide timely customer support and communications with its existing and new customers.

Founded in 1972, JCET/JCAP is the leading packaging service provider in China. The company has a broad product portfolio, ranging from wafer bumping, WL-CSP to leadframe packaging and testing. JCET/JCAP has strong IP positions in Cu pillar bumping and FBP (QFN type) packaging.

In the past 5 years, JCET/JCAP has enjoyed around 30% CAGR with the 2006 revenue reaching $240M. JCET/JCAP has a broad range of customer base with about 50% of its revenue derived from overseas markets. The company has regional offices and customer service across China, United States, Taiwan and Europe.

For further information, contact JCET North America Operations, 41341 Joyce Ave., Fremont, CA 94539 USA, Tel. (510) 573-3612, Fax (510) 573-3613, email: bli@jcet-us.com, website: www.jcet-us.com.

Carnegie Mellon Alumnus McWilliams Establishes Graduate Student Fellowship

PITTSBURGH, PA – Carnegie Mellon University alumnus Bruce McWilliams, chairman, president and CEO of Tessera Technologies; and his wife, Astrid McWilliams, have given the Mellon College of Science (MCS) more than $1 million to establish an endowed fund for the Astrid and Bruce McWilliams Fellowship in the Mellon College of Science. The fellowship will support MCS graduate students conducting leading-edge research in emerging fields such as nanotechnology, biophysics and cosmology.

"Carnegie Mellon is one of the nation's top-ranked universities. As a student there, I received a scholarship that enabled me to pursue my scientific studies. Through this fellowship, Astrid and I hope to give back to the Mellon College of Science and its brightest minds as they make their mark on science and the industry," McWilliams said.

Since June 1999, McWilliams has served as chief executive officer, president and a member of the board of directors of Tessera Technologies. He was named chairman of the board in February 2002. Tessera is a leading provider of miniaturization technologies for the electronics industry.

McWilliams earned his bachelor's, master's and doctor's degrees in physics at Carnegie Mellon, and he serves on the advisory board for the Department of Physics.

The Mellon College of Science at Carnegie Mellon includes the departments of biological sciences, chemistry, mathematical sciences and physics, and serves as home to a number of interdisciplinary research centers. MCS faculty and students collaborate with other top-ranked Carnegie Mellon programs to advance research and education in emerging fields including nanotechnology, environmental science, bioimaging, biosensors and computational biology.

For more information visit www.tessera.com.

Asymtek Receives 2007 SMT China VISION Award

CARLSBAD, CA – Asymtek has announced that it has received a 2007 SMT China VISION Award from SMT China magazine for its Axiom™ X-1022 high-volume dual-lane dispensing system. The Vision Awards recognize the companies and products that serve as benchmarks of excellence within the surface mount industry. Judged by an independent panel of industry experts, Asymtek was selected the winner in the dispensing category. Evaluations were based on the Axiom system's overall performance, reliability, economic merits and ease of use. The SMT China VISION award was presented at a ceremony held during Nepcon Shanghai.

Asymtek's Axiom X-1022's dual-lane configuration increases throughput by 60 to 80 percent over single-lane systems. The system allows parallel processing on two lanes for continuous dispensing, eliminating lost time in non-dispensing activities such as material flow-out and substrate loading/unloading. Underfill can flow out in one lane while underfill material is jetted in the other. It lowers cost-of-ownership without adding another full system to the production line, minimizing manufacturing cost per square foot.

Visit www.asymtek.com for more information.

SIX SIGMA Solder Column Technology Used in CFEsat

MILPITAS, CA – SIX SIGMA is pleased to announce that it's SolderQuik® column grid array technology has been used to ruggedize FPGA microcircuits on-board the Cibola Flight Experiment Satellite (CFEsat). The satellite, which was launched on March 08, 2007, is equipped with an experimental supercomputer that utilizes columnized FPGAs commonly known as Column Grid Array (CGA). The same SIX SIGMA SolderQuik® technology is also an integral part of numerous other military and aerospace programs.

SIX SIGMA is proud to welcome CFEsat into the family of military and aerospace programs that currently use SolderQuik® column grid array technology.

For information about column grid array technology, contact SIX SIGMA at 408-956-0100 x1 or go to their website at www.sixsigmaservices.com/columnattach.asp.

Asymtek Receives Intel 2006 SCQI Award for Fourth Consecutive Year

CARLSBAD, CA – Nordson Corporation has reported that its Asymtek business has received Intel Corporation's 2006 Supplier Continuous Quality Improvement (SCQI) award. This is the fourth consecutive year Asymtek has been honored with the SCQI, Intel's most prestigious award and highest honor for its suppliers for outstanding commitment to quality and performance. Asymtek, which received the award for its efforts in supplying Intel with automated dispensing systems, was one of only 10 companies to receive a 2006 SCQI award.

Visit www.asymtek.com for more information.

RENESAS and KINESYS - ALPS Agreement

KINESYS Software Inc. and RENESAS Eastern Japan Semiconductor Inc. have signed an OEM agreement that will have RENESAS offer ALPS OEM as it's primary wafer and strip mapping software. RENESAS was the number one Die attach supplier in 2005 and looks to lead the industry again in 2006 and 2007.

KINESYS and RENESAS are joining forces to offer the industry a very powerful technology in die attach that allows full compliance with the latest SEMI Standard E142. Combined with other assembly process steps, it furthermore enables the complete die traceability from wafer probe to final device test and singulation. The ability to offer Single Device Traceability (SDT) to the backend assembly market will increase over time, as KINESYS expands its OEM Partnership Program to other equipment venders and process steps within final assembly and test.

RENESAS and Kinesys are already cooperating with IDM's and Subcontract assembly companies to rollout complete SDT in 2007, a trend that is here to stay as end users of sophisticated and complex IC packages demand both process and failure traceability on a component level.

For additional information on RENESAS or KINESYS products and services visit www.kinesyssoftware.com or www.tosemi.renesas.com.

Indium Corp Expands Sales Efforts in the US Southwest

CLINTON, NY – Indium Corporation announced that KTEC Equipment and Supplies has become its distributor covering the state of Arizona. KTEC is responsible for distributing Indium's solder pastes, rework fluxes, wave fluxes, flux-cored wire, solder bar, solid wire, and tape & reel solder preforms.

KTEC Equipment and Supplies is an industrial distributor with highly integrated supply solutions for the electronic manufacturing industry. Established in 1985, KTEC is a federally recognized minority-woman-owned company. With a new facility, and over 15,000 square feet of warehouse space, KTEC is positioned to support the ever-demanding needs of the electronics manufacturing industry.

For more information about Indium Corporation visit www.indium.com or email askus@indium.com.

Asymtek Introduces New Axiom X-1030 Series Inline Flux Dispensing System

CARLSBAD, CA – Asymtek has announced the release of its new Axiom X-1030 Series dispensing system, designed for selective jetting of traditional flux, no-clean solder fluxes and other precise coating applications. Available in single or dual lane configurations, the closed-loop X-1030 dispensing system optimizes underfill and package reliability – improving production throughput and equipment utilization by as much as 60-85% with the X-1032's dual lane multitasking capabilities. Configured with Asymtek's DJ-2200 DispenseJet® valve with coaxial air technology, the Axiom X-1030 Series is ideal for jetting ultra-thin flux film builds.

The Axiom X-1030 Series dispensing system is configured with Asymtek's Fluidmove® for Windows® XP (FmXP) software for precise control of the dispensing pattern. The Axiom system interfaces with other equipment upstream and downstream using SMEMA-standard hardware and software protocols.

For more information visit www.asymtek.com.

AIT Receives JEDEC Approval for Its Etched Leadless Package

SINGAPORE – Advanced Interconnect Technologies has announced that it has received approval from the prestigious Joint Electron Device Engineering Council (JEDEC) for its QFN-style Etched Leadless Package (ELP) technology. JEDEC, the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry, approved AIT's Microelectronics Outline document MO-247 and Design Guide 4.19 for ELP.

AIT's patented ELP is a Quad lead-free staggered and in-line multi-row package with metallized terminals along the edges of the bottom surface. The distinctive design makes the leadframe mechanically and thermally robust, eliminating distortions and deformations during the chip attach and wire-bonding process. The package is offered in two- or three-row configurations. Compared to other QFN packages currently available in the market, ELP offers several benefits, including smaller footprint, lower cost and design flexibility for higher I/O count.

For more information please visit www.aithome.com.

Infotonics Selects SUSS Bonding Systems for MEMS R&D Center

MUNICH – SUSS MicroTec has announced that Infotonics, a collaborative, world class Center of Excellence in photonics and microsystems, has selected the SUSS ABC200 wafer bonding cluster tool and FC150 device bonder as strategic investments in their MEMS packaging lab.

With corporate partners such as Corning, Eastman Kodak, and Xerox, as well as relationships with over 20 universities, Infotonics has played a central role in groundbreaking work to benefit the biomedical and communications industries. Infotonics' core competencies include the design, simulation, fabrication, packaging, test and metrology for MEMS and MOEMS devices. By using the facilities at Infotonics, customers can develop and deliver innovative products at reduced risk and cost, accelerating their time to market.

STATS ChipPAC Receives Intel's PQS Award

U.S. and Singapore – STATS ChipPAC Ltd. was named a recipient of Intel Corporation's Preferred Quality Supplier (PQS) award for outstanding performance in providing products and services deemed essential to Intel's success. The company was recognized for its efforts supplying Intel with full turnkey packaging and test services. STATS ChipPAC and 43 additional PQS award winners were honored at a celebration in Burlingame, California on March 27.

The PQS award is part of Intel's Supplier Continuous Improvement (SCQI) process that encourages suppliers to strive for excellence and continuous improvement. To qualify for PQS status, suppliers must score 80 percent on a report card that assesses performance and ability to meet cost, quality, availability, delivery, technology and responsiveness goals. Suppliers must also manage and deliver on a challenging improvement plan and a quality systems assessment.

Further information is available at www.statschippac.com.

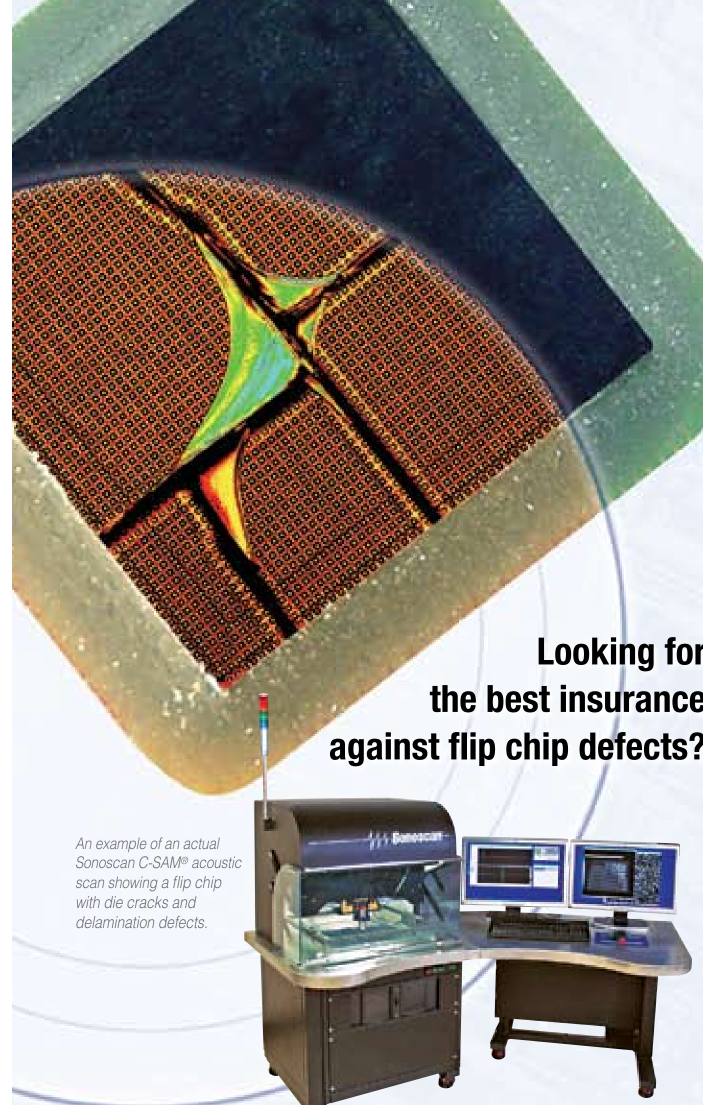
Dedicated R&D Activity Will Focus On Advanced Wafer Integration

U.S. and Singapore – STATS ChipPAC Ltd. has announced the establishment of a new R&D facility located in Singapore which will be dedicated to developing next generation technology including through silicon via (TSV) and microbump bonding for three dimensional (3D) die, silicon substrate based packaging solutions, and embedded active die technology. The new R&D facility includes over 10,000 square feet of Class 10, 100 and 10K cleanroom space with an additional 9,000 square feet of space available for future expansion. The R&D operation will specialize in wafer level processing with an equipment set for photolithography, plasma etching and deep reactive ion etching (DRIE), wafer thinning, and wafer bonding. A strong engineering workforce of 40 employees will focus on advanced wafer integration technology.

Further information is available at www.statschippac.com.

Air Liquide Electronics Thinks Outside the Fab for Copper Cleaning Applications

HOUSTON and DALLAS, TX – Air Liquide Electronics U.S. LP announces the recent commissioning of a new Chemical Mechanical Planarization (CMP) applications and development laboratory near its Dal-



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las, Texas headquarters. The new facility, a multi-million dollar investment by the company, focuses on the CuClean family of post CMP copper clean chemistries, as well as other innovative CMP solutions.

Chemical Mechanical Planarization is a semiconductor manufacturing process that uses slurries consisting of abrasive particles and ancillary chemicals to clean and condition semiconductor wafers during the fabrication of integrated circuits. Post CMP cleaning is a subsequent step that removes organic and particulate contaminants that remain on the wafer surface from the CMP process.

The new facility features an industry-standard 200 mm integrated polisher/cleaner tool and associated surface and chemical metrology equipment. The CMP platform is equipped with multiple distribution lines for slurries and cleaning chemistries used to assist in evaluating materials and consumables as well as customer processes. These tools and the expert capabilities available at the facility give customers access to engineered solutions to their CMP needs without significant impact to ongoing operations, enabling them to test real time solutions and benefit more quickly from potential cost savings.

For additional information on Air Liquide Electronics' CMP offerings, contact: copper.clean@airliquide.com.

Gel-Pak's New Product Selection Wizard Optimizes Die Carrier Selection

HAYWARD, CA – Gel-Pak, a division of Delphon Industries, has announced the launch of its new web-based Product Selection Wizard (PSW), an interactive program that uses a series of targeted questions to recommend the ideal Gel-Pak carrier based on each customer's detailed application. The product selection wizard is available through the company's website.

Gel-Pak manufactures custom Gel-Boxes, Gel-Trays, Gel-Films, and Vacuum Release (VR) carriers that offer maximum protection during the shipping, handling and processing of valuable devices. The Product Selection Wizard was created to assist customers in finding the optimum Gel-Pak carrier for their particular device and application.

For further information on Gel-Pak's product line, please visit www.gelpak.com.

QLP Announces Industry Breakthrough in Plastic Hermetic Packaging

WILMINGTON, MA – Quantum Leap Packaging, Inc. (QLP) a leading provider of high performance, air cavity packages for semiconductor assembly has announced the availability of HermeTech™ , the industry's first hermetic plastic package that meets JEDEC standards.

QLP is manufacturing HermeTech™ plastic air cavity QFNs that maintain hermetic leak rates of less than 5x10-8 atm cc/s He, and pass full Mil Spec reliability tests.

Through a combination of its unique Quantech™ material technology, and innovative UltraSeal™ ultrasonic lid process, QLP has developed HermeTech™ plastic hermetic QFNs that feature tailorable properties, low moisture permeability and high temperature stability that enable true hermetic performance.

Ideal for advanced packaging applications such as Image Sensors, HB-LEDs, MEMs, LDMOS and RF Microwave devices, QLP's HermeTechTM QFNs provide packaging solutions to critical needs such as low

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DESCRIPTION

The silicon based MSM series microphones are integrated with specialized pre-amplification ASIC to provide high sensitivity, high signal to noise ratio output from a capacitive audio sensor. Packaged for surface mounting and high temperature re-flow assembly, it routinely operates in adverse conditions that would permanently damage conventional microphones

FEATURES

- Available in Top Mount, Reverse Mount, Differential
- Sensitivity Ranges, -20dB to -45dB
- Low Profile, 1.25mm
- Operating Voltage, 1.5 ~ 3.6V
- Current Consumption, 150µA Typical
- S/N Ratio, 58dB Typical
- THD less than 1% @ 110dB SPL
- Sensitivity Variation, ≤1.5dB
- Ultrasonic Range, 20KHz ~ 80KHz
- Operating Temperature -40°C to 100°C
- Reflow Temperature, 260°C
- RoHS Compliant

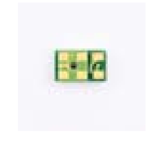
APPLICATIONS

- Mobile Phones
- Laptops Computers
- PDA
- Portable Media Player
- MP3 Player
- Digital Camera
- Video Camera
- Voice Conferencing System
- Hands Free Car Kit
- Ultrasonic Applications
- Microphone Arrays
- Security System
- Industrial Applications - Noise Monitoring, Safety, Flow Monit

Top Mount

MSM1C MSM2C MSM3 / MSM3D

Reverse Mount



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STATS ChipPAC's New Fan-in Package on Package Solution Drives Functional Integration in a Smaller Footprint

U.S. and Singapore – STATS ChipPAC Ltd. has announced a new Fan-in Package on Package (FiPoP) solution which delivers increased functional integration in a smaller form factor, flexibility in stacking conventional memory packages on top, improved final assembly yields, and a lower overall cost as compared to conventional PoP solutions. FiPoP has a versatile design which accommodates multiple die and larger die sizes in a reduced footprint and the flexibility to stack off the shelf memory packages with center ball grid array patterns on the top surface.

STATS ChipPAC's new Fan-in PoP solution opens up the range of integration options in the bottom PoP package while allowing greater freedom in stacking off the shelf memory packages on top. Fan-in PoP provides the flexibility to stack multiple logic, analog and memory die in the bottom PoP package and accommodates larger die sizes in a reduced footprint as compared to conventional PoP designs. The Fan-in PoP structure provides the unique advantage of being able to mount smaller conventional memory packages with center ball grid array patterns on top.

STATS ChipPAC has developed two versions of Fan-in PoP. One version incorporates a fully tested Internal Stacking Module (ISM) package for integration of fully tested memory or other device types within the bottom package. The second version integrates probed good or known good die stacked in the bottom package. Conventional memory packages can be stacked on top of either Fan-in PoP design during the board mount process.

Further information is available at www.statschippac.com.

Tessera Unveils World's First Wafer-Level Camera Technology for Mobile Phones

SAN JOSE, CA – Tessera Technologies, Inc. has announced OptiML™ WLC (also known as OptiuL™ WLC), a new wafer-level camera technology designed to significantly advance the integration of miniaturized cameras in mobile phones, personal computers, security cameras, and other electronics. Tessera's OptiML WLC technology makes it possible for cameras to be manufactured at the wafer level, drastically reducing the size and total bill of material cost of camera modules. As a result of these and other significant benefits, Tessera is providing the electronics industry a powerful tool for integrating cameras into a wider range of electronic products.

Tessera's solution is designed to overcome the cost, size and manufacturing roadblocks facing the industry as cameras become pervasive in mobile phones and other electronics. Using OptiML WLC technology, thousands of lenses are manufactured simultaneously on a wafer, and then bonded at the wafer level to create the optical element of the camera. The result is simplified assembly and up to 30% cost savings for the optical component of the camera module. OptiML WLC technology also reduces the size of the camera to a minimum, delivering up to 50% size reductions over conventional camera modules in camera phones today.

For more information go to www.tessera.com.

K&S Releases A New Ultra Soft Copper Wire

FORT WASHINGTON, PA – Kulicke & Soffa Industries, Inc. introduces the new MaxSoft™ copper bonding wire engineered for a variety of discrete and IC applications. This new copper wire has unique physical properties that reduce IC bond pad stress and significantly improve 2nd bond strengths.

With the new MaxSoft copper wire, customers now have a more reliable and cost-effective technology for fine wire utilized in copper wire bonding of ICs.

Applications using copper wire for bonding can prove challenging since copper inherently deforms less readily than gold wire, causing higher stress on the bond pad. K&S laboratory results have shown that due to its lower wire hardness, MaxSoft reduces pad damage and provides stronger intermetallic connections.

Second bond strength and consistency are more challenging attributes for copper wire compared to gold wire, particularly in fine-pitch applications. This has created limitations to copper wire bonding. During K&S testing, MaxSoft obtained up to 35% higher 2nd bond pull responses compared to conventional copper wire, with increased bonding robustness.

The new MaxSoft copper wire is available from 0.8 to 1.3 mil diameters and has a long shelf life of six months when stored in the recommended conditions inside the original packaging.

Visit Kulicke & Soffa's on the web at www.kns.com.

Tessera Introduces Next-Generation Interconnect Platform

SAN JOSE, CA – Tessera Technologies, Inc. has announced the MicroPILR™ Interconnect platform, a highly innovative technology family that is designed to revolutionize the interconnect within semiconductor packages, substrates, Printed Circuit Boards (PCBs) and other electronic components. The novel interconnection is achieved through low-profile, pin-shaped contacts which replace conventional technologies used today, such as solder balls on semiconductor packages and plated vias in package substrates and PCBs. These contacts deliver a number of key benefits needed to meet emerging product roadmaps, including significantly reduced profile, fine pitch, improved electrical and thermal performance, and enhanced reliability. By addressing the technical limitations of current generation interconnect, Tessera's MicroPILR platform has the potential to become a fundamental building block of next-generation mobile, computing and consumer electronic products.

A key demonstration of the

technology has been in a high density, package stacking application. Working closely with one of the world's preeminent semiconductor manufacturers, Tessera has developed an 8-die FLASH package stack that is less than 1.2 mm thick. Each individual package can be tested prior to stacking which results in near 100% stacked yield.

With the unveiling of this new technology, Tessera is introducing its next-generation packaging family while significantly expanding its product offering to include PCBs and other interconnect applications. Prismark estimates the interconnect market (including multilayer PCBs and advanced package assembly) will grow from approximately $34Bn in 2006 to $51Bn in 2011.

For more information on Tessera's MicroPILR technology family, go to www.tessera.com.

SUSS Unveils the KADETT; a New High Accuracy Placement and Bonding System for R&D

FRANCE – SUSS MicroTec has unveiled the KADETT, a new High Accuracy Placement and Bonding ystem especially configured for R&D laboratories, universities and pre-production environments.

The new SUSS KADETT Semi-Automatic Device Bonder is a flexible and open platform for accurate assembly and bonding of devices on a large variety of substrates. The machine performs accurate Pick and Place functions. A wide range of bonding processes including In-Situ Reflow, Thermo-Compression, Thermo-Sonic and Adhesive Bonding are available for forces up to 75N.

The KADETT, originally developed by the Paul Scherrer Institute, has been proven in the field for bonding Ionizing Radiation Detectors and it is also well suited for advanced packaging, micro-optics or MEMS assembly.

Accurate alignment is automatically achieved by a vision system which uses two independent high resolution video microscopes (chip and substrate) with a high resolution (0.1μm) XY alignment stage. The flexible architecture of the SUSS KADETT enables the integration of many processing modules such as a UV glue curing system, Ultrasonic bonding head and many others. ◆

North American Semiconductor Equipment Industry Posts April 2007 Book-To-Bill Ratio of 1.00

SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.60 billion in orders in April 2007 and a book-to-bill ratio of 1.00 according to the April 2007 Book-to-Bill Report published by SEMI. A book-to-bill of 1.00 means that $100 worth of orders were received for every $100 of product billed for the month.

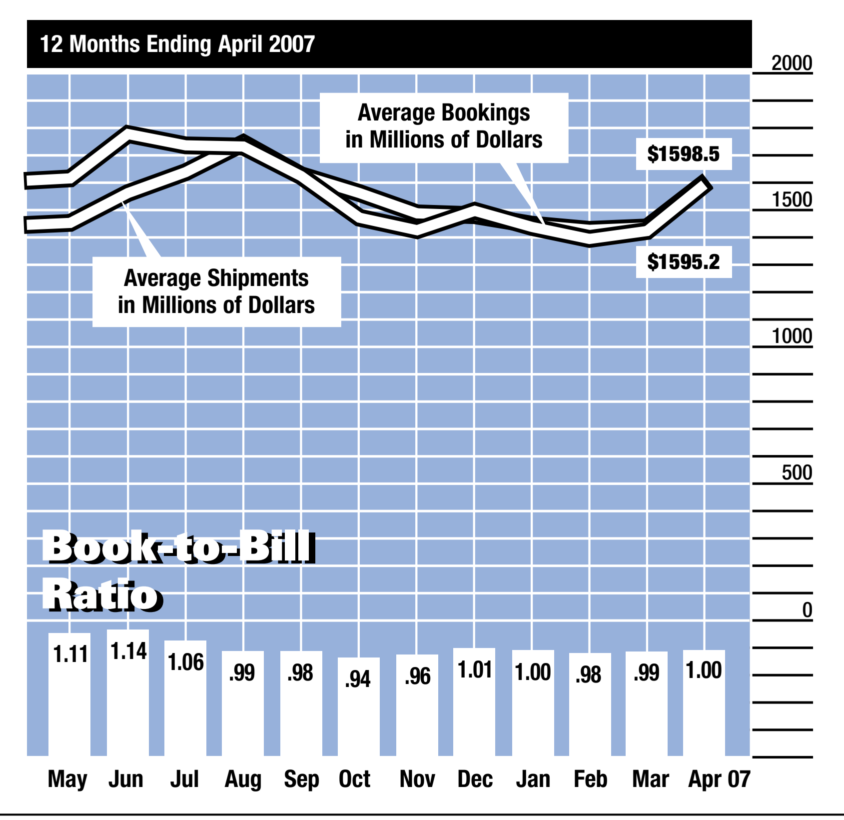
The three-month average of worldwide bookings in April 2007 was $1.60 billion. The bookings figure is over 12 percent higher than the final March 2007 level of $1.42 billion and even with the $1.60 billion in orders posted in April 2006.

The three-month average of worldwide billings in April 2007 was $1.60 billion. The billings figure is over 11 percent than the final March 2007 level of $1.44 billion and almost 11 percent higher than the April 2006 billings level of $1.44 billion.

"This year, several large integrated device manufacturers are believed to be investing a substantial part of their capex in the first quarter. This is one reason that the April book to bill report shows strong gains in both billings and bookings for new semiconductor equipment from North American based suppliers," said Stanley T. Myers, president and CEO of SEMI.

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments.

Shipments and bookings figures are in millions of U.S. dollars. ◆



MEPTEC Member Company Profile

Pac Tech is a world leading provider of advanced wafer bumping, packaging, and solder-ball placement equipment. As an innovator in the area of laser assisted solder-jetting processes and chip bonding, Pac Tech also provides state-of-the-art worldwide contract services for low-cost wafer level bumping and packaging offering competitive pricing and the highest quality.

PAC TECH is divided into two unique business units with 150 employees worldwide. The Wafer Level Packaging and Bumping business unit offers state-of-the art wafer bumping and packaging services based on a proprietary electroless nickel under-bump metallization. The Advanced Packaging Equipment business unit focuses on manufacturing special equipment designed for advanced laser bonding and wafer bumping.

Since its founding, Pac Tech has received more then 50 patents for products developed in areas relating to semiconductor interconnection, including wafer bumping, flip-chip, chip-scale packaging and laser bonding technologies. Pac Tech has also formed alliances with companies in the United States, Europe and Asia for licensing, equipment sales, and contract wafer bumping services.

In 1997, Pac Tech began operations from its new, permanent headquarters located in Nauen, Germany. This 108,000 square foot facility is designed for cleanroom, subcontractor, wafer bumping with a capacity of 300,000 wafers per year, as well as equipment design, development, and manufacturing.

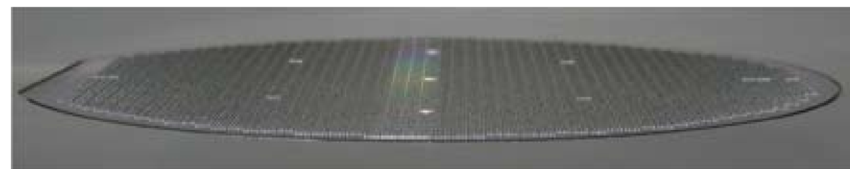
In 2002, Pac Tech USA - Packaging Technologies Inc., a wholly owned subsidiary of Pac Tech GmbH, opened its new 10,000 square foot contract wafer bumping facility in the heart of Silicon Valley,

Pac Tech GmbH Facility in Nauen, Germany

California. The facility has a wafer bumping capacity of 600,000 wafers per year and is capable of handling wafers up to 300mm.

In February 2006, Nagase Co. Ltd., is a major Japanese trading and manufacturing company with over 3,500 employees worldwide and sales of over $6 billion U.S. dollars, acquired a 60% share of Pac Tech GmbH. Pac Tech and Nagase have been working together since 1998. Licensing the Pac Tech process resulted in Nagase founding Alpha Bumping Technology (ABT) in Fukui, Japan. Out of its new Fukui facility, Nagase/ABT offers the electroless Ni/Au bumping process for the Japanese market.

In December 2006, Pac Tech Asia Sdn. Bhd., a wholly owned subsidiary of Pac Tech GmbH, purchased its new 53,500 square foot contract wafer bumping facility in Penang, Malaysia. 40,000 square feet of the facility floor space will be dedicated to manufacturing much of it in a clean room environment. When completed, the facility will be equipped with the latest generation of equipment aimed at supporting semiconductor market requirements for low-cost wafer bumping and backend processing. Like the Silicon Valley facility it will have an initial capability of processing 600,000 wafers per year will handle wafers up to 300mm but will add capability with expected growth in demand.



WL-CSP wafer after solder-ball attach

Pac Tech is well positioned to improve its position as a global leader in advanced packaging equipment manufacturing, contract wafer-bumping services, and turnkey equipment solutions. The new facility will soon become Pac Tech's largest with respect to its total wafer volume and available process capabilities, including back-end processing. It is designed to meet the most competitive demands of the market for low-cost and high volume production.

While a wide range of contract services will be offered at the facility, Pac Tech plans also to begin manufacturing its plating systems and solder ball placement equipment at the site.

Pac Tech's Asian facility in Penang, Malaysia

Equipment

Advanced Solder-Ball Bumping (Solder- Jetting)

The solder-ball bumping equipment is able to place and reflow 60μm to 760μm solder balls of various lead or lead-free alloys, with lead pitches of ≥100μm. The SB2-Jet product line offers ball placement rates of up to 10 balls per second. The laser solder ball bumping is ideal for quick-turn, fluxless, maskless bumping on wetable surfaces suitable for wafer-scale CSP, flip-chip, BGAs, optical component attach, MEMs, hard disk drive assembly, and 3-D packaging.

Low-Cost Wafer Bumping

Pac Tech's advanced modular Ni/Au and Ni/Pd/Au bumping equipment offers fully automatic electroless bumping for wafers ranging in size from 4- to 12-inches. Normal output for 5μm nickel UBM plating with 0.05μm immersion gold onto aluminum or copper pads on an 8-inch wafers is 150 wafers per hour.

Pac Tech's unique process and chemistry control features place this equipment at the forefront of the industry, setting the standard for performance and quality.

Laser Flip-Chip Attach

The LAPLACE system provides an integrated solution for flip-chip and capacitor/resistor attach. The laser-assisted assembly process allows placement and reflow/curing at the same time at minimal thermal stress and can be applied

for soldering, ACF, and NCP interconnections. The integrated dispensing unit in the flip-chip assembly platform allows a maximum flexibility for flux, solder paste, and/or ACF, NCP dispensing.

With up to 5,000 placements per hour (pick and place) LAPLACE is a solution for Smart Cards, Smart Label products, LCD-drivers, flip-chip on flex and flip-chip on board applications. Soldering and curing of underfill is done simultaneously by use of a laser.

Additional Equipment Solutions

In addition to the systems described above, Pac Tech manufactures equipment for Micro Gang Ball Placement, Laser Marking, Wafer Spin Coating and Flip-Chip Bonding.

Services

Pac Tech now has three facilities offering state-of-the-art electroless Ni/Au wafer bumping and selected backend services. Using the most advanced technology and processes available in the industry, Pac Tech offers customers highly competitive, low-cost bumping technology for quick-turn and mass-production quantities. A highly trained team dedicated to customer satisfaction accomplishes this for each and every customer, regardless of size.

Advanced Processes

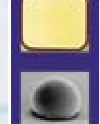
- Low-cost wafer bumping using electroless Ni/Au and Ni/ Pd/Au
- Solder stencil printing
- Solder-ball placement for wafer level CSP
- Wafer thinning
- Backside metal sputtering
- Wafer backside laser marking
- Wafer sawing
- Electrical testing (Available in Asia and in Germany Q1/2008)
- Tape-and-reel processing (Available in Asia 2008 and in Germany Q1/2008)

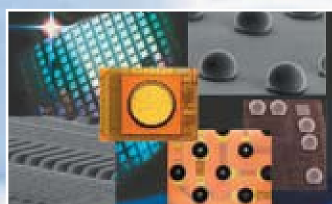
Applications Supported

- Ni/Au under-bump metallization for copper and aluminum devices (flip-chip)
- Solder-ball placement for wafer-level CSPs down to 200μm ball diameters
- Micro solder-ball placement for fine-pitch applications down to 120μm (high I/O count flip-chip)
- Tall Ni/Au bumping for Smart Card and Smart Label applications (RF ID)
- Ni/Pd/Au bumping for advanced power MOSFET devices and gold wire bonding applications
- Low-cost Ni/Au metallization and screen-printing for solar cells and photovoltaic devices
- Fluxless and contactless solder jetting for MEMS and opto-electronics
- 300mm wafer capability

Pac Tech's GBP-200 Gang Ball Placement Equipment

PacLine-300 A50 Wafer Bumping Equipment





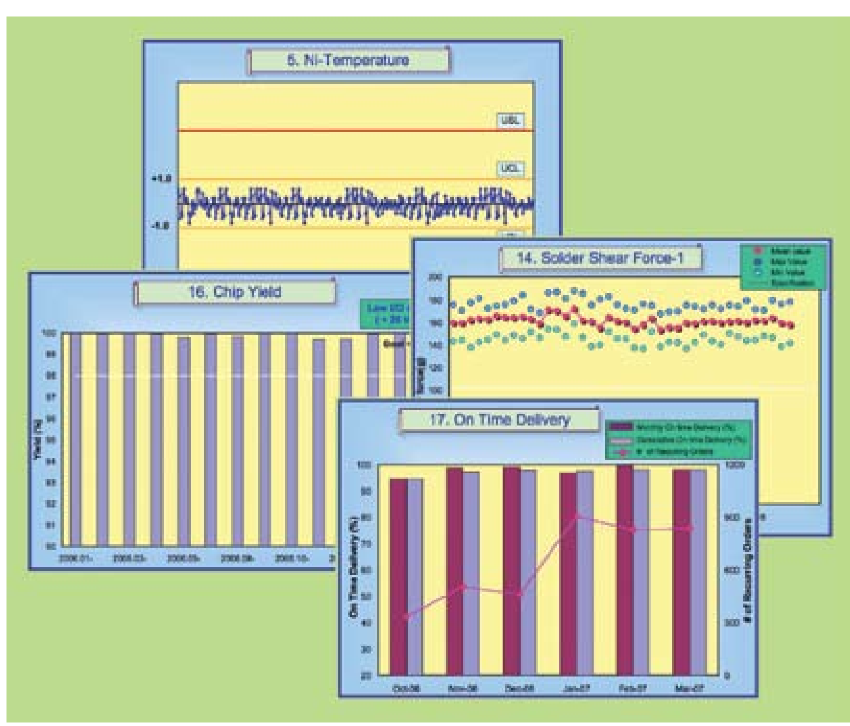
Pac Tech's various bumping applications

Pac Tech's LAPLACE For Laser Flip-Chip Attachment

Quality

Customer satisfaction is the first order of business for Pac Tech. Pac Tech is committed to provide equipment and advanced packaging services by applying the high quality and reliability standards demanded by today's customers. To accomplish this, Pac Tech uses state-of-the art process monitoring tools including electronic control charts and statistical process controls (SPC). Detail orientation to every customer's needs is what Pac Tech's goal — whether the volume is large or small. Systems are in place for pro-actively soliciting customer feedback to ensure customer satisfaction.

Pac Tech's Nauen, Germany facility is ISO 9001:2000 and ISO TS 16949:2002 certified and Pac Tech's Santa Clara, California facility is ISO 9001:2000 certified.



Typical Pac Tech SPC monitoring charts

Pac Tech's Quality Policy

"Pac Tech's primary objective is the complete understanding of all customer requirements in accordance to the company philosophy of being a supplier of highly specialized innovative services for the forward looking IC packaging technology market. To realize this objective strongly depends on the quality of their products and services. Quality is a company obligation to all customers and therefore a continuous task of all employees. Proceeding from these principles, Pac Tech wants to be a reliable partner to their customers as well as for their suppliers and business partners."

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Frame Level Packaging: Performance Gain with Less Pain

An Integrated Solution for Performance Enhancement

Dr. Charles Lin and Jerry Tan
Bridge Semiconductor Corporation

IC packaging will remain a key enabler in the development of future ICs and devices. New IC packaging technologies are often notoriously expensive to implement and frequently result in significant changes to the manufacturing infrastructure. This article describes how an innovative and yet practical frame level packaging approach can be used to deliver enhanced performance packages at competitive cost using a smart combination of existing manufacturing technologies. The result will still require package and technology qualification; however, the manufacturing infrastructure in place will not require expensive new equipment.

With new devices, technologies and applications emerging in many market segments, packaging technology is now a critical competitive factor as it affects operating frequency, power, complexity, reliability and cost. While many players have developed innovative package designs using lead-frame, laminate and wafer level packaging technologies, very few have seriously examined the possibilities of combining the competitive advantages of these technologies in one package. Bridge Semiconductor Corporation has successfully developed an innovative and yet practical Frame Level Packaging approach by combining various package-specific electrical, mechanical and thermal strengths in a packaging methodology with the objective of achieving enhanced performance and functionalities at competitive cost as these are keys for market acceptance.

Key Learning from Existing Packaging Technologies

Generally, lead-frame based packages are well-known for their excellent reliability and thermal performance made possible using a molded structure and copper based frame to ensure minimal CTE mismatch. Though lead-frame based packages offer the most competitive cost structure and are suitable for medium I/O applications, the technology is typically constrained by having only fan-out capability, insufficient design layout flexibility and relatively higher parasitics.

It can be said that laminate-based packages were developed to address the limited I/O in lead-frame based packages. Better design flexibility becomes achievable using advanced PCB multi-layer technology for finer routing features. With the rising popularity for new functionalities and increased capacity within a package, assembly processes have also been successfully developed using laminate-based substrates with Surface Mount Device (SMD) assembly and 3D stacking capabilities to address market needs. However, since laminate typically uses low thermal conductive material, it may experience limitations in high power device applications.

Wafer level packages are well-known for their excellent electrical performance made possible with redistribution layer on the wafer surface and flip chip technologies. However, while WLP provide fan-in only capability and attractive form factor, there are costs and yield concerns especially if there are insufficient volume and limited good dies on the wafer. Another concern involves the necessity to redesign the PWB when die shrinks as the footprint will likely change.

What is Frame Level Packaging?

Frame level packaging is a technology which uses a copper frame as the platform to manufacture advanced packages with enhanced performances. The conceived copper base frame has been fortified with functional features such as routing circuitry to enable single chip, flip chip, 2D and 3D Modules to be packaged with BGA, LGA and QFN formats incorporating specific electrical, mechanical and thermal strengths found in existing packages.

Integrating the key learning of conventional packages, this technology can accommodate different devices in combination with various interconnect technologies (e.g., wire bonding, flip chip, and surface mounting) within the same package and is capable of handling low to moderate I/O density requirements, as typified by DRAM, Flash, Analog, RF, Optoelectronics and other ICs with less than 200 total I/Os and adequate silicon area.

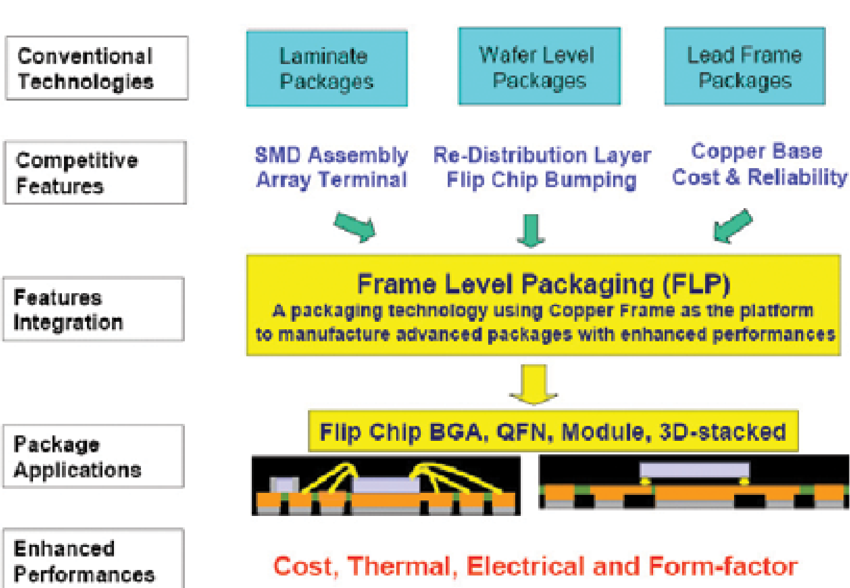


Figure 1. Frame Level Packaging: an integrated approach.

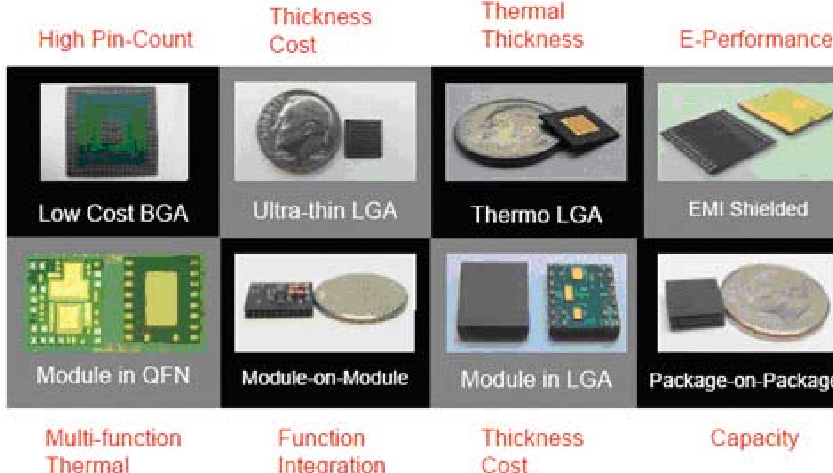


Figure 2. Enhanced performance features.

Broadly speaking, frame level packaging provides a manufacturing platform for integrated device manufacturers (IDMs), fabless semiconductor houses, assembly houses and substrate suppliers to tap on and enjoy "Integration Across Many Technologies and Markets Simultaneously". The design flexibility features & enhanced performances offered by frame level packaging integration provide an optimal solution for a variety of package options as illustrated in figure 1.

Performance Features

Generally, frame level packages are very suitable for small size and ultra-thin packages that require excellent electrical and thermal performance (see figure 2). Any application requiring high frequency and high power package performance, light weight, and small package size may choose the frame level package, especially for telecommunications (wireless applications like cellular phones, handsets, wireless cards, base station and wireless LANs), portable products (personal digital assistants, digital cameras, portable media players and camcorders) and low to medium lead count packages (information appliances application).

Where Does Frame Level Packaging Fit?

In any discussion on new technologies, the controversial and often emotional subject on "where does it really fit" invariably rears its ugly head. As no one packaging technology is superior to another and to better envisage what frame level packaging is capable of achieving, five performance metrics have been selected for comparison with the expected performances of both frame level and existing packages – 1) form-factor, 2) cost, 3) electrical performance, 4) thermal performance, and 5) design flexibility.

The performance metrics indicate how packages built using frame level packaging are expected to perform compared with selected existing packages – i.e. to deliver cost competitive packages with design flexibility to achieve superior electrical & thermal performances and attractive form factor. Two examples are being described to illustrate the performance limitations of and challenges faced by existing packages to provide insights on the issues that frame level packaging undertakes to overcome.

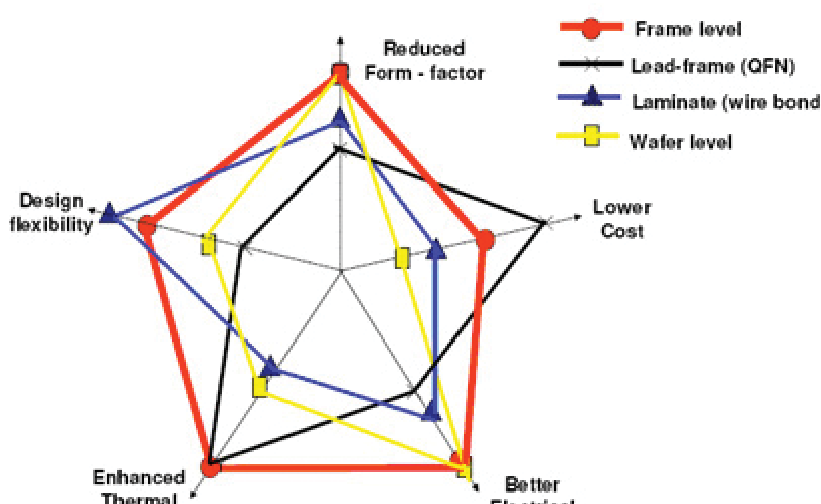


Figure 3. Expected performance metrics.

What Issues Do Frame Level Packaging Address?

In high performance or form-factor driven type applications, wafer level packages have been proposed due to electrical and size advantages. However, WLPs have not gained wide adoption for many devices due to the Re-Distribution Layer (RDL) limiting the package within the die dimension, coupled with the costly thin film manufacturing process.

Currently, the QFN package has been proposed for telecommunication module applications as the exposed die paddle can serve as a common ground and allow direct heat dissipation. However, as the QFN mechanical structure makes it difficult to incorporate solder mask features to accommodate passive components assembly, the industry is inclined to stay with laminate type packages as a trade-off. This could result in potential lost opportunities for QFN packages as passive assembly capability is a much needed requirement in many wireless applications.

While a number of new processes have evolved to provide high density interconnects (HDI) including sequential build up substrate (SBU), not only are the substrate costs prohibitive, its technical and reliability limitations are significant. As the wiring density and the through holes dimension of the core are significantly coarser than those in the build-up layers, the core can provide only limited wiring function for the connection between the front and back side of the build up layers. As a result, even though flip chip terminal pitches can be easily accommodated by the wiring capability in the build-up layers, the through-hole in the core actually imposed a severe restriction on the wiring capability of the second build up layer. In addition, the plated through holes in the core often destroys the integrity of the voltage layer as it increases capacitance loss and electrical noise.

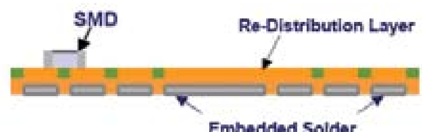


Figure 4. Fortified copper frame.

Frame level packaging aims to resolve these issues amongst others and can address specific application needs using the conventional manufacturing infrastructure. The technology platform addresses the industry needs by adopting standard industry package outlines, footprints, materials & processes to accelerate industry acceptance.

Fortified Copper Frame

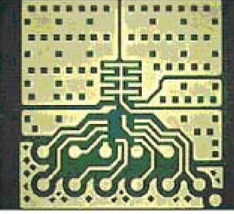
Frame level packaging uses a standard copper frame for the processing panel as a key learning from lead-frame based packages since the material has excellent thermal conductivity and dimensional stability if properly configured (see figure 4). In addition, copper is widely used in the lead-frame and PCB industries, making it the most cost-effective and popular material from the infrastructure readiness viewpoint.

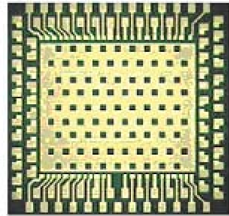
While conventional leaded packages use copper as a base material from which lead fingers are etched or stamped to fan-out the I/O pads, frame level packaging uses a solid copper frame as a base to populate electrical traces and bonding pads. A key learning from wafer level packaging that has been incorporated into the fortified copper frame is the redistribution (RDL) concept with SMD pads being defined simultaneously (see figure 5). The integration of these concepts and features on the copper frame provide for total design flexibility to enable different active and passive devices to be housed within the same package using various interconnect technologies including wire bonding, flip chip, and surface mounting.

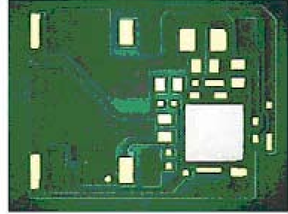
One other laminate-based feature that has been successfully implemented on the copper frame to accommodate higher IO is array terminals. Specifically, solder is embedded on the array terminal copper frame and as solder is locked in the terminals and kept in position by encapsulant during assembly, this feature provides for an extremely high level of board reliability.

In essence, the fortified copper frame serves as 1) a carrier with pre-defined terminal pads for active and passive device assembly, 2) a base for electrodepositing a layer of electrical routing circuitry, and 3) a processing panel in which selective parts will be removed during assembly to achieve enhanced performance and functionalities.

While figure 4 and figure 5 illustrate the key features of the fortified copper frame with a single layer, the fortified copper frame can be further enhanced to serve as a metal-based core carrier to manufacture a high density interconnect (HDI) multi-layer build up substrate to achieve high signal integrity and smaller form-factor for applications in a wide range of advanced packaging innovations including flip chip (FC) and chip-scale packaging (CSP).







Structure Highlights

- Base material: Copper sheet(0.127 mm)
- Routing circuitry (RDL): Electroplated nickel/copper
- Mesh type die paddle design
- Die paddle material selection: Cu/Au/solder mask
- Electrolytic Ni/Au for W/B, flip chip and SMD assembly
- 1st level Interconnects: wire bond, flip chip
- Pre-defined contact terminal with lead-free solder (Sn-Ag-Cu)

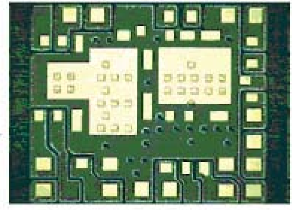


Figure 5. Re-Distribution Layer (RDL) concept incorporated into fortified copper frame.

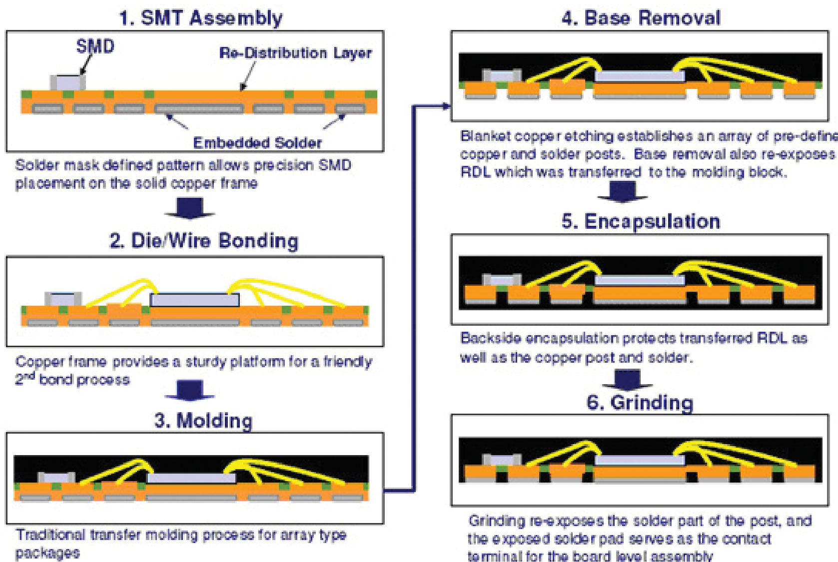
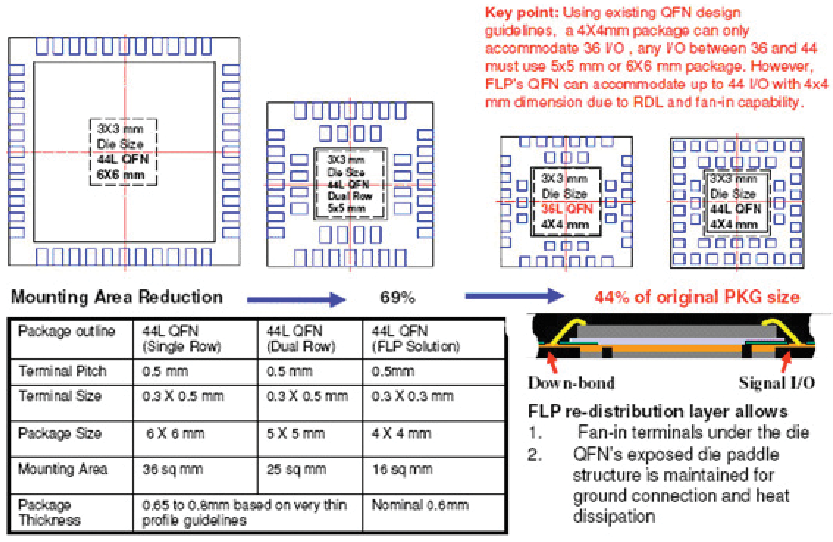


Figure 6. Frame level packaging assembly flow.



Package outline	44L QFN (Single Row)	44L QFN (Dual Row)	44L QFN (FLP Solution)
Terminal Pitch	0.5 mm	0.5 mm	0.5mm
Terminal Size	0.3 X 0.5 mm	0.3 X 0.5 mm	0.3 X 0.3 mm
Package Size	6 X 6 mm	5 X 5 mm	4 X 4 mm
Mounting Area	36 sq mm	25 sq mm	16 sq mm
Package Thickness	0.65 to 0.8mm based on very thin profile guidelines		Nominal 0.6mm

Figure 7. Frame level form factor application.

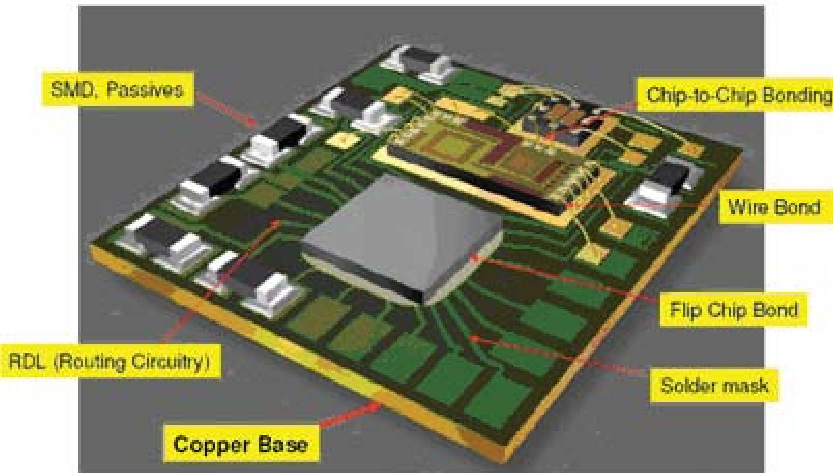


Figure 8. Integrated functionalities using frame level packaging.

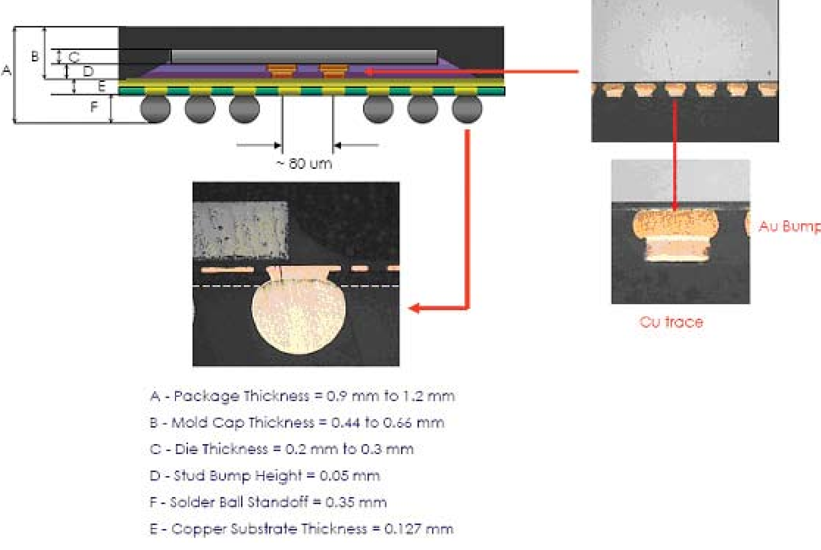


Figure 9. Flip chip GGI BGA structure using frame level packaging.

Assembly Flow

Frame level packaging assembly solutions are built on matured conventional packaging processes as illustrated in figure 6. However, as solid copper serves primarily as a processing panel, there is a need to remove this conductive base after chips and components are assembled and molded. This base removal process will establish an array of isolated solder pads which are each connected to specific IC pads through corresponding electrodeposited electrical traces. The solder pads, comprised of pre-defined copper and solder posts called "terminals", could have dimensions as small as 0.25 x 0.25 mm and these solder pads are reflowed during surface mount assembly. The terminals which are formed on the fortified copper frame during the etching process can be arranged in BGA format or QFN layout. This backend etching approach provides industry with opportunities for the development and implementation of higher efficiency processes and manufacturing platforms to meet the needs of a broad range of next generation packages.

The selective etching of base copper on the embedded solder copper frame followed by encapsulation provides for excellent mechanical support, protection, uniformity and better board-level reliability for the frame level package terminals compared with conventional solder mask defined or non-solder mask defined solder terminals in laminate or ceramic BGA.

Following encapsulation, the subsequent grinding process ensures that terminal height and quality are precisely controlled to achieve ultra-thin package requirements. Where ultra-thin requirements are not be required, a no-grinding assembly flow is available for manufacturing implementation.

Form Factor Application

With increasing need for ultra-thin, smaller packaging, frame level packaging can be the excellent platform to achieve the smallest form factor with enhanced performance. For example, a typical 44 I/O device will require a minimal standard 6x6 mm 0.5 mm pitch single row QFN package to accommodate. If 5x5 mm is required, dual rows QFN become a must for terminal arrangement and inevitably this dual row arrangement will place a restriction on the allowable die size. Hence, any die more than 3x3 mm in a 44L 4x4 mm QFN package will not be practical with reasonable manufacturing yield. However, with frame level packages, a standard 4x4 mm QFN package can be easily achieved (see figure 7).

Module Application

Frame level packaging provides design flexibility for a wide spectrum of packages to be built on the fortified copper frame with enhanced features. In addition, multiple devices can be housed within the molded package using various interconnect technologies to provide integrated functionalities (see figure 8).

GGI Flip Chip Application

Although solder flip-chip assembly is a straight forward technique for frame level packaging, a smart combination of gold stud bumping and gold-gold interconnect (GGI) could possibly offer the lowest cost and most reliable flip chip packaging solution (see figure 9). GGI is a gold-to-gold interconnect formed by thermo-sonic bonding between gold stud bond and gold pad. This gold-gold joint provides superior bond strength due to the monolithic structure of the gold material. This interconnect also maintains low contact resistance, sustains high current flow, and provides superior high frequency performance (low inductance) when compared to wire bond, solder or conductive adhesive materials. Using a copper frame as the bonding base, this thermo-sonic bonding process can reliably handle large die sizes up to 10 mm square, fine bond pad pitches of 80 μm, and I/O counts up to one hundred in high volume manufacturing.

Summing Up

IC packaging technologies will continue to evolve and grow in importance, especially to contain costs and improve performance. The reality of a practical manufacturing platform offering rich opportunities for enhanced thermal, mechanical, electrical performance and attractive form factor with a competitive cost structure has arrived through the introduction of frame level packaging. ◆

Understanding China's Impact on the Semiconductor Industry

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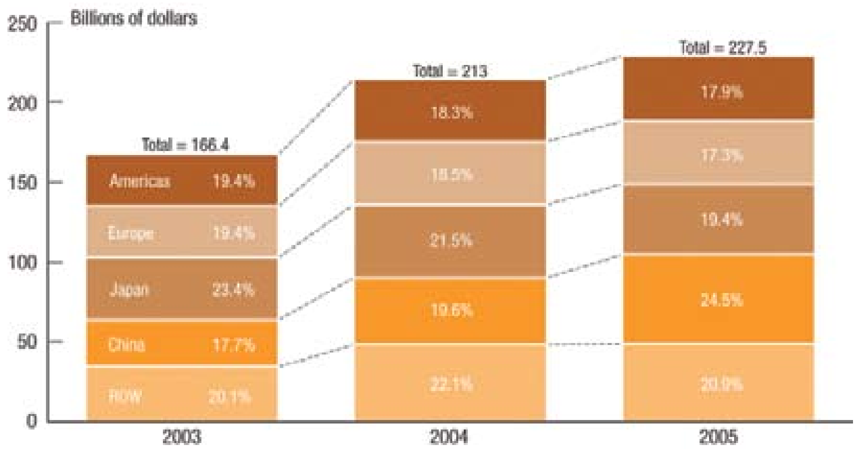
PricewaterhouseCoopers Technology Center

By now there should be no question that China has become a crucial player in the global semiconductor industry. But what industry participants may not realize is that Chinese manufacturing of electronic systems accounted for nearly all of worldwide semiconductor market growth in recent years. Semiconductor consumption in China grew 31 percent in 2005 to reach a new peak of $56 billion and 24 percent of the worldwide market, exceeding the markets in Japan, North America, Europe and rest of the world for the first time. As best we can determine at this time, semiconductor consumption in China grew a further 28 percent in 2006 to $73 billion, accounting for 29 percent of the worldwide market.

China's semiconductor consumption grew during the industry downturn of 2001 and 2002 and continued to grow several times faster than worldwide consumption in the following years. During this decade, China has been taking share aware from other market participants. By 2010, more than one third of the worldwide market for semiconductors could be in China. As a result, if semiconductor companies are not well positioned to serve the Chinese market they face a significant disadvantage.

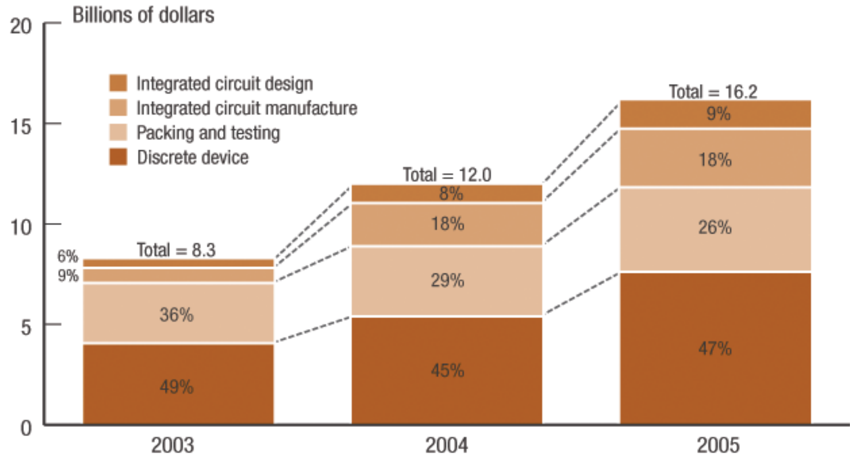
Of the 70 leading worldwide semiconductor suppliers, more than half had below average share of the Chinese market in 2005. This indicates that many major semiconductor companies need to improve their position in China if they want to continue to capture new demand growth. They may need to enhance local presence and business development efforts in order to achieve long term success in China. It is worth noting that despite China's substantial demand for semiconductors, no Chinese companies ranked in the top 70 suppliers to China in 2005.

Growth in electronic systems built in China for export accounts for a substantial portion of semiconductors consumed in China. Almost two thirds of the semiconductors consumed in 2005 were for products exported out of the country, up from 60 percent in 2004. At the same time, a substantial percentage of this demand is also the result of electronic goods produced by Chinese original equipment manufacturers (OEMs). We estimate that 26 percent of Chinese semiconductor demand in 2005 was from domestic OEMs, compared with 20 percent the previous year.



Source: CCID, SIA, 2006

Figure 1. Worldwide Semiconductor Market by Region, 2003-2005.



Source: CCID, CSIA, PwC, 2004-2006

Figure 2. China's Semiconductor Industry by Sector, 2003-2005.

Industry and Market Definitions

Whenever discussing China's impact on the semiconductor industry it is important to distinguish between China's semiconductor market and its semiconductor industry. Semiconductor market refers to the total quantity of semiconductors purchased or consumed in China. Semiconductor industry refers to all companies in China that design, manufacture, package, or test semiconductors, and it includes both multinational and domestic entities involved

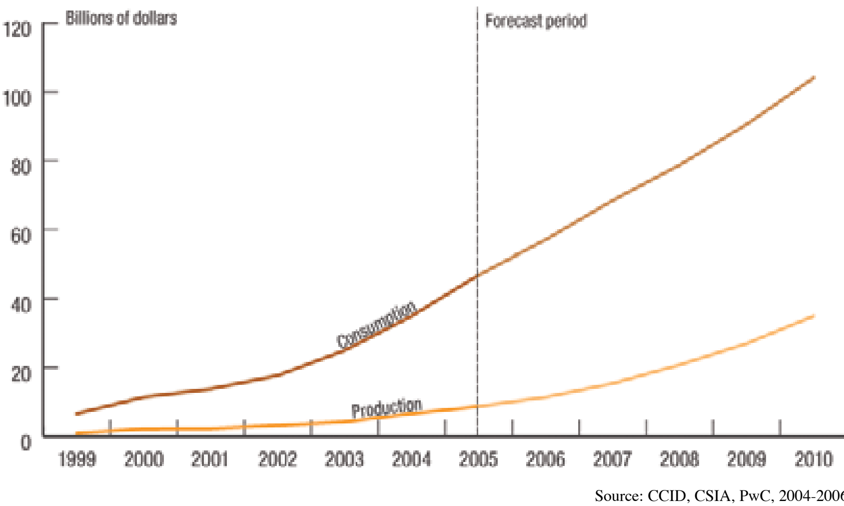


Figure 3. Comparison of China's Integrated Circuit Consumption and Production.

in semiconductor supply or production. Generally as locally reported, China's semiconductor industry is made up of discrete device, packaging and testing (both IDMs and SATS), IC manufacturing (including both foundries and IDMs with wafer fabs), and IC design companies.

China's reported semiconductor industry revenues increased by 35 percent in 2005 to $16.2 billion and accounted for about 6 percent of worldwide production revenue, up from 5 percent in 2005 and 2 percent in 2000. Discrete and IC packaging and testing production accounted for more than 70 percent of China's semiconductor production revenues. IC manufacturing, mainly IC foundries, and fabless IC design companies accounted for the remainder and were growing faster.

Discrete Device

China's discrete device industry continued to be the largest but least publicized sector, accounting for more than 45 percent of semiconductor industry revenue during the first six years of this decade. It increased 41 percent in 2005 to $7.6 billion, representing almost 22 percent of worldwide discrete device revenue. Without the currency revaluation effect, China's discrete device industry grew by $2.0 billion in 2005, while the reported worldwide industry grew by only $400 million. This data suggests that $1.6 billion of discrete device production shifted from other locations to China in 2005—a 5 percent shift in a single year.

Western awareness is low regarding the strength of the discrete market (as well as other areas of the Chinese semiconductor industry), and its associated impact on pricing. For example, because the World Semiconductor Trade Statistics (WSTS) does not have the participation of any Chinese semiconductor companies, it could be missing significant discrete device demand or consumption that is completely satisfied by local Chinese companies. As a result, multinational semiconductor companies may be under-reporting the size of the worldwide discrete and total semiconductor market. And they may be unaware of potential competitors that are developing in a very cost-sensitive environment and are establishing supplier relationships with major electronic manufacturing services (EMS), original design manufacturer (ODM), and original equipment manufacturer (OEM) customers.

Packaging and Testing

IC packaging and testing is the second largest sector of China's semiconductor industry and has the most multinational company participation. It has accounted for almost 30 percent of industry revenue for the first six years of this decade. The value of China's IC packaging and testing production increased in 2005 to represent almost 11 percent of the value of worldwide production, while China's reported IC unit production represented 22 percent of worldwide units. As best we can determine, the value of China's IC packaging and testing sector production increased by a further 45 percent in 2006.

China had 90 semiconductor packaging, assembly and test (SPA&T) facilities (both IC and discrete) by the end of 2005, representing 22 percent of total worldwide SPA&T facilities. Sixty-three of these were SATS facilities, of which 34 belonged to foreign companies and 27 were IDM facilities owned by foreign companies. During 2005, China added a net of 8 SPA&T facilities, or 75 percent of the SPA&T net additions worldwide. Those 2005 additions were large facilities that accounted for more than 90 percent of the net SPA&T manufacturing space added worldwide, thereby continuing the trend of China having the largest share of new SPA&T facilities added worldwide. Various incentives and relatively low land and construction costs have encouraged companies to build large SPA&T facilities and hold significant portions of the manufacturing floor space in reserve for future rapid capacity expansion.

IC Manufacturing

Although IC manufacturing, which has been primarily foundry wafer production, is only the third largest sector of China's semiconductor industry it is the one that attracts the most international press interest. That is probably because of the large capital investments required, the potential equipment market it represents, political concerns over advanced technology transfer, and its potential for disruptive foundry wafer price wars. IC manufacturing has grown faster than the two larger sectors and accounted for 15 percent of China's semiconductor industry revenues during the first six years of this decade.

In 2005, China had 75 wafer fabrication plants in production that would allow China to increase its share of total worldwide semiconductor wafer production from the 2 percent realized in 2003 to more than 7 percent by 2008. During the prior two years, China had put in to production a net of 15 additional wafer fabrication modules—an increase in potential capacity of 49 percent— which accounted for 13 percent of worldwide wafer fab capacity added during 2004 and 2005. Seventy-four percent of China's current wafer fabrication capabilities will be dedicated to foundry production, compared with the worldwide 25 percent, which means that China could increase its share of worldwide foundry production to almost 23 percent by 2008.

IC Design

While IC design is still the smallest

sector of China's semiconductor industry, it is clearly the fastest growing segment and the focus of most local government interest and support. Although it accounted only for 9 percent of China's semiconductor industry revenues for the first six years of this decade, it has been growing at a compounded average growth rate of 69 percent and reached more than 11 percent of industry revenues in 2006. The number of IC design or fables semiconductor companies in China has grown from less than 100 in 2000 to almost 500 by 2006. Most are small companies with more than half having less than 50 employees in 2005. Most are also Chinese companies, with no more than 20 percent being design units (or activities) of foreign-invested or subsidiary multinational companies.

During 2005, China's first IC design enterprise broke the $100 million revenue mark, as Actions Semiconductor reported $155 million in revenue. Also during 2005, Actions Semiconductor and the second largest Chinese fabless semiconductor company, Vimicro ($95 million in revenue), were the first Chinese fables semiconductor companies to be successfully listed on the NASDAQ stock exchange. Despite these noteworthy milestones, the majority of IC design companies contribute significantly less to the market: only 11 of China's design enterprises achieved 2005 revenues of more that $25 million and just 30 enterprises had revenue of more than $5 million.

At the same time, China's 11th Five Year Plan, which covers 2006 through 2010, calls for the development of five IC design companies with revenues of $375 to $624 million and 10 companies with revenues of $125 to $375 million. If this goal is realized, these 15 companies alone would contribute IC design revenue of $3.1 to $6.9 billion by 2010, which would place China's share of worldwide fabless semiconductor revenue at 6 to 8 percent. This share would constitute no more than 3 percent of the total worldwide IC industry revenue in 2010. History indicates that this is a rationally possible but unlikely outcome that could have a noticeable but moderate impact on the semiconductor industry.

Consumption / Production Gap Challenges and Opportunities

Probably the most significant overall outcome of China's semiconductor activity to date has been the every increasing IC consumption/production gap—the difference between IC consumption and IC industry revenues. In 2006, the gap, continued to increase at a faster rate than previous years, despite the significant government plans and efforts to contain it. This consumption/production gap has now grown from $5.9 billion in 1999 to more than $48 billion in 2006, and the Chinese authorities expect that it will continue to increase through at least 2010. It represents both an opportunity and challenge for the established multinational semiconductor industry. Over the near term, it represents an unparalleled market opportunity, but over the longer term it represents a domestic industry void that will inevitably get filled. This will likely be accomplished through a combination of transfer and expansion by multinational companies and the emergence and growth of significant Chinese companies. ◆

Ed Pausa is a retired semiconductor executive with more than 40 years industry experience; he is currently Director at PricewaterhouseCoopers Technology Center. For a more comprehensive review of these topics, see the PwC study series that he authored, "China's Impact on the Semiconductor Industry" at www.pwc.com/techcenter.

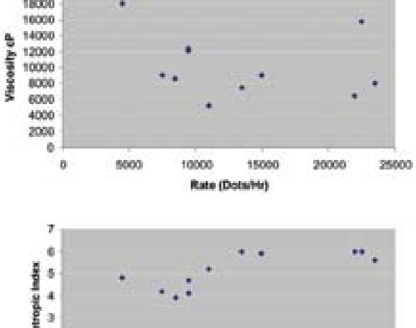
Die Attach Performance Indicators: Are Standard Industry Tests Adequate?

Michael Buckley, Julie Bradbury and George Carson
The Electronics Group of Henkel

It's a common practice in the semiconductor manufacturing industry to quote stats from a materials data sheet to suggest what that material's performance may be. In relation to die attach materials in particular, you may hear terms like viscosity and thixotropic index to predict dispensability or die shear to predict the material's bond strength. All of these are very common and widely used industry tests which have become somewhat standard. But, are they standard because they've been all we've had up until this point or because they are really useful indicators of a material's performance?

Let's take a look at viscosity as a predictor of a die attach material's dispensability. Listed on most materials datasheets, is the thixotropic index – basically the ratio of the liquid viscosity at different shear rates. Usually greater than one, the thix index describes the tendency of a fluid to flow more readily as it's sheared more rapidly (shear-thinning). In the majority of cases, the viscosity of any given die attach paste will be somewhere between 8,000 to 12,000 cP, which is intended to be an indication of the material's dispensability characteristics. In truth, however, viscosity alone is not a good predictor of dispensability. A die attach viscosity measurement may predict dispense rate for a consistent PSI (pound per square inch pressure), but only if the same sized dispense needle is being used. And, herein lies the problem. There are a plethora of different dispensers for a variety of different manufacturing requirements, employing auger screw (Archimedes), time/pressure and positive displacement technologies. Positive displacement pumps, which rely on a motor-driven piston to force the fluid through a needle, eliminate almost all dependence on viscosity. So dispense rate is highly dependent upon the dispensing tool and its dispense characteristics, which is why viscosity is not the sole predictor of material behavior. In fact, Henkel's recent research indicates that when you use the proper chemistry and fillers, even materials with higher viscosities – say at 14,000 CPS – can dispense faster without tailing than those at lower viscosities, and deliver better overall results.

Just as viscosity and thixotropic index measurements are not the sole predictors of dispensability, die shear strength isn't necessarily a good predictor of package strength. The die shear test does provide data on the strength of the material bond for die of various sizes, but is not a reliable predictor of moisture preconditioning (MRT, JEDEC, etc.) performance. Though there have been different approaches such as hot/wet die shear and quick kill tests, which may suggest the die's strength when exposed to moisture, these tests are still insufficient for total package performance. In fact, a material may have good die shear strength, yet fail to perform well in a manufacturing environment because it isn't evaluated with mold compound and in a reflow environment. Datasheets typically provide information on the die attach die shear strength, moisture absorption and modulus among other properties and often these results are cobbled together and an assumption is made that the material will do well in JEDEC testing. In truth, however, many of these characteristics do not correlate at all to good JEDEC performance. Even though the bond strength may be good, if the package goes through reflow and the mold compound pops off, then die shear doesn't mean much in the way of package performance prediction.



Correlation of Viscosity and Thixotropic Index to the Dispensability of Commercial Die Attach Pastes.

It's not to say that these measurements and standard test procedures don't have a place in materials manufacturing. They do. These types of test are very good for materials consistency checks to validate the materials manufacturing process, but they are not the optimum measure of die attach materials performance. The only true way to evaluate a material's behavior in-package is to test the material in a package, which is precisely Henkel's approach. As the only materials developer and formulator with a complete materials portfolio for the entire semiconductor package and PCB assembly value chains, the experts at Henkel understand the relationship between various materials – such as die attach and mold compound, for example – and what materials properties need to be optimized to ensure reliability, manufacturability and long-term performance. Plus, the unmatched manufacturing facilities at Henkel's Irvine, California Research and Applications Lab enable complete package prototyping, production and evaluation. This comprehensive materials development methodology enables Henkel to produce the most sophisticated materials available in the market today. And, not just materials with good thixotropic indices – materials that will work!

To find out why it takes more than standard industry metrics to predict die attach materials performance, contact a Henkel expert today at 949-789-2500 or log onto www.henkel.com/electronics. ◆

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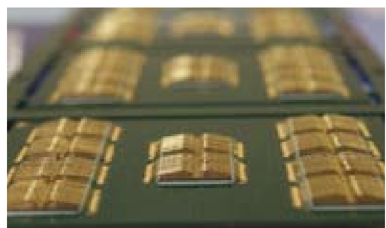

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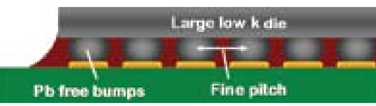

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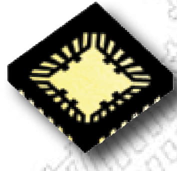

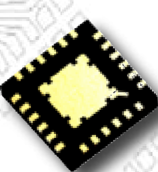

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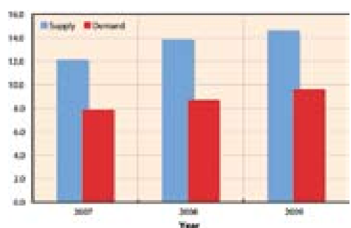

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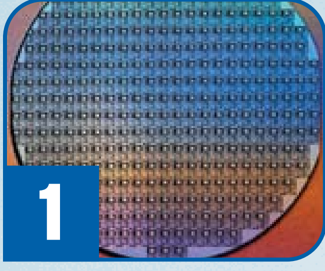

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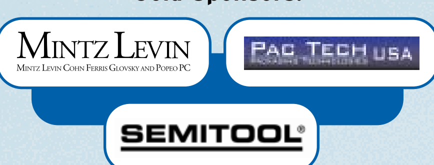

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1	2	3	4 INDEPENDENCE DAY	5	6	7
8	9	10	11	12	13	14
15	16	17	18 **SEMICON WEST 2007** July 16 - 20 Moscone Center, San Francisco, California	19	20	21
22	23	24	25	26	27	28

AUGUST 2007

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
29	30	31	1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	1

SEPTEMBER 2007

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
2	3 LABOR DAY	4	5	6 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	7	8
9	10 **KGD PACKAGING & TEST WORKSHOP** September 9-12 Embassy Suites, Napa, California	11 PATRIOT DAY	12 **FSA SUPPLIERS EXPO & CONFERENCE** September 12 Santa Clara, CA	13 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley Sunnyvale, CA	14	15
16	17	18 **INTERNATIONAL WAFER LEVEL PACKAGING CONFERENCE** September 17-19 Wyndham Hotel, San Jose, California	19	20	21	22
23 30 AUTUMN BEGINS	24	25 **MEPTEC MEDICAL ELECTRONICS SYMPOSIUM** Arizona State University Tempe, Arizona	26	27	28	29

Can Package Substrate Technologies Continue to "Bridge the Gap"?

Rich Rice, Senior Vice President of Sales, North America
ASE (U.S.) Inc.

I have been challenged, more times than I can remember, by customers with some tough questions. "Why is my assembly cost higher than my die cost?" "Isn't the packaging world keeping up with technology required to keep my expected assembly costs in alignment as I project them into the future?"

These are straightforward questions that do not have such simple, straightforward answers. To attempt to bring light to this discussion, I would like to serve some food for thought.

Over the last five years, wafer lithography in high volume production has progressed from 180nm to 90nm, with 65nm now ramping up. Even though this is not necessarily realistic, if functionality is kept constant, the resultant die size is 1/4 to 1/8 the size of the die manufactured in the 180nm node. So how has PCB technology for motherboards progressed during the same time?

An indirect indicator is the pitch of the packages that serve those high volume electronic applications. PC motherboards, logic chipsets, and graphics ICs have been manufactured with 1.0mm ball pitch, with some moving to 0.8mm pitch. For mobile handsets, where space savings and relieving these constrains are critical, the BGA ball pitch has been fairly stagnant at 0.8-0.5mm for years, with some recent activity to move toward a ball pitch of 0.4mm.

The reality is that the rate of PCB technology advancement is not keeping up with Moore's law. But, does it have to? Do I need a smaller TV or home PC? Do I need a smaller phone? Or digital camera? It has become apparent that the need for more advanced PCB technologies is heavily driven by the need to reduce the size of the appliance, and some have become stagnant or moved slowly for years.

As wafer lithography continues its drive to comply with Moore's Law, and motherboard technology for electronic appliances is only driven hard when space can be saved, it seems logical that the gap between the IC and motherboard will continue to increase. This is where the package substrate must fill the gap.

If this lithography gap between IC and motherboard continues to widen, how can the package substrate bridge it while continuing to be 15% lower cost every year? Without significant innovation into material cost reduction, this goal is not easy. For wirebond packages, we rely on gold wires to bridge some of this gap, but commodity gold prices continue to rise. Can we continue to reduce the gold wire diameter to offset this trend?

For flip chip packages, the substrate and bump are the only materials to bridge the gap between the IC and motherboard. Can we make cost-effective flip chip substrates that bridge this ever widening gap between the nanometer based technology on the die and the motherboard PCB technology that might not need to shrink due to its practical useful size? Can package substrate technologies utilizing wafer foundry lithography equipment bridge this gap from IC to motherboard cost-effectively?

Another aspect of package substrate technology is to do what the IC manufacturers do. They add functionality onto their IC to increase the value by reducing the total number of chips in the system. Today, we are seeing developments in not only using patterning to create passive components, but also embedding active components within the structure of the substrate. Is this a practical and cost-effective approach for package substrate technology? With more and more specialization in various electronic applications, I am sure that, with innovation and investment, this will become practical and cost-effective for some but not for all types of IC packages and electronic systems. There will be end use applications that have a need for the benefits that these innovations bring, and hopefully their usefulness will expand toward many different types of applications in the future. After all, as engineers, we always like to see what we invent to have long term usefulness within the industry.

The reality of all of this is based in economics. If there are end use applications that have high enough revenue and margin to fund the development of these innovations, whether cost reduction or increased functionality, they will happen. Our industry is filled with dynamic, determined engineering leaders that can do almost anything they put their minds toward.

So, what about the answers to the questions that my customers ask me? I strongly dislike giving them an answer of "maybe". If there was as much R&D funding going on in substrates as for wafer lithography, I could confidently state that package substrates will be able to keep up with Moore's Law as well as meet the cost reduction demands of the industry. The reality is that package substrate R&D is a fraction of wafer foundry R&D.

And what is our hope for meeting these challenges as an industry? I believe it lies in the economics, as well as the innovation of those determined engineers who are trying to make a buck, and to see their inventions put to good use. During the upcoming November symposium assembled by MEPTEC, entitled "Substrates: The Foundation of Packaging", I trust we will see the contributions that these men and women are offering to meet these tough challenges. ◆

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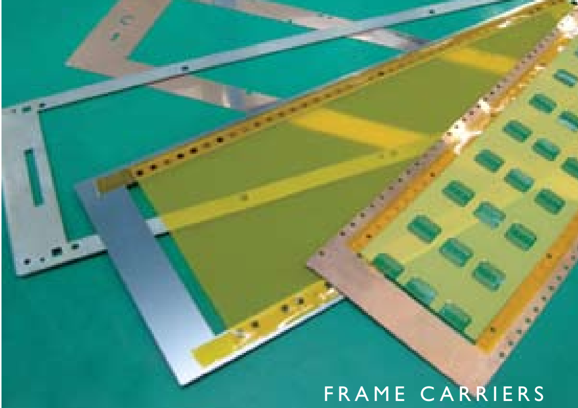

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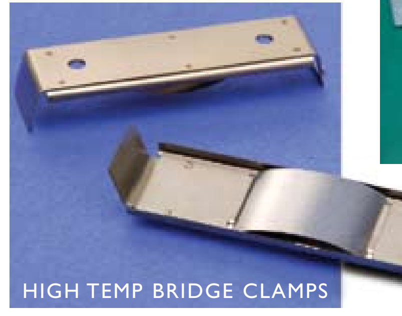

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