MEPTEC turns 30!
See Special Pull-Out Section for New Services

MEPTEC report

Volume 12, Number 2

ARTER TWO 2008

A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Amkor Technology, Inc. has announced that Ken Joyce has been appointed President of the company. Gil Tily has been named Chief Administrative Officer and Executive Vice President, succeeding Mr. Joyce in that role. Eric Larson will join the company as Executive Vice President Product Management Group. *page 12*

Sonoscan has introduced a new capability for its line of C - SAM acoustic microscopes that reveals the external surface topography of a device at the same time as its internal features, known as the Acoustic Surface Profile (ASP) module. *page 14*

CAD Design Software announces the results of a major LTCC design test conducted by a leading U.S. defense foundry. The result is a dramatic reduction in overall design time. *page 17*

March Plasma Systems has announced that it has released the PM-100 plasma system, which is designed to be a low-cost, highly effective plasma treatment solution for treating electronic components, printed circuit boards, and medical & life science devices. *page 19*

SEMICON West returns to Moscone Center in San Francisco July 15 through 17. *page 23*

The 3rd Annual MEPTEC

Medical Electronics Symposium

Technology Concepts Enabling Product Reality

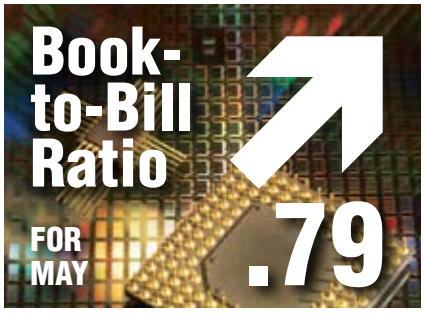
One Day Technical Symposium at Arizona State University Coming to Tempe, AZ September 25th ... page 4

MEMBER COMPANY PROFILE

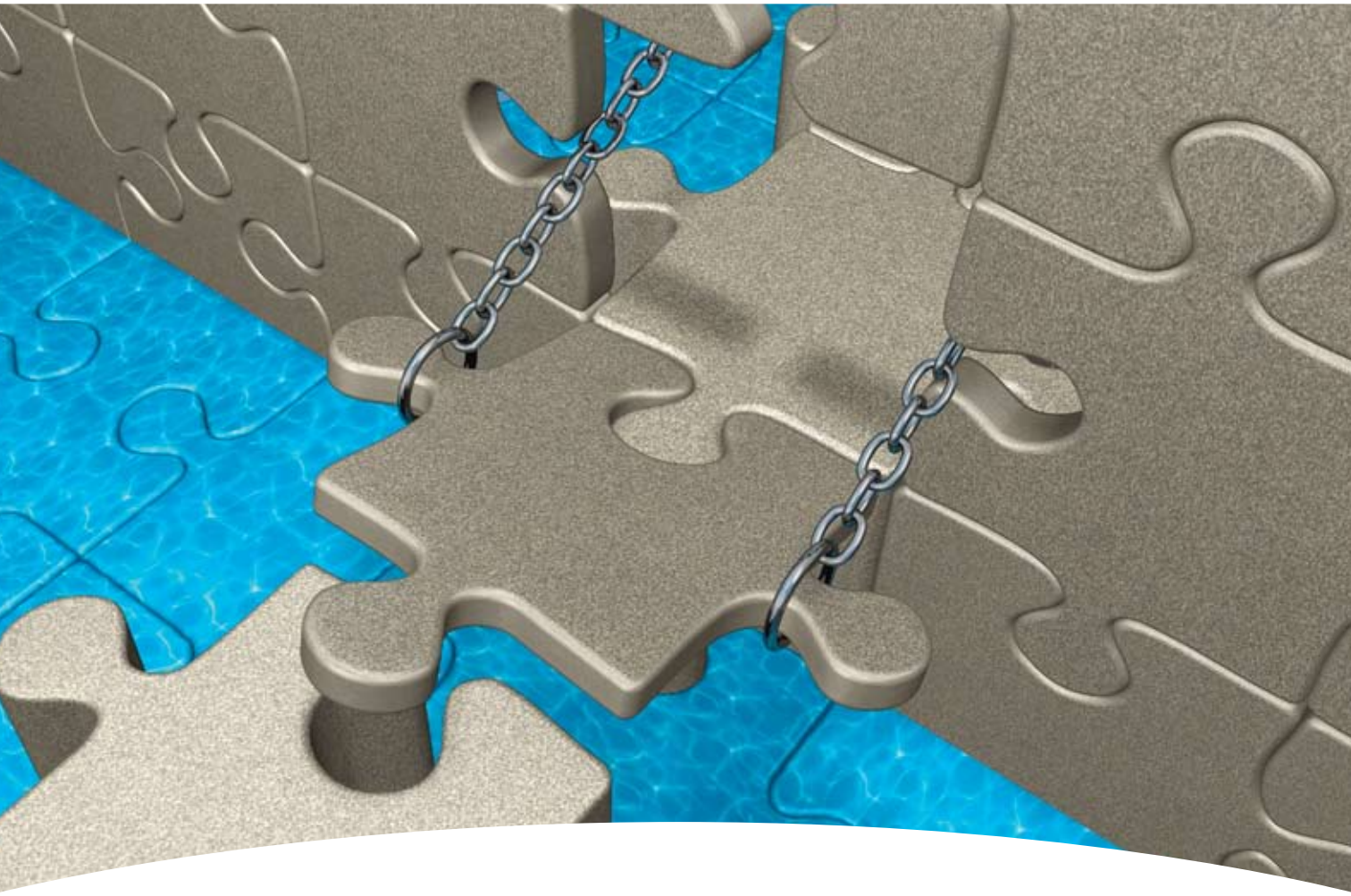
Rudolph Technologies has developed a line of fully-automated systems for thin film process control that are used in major fabs around the world. Opaque films are measured with the patented Picosecond Ultrasonic Laser Sonar (PULSE®) technology, simultaneously measuring thickness and other properties.

Rudolph Technologies has an established, long-term presence in the wafer processing fab as well as the packaging and test floor. The company maintains a leadership position by investing in aggressive research and product development to meet customer demand for performance and productivity. In addition, Rudolph's involvement in research programs and application initiatives with customers, industry consortia and other equipment suppliers is aimed at addressing critical challenges in microelectronics manufacturing. *page 10*

Semiconductor equipment bookings decrease 5% over April 2008 level. *page 18*



innovation



Finding new ways to solve problems—whether it's new obstacles that arise or the usual process challenges—we're here to offer a unique combination of strengths.

Recent example: our award-winning printable phase change material. Honeywell's ongoing research and development in chemistry, metallurgy, and the processes that bring them together—from our new packaging R&D facility in Spokane, Washington, to our technology center in Shanghai, China—ensure that wherever challenges arise, we'll continue to create solutions that solve them. And as a partner to most of the top semiconductor houses worldwide, our technology portfolio is consistently at the forefront of invention, empowering the global leaders of innovation. Honeywell Electronic Materials—helping the manufacturers of today navigate the future.

Honeywell

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MEPTEC
MicroElectronics Packaging & Test Engineering Council

30th MEPTEC Anniversary

Dear MEPTEC Members and Supporters,

We're pleased to announce that 2008 marks the 30th year that MEPTEC has served the semiconductor packaging and test engineering industry! Since our inception in 1978 we have continued to be committed exclusively to packaging, assembly and test, and are dedicated to the advancement of our industry. Over the years MEPTEC has provided a forum for semiconductor professionals to learn and exchange ideas that relate to packaging, assembly, test and handling.

We'd like to inform you of several exciting new products and services for 2008:

- A brand new, totally redesigned website – now online.
- New affordable advertising and promotion opportunities
  - Web banners
  - A totally new print publication: the TECH Report
  - Member company "spotlights" on the MEPTEC homepage (limited number each month)
- "Education Network Series" seminars and workshops
- MEPTEC Report Newsletter archives online from 2004 to present
- New Symposium CD pricing and packages
- And coming soon... MEPTEC Creative Services
  - Company newsletter design and production
  - Website design and maintenance
  - Event/meeting planning

Please see our special pull-out section in this issue for a more detailed description of these services. Further information on these items is also now available at www.meptec.org.

We look forward to an exciting new year, and thank you for your continued support!

Regards,

Bette Cooper
President, MEPTEC
Editor, The MEPTEC Report

PO Box 222, Medicine Park, OK 73557
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Editor
Bette Cooper

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Gary Brown

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Kim Barber

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Council Update

It's that time again: summertime, which in our industry means Semicon West. As every year, thousands will descend on San Francisco. This issue is being distributed there, so if you've picked one up and are reading this, thank you!

MEPTEC's next symposium will be on Thursday, September 25, and once again we'll be holding our annual Medical Electronics event on the Tempe campus of **Arizona State University** in the beautiful Old Main building MEPTEC's *3rd Annual Medical Electronics Symposium: Technology Concepts Enabling Product Reality* will be co-sponsored by **ASU** and **Connection One and the Ira A. Fulton School of Engineering**. Driven by strong global demand from health conscious consumers in receiving the best medical diagnosis and treatment available, this symposium will focus on advanced technologies in medical electronic products. Industry experts will present on the revolutionary concepts and enabling technologies driving future product trends. Registration is open on the web; please go to www.meptec.org for more details and to register.

In this issue we offer a follow up of our most recent symposium from **Julia Goldstein**, contributing editor for **Advanced Packaging Magazine**, on the *"6th Annual MEPTEC MEMS Symposium – MEMS Market Evolution: From Technology Push to Market Pull"*. Julia points out that with MEPTEC's first MEMS symposium in 2003, MEMS was "a technology with potential". Five years later it's obvious the potential has been realized. We'd like to thank Julia for this summary (see page 8).

Our first feature article is contributed by **Giles Humpston** of **Tessera**, one of our long time Corporate members. Titled *"Wafer Level Cavity Package Using Via-through Pad Interconnections"*, this article discusses the solution which is being progressively adopted by the industry, which is to package the semiconductor die using wafer-level technology. He covers wafer-level package interconnects, electrophoretic materials and reliability issues. See page 20 for this interesting and thorough article.

Our second feature article is written by **Kelly McKendrick** of **ASAT**, another long time MEPTEC Corporate member. Written in first person, he talks to us about *"Thin" QFN, TAPP and fpBGA Packages"*. He takes us through his journey starting in 1980 as a "Fab Rat" working on 3" wafers and thinking 4" wafers were huge. He asks, what is the ultimate "thin" package? He also poses an interesting scenario: "Just when you think you have the final "Green" package and process, someone finds yet another substance that makes the green not so green anymore!". Read this insightful and informative piece on page 24.

Our editorial this issue is from **Gary Alexander**, Executive Director of the **Surplus Equipment Consortium/Network, Inc.**, or **SEC/N**. His editorial on page 34 is titled *"Evolving The Global Secondary Market"*. Advisory board member **John Crane** introduced us to this group, and he found they had some interesting things to share. SEC/N was founded based on the efforts and concerns of the **SEMATECH Surplus Equipment Council** (SSEC). As Gary says (quoting Bob Dylan), "The times they are a-changing" – especially when it comes to the global secondary market.

MEPTEC Advisory Board member **Mary Olsson** of **Gary Smith EDA** asks the question: *"Is 2008 the Year for Analog Mixed-Signal?"* in her Industry Analysis on page 6. She reviews the Analog/Mixed-Signal EDA Landscape, sales revenues, first quarter earnings and sequential quarterly earnings of Analog/Mixed Signal companies, and discusses supply side issues as well. We'd like to thank Mary for her contribution to this issue.

Our Member Company Profile this issue is Corporate MEPTEC Member **Rudolph Technologies**. Rudolph has a long history, starting in 1940 as an importer of microscopes and scientific instruments. In 1996 they expanded into metrology technologies, and was renamed Rudolph Technologies, Inc. During the years of 2002-2007 several acquisitions contributed to their growth, and they have evolved into a process characterization leader in the semiconductor industry. See their profile outlining their interesting history and many services on page 10.

We'd like to thank all of our contributors for making this another great issue. If your reading this publication for the first time at the Semicon West show, or another of the many events where we distribute the MEPTEC Report, we hope you enjoy it.

Thanks for joining us! ◆

Special Thanks to Kim Barber

School's out, Summer's here, and people are on the move... including our own Kim Barber. Kim is taking advantage of the Summer Break to relocate her family of three, along with husband Brian, to sunny Southern California from the San Francisco Bay Area.

We'd like to take this opportunity to thank Kim for her hard work over the last four years as MEPTEC Director of Sales and Marketing. Her efforts have helped MEPTEC experience growth in both our events and the MEPTEC Report.

While Kim is "on the move" feel free to contact Gary Brown at gbrown@meptec.org for any of your sales and marketing needs. ◆

Is 2008 the Year for Analog Mixed-Signal?

Mary A. Olsson
Gary Smith EDA

Since the first of this year, Gary Smith EDA has been interviewing and surveying companies in the Analog/Mixed-Signal EDA landscape to uncover answers to the question "Is 2008 going to be the year where analog design automation moves forward and catches up with digital design automation?"

According to the majority of Analog/Mixed-Signal Design Tool start-ups, the market for custom IC design solutions, which includes analog/mixed signal designs, could reach $700 million in 2008. The Gary Smith EDA forecast for Custom Analog/Mixed-Signal ICs is $427 million in 2008. The majority of this growth is being driven by the wireless and consumer market applications. Thus a huge opportunity exists for 100 percent automation in analog/mixed-signal, if the layout tools existed. According to the majority of all interviewed and surveyed, the process is still predominately manual, and most of the older tools are insufficient for designs below 90nm. No one has yet to make an automated custom layout tool acceptable to analog/mixed-signal device designers. The industry is lagging as it deals with "your grandfather's analog design process".

Except for the majority of EDA start-ups, many listed in Figure 1; most of the tools being used in the analog/mixed-signal design flow today are pre-1998 generation. Analog/Mixed-Signal design flows now range from 9 months to as long as 18 months, especially for high-end design applications. Users like Texas Instruments, STMicroelectronics, Qualcomm and Broadcom are shifting mixed-signal designs (also called ASPs and ASSPs) to 65nm and 45nm processes in 2008 and 2009. If they could automate layout, physical design would be measured in days and

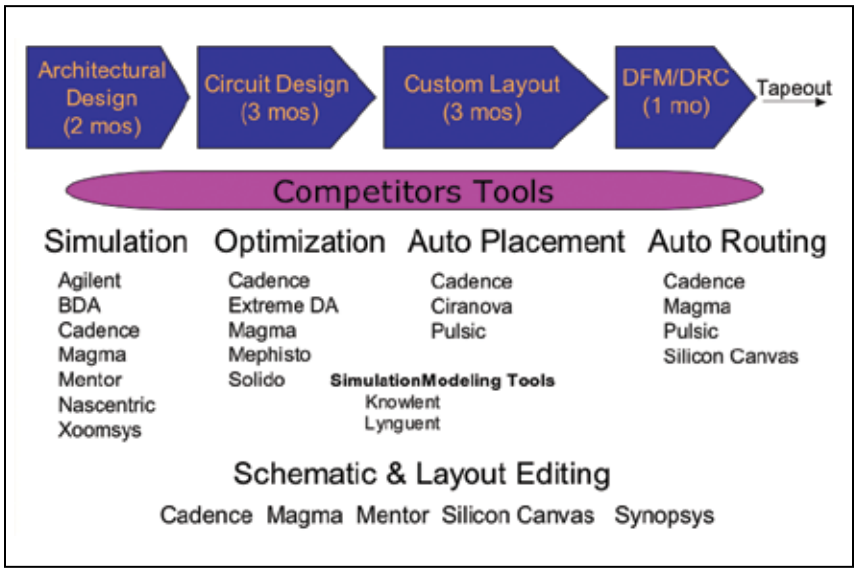

Figure 1. Analog/Mixed-Signal EDA Landscape. *Source: Ciranova & GSEDA May* 2008

Exchange	Stock Symbol	Company	Revenue 2007	Sales Revenue Q1/2007	Sales Revenue Q2/2007	Sales Revenue Q3/2007	Sales Revenue Q4/2007
NYSE	ADI	Analog Devices	$2,521	$591	$669	$637	$624
-	-	Avago Technologies	$1,535	$375	$386	$381	$393
NASDAQ	BRCM	Broadcom	$3,776	$901	$898	$950	$1,027
NASDAQ	DIOD	Diodes Inc.	$401	$92	$96	$105	$108
NASDAQ	EXAR	Exar	$69	$16	$17	$15	$21
NYSE	FCS	Fairchild	$1,670	$403	$409	$427	$432
-	FSL	Freescale	$5,722	$1,361	$1,376	$1,446	$1,539
FSE/NYSE	IFX	Infineon	$6,478	$1,506	$1,557	$1,736	$1,679
NASDAQ	ISIL	Intersil	$757	$168	$178	$198	$213
NASDAQ	LLTC	Linear Technology	$1,093	$255	$268	$281	$289
NASDAQ	MRVL	Marvell	$2,672	$622	$635	$657	$758
NASDAQ	MXIM	Maxim Integrated Circuits	$2,070	$476	$531	$523	$540
TSE**	2454	MediaTek Inc.	$2,626	$491	$601	$871	$664
NASDAQ	MCRL	Micrel	$258	$63	$65	$65	$65
NASDAQ	MCHP	Microchip	$1,033	$258	$264	$259	$253
NASDAQ	MSCC	Microsemi Corporation	$463	$107	$114	$120	$123
NYSE	NSM	National Semiconductor	$1,857	$431	$456	$472	$499
-	-	NXP	$7,659	$2,249	$1,757	$1,864	$1,789
NASDAQ	ONNN	ON Semiconductor	$1,493	$348	$356	$381	$408
NASDAQ	PSEM	Pericom Semiconductor	$141	$30	$32	$38	$41
NASDAQ	PMCS	PMC-Sierra	$449	$104	$105	$117	$124
NASDAQ	QCOM	Qualcomm	$9,292	$2,221	$2,325	$2,306	$2,440
NASDAQ	RFMD	RF Micro Devices	$993	$257	$212	$256	$268
NYSE	STM	STMicroelectronics	$10,001	$2,276	$2,418	$2,565	$2,742
NYSE	TXN	Texas Instruments	$13,834	$3,191	$3,424	$3,663	$3,556
NYSE	VSH	Vishay/Siliconix	$2,833	$658	$716	$730	$730
		Total	$81,698	$19,449	$19,864	$21,063	$21,322

* Denotes US Dollars from Euros, ** Denotes Taiwan Stock Exchange

Table 1. Sales Revenue of Analog/Mixed-Signal Semiconductor Companies, 2007 (Millions of Dollars) *Source: GSEDA May 2008*

not weeks or months.

The value to these companies and their designers would include:

- Faster delivery time to market
- Better opportunity for increased revenue from IP re-use and process node migration
- Better quality of result (QoR) at process technology below 65nm

Supply Side Issues

In 1998 worldwide analog revenue was $9 billion. Standard analog product revenue was $7 billion and mixed-signal was $2 billion. 115 analog device suppliers served the entire 1998 analog market. By year-end 2007 the entire analog market reached almost $37 billion in revenue for device suppliers, according to WSTS 2008 statistical reports. The standard products arena that includes interface, data converters operational amplifiers and other analog, reached almost $15 billion in revenue. The application specific products (ASPs) designed into computer, communications, consumer, automotive, industrial and military sectors rose to $22 billion in revenue.

Table 1 lists the corporate sales revenue performance of companies that provide quarterly data and/or are publicly traded in the United States. These are the largest suppliers to the worldwide analog/mixed-signal merchant market. The top five companies, Texas Instruments, STMicroelectronics, Qualcomm, NXP, and Broadcom, are the largest suppliers to the mixed-signal or application specific analog markets, having captured the greatest share of designs into the wireless communications and consumer sectors.

Table 2 provides detailed information for these same companies for first quarter 2008 over first quarter 2007. Overall revenue growth in first quarter 2008 was up 9.1 percent over first quarter 2007. Net income was up 53.4 percent. This is viewed as a positive factor as many have expressed that unsettling market news, lower customer bookings and a persistent downward pressure on device average selling prices, were signs pointing to a downward slide in revenue in the first half of 2008. In Table 3 the first quarter of 2008 showed a slight decline (0.5) percent in overall growth versus the fourth quarter 2007 sales revenues. However, net income for the stronger competitors on both the standard analog and application specific analog products areas carried net income to an increase of 53.5 percent. It is important to note that although earnings are down considerably for many in the analog segment, some analog companies are making money. Historically, the analog market players are aware of cycles in the industry, and a downward market presents plenty of opportunity to cut back on production, absorb costs and reinvest in R&D.

Summary

What has been evident during this research process is that there is a definite shift (vendors and users) away from single vendor in-house proprietary solutions to design tool integration via partnering, alliances and mergers. Users are seeing this as a tremendous opportunity to build relationships with new EDA tool suppliers, accelerate growth in application specific analog and expand positions with existing and new OEM customers. In the face of increasing circuit complexity and high performance SOC designs, many EDA start-ups and a few steadfast major leaders are ready to announce key automated layout tools to drive the market forward. The DAC 2008 event in June may be a turning point for both vendors and users in the analog/mixed-signal space. ◆

Exchange	Stock Symbol	Company	Sales Revenue Q1/2007	Sales Revenue Q1/2008	Change (%)	Net Income Q1/2007	Net Income Q1/2008	Change (%)
NYSE	ADI	Analog Devices	591.3	613.9	3.8%	153.2	370.7	141.9%
-	-	Avago Technologies	375.0	402.0	7.2%	6.0	4.0	-33.3%
NASDAQ	BRCM	Broadcom	901.5	1,032.2	14.5%	61.0	74.3	21.8%
NASDAQ	DIOD	Diodes Inc.	92.0	95.6	3.9%	13.0	14.2	9.2%
NASDAQ	EXAR	Exar	16.9	18.4	8.9%	(6.3)	(174.5)	2674.8%
NYSE	FCS	Fairchild	402.6	406.3	0.9%	6.3	17.1	171.4%
-	FSL	Freescale	1,361.0	1,405.0	3.2%	(539.0)	(245.0)	-54.5%
FSE/NYSE	IFX	Infineon*	1,506.4	1,625.0	7.9%	(17.0)	(2.1)	-87.5%
NASDAQ	ISIL	Intersil	167.7	203.7	21.5%	33.1	67.1	102.7%
NASDAQ	LLTC	Linear Technology	255.0	297.9	16.8%	98.6	99.2	0.7%
NASDAQ	MRVL	Marvell	622.0	844.7	35.8%	(140.6)	1.3	-100.9%
NASDAQ	MXIM	Maxim Integrated Circuits	475.8	487.4	2.4%	250.7	269.3	7.4%
TSE**	2454	MediaTek Inc.**	490.5	636.5	29.8%	257.4	132.4	-48.6%
NASDAQ	MCRL	Micrel	63.1	66.1	4.7%	17.9	8.4	-53.1%
NASDAQ	MCHP	Microchip	258.2	260.4	0.9%	127.7	76.7	-40.0%
NASDAQ	MSCC	Microsemi Corporation	106.7	126.7	18.7%	(19.6)	9.8	-150.1%
NYSE	NSM	National Semiconductor	431.0	453.4	5.2%	73.7	71.2	-3.4%
-	-	NXP*	2,249.0	2,338.0	4.0%	(535.8)	(120.1)	-77.6%
NASDAQ	ONNN	ON Semiconductor	347.8	421.9	21.3%	54.0	20.8	-61.5%
NASDAQ	PSEM	Pericom Semiconductor	30.2	41.2	36.4%	2.6	4.1	58.4%
NASDAQ	PMCS	PMC-Sierra	103.7	125.0	20.6%	(15.8)	(42.2)	166.7%
NASDAQ	QCOM	Qualcomm	2,221.0	2,606.0	17.3%	726.0	766.0	5.5%
NASDAQ	RFMD	RF Micro Devices	257.3	221.9	-13.7%	30.1	(16.5)	-154.6%
NYSE	STM	STMicroelectronics	2,276.0	2,478.0	8.9%	74.0	(84.0)	-213.5%
NYSE	TXN	Texas Instruments	3,191.0	3,272.0	2.5%	516.0	662.0	28.3%
NYSE	VSH	Vishay/Siliconix	658.2	733.3	11.4%	50.0	(24.6)	-149.2%
		Total	19,450.7	21,212.4	9.1%	1,277.2	1,959.7	53.4%

* Denotes US Dollars from Euros, ** Denotes Taiwan Stock Exchange

Table 2. First Quarter Earnings, Analog/Mixed-Signal Semiconductor Companies, 2007/2008 *Source: GSEDA May 2008*

Exchange	Stock Symbol	Company	Sales Revenue Q4/2007	Sales Revenue Q1/2008	Change (%)	Net Income Q4/2007	Net Income Q1/2008	Change (%)
NYSE	ADI	Analog Devices	623.5	613.9	-1.5%	97.9	370.7	278.7%
-	-	Avago Technologies	391.0	402.0	2.8%	(2.0)	4.0	-300.0%
NASDAQ	BRCM	Broadcom	1,027.0	1,032.2	0.5%	90.3	74.3	-17.7%
NASDAQ	DIOD	Diodes Inc.	107.6	95.6	-11.2%	18.3	14.2	-22.4%
NASDAQ	EXAR	Exar	20.7	18.4	-11.3%	(11.7)	(174.5)	1394.1%
NYSE	FCS	Fairchild	431.9	406.3	-5.9%	34.0	17.1	-49.7%
-	FSL	Freescale	1,539.0	1,405.0	-8.7%	(525.0)	(245.0)	-53.3%
FSE/NYSE	IFX	Infineon*	1,678.9	1,625.0	-3.2%	(609.0)	(2.1)	-99.7%
NASDAQ	ISIL	Intersil	212.6	203.7	-4.2%	40.3	67.1	66.5%
NASDAQ	LLTC	Linear Technology	288.7	297.9	3.2%	93.8	99.2	5.8%
NASDAQ	MRVL	Marvell	758.2	844.7	11.4%	(140.6)	1.3	-100.9%
NASDAQ	MXIM	Maxim Integrated Circuits	540.0	487.4	-9.7%	285.3	269.3	-5.6%
TSE**	2454	MediaTek Inc.**	664.1	636.5	-4.2%	134.0	132.4	-1.2%
NASDAQ	MCRL	Micrel	64.6	66.1	2.3%	8.4	8.4	-0.4%
NASDAQ	MCHP	Microchip	252.6	260.4	3.1%	80.1	76.7	-4.3%
NASDAQ	MSCC	Microsemi Corporation	123.5	126.7	2.6%	8.6	9.8	14.0%
NYSE	NSM	National Semiconductor	499.0	453.4	-9.1%	90.6	71.2	-21.4%
-	-	NXP	1,789.0	2,338.0	30.7%	3.1	(120.0)	-3971.0%
NASDAQ	ONNN	ON Semiconductor	407.9	421.9	3.4%	61.1	20.8	-66.0%
NASDAQ	PSEM	Pericom Semiconductor	40.7	41.2	1.1%	4.4	4.1	-5.8%
NASDAQ	PMCS	PMC-Sierra	123.6	125.0	1.2%	(5.1)	(22.7)	345.9%
NASDAQ	QCOM	Qualcomm	2,440.0	2,606.0	6.8%	767.0	766.0	-0.1%
NASDAQ	RFMD	RF Micro Devices	268.2	221.9	-17.2%	(15.1)	(16.5)	9.1%
NYSE	STM	STMicroelectronics	2,742.0	2,478.0	-9.6%	20.0	(84.0)	-520.0%
NYSE	TXN	Texas Instruments	3,556.0	3,272.0	-8.0%	756.0	662.0	-12.4%
NYSE	VSH	Vishay/Siliconix	729.6	733.3	0.5%	4.9	(24.6)	-603.6%
		Total	21,320.0	21,212.4	-0.5%	1,289.6	1,979.3	53.5%

* Denotes US Dollars from Euros, ** Denotes Taiwan Stock Exchange

Table 3. Sequential Quarterly Earnings, Analog/Mixed-Signal Semiconductor Companies, Q4/2007 and Q1/2008 *Source: GSEDA May 2008*

6th Annual

MEPTEC MEMS Symposium

MEMS Market Evolution – From Technology Push to Market Pull

Julia Goldstein
MEPTEC Advisory Board Member
Contributing Editor, Advanced Packaging Magazine

When **Advanced Packaging Magazine** covered MEPTEC's first MEMS Symposium in May 2003, MEMS was a technology "with potential" that needed to move from a technology-driven to a market-driven approach to succeed commercially. This year's Symposium on May 22 was subtitled "MEMS Market Evolution – From Technology Push to Market Pull," suggesting that the potential has been realized. Sessions were focused on market segments (consumer, automotive and biomedicine) rather than technologies.

Yole Developpment's MEMS market forecast, presented by **Jeff Perkins**, showed consumer applications as the fastest growth area over the next five years. Consumer applications are projected to be over 40 percent of the MEMS market by 2012. According to Yole's just-released world MEMS market report, RF MEMS will grow fastest, followed by microfluidic chips for drug delivery and silicon microphones.

Players in the MEMS industry, from start-ups to Fortune 500 companies, have been working together as part of the **MEMS Industry Group** (MIG) to develop strategies for addressing industry challenges. Their focus during the past year has been on packaging, and MIG Managing Director **Karen Lightman** presented findings from their annual technical meeting last month. The MIG reports that use of wafer level packaging and through silicon vias (TSVs) is continuing to increase and that many device manufacturers are already bonding a capping wafer to the device prior to die singulation. Wafer Level Chip Scale Packaging is also emerging, especially for applications in RF IC's and MEMS filters, and is under development for optical MEMS device applications.

Emphasizing the shift from automotive to consumer markets, **Dr. Ken Yang**, manager of Advanced MEMS Development at **Analog Devices, Inc.**, presented 3-axis accelerometers used for cell phone and gaming applications. Yang discussed the advantages of laser dicing from the front side of the wafer to streamline the dicing process and reduce street size. He also described using TSVs to enable using an ASIC as the cap for a MEMS accelerometer, as well as in-situ capping to reduce cap thickness.

While the automotive market is growing slowly, there are opportunities in this sector, particularly for combustion control. **Dr. Venkat Chandrasekaran** of **Sensata Technologies** explained how microscale pressure sensors can control exhaust gas recirculation (EGR) in diesel engines. A MEMS pressure sensor is integrated into an existing glow rod inside the combustion engine, allowing tighter, closed-loop control over the combustion process. Researchers at **UC Berkeley** are developing a micro solid-state oxygen sensor based on yttria-stabilized zirconia to better control EGR and reduce smog emissions. As presenter **Jonathan Rheaume** noted, additional process development is needed to make these sensors viable for high volume manufacturing.

After an overview of BioMEMS packaging by **Dr. Leslie Field**, founder of **SmallTech Consulting**, **Zachary Ota Lee** discussed research at **UC Berkeley** aimed at solving the real-life problem of vaccine delivery in third world countries. Lee, a Ph.D. student of **Dr. Dorian Liepmann**, described a patch that uses microneedles for transdermal drug delivery. An array of 400 microneedles over a one cm^2 patch effectively vaccinates using one-tenth the dose required for traditional shots and eliminates much of the human error that occurs in storage and dilution when traditional vaccines are used in developing countries.

Dr. Luke Lee, Professor of Bioengineering at **UC Berkeley**, mentioned a number of biomedical applications in his keynote talk on "BioPOETIC" (Biologically-inspired Photonics-Optofluidics-Electronics Technology-based IC) packaging. As Dr. Lee explained, biologic chips are starting to surface in the medical market. Cells, like transistors, can be manipulated via biophotonic processes to eventually create high speed "biologic microprocessors." A wide variety of these chips are being developed to enable applications from microfluidic cell culture to artificial livers and compound eyes. ◆

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Rudolph Technologies

Process characterization solutions for microelectronics manufacturers: inspection, measurement, data analysis and test

Rudolph Technologies has an established, long-term presence in the wafer processing fab as well as the packaging and test floor. The company maintains a leadership position by investing in aggressive research and product development to meet customer demand for performance and productivity. In addition, Rudolph's involvement in research programs and application initiatives with customers, industry consortia and other equipment suppliers is aimed at addressing critical challenges in microelectronics manufacturing.

Process Control Metrology

Rudolph has developed a line of production-worthy, fully-automated systems for thin film process control that are used in major fabs around the world. Opaque films are measured with the patented Picosecond Ultrasonic Laser Sonar (PULSE®) technology, simultaneously measuring thickness and other properties of five or more metal film layers in a non-contact manner. To measure transparent films, Rudolph's S3000A Systems offer laser ellipsometers using patented Focused Beam Ellipsometry (FBE) technology.

Automated Macro Defect Inspection

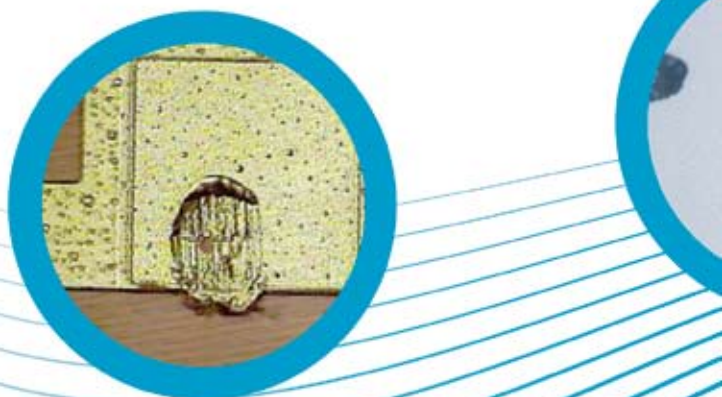
Chip manufacturers deploy macro defect inspection throughout the fab to monitor key process steps and gather process-enhancing information. The all-surface Explorer™ Inspection Cluster allows for a modular, flexible approach to meet specific process needs, and features a completely redesigned software interface focused on reducing cost of ownership. Rudolph maintains a leadership position in the back-end with a comprehensive solution for automated macro inspection with unique wafer handling capability.

Probe Card Test and Analysis

Added to the Rudolph portfolio in late 2007, this technology helps users to access the probing process, identify and analyze issues within the process and define solution options. Rudolph probe systems include high-resolution 2D and 3D probe mark and probe tip inspection as well as test and analysis for probe cards.

Data Analysis and Review

A complete suite of fast and effective software solutions has been developed and is supported by a dedicated Rudolph team. These products deliver fabwide and tool-specific yield and productivity management solutions to help process engineers turn raw data into useful information. Yield Optimizer™, for instance, is a powerful tool that analyzes the



relationships between in-process metrology measurements and end-of-line yield and electrical test results. It then will recommend changes to the in-process metrology targets to optimize the average end-of-line yield. Despite its highly complex algorithms, this product requires minimal training and setup time.

Supporting a Global Customer Base

The world's leading device manufacturers want to partner with suppliers who maintain regional operations centers for process support. Rudolph facilities, staffed with trained applications and service personnel, are strategically located in every semiconductor manufacturing region of the world. ◆

Rudolph History

1940 Otto Rudolph forms O.C. Rudolph & Sons, an importer of microscopes and scientific instruments that eventually becomes Rudolph Research Corporation.

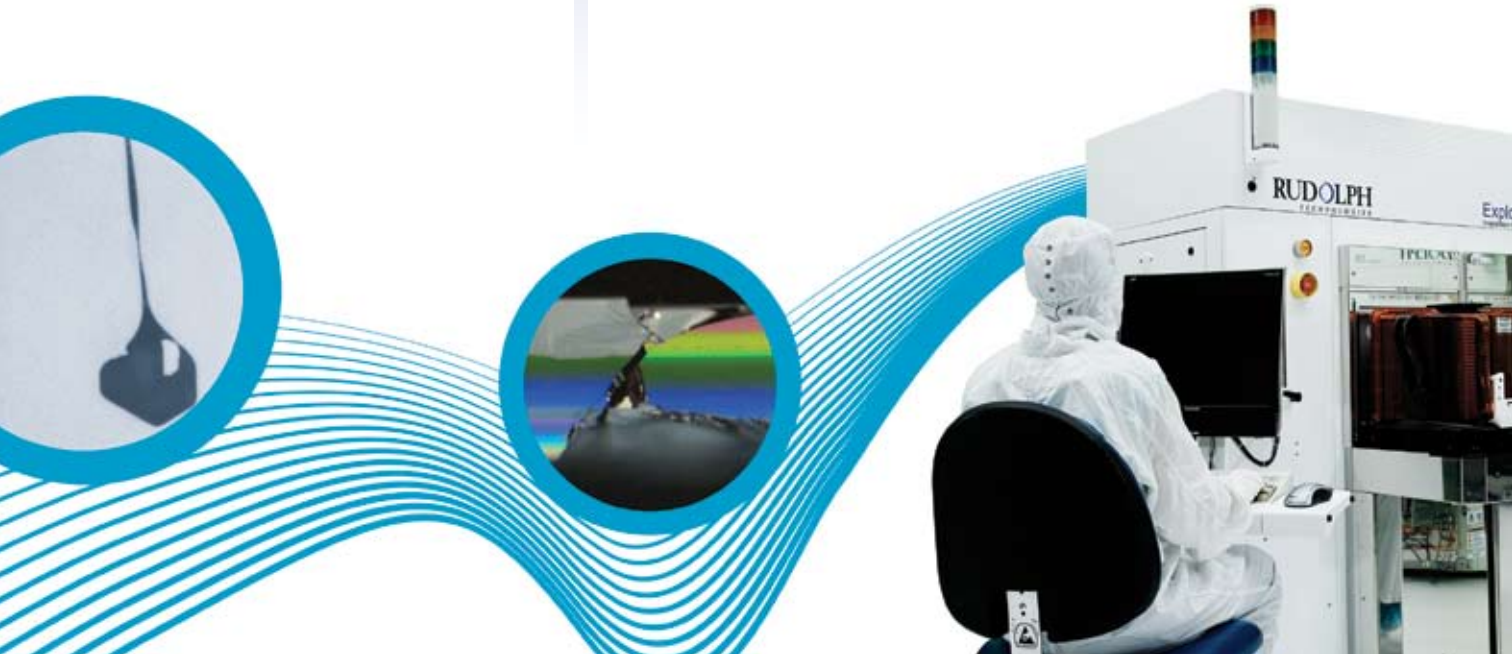
The company continued to evolve, making breakthroughs such as the industry's first production-oriented ellipsometer for thin-transparent film measurements.

1996 Investors contributed millions to bring Rudolph into the 21st century by expanding into additional metrology technologies. Its customer base was growing; the new organization was named Rudolph Technologies, Inc.

1999 The company went public in 1999 (RTEC: NASDAQ); virtually all of the leading semiconductor firms were now placing orders for Rudolph systems. Investment in R&D programs continued, a new facility opened, and a new copper film measurement tool, the MetaPULSE®, was introduced.

2002-2007 Several acquisitions contributed to Rudolph's growth following the turn of the century. ISOA, Inc., a Texas-based defect control company was acquired in 2002. This deal brought macro defect inspection into the company's growing portfolio. A merger with Minnesota-based August Technology Corporation added more inspection and analysis products to the company's product offering. The company remained based in Flanders NJ, now headquarters for its Metrology Business Unit. The Minnesota operation became home to the Inspection Business Unit, and a third Business Unit was established in Lowell, Massachusetts, to house the Data Analysis & Review group. Additional acquisitions in 2007 and 2008 of probe card test/analysis systems and 2D/3D inspection capability complemented the company's established presence in final manufacturing and test.

From its origins as an importer of microscopes and scientific instruments over 65 years ago, Rudolph has evolved into a process characterization leader within the semiconductor industry.



STATS ChipPAC Appoints Hal Lasky Chief Sales Officer

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd., has announced the appointment of Hal Lasky as Executive Vice President and Chief Sales Officer for the Company.

Lasky will report directly to Tan Lay Koon, STATS ChipPAC's President and Chief Executive Officer, and will have overall responsibility for the Company's worldwide sales and product line management organization. He will provide the leadership on the Company's business, customer and product strategy. Lasky will be based in the United States.

"Hal is a world class executive with proven leadership and achievements in managing large scale global sales and product line organizations in the semiconductor industry. I am delighted that a person of Hal's caliber has agreed to join our senior management team to help take STATS ChipPAC to the next level of success," said Tan Lay Koon, President and Chief Executive Officer, STATS ChipPAC.

Prior to joining STATS ChipPAC, Lasky spent 24 years at IBM Corporation where he held a number of key leadership positions, most recently as Vice President of Worldwide Semiconductor Sales for IBM's Global Engineering Solutions group with responsibility for IBM's worldwide semiconductor revenue, sales strategy and strategic relationships with clients in the consumer, communications and IT markets. Prior to that, he held various senior management positions in IBM's Systems and Technology Group, Microelectronics Business Line and Interconnect Products Business Line.

Lasky holds a Bachelor of Science degree in Ceramic Engineering from Rutgers University and a Master's degree in Materials Science and Engineering from Columbia University. He is also a graduate of the IBM Client Executive Program at Harvard Business School.

Amkor Technology Names Eric Larson Executive VP of Product Management Group

CHANDLER, AZ – Amkor Technology, Inc. has announced that Eric Larson will join the company as Executive Vice President Product Management Group. Larson, 52, will report to Ken Joyce, Amkor's President and Chief Operating Officer, and will have overall management responsibility for Amkor's Pro-duct Business Units, including Wirebond Products, Wafer-Level Processing and Flip-Chip Products, Test Services, R&D, Emerging Technologies and Corporate Development.

Larson brings more than 24 years of semiconductor and technology sector leadership experience to his new role. Larson started his career at Hewlett Packard where he worked for 17 years in a number of senior management positions including General Manager of the Integrated Circuits Business Division and General Manager of the Mobile Business Operation. He also served 7 years in senior management positions at Amkor from 1996 to 2003, including as President of our Wafer Fabrication business and Executive Vice President of Corporate Development. Larson is re-joining Amkor after having served in executive management positions with several start-up ventures.

For more information about Amkor visit www.amkor.com.

Ken Joyce Named President of Amkor Technology

CHANDLER, AZ – Amkor Technology, Inc. has announced that Ken Joyce has been appointed President of the company. Joyce, 61, will al-so continue as Chief Operating Officer and will report to James Kim, Chairman and Chief Executive Officer. Joyce joined Amkor in 1997 and was CFO for more than 8 years before becoming Chief Administrative Officer in November 2007 and Chief Operating Officer in February 2008.

"Ken Joyce is exceptionally well qualified for this position. Ken has been a respected, proven leader for us and has the skills and experience to continue building our business and executing on our strategy," said James Kim, Chairman and Chief Executive Officer of Amkor.

Gil Tily has been named Chief Administrative Officer and Executive Vice President, succeeding Mr. Joyce in that role. Tily, 54, will remain as General Counsel and Corporate Secretary, reporting to James Kim, and will have responsibility for Finance, Legal and Human Resources.

For more information about Amkor visit www.amkor.com.

AmTECH Strengthens Their Commitment to Quality

SAN JOSE, CA – AmTECH Microelectronics, Inc. is a leading Silicon Valley provider for SMT, COB, COF and IC Assembly since 1993. They have reinforced their focus on quality, service and FQA product yield by adding key process

equipment such as YESTech Automated Optical Inspection (AOI) and XYLON/FeinFocus XRAY equipment. Their new YESTech AOI equipment has advanced 3-megapixel Thin Camera, RGB Fusion Lighting and telecentric lenses which enable exceptional defect coverage and extremely low false call rate which is necessary in order to improve quality and increase throughput of today's manufacturing process.

AmTECH has built a reputation to be a premier supplier for Chip-On-Board and Chip-On-Flex technology and has now added additional K&S Automatic Gold ball bonder capabilities to support IC Assembly and other fine-pitch wire bonding applications in their Cleanroom ISO 7 (Class 10,000).

Call 408-227-8885, email info@amtechmicro.com or go to www.amtechmicro.com for more information.

SUSS MicroTec Signs License Agreement with Philips Research to Develop a New NanoImprinting Technology

MUNICH – SUSS MicroTec, supplier of innovative solutions for the 3D, MEMS, Advanced Packaging and Nanotechnology markets, has entered a license agreement with Philips Research, Eindhoven, The Netherlands, for a new enabling technology called Substrate Conformal Imprint Lithography (SCIL). The aim of this cooperation is to bring an existing equipment platform with this additional Nanoimprinting (NIL) feature to the market, enabling new approaches to large-area imprint applications along with excellent printing resolution and repeatability.

This new imprint technology for sub-50nm patterning is bridging the gap between small rigid stamp application for best resolution and large-area soft stamp usage with the usual limited printing resolution below 200nm. SCIL is an enabling technology offering the best of two worlds – large-area soft stamps with repeatable sub-50nm printing capability, avoiding stamp deformation as no contact force is applied, non-UV based curing at room temperature and allowing high aspect ratios even up to 1:5 and more.

The lab aligner platform from SUSS MicroTec, handling the 150 and 200 mm UV-lithography like MA6 and MA8, will be available and upgradeable with this feature. Immediate availability for sampling is given with the current test setup. Market introduction with fully implemented SCIL functionality into SUSS' lab aligners is scheduled for later this year.

OLOVO Announces Agreement for Supplying Advanced Packaging Wafer Bumping Plating Anodes

OLOVO, LLC, a leading low-alpha and interconnect materials supplier, has reached an agreement with Semitool, Inc. whereby OLOVO has become licensed to supply anodes for use in Semitool's electrochemical deposition systems. OLOVO's qualification as an authorized vendor allows OLOVO to expand the reach of its low-alpha products to Semitool's customer base and to provide them with an additional source of specialty low-alpha and interconnect materials.

According to Peter Emanuel, VP of Sales at OLOVO, "We are extremely happy with this arrangement with Semitool, and we look forward to supplying Semitool's customer base with high quality plating anodes, which are a key component in the wafer bumping process. We believe this offers tremendous mutual benefit to our respective companies and clients."

OLOVO, LLC is a supplier of low-alpha products which help reduce 'soft errors' in sensitive flip-chip applications. Soft errors are mistakes in logical calculations caused by collisions between alpha particles and logic components in embedded memory and high-speed integrated circuits. Traditional solder materials used in flip-chip interconnect are naturally high in alpha particle emission, causing unacceptable soft error rates in circuit devices. OLOVO is a privately held company with headquarters in Menlo Park, California, USA.

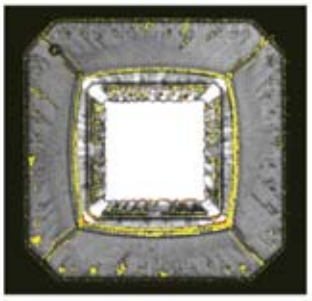
For more information visit www.olovo.com.

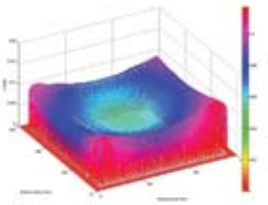
Sonoscan Introduces Acoustic Profiling Module

ELK GROVE VILLAGE, IL – Sonoscan has introduced a new capability for its line of C - SAM acoustic microscopes that reveals the external surface topography of a device at the same time as its internal features. Known as the Acoustic Surface Profile (ASP) module, this important mode can be used to measure warpage of plastic integrated circuits, flip chips, substrates, circuit boards, etc., without any sample preparation.

ASP is available as a cost effective option on new C-SAM acoustic microscope systems as well as a retrofit to many systems acquired over the last few years. ASP works by collecting acoustic surface data and displaying it as a color-coded image in which each color corresponds to a topographical distance measurement. The sensitivity of the ASP is in the micron range and is not dependant upon the surface smoothness, color or optical characteristics.

Warpage at the surface of a part is often associated with internal problems such as cracks and delaminations that can cause electrical failures. For example, the surface profile of a plastic-encapsulated IC may show warpage in one quadrant. Internally, the same quadrant may reveal lead-frame delaminations. Having both images makes it easier to identify the processes that are causing the problem.





Planar acoustic image of BGA (left) reveals multiple anomalies (yellow, dark gray) between molding compound and substrate around the periphery of the component. Acoustic Surface Profile (right) shows that the vertical warpage from the center of the part to the corners is 125 microns.

The value of ASP is that it displays both the surface profile and the internal features on a single instrument, eliminates the need to buy a second instrument, and requires no additional scanning time, as the profile data is taken at the same time as the acoustic image data. If a part is tilted, ASP corrects for tilt before profiling the surface.

For more information contact Steve Martell, manager of technical support services, Sonoscan, Inc., 2149 E. Pratt Blvd., Elk Grove Village, IL USA 60007. Phone: 847 437-6400 x 240. Email Info@sonoscan.com.

Precission Process Introduces the Excellite FSP

Process Partners International, the partner effort between Precision Process Equipment and PAT, has expanded their team to include Sidney Qiu, Sales & Service Engineer now located in Shenzhen City Mainland China. Contact Sidney at +86 13510083568 or email sqiu@processpartnersinternational.com.

Precision Process has also introduced the Excellite FSP: A New Dimension for Flexible Substrate Plating Technology. Ever increasing demands for HDI production processes call for innovative, future-oriented solutions. The Excellite FSP is a roll-to-roll, continuous strip, electroplating and wet processing system designed principally for flex circuits, RFID, and solar cells while having a variety of other electronics and metal finishing applications. View the full brochure at http://www.processpartnersinternational.com/pdfs/PPE_FlexibleSubstrate_RFIDBrochure.pdf

New Centipede Systems Optical Socket Is Ideal for Testing Wafer-Level Camera Chips

SAN JOSE, CA – Centipede Systems has developed a new optical socket suitable for testing the current and next-generation wave of chips used in wafer-level camera modules.

The initial optical socket entry, part of Centipede's Centurion™ product line, is offered in a clamshell configuration for an individual integrated circuit. Currently, Centipede's optical sockets with a grid pitch as small as 0.4mm are available.

Testing camera chips requires that the surface of the device be held accurately in the optical plane without deviation or deflection caused by contactor forces. To ensure accuracy, Centipede's optical sockets align a datum plane on the chip's surface to the lens or optical system with minimal stress on the chip.

"Most existing test socket technology is about a half century old and incapable of testing complex optical chips," noted Dr. Thomas H. Di Stefano, president of Centipede Systems. "Although our initial optical sockets are for testing single camera chips, we are developing sockets for testing arrays of camera chips".

One of the leading providers of optical technologies, based in San Jose, California, is an early adapter of Centipede's optical sockets for wafer-level camera chips, Dr. Di Stefano noted.

Centipede Systems is a technology leader in connectors and sockets in applications where performance, power and density are critical.

ASM Pacific Launches MCM12 Automatic Multi-Chip Bonder

HONG KONG – ASM Pacific Technology has announced its latest generation large area chip bonder to address the growing market for MCM, SIP, and hybrid applications. The MCM12 is a fully automatic multiple die, SMD, and flip chip bonding system with up to 12 inch wafer handling capability. A variety of processes can be integrated on this single platform solution including: direct die, flip chip, stack die, and SMD bonding.

It is highly flexible and can handle a wide range of die sizes and presentation modes. The MCM12 is equipped with a fully programmable dispensing system and automatic pick up and ejector tool changing systems. The bondhead can achieve 800 gram force and is

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programmable to automatically change up to 14 different pick up tools. High accuracy and throughput are achieved with this linear motor driven, gantry style platform. In flip chip operation, the machine is capable of +/- 10 micron accuracy.

The MCM12 material handling system addresses leadframe and substrate sizes up to 200mm x 300mm in stand alone and SMEMA configurations. Workholder conversion is simplified by using motorized tracks with dedicated vacuum anvil blocks.

For die presentation, the MCM12 can accommodate sawn wafers up to 300mm diameter on film frames, sawn wafers on rings, and waffle packs. In addition, up to 5 types of passive components in tape and reel format can be accommodated on the optional front loading SMD handling module.

The three in one operation linear motor driven process head contains the bondhead, writing dispense system, and down looking inspection and alignment camera. Full vision capability includes alignment and inspection of epoxy dispense pattern, die, and post placement inspection.

For more information email inquire@asmpt.com, or visit www.asmpacific.com.

Major Breakthrough in Ceramic Design Software

SAN JOSE, CA – CAD Design Software announces the results of a major LTCC design test conducted by a leading U.S. defense foundry. After substantial development followed by implementation at a key government prime contractor site, the result is a dramatic reduction in overall design time. The prime defense contractor reported, "The special LTCC design and Gerber package that CDS has designed for LTCC has essentially allowed us to reduce our tooling generation time for complex cer-amic designs from 40-80 hrs to 2-8 hrs. This is a significant savings in cost, production flow and quality of our LTCC products."

"Through working closely with numerous military and commercial LTCC customers and material suppliers, we have been able to incorporate new automation functionality and materials handling capabilities in our Hybrid/MCM Design Suite that allow our customers to dramatically reduce their design time. We are very pleased that our customers are experiencing substantially reduced time to market, a benefit now available to all of our customers", said Gordon Jensen, CAD Design Software's vice president of sales and marketing.

Call 408.436.1340, e-mail info@cad-design.com, or go to www.caddesign.com for more information.

STATS ChipPAC Introduces Tool to Reduce Cycle Time & Increase Flexibility of RF Designs

UNITED STATES and SINGAPORE – STATS ChipPAC Ltd. has announced a new IPD Products Databook which contains a library of silicon-based Integrated Passive Device (IPD) designs to assist semiconductor companies in reducing design cycle time and increasing integration options in Radio Frequency (RF) applications.

With the growing industry trend for increased integration in a smaller form factor, passive devices such as filters, diplexers, baluns and matching networks are being placed in packages alongside active semiconductor integrated circuits (ICs). As wireless systems have become smaller, there has been an increasing need to shrink passive devices, especially in terms of height. Design specifications, however, often compromise performance to achieve the desired level of miniaturization.

By integrating and fabricating passive devices at the silicon wafer level, STATS ChipPAC is able to produce IPDs in both wire bond and flip chip format which are significantly smaller, thinner and higher performing than standard dis-crete passive devices that are commercially available. Silicon-based IPDs enable semiconductor companies to effectively reduce device footprint and reduce interconnect complexity, while improving component tolerance, yield and reliability in RF applications such as GSM/DCS and CDMA cellular phones, Wireless LAN 802.11 a/b/g and WiMax systems.

The complexity of designing RF circuits typically translates into multiple design iterations and longer evaluation cycles. This is a factor that affects the speed at which semiconductor companies are able to bring their products to market. STATS ChipPAC has taken the next step in complex RF integration designs by offering semiconductor companies a tool to reduce cycle time and increase the flexibility of their RF module designs. The new IPD Products Databook contains technical information such as size, layout, component values and basic tolerances for complete IPD structures in a wide range of products.

For more information go to www.statschippac.com.

North American Semiconductor Equipment Industry Posts May 2008 Book-To-Bill Ratio of .79

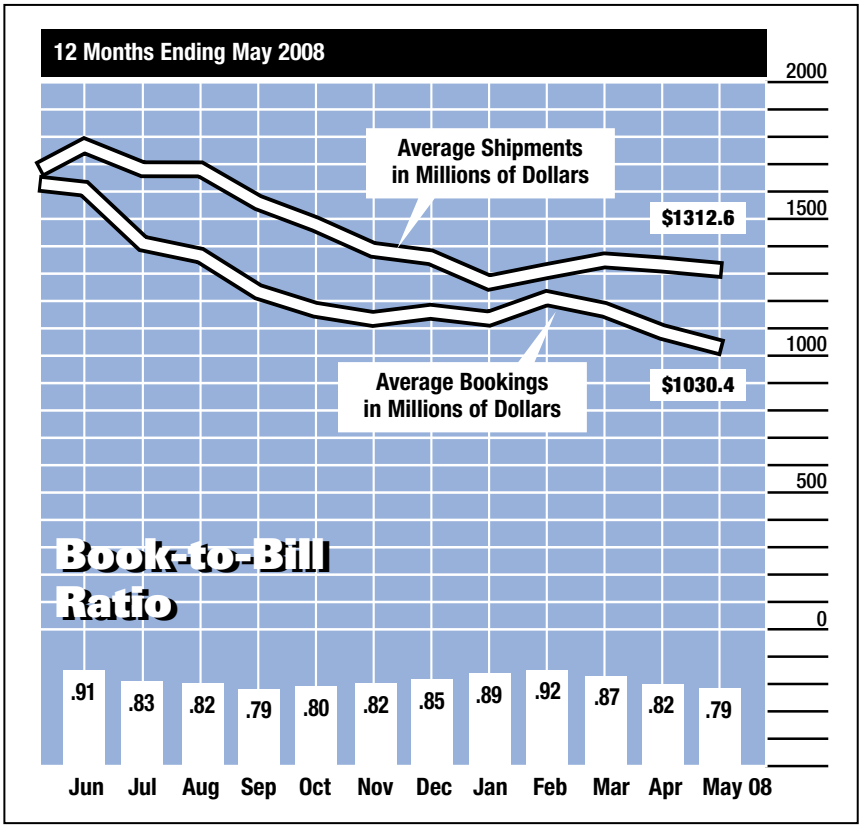
SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted $1.03 billion in orders in May 2008 (three-month average basis) and a book-to-bill ratio of 0.79 according to the May 2008 Book-to-Bill Report published by SEMI. A book-to-bill of 0.79 means that $79 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in May 2008 was $1.03 billion. The bookings figure is about five percent less than the final April 2008 level of $1.09 billion, and about 37 percent less than the $1.64 billion in orders posted in May 2007.

The three-month average of worldwide billings in May 2008 was $1.31 billion. The billings figure is about two percent less than the final April 2008 level of $1.34 billion, and about 21 percent less than the May 2007 billings level of $1.67 billion.

"Booking are approaching levels observed in 2005, which was the last time the semiconductor industry reported a year-over-year decline," said Stanley T. Myers, president and CEO of SEMI. "The data does not indicate a change in this trend over the next quarter."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



(continued from page 18)

March Plasma Systems Announces Low-Cost PM-100 Plasma System

CONCORD, CA – March Plasma Systems, the global leader in advanced plasma treatment systems, has announced that it has released the PM-100 plasma system, which is designed to be a low-cost, highly effective plasma treatment solution for treating electronic components, printed circuit boards, and medical & life science devices. The PM-100 plasma system is ideally suited for laboratories, universities and research and development (R&D) facilities that are highly sensitive to the cost of capital equipment.

"The PM-100 plasma system opens up a new world of economical plasma processing for small-budget operations," said Frank Huysmans, vice president of sales at March Plasma Systems. "These facilities typically know and understand the value of plasma treatments, but have been locked-out from acquiring equipment due to high system costs. The PM-100 plasma system instantly solves this dilemma, and provides the plasma capabilities that laboratories, universities and R&D facilities require at an extremely attractive price point."

The PM-100 plasma system comes with a 12-month limited warranty on parts and labor, and is available for shipment to customers world-wide. Contact March Plasma Systems for further information.

Attendance Numbers Confirm IPC Show in Vegas All About Getting Down to Business

BANNOCKBURN, IL – IPC – Association Connecting Electronics Industries® has released the audited attendance figures for IPC Printed Circuits Expo®, APEX® and the Designers Summit held April 1–3, 2008, at Mandalay Bay Resort & Convention Center, Las Vegas. Participation in the educational offerings including the Technical Conference, Tutorials/Workshops, Management Meetings and Designers Day put the event in the IPC record books with 2,773 educational program attendees, a 45 percent increase over 2007 and a 26 percent increase over 2006 in Anaheim.

As many trade publications have reported, the increased participation was evident throughout the show. Many committee meetings were packed, luncheons were filled to capacity, and special events like the Women in Electronics networking meeting and first-timers breakfast were standing room only.

To punctuate the fact that IPC APEX EXPO™ is global, international attendance grew from 12 percent in 2007 to 16 percent in 2008, with representatives from 47 countries. Total verified attendance was 5,102.

The exhibitor base was as strong as ever before with 442 exhibiting companies. Exhibitor attendance for 2008 was 4,174, bringing total verified visitors for the event to 9,276. These numbers only tell part of the story. As an exhibitor, Christopher Perry, EMC Global Technologies, Doylestown, Pa., said, "The show was really good. We are very pleased with the traffic and the leads."

IPC President Denny McGuirk said the responses from exhibitors and attendees validated the choice to move the event to Las Vegas. "Judging from the preliminary results of surveys from both attendees and exhibitors, Las Vegas was an unqualified hit. When we asked, 'How was Las Vegas as a destination for an IPC show?' 45 percent of attendees gave the event the highest rating – they loved it," McGuirk said. ◆

Wafer Level Cavity Package Using Via-through Pad Interconnects

Giles Humpston
Tessera, Inc.

Solid state images are manufactured in vast numbers. Typically each year more than one billion are made for the cell phone, automotive and computer industries. However, the continued drive toward solid state imagers having ever greater pixel numbers and smaller pixels adversely affects yields. The mechanism for loss is contamination of the delicate optical sensor during assembly of the camera module. The solution being progressively adopted by industry is to package the semiconductor die, preferably using wafer-level technology owing to the favorable economics of the process.

One of the more challenging aspects of wafer-level packaging is the interconnect scheme. Of the choice between top, side or bottom contacts, bottom contacts are attractive since they permit the imager die to be face-upward, which is the orientation necessary for use in a camera module. While through silicon vias (TSVs) are technically attractive for this application, the technology can not yet deliver on price and reliability.

Described is a cavity package for solid state image sensors that is fabricated at the wafer level. This package uses a novel TSV interconnect that makes direct contact to the die bond pads through the thickness of the silicon. The small size and location of the interconnect leaves the rear face of the package available to support a ball grid array interface, making the package compatible with surface mount assembly processes. Unusually, the materials of the package construction are sourced from the automotive industry where they are used in huge volume and are therefore very cheap. This is done to keep costs as low as possible. Packaged imagers are able to surpass by a wide margin, the exacting reliability requirements of the automotive industry, both at the package and board level.

Introduction

Typically each year more than 1 billion image sensors are manufactured. These primarily find application in portable electronics products such as camera phones, digital still cameras and increasingly in webcams, laptop computers, toys and cars. Predictions are this market will continue growing for some years as cell phones with multiple cameras become the norm and automotive driver aids enter the video age. This usage could entail 10 or more cameras being installed on each vehicle and grow to be a market equal in volume to camera phones. Optical mice are also based on image sensing technology, but are usually counted separately from camera modules because, by comparison, their resolution is very low and there are considerable differences in the optics design.

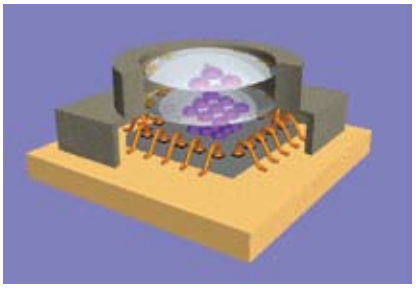


Figure 1. Camera module assembled using chip-on-board processes. The lens turret housing forms a seal over the exposed die. Drawing not to scale. *Source: Tessera*

In common with most other semiconductor devices, solid state image sensors require some form of enclosure in order to ensure longevity. Traditionally for imagers this was achieved using chip-on-board (COB) assembly processes. In this scheme the imager is attached to a substrate, using a conventional die attach adhesive and wire bonds form connections between bond pads on the die and lands on the substrate. The substrate forms the base of the enclosure. Over the die is then placed a lens turret, which houses the optical train of the camera. The lens turret is sealed to the substrate so the lower optical surface in the lens train, in combination with the sidewalls of the turret, forms the enclosure for the die. This is illustrated in Figure 1. Typically the optical train will comprise between two and four lenses, a stop, two apertures and an infra-red filter. The infra-red filter is necessary because silicon image sensors are sensitive to radiation longer than the human eye can perceive.

COB assembly has two principal drawbacks. The first is that the cost of assembly is incremental for each camera module manufactured because the process involves integrating parts in a singular manner. A second limitation is that the imager die is totally unprotected until the final assembly operation when the lens turret is attached. Current leading-edge CMOS imagers have pixels that measure 1.75μm on a side and road maps of the semiconductor companies show this reducing to 1.4μm in 2009. This in itself is not a problem except the optically active area of the image sensor is covered with tiny polymeric lenses to help boost the signal-to-noise ratio. If a particle larger than about 20% of the pixel dimension lands on an imager it results in a black spot in the image. The polymeric lenses are mechanically extremely fragile and incompatible with most solvents, so are virtually impossible to clean. Many back-end semiconductor assembly processes, like wafer sawing, die thinning, die attach and wire bonding were never designed to be ultra-clean. It is therefore not surprising that more than 90% of defects in camera modules, identified on first test, are related to contamination by particles[1]. The short-term solution is to invest in clean rooms and operator training. However, many solid state camera module manufacturers are already operating Class 10 environments, or better, so there is not a great deal of scope for further improvement at affordable cost.

Wafer Level Packaging

Wafer-level packaging (WLP) is an alternative approach to providing a protective enclosure for solid state imagers. The basis of the process is to package the die while they are still in wafer form before the start of the back end assembly processes. The wafer is then singulated to free individually packaged die.

Wafer-level packaging provides three benefits that have great value for image sensors. Firstly, the costs of packaging are shared among the good die on the wafer. With typically several thousand die on a 200mm diameter image sensor wafer this greatly reduces packaging costs per die compared with discrete packages. Secondly, the dies are protected from the very first step of the process so that yield loss from

Figure 2. Formation of a wafer-level cavity package. Left - the device wafer containing five die. Middle - application of the seal material to form a picture frame around the perimeter of each die. Right – attachment of a lid material to seal the cavity over each die. Singulation frees the packaged die from the wafer, an example of which is shown in Figure 3. *Source: Tessera*

contamination by particles is effectively eliminated; not only can the glass surface be cleaned easily, but any remaining contamination is away from the focal plane and hence must be proportionately larger to appear as a defect in the image. The final benefit is that it is possible to provide the packaged die with a ball grid array (BGA) interface on its underside. This permits the camera module to be soldered to the main printed circuit board of the product at the same time as all the other semiconductor and passive components. Without this feature the camera module has to be assembled separately and connected to the main board by a flexible circuit and connector. Unreliability of these connectors is the major cause of field returns of camera phones with reportedly defective imagers. Owing to these benefits it is forecast that by 2012 more than 65% of all imagers will be enclosed in a wafer-level package with a BGA interface[2].

A wafer-level cavity package for an image sensor is achieved by forming a picture frame of adhesive around each die on the wafer, attaching a glass wafer and then sawing the assembly to yield individual die, each with a cover over the delicate image sensor area. This process is illustrated schematically in Figure 2. The requirement for the cavity owes to the lenses on the surface of the imager; an air space being necessary to achieve maximum refractive index change at the lens/air interface. Typically, the cavity height is around 40μm.

Wafer Level Package Interconnects

One of the major challenges of wafer level packaging is making contact to the bond pads. Bond pads in their traditional location on the front face of the die are rendered inaccessible by the glass cover that protects the optically sensitive area of the die. An obvious solution is through silicon via (TSV) technology. There are many variations of TSVs, a common implementation being a hollow pipe, with near-vertical sidewalls, machined through the thickness of the silicon. Onto the sidewalls of the pipe is applied a dielectric film overlaid with conductive metal. The through via is machined by deep reactive ion etching using the Bosch process[3].

Despite being technically possible for many years, TSVs have never been adopted in high volume manufacture. There are several reasons for this notable amongst which is the high capital cost of the equipment required, the slow etch rate of silicon, which curtails throughput, and the complexity of the additional process steps to fabricate conductive vias that are simultaneously insulated from the silicon through which they pass. There are also issues of reliability that have not yet been satisfactorily solved without additional cost. Points of weaknesses in the design include dielectric and conductive coating of the side walls of a high aspect ratio pipe; the 90 degree bends at the top and base of the pipe that the redistribution layer (RDL) must traverse and maintain connectivity during thermal cycling; and the difficulty of cleaning the back of the bond pad so the RDL can make an Ohmic contact, when it is the bottom of a long narrow pipe.

A modern wafer level package for image sensors is typified by the SHELLCASE® MVP solution, an example of which is shown in Figure 3. In this design connection between the bond pads and the ball grid array on the rear face of the package is by a via-through-pad technology. This solution means there are few restrictions on the bond pad size, pitch or location, making it directly compatible with the majority of existing CMOS imagers. The dicing lanes can be as narrow as the silicon design rules allow, which helps to maximize the number of die per wafer and decrease unit cost. The packaged imager thickness is approximately 500μm, making it imminently suitable for electronics products where the current fashion is for extreme thinness.

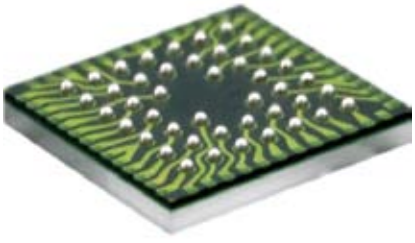


Figure 3. Image sensor packaged at the wafer level and provided with a ball grid array interface to simplify and cheapen attachment to a printed circuit board. *Source: Tessera*

The via-through-pad interconnect superficially resembles a TSV but the differences are important and have profound implications for the product cost and reliability. In this contact the RDL penetrates through the thickness of the bond pad to form a circumferential edge contact. Because the act of penetrating the bond pad exposes fresh metal at the circumference this solution obviates the difficulty of making Ohmic contact between the RDL and the bond pad. The via-through-pad contact is structurally identical to the well established edge contact[4] and hence has the same inherent reliability. Indeed, edge contacts have an in-service record exceeding a decade, based on a sample size of nearly 50 billion interconnects.

Via-through-pad interconnects require passageway through the silicon wafer. However, unlike TSVs, the opening is purely mechanical and needs only to expose sufficient area of the bond pad to permit formation of the via-through-pad edge contact. Consequently the alignment accuracy and limits on pitch are modest since several interconnects can share a single passageway. Because the passageways through the silicon do not have to be individual, the profile of the openings can be relaxed to a trapezoid with rounded corners. This eliminates two of the major sources of unreliability of TSVs. Finally, because via-through-pad interconnect is based on polymer technology with a single RDL it is very cost-effective compared with other TSV solutions.

Electrophoretic Materials

One of the main costs of wafer level packages is the bill of materials. Traditional polymer dielectric materials used by the semiconductor industry, like polyimide and

photo-imageable epoxies, are too expensive for a product where the ultimate goal is a video graphics array (VGA) camera module priced at under $1. A solution was identified in the form of a mature product, used in high tonnage by the automotive industry and consequently exceedingly low cost. Electrophoretic paints are materials that are deposited using the principle of electrostatic attraction. An electrocoat system applies a direct current charge to a metal part immersed in a bath of oppositely charged paint particles (see Figure 4). The paint particles are drawn to the metal part and adhere to it forming an even, continuous, film over the surface until the coating reaches the desired thickness. At that thickness, the film insulates the part so attraction stops and electrocoating is complete. The thickness is controlled by the voltage applied to the electrocoat bath and typically ranges from 5-75μm for a potential of 50-300volts.

Electrophoretic paints were developed to improve the corrosion resistance of car bodies with added benefit of excellent color and gloss control compared with sprayed paints. They do not contain heavy metals, generate little or no hazardous air pollutants and liberate very low levels of volatile organic chemicals. Above all, they are very low cost and some grades of electrophoretic paint can endow steel parts with corrosion resistance in excess of two thousand salt spray hours.

Data sheets for electrophoretic paints attest that they can only be applied to metals because the whole of the part to be coated must form either a cathode or anode in the electrochemical cell. Fortunately, because electrophoretic materials are potential rather than current driven, it was found that semiconductor grade silicon possesses sufficient electrical conductivity to allow direct coating, greatly simplifying the process flow.

Electrophoretic paints have high electrical resistivity and low dielectric constant[5]. These characteristics coupled with the excellent surface coverage makes the materials an excellent choice for the dielectric film of a wafer level package to insulate the RDL from the silicon die.

Reliability

Components intended for integration into products must be fit for purpose. Meeting this criterion is usually demonstrated by subjecting batches of components parts to various environmental regimes, which must be survived. For conventional semiconductor parts these tests are defined by Standards, one of the more arduous of which is the test for resistance to moisture ingress. Components housed in wafer level packages destined for camera phones must pass the JEDEC moisture sensitivity level 2 (MSL2) test. This entails exposing the parts to an atmosphere at 85°C, 60% relative humidity for 168 hours, followed by exposure to various thermal regimes, including thermal cycling. A typical test sample comprises a minimum of 3 lots of 77 parts taken from production batches manufactured on different days by different shifts on the full range of equipment available. It was found that parts protected by a layer of electrophoretic material approximately 15μm thick would not only pass these tests easily but could also pass the far more exacting standard for automotive components (see Table 1). This test involves exposure to MSL1 (85°C, 85% RH for 168 hours), followed by thermal regimes double the duration of those required for cell 'phone applications. Indeed, first failure did not occur unit nearly three times the test duration had passed6.

Test and Standard	Conditions and Duration
Preconditioning – moisture soak level one (MSL1) JESD22-A113-D	125 +5/-0°C, 24hrs 85 +/-20°C; 85 +/-5% RH, 168hrs Gradient <30°C/sec 100-150°C for 60-120sec 183°C for 60-150 sec 265 +0/ -5°C for 10-30 sec Gradient <6°C/sec Time from 25°C to peak <8 min x 3 cycles
Temperature and humidity after MSL 1 JESD22-A101-B	85 +5/-0°C 85 +/-2°C; 60 +/-3% RH 2000 hrs
High temperature storage after MSL 1 JESD22-A103-A	150 +/-5°C 2000 hrs
Thermal cycling after MSL 1 JESD22-A104-B	Min: -40 +0/-10°C ; Max: 125 +15/-0°C 32 cycles/ day 2000 cycles

Table 1. Reliability Standard for imagers destined for automotive applications

Conclusions

Packaging of solid state imagers is preferably accomplished at the wafer level since this approach is compatible with surface mount assembly and provides for a more compact, more reliable and lower cost solution than COB assembly. Protection of the front face of the imager is provided by a cover glass. This part obscures the bond pads on the die necessitating contact to be made either at the edges of the die or through its thickness. Because through silicon vias (TSVs) are not yet a commercial reality an alternative approach based on via-through-pad interconnects has been developed. This is a low cost solution because it is based on extremely cheap polymers developed for the automotive industry and a readily available equipment set. There are few restrictions on the bond pad size, pitch or location, making it directly compatible with the majority of existing CMOS imagers. The packaged imager is able to meet and surpasses both cell phone and automotive reliability standards for components and board level systems. ◆

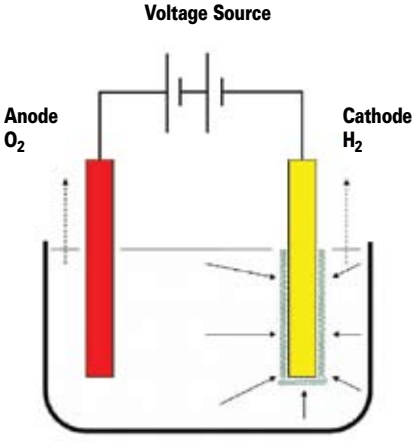


Figure 4. Principle of a cathodic electrocoating system. *Source: Tessera*

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"Thin" QFN, TAPP® and fpBGA Packages

Kelly R. McKendrick Sr.
Senior Field Applications Engineer, ASAT, Inc.

In early 1980 I started out as a Fab Rat in a state of the art 3 inch fab complete with emulsion masks and Kasper aligners. Metal etching was a pair of rubber gloves turning wafers in a cassette holder that went up and down in acid. Soon came our brand new 4 inch fab. I remember how big those wafers seemed. Later we heard rumors of 5 & 6 inch wafers and not long after that 8 inches. They were not wafers but silicon Frisbee's. Line width geometries were measured in microns. Like the 4 minute mile, 1 μm was a goal many thought would not be broken.

In the assembly world back then DIP's ruled and an 84 pin PLCC was really impressive. So was the price at several dollars. Soon came the revolution of QFP. Some had bumpers and some did not. 6 mil coplanarity was a challenge. 100 pins turned into 160 and then into 208 pins. Pricing came way down and the ultimate goal for a long time was a penny a pin. In the wire bond world 5 mil (127 μm) bond pad pitch was "Fine Pitch" and this was pushing the wirebond equipment vendors at the time to their limits.

"Thin" packaging at first was anything that was surface mounted. QFP's soon morphed into the ultimate thin package, the 1.0 mil thick TQFP. I was impressed and wondered how they could get a package to be so thin. To support these thin packages, the messy process of back lap soon gave way to back grind. Getting a wafer down to less than 12 mils was a real chore.

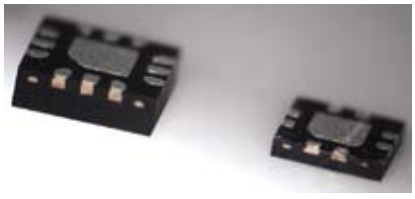
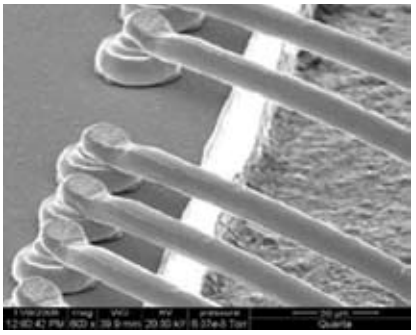


Figure 1.

Lead Frame	127 µm thick
Die Attach	die thickness: 100 µm
Wire Bond	50 µm loop height max.
Molding	250 µm mold thickness

Table 1.



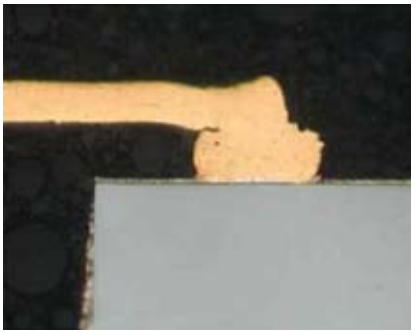


Figure 2.

Figure 3.

JEDEC came up with package profile height codes, such as "U" for Ultra Thin (0.65 mm max.), "X1" for Extra Thin (0.5 mm max.), "X2" for Super Thin (0.4 mm max.), "X3" for Paper Thin (0.3 mm max.) and "X4" for Die Thin (0.25 mm max.). Here at ASAT, we are working with several "Thin" packages. Among these are the X2-QFN package, the X3-TAPP package and the U-fpBGA package. Without going into too much detail, let me just give you a taste of how these packages look and are put together.

X2-QFN (0.4 mm max.)

Just like the TQFP package of not so long ago, die thickness, wire looping, mold thickness, and warpage are key factors to the success of this technology. In Figure 1, you can see that the standard V-QFN that was once considered thin looks thick when compared to the X2-QFN package.

In Table 1 you can see that several factors are critical in making this package. Die thickness must be 4 mils max (100 μm). With the advances in back grind technology, a 2 mil thick (50 μm) die is now realistic.

Wire loop height is also a critical factor. With the advances in wire bond technology 2 mil or 50 micron high wires are now realistic. See Figure 2.

Material sets have come a long way since the first time I tried to mold a large QFN lead frame that looked more like a potato chip than a flat strip. Thinner is not easier to mold. It brings on many more challenges and issues, especially when you add more recent factors into the equation such as MSL and Lead Free. See Figure 3 for a cross section of the X2-QFN.

X3-TAPP (0.3 mm max.)

Like the X2-QFN, the X3-TAPP, compared with the 0.8 mm version W-TAPP, shows quite a contrast. See Figure 4.

TAPP is a unique design and process and can be a tad bit thinner compared to a QFN with the same mold cap. Like the X2-QFN the same assembly rules apply except

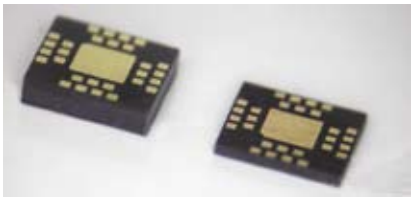


Figure 4.

the mold cap does not sit on top of a leadframe. Instead, the build-up metallization is embedded in the molded package body. See the cross section in Figure 5.

TAPP brings other advantages besides thickness. Higher pin counts in the same amount of space. Up to 3 multiple rows can be designed in with an optional floating power ring that can be added as one of the rows. TAPP also brings some improved electrical and thermal characteristics. TAPP also offers design flexibility due to its build-up technology that is otherwise not possible with leadframe-based packages.

U-fpBGA (0.65 mm max.)

The BGA package has changed a lot since it was first introduced many years ago. Like other packages the trend is always more I/O's, finer ball pitch, reduced lines and spaces, smaller outline and as you can see from the chart (Figure 6), thinner profiles.

Like any other "Thin" packages, this too requires special specs and materials. See Table 2.

Additionally, ASAT's U-fpBGA offers a full matrix of solder balls. See Figure 7 for a cross section of the U-fpBGA package.

A U-fpBGA is an excellent choice for higher pin counts in a small space. What used to be a fairly thick package has become a formidable competitor to the traditional thin packages.

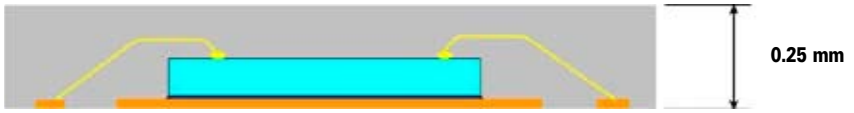


Figure 5.

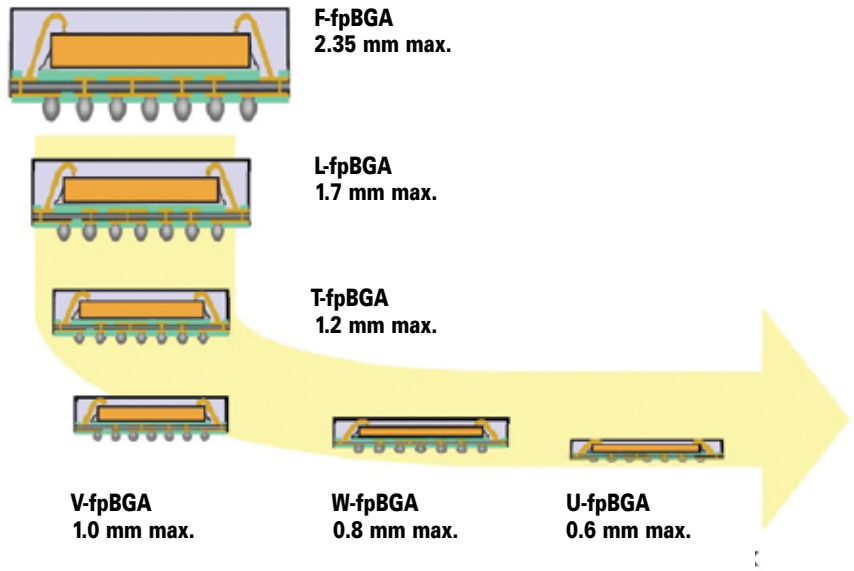


Figure 6.

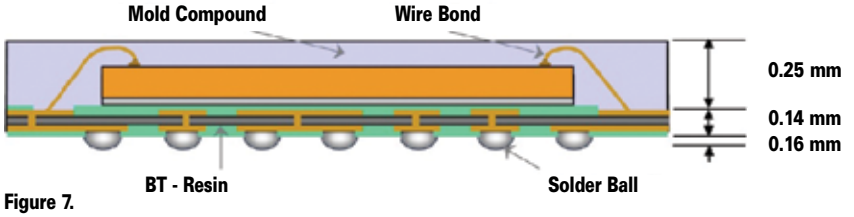


Figure 7.

Substrate	- 2 layers, - 140 µm thick
Backgrind	89 µm die thickness
Die Attach	25 µm (max.) thickness DAF
Wire Bond	Ultra low looping (50 µm max.) to accommodate the 250 µm thin mold
Molding	250 µm thin mold cap
Solder Ball Attach	Nominal 150 µm standoff
Warpage	Consideration: Substrate design, BOM selection & Die-to-mold vol. ratio

Table 2.

Other Factors

As briefly mentioned before other factors are now a huge part in determining package options and reliability. These seem to be especially prevalent in the thin packaging world. Two of the more common factors are MSL levels and Lead Free or "Green" packaging.

In the past MSL 3 was considered very good. Often parts would pass MSL level 1 but usually not on a consistent basis. Now MSL level 1 in thin packages is actually very doable and getting to be more and more of a standard requirement and not just a dream. With the increased reflow temperatures due to lead free/Green requirements, MSL 1 for most thin packages is now the standard.

"Lead Free" is quickly evolving into the more politically correct word "Green". I think the real question is what is "Green". Just when you think you have the final "Green" package and process, someone finds yet another substance that makes the green not so green anymore. I am not convinced that we will ever get a totally "Green" package. But hopefully we can come to some agreement on a standardized shade of Green. Even small changes can affect the manufacturability, MSL level and the assembly process of thin packages.

So what is the ultimate "Thin" package? We could have some fun debating this but my guess would be a Wafer Scale Package (WSP) ground to whatever thickness we can grind the die down to. Unless we come up with some new Star Trek technology I can not think of anything else we can do. But then again 28+ years ago who would have imagined that we would be doing packages less than 0.4 mm thick for pennies, parts would have more die and components than many PC boards back then, memory packages would have 8+ thin dies stacked on top of each other and wafers would be 12 inches with geometries measured in nanometers. In the meantime we will try and meet our customers' needs and work toward the "Ultimate" thin package, whatever that may be. ◆

Drop Shock Performance AND Temperature Cycling Reliability from a Single Lead-Free Alloy?

Robert Healey and Ranjit Pandher
Cookson Electronics Semiconductor Products

In the early 2000s when semiconductor package assemblers began making the switch to leadfree solder sphere alloys, the most common choices were alloys like SAC305 or SAC405. These "high-Ag" alloys were adopted as the standard, and experience was gained using them over the following years. It became well understood that high-Ag alloys demonstrated acceptable thermal cycling reliability, in many cases even better than Sn63/Pb37. However, as the handheld device market continued to grow, it became evident that high-Ag alloys were deficient to Sn63/Pb37 for dropshock performance. Since drop-shock resistance is a critical attribute for components going into handheld devices, alternate materials had to be explored.

In the past three years, alloys like SAC105 and SAC125 have been adopted for use in such parts. These "low-Ag" alloys exhibit superior drop-shock or impact resistance compared to their high-Ag predecessors. However, temperature cycling performance was sacrificed.

As a result, most semiconductor package assemblers are forced to utilize multiple lead-free alloys depending on desired performance attributes, package requirements, and end customer specifications. Today, most component assemblers are using at least two (and in many cases even more) lead-free solder sphere alloys to meet various package requirements.

Cookson Electronics has engaged in a significant program to develop a solder sphere alloy which provides the drop-shock performance of SAC105 or better, combined with the temperature cycling performance of SAC305 or better.

Cookson Electronics' SACX® alloy demonstrates extremely encouraging results. The SACX® alloy is comprised of 0.3% Ag / 0.7% Cu / plus "X". Test data shows that this alloy offers the targeted combination of excellent drop shock performance AND temperature cycling reliability. The following key attributes contribute to this alloy's exceptional reliability performance:

- Low Ag reduces the probability of Ag3Sn intermetallic precipitation in the bulk solder which results in improved drop shock resistance.
- "X" addition increases solder spread and wetting which improves the overall integrity of the solder joint.
- "X" addition controls the interfacial IMC thickness which improves drop-shock resistance.
- "X" addition also modifies the bulk grain structure, resulting in:
  - Increased solder strength
  - Improved creep resistance
  - Improved temperature cycling reliability

Cookson Electronics utilizes the JEDEC test protocol for measuring drop shock resistance. Figure 1 shows the relative drop-shock performance of SAC305 vs. SAC105 vs. SACX®.

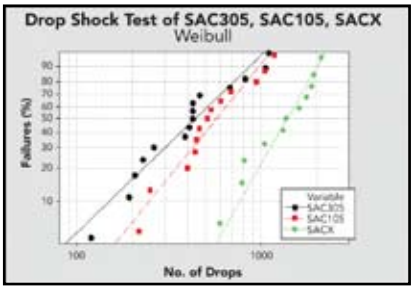


Figure 1. Drop Shock test results using 0.30mm (12mil) spheres at 0.5mm pitch attached to CABGA84 substrate with NiAu pad finish.

For this evaluation Cookson Electronics is testing temperature cycling under the following conditions: -55°C to 125°C with a 10 minute dwell at each stage. Figure 2 shows the relative performance of the alloys under test.

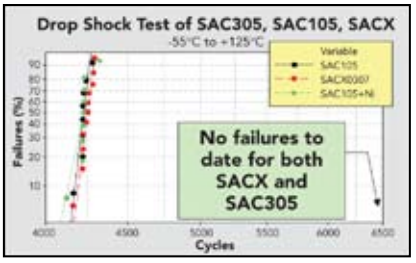


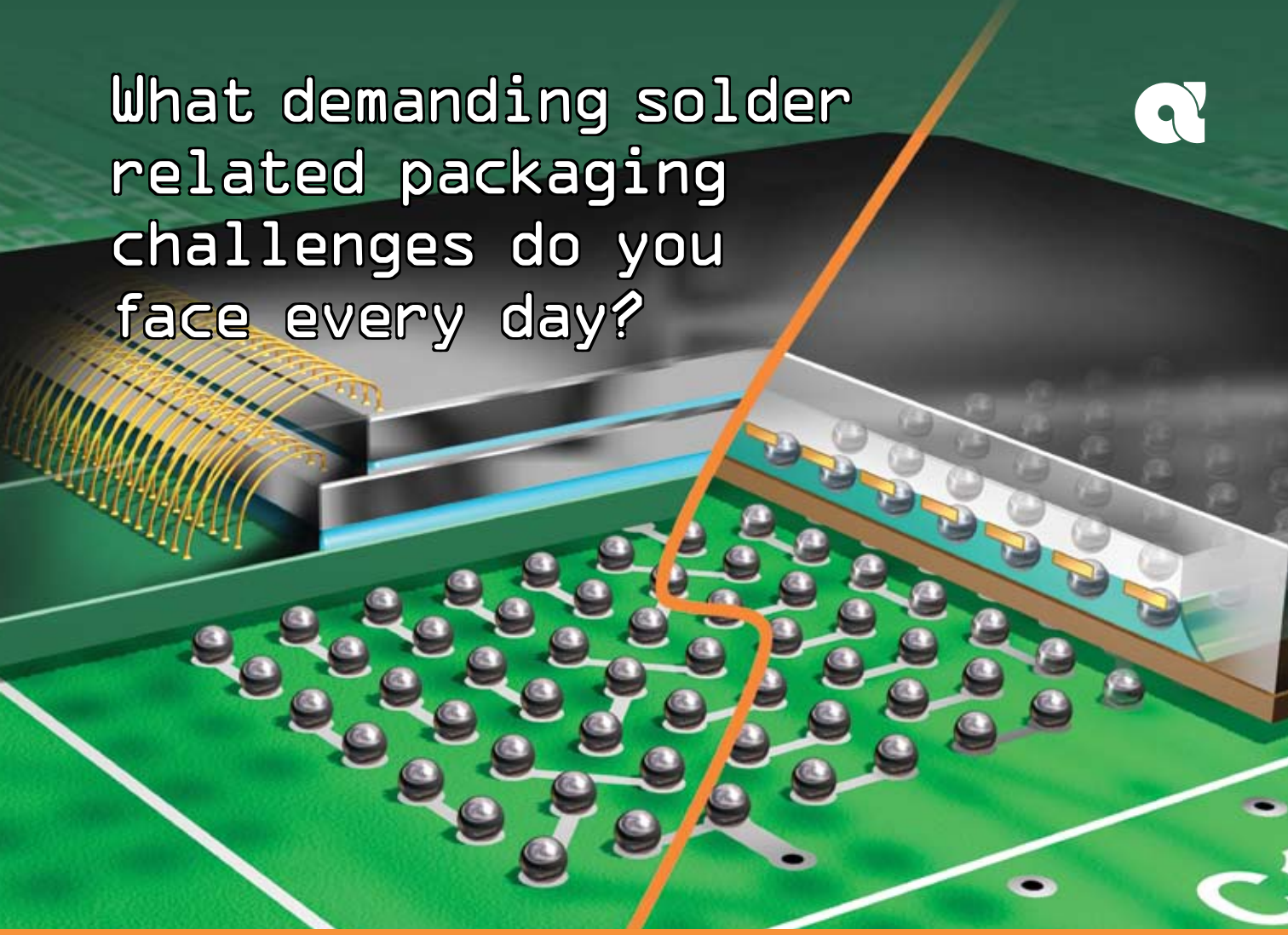
Figure 2. Temperature cycling test results. Test conditions are -55°C to +125°C with a 10 minute dwell at each stage.

The other low-Ag alloys all failed around the same time at approximately 4,000 – 4,300 cycles. The SACX® and SAC305 alloys have yet to fail, having already survived >6,500 cycles to date. This already represents over 60% improvement compared to the other low-Ag alloys and still going strong.

This excellent combination of drop shock and temperature cycling reliability could allow component assemblers to converge to a single lead-free alloy which meets all demanding reliability requirements.

In addition to solder spheres, Cookson Electronics offers other SACX® family solder products, such as solder paste, cored wire and bar solder. To learn more, please contact your local Cookson Electronics Semiconductor Products representative or visit www.cooksonsemi.com. ◆

What demanding solder related packaging challenges do you face every day?



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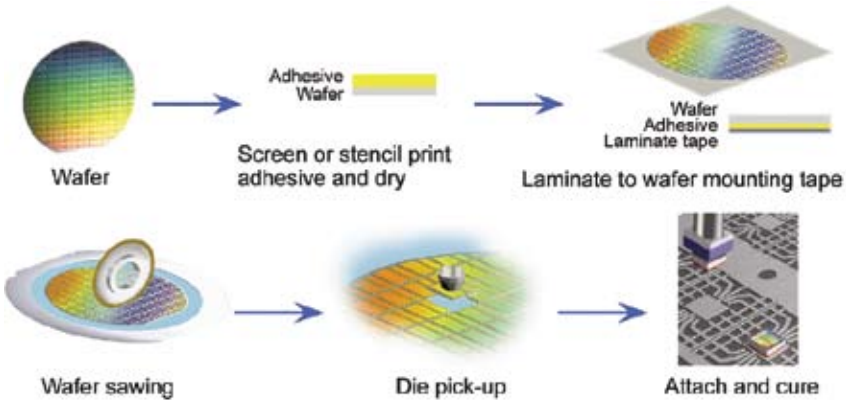
We've Got Your Back:

New Wafer Backside Coating™ Technology Offers Speed, Throughput and Cost-Effective Advantages over Alternative Materials & Methods

Davy Nakada
The Electronics Group of Henkel

While many advances in die attach methods and materials have taken center stage in recent months, there is one novel technology that has quietly emerged on the scene as, perhaps, one of the most innovative breakthroughs in die attach technology. The process, termed Wafer Backside Coating™, uses traditional materials deposition technologies – screen printing, stencil printing or spin coating – to efficiently coat the backside of wafers with die attach materials. The benefits of this technology include reduced costs, increased units per hour (UPH), tighter material control and the maximization of die footprint area through elimination of the fillet.

With conventional die attach pastes, material is deposited using an automated dispensing machine. And, while this is certainly a viable and popular approach, there are inherent drawbacks to this technique. First, because dispensing is a serial process, deposits of material can only be put down one or two at a time, depending on the number of dispense nozzles employed. So, the only way to increase throughput is to add more dispensing systems, which requires a substantial investment. Set-up time is also a major concern, particularly with highly miniaturized die which require the utmost precision. In these situations, machine set-up can take many hours. A second challenge with dispensing methods is maintaining a high level of quality and reliability. Placing a die into a very small dot of material is a delicate procedure and must be performed with near perfect accuracy to ensure a high-yield result. If the die is placed with too little force, the adhesive may not cover all of the die area. Conversely, if the die is placed with too much force, material may pushed out from under the die and adversely affect the bondline or flow past the desired die pad area. Die placement must also be level to avoid die tilt, a condition which may make wirebonding problematic or severely reduce reliability. In addition, there are certain applications which are simply not manufacturable with traditional die attach pastes. Chip-on-Lead devices, for example, have no pad on which the die sits so a controlled flow die attach material is the only solution.



Wafer Backside Coating Process Flow

These devices which require an alternative to traditional die attach pastes in combination with the industry's relentless drive for highly miniaturized die, smaller footprint packages is what led to the development of Henkel's Ablestik® 8000™ series Wafer Backside Coating™ (WBC) materials. Working in close cooperation with printing leader, DEK, the Ablestik product development team engineered a series of materials that combine exceptional die attach performance with the speed and ease-of-use provided by a screen or stencil printing platform. Offered in both conductive and non-conductive formulations, these Henkel die attach materials have effectively enabled applications such as chip-on-lead which were heretofore not cost-effectively manufacturable. While film is also a controlled flow solution, the cost of film is as much as 30% higher than that of liquid die attach paste materials. So, for low-ticket products, film methodologies are cost-prohibitive. Not only are there cost saving benefits to WBC materials, but there are substantial throughput and material control advantages as well. Using a highly accurate printing platform in combination with a tool set that delivers handling stability for ultra thin wafers, the wafer coating process only takes between 10 and 15 seconds. With a printer, the entire backside of the wafer is coated with die attach materials in one single stroke, as opposed to individual dot deposition that occurs with a dispensing system. Bondline thickness can be controlled to customer specifications and material thickness is consistent across the entire wafer. This technique has effectively achieved coatings as thin as 20 microns on wafers as thin as 100 microns and up to 300mm in diameter. Once the wafer is coated, the material is then B-staged so that the wafers can be easily stored for use at a later date.

While many materials manufacturers offer what they call a B-staging dual cure mechanism, not many can truly deliver on the essential characteristics for robust performance. In the B-staging process, the die attach material is advanced to a secondary state that is, in essence, a partial cure and is generally achieved with either a thermal or UV process. Henkel's Ablestik 8000 series are thermal cure B-staged materials. In order for B-staging to be effective, it is imperative that the material becomes film-like but not tacky. If the material remains tacky, foreign material contamination is highly likely. When B-staged properly, the WBC material is designed to be tack free and ready for subsequent processing or stored until required at a later date.

Currently, WBC materials are used in production for single die configuration devices. The technology has not yet been adopted for stacked die applications. This is primarily due to the bondline limitations and wafer handling requirements with current application methods. However, development work is underway and <10 micron thicknesses have been achieved with Ablestik WBC materials using novel application processes. It is certainly conceivable that WBC will replace film-based die attach materials in the not too distant future and Henkel's Ablestik brand products will undoubtedly be at the forefront.

For more information on the Ablestik 8000 series or any of Henkel's die attach materials, call Henkel headquarters at 949-789-2500.◆

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JULY 2008			1	2	3	4 INDEPENDENCE DAY	5
	6	7	8	9	10	11	12
	13	14	15 **SEMICON WEST 2008** Exhibits July 15 - 17 Moscone Center, San Francisco, California	16	17	18	19
	20	21	22	23	24	25	26
	27	28	29	30	31	1	2
AUGUST 2008	3	4	5	6	7	8	9
	10	11	12	13	14	15	16
	17	18 **2008 SMTA INTERNATIONAL** August 17 - 24 Disney's Coronado Springs Resort, Orlando, Florida	19	20	21	22	23
	24	25	26	27	28	29	30
SEPTEMBER 2008	31	1	2	3	4 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	5	6
	7	8 **KGD PACKAGING & TEST WORKSHOP** September 7 - 10 Embassy Suites, Napa, California	9	10	11 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley Sunnyvale, CA	12	13
	14	15	16	17	18	19	20
	21 28	22 29 AUTUMN BEGINS	23 30	24	25 **MEPTEC MEDICAL ELECTRONICS SYMPOSIUM** Arizona State University Tempe, Arizona	26	27

Evolving the Global Secondary Market

Gary Alexander, Executive Director
SEC/N® (Surplus Equipment Consortium / Network, Inc.)

In 1998 SEC/N® (Surplus Equipment Consortium/Network, Inc.) was founded based on the efforts and future concerns of the SEMATECH Surplus Equipment Council (SSEC).

Established in the late 1980's, the charter of the SSEC was to promote the buying and selling of used equipment between the SEMATECH member companies. Over the next 10 years, the SSEC accomplished its objectives, as well as having a positive influence on the U.S. semiconductor industry. However, the SSEC also came to realize that the evolving global secondary market represented challenges that they would not be able to effectively address.

In 1998, SEC/N picked-up where the SSEC left off:

- With a global focus on promoting professionalism and SEC/N's Code of Ethics.
- Developing used equipment related standards.
- Addressing common secondary market issues.
- Providing objective and timely information to its members and the industry.

Over the next several years, SEC/N grew to over fifty member companies including OEM's, device manufacturers, independent refurbishers, equipment brokers, and service providers. Historically, the majority of SEC/N members have been associated with wafer fab operations, with some representation from the backend segment of the business.

In 1999, SEMI (Semiconductor Equipment & Materials International) formally recognized SEC/N and over the past nine years, the two have worked together to provide informational seminars on the global secondhand equipment market at SEMICON exhibitions around the world. Unfortunately, other industry associations have not been as openly supportive of the secondary market.

In 2003, SEC/N was reincorporated as a 501 (c)(6), not-for-profit, member based organization, governed by a board of elected and appointed directors.

Secondary Market Growth

Estimations vary as to the size of the global market for secondhand goods. Why? Because there are an infinite number of potential sellers and there is no universal agreement as to which transactions to include or where in the transaction process to take the measurement. Additionally, many companies consider their secondary market activity to be confidential.

However, given what is available from key secondary market sources, it is safe to assume that the global secondary market for semiconductor and electronics manufacturing equipment in 2007 exceeded $6 billion. Prior to the mid-Nineties, the United States led all countries in both sales and purchases of secondhand electronics manufacturing equipment. The trading of used equipment in Europe and Japan was mostly internal and somewhat clandestine. The most significant and documented upward movement of the global market began with the ramp-up in the mid-Nineties of the foundry business in Taiwan.

Today, U.S. companies are primarily suppliers of used equipment to the global secondary market. For the past several years, the undisputed leader in the global purchasing of semiconductor used equipment has been the Peoples Republic of China. However, due to increasing labor and inflation rates, plus a decrease in government incentives and a 50% decline in their financial market, China no longer provides the same level of attraction for electronics manufacturing investment. More and more wafer manufacturers are now starting to show a serious interest in the Southeast Asia region.

Secondary Market Maturity

The initial encouragement for the founding of SEC/N came primarily from the device manufacturers. As both the sellers and the buyers of used equipment, they were very concerned about the quality, timeliness, costs, professionalism and ethics of the various middlemen involved; as well as the evolution of the global markets. At that time, most original equipment manufacturers (OEM's) had little or no interest in the secondhand market for their equipment and "wished" it would go away.

Over the past decade, there has been a virtual 180 degree shift in thinking on the part of both the device manufacturers and OEM's. Device manufacturers today exhibit little or no proactive interest in the future of the secondary market. On the other hand, many OEM business plans now incorporate formal used equipment strategies and programs. Why? Because the device manufacturers have virtually outsourced most of the secondhand equipment activities and the OEM's now understand the value of refurbishing their own equipment, especially during downturns in business.

A common challenge that most companies continue to face is the secondary market's global evolution. This challenge has been especially hard on brokers and independent refurbishers. Their difficulties in being able to resource a global infrastructure and unfortunate experiences in attempting to develop global partners often give the OEM's an edge.

Overall, the evolution in both growth and maturity has not been smooth, often resulting in negative publicity and many casualties.

The Future

As Bob Dylan's song warns, "The times they are a-changing." This is especially true when it comes to the global secondary market. For example:

- The market for secondhand goods is rapidly becoming the largest business in the world, if not already so.
- Markets for more mature technologies continue to evolve in developing countries.
- Government instability and differences in ideologies show little sign of improving.
- Given the escalation in labor and transportation costs, plus the impact of currency translation, future "low cost manufacturing" just might be closer to home than you think.
- Alliances, acquisitions, and bankruptcies will continue to impact the dynamics of the secondary market.
- Escalating capital investment in support of new technologies will result in less capital being available for mature technologies and the need to better utilize capital tied up in warehoused and depreciating surplus assets.
- Increased interest by governments and organizations such as the World Trade Organization, ANSI and ISO are moving the world's market for secondhand goods towards more standards, laws and certifications.

The bottom line is that going forward; no company will be immune from the need to embrace the global market for secondhand goods. Future success will be dependent on knowledge, past lessons learned, commitment, and a bit of luck.

SEC/N and SEMI's joint efforts are excellent sources of objective and timely information. Expanding those efforts across the electronics industry offer both an opportunity and a challenge.

And as for commitment and luck, you are on your own. ◆

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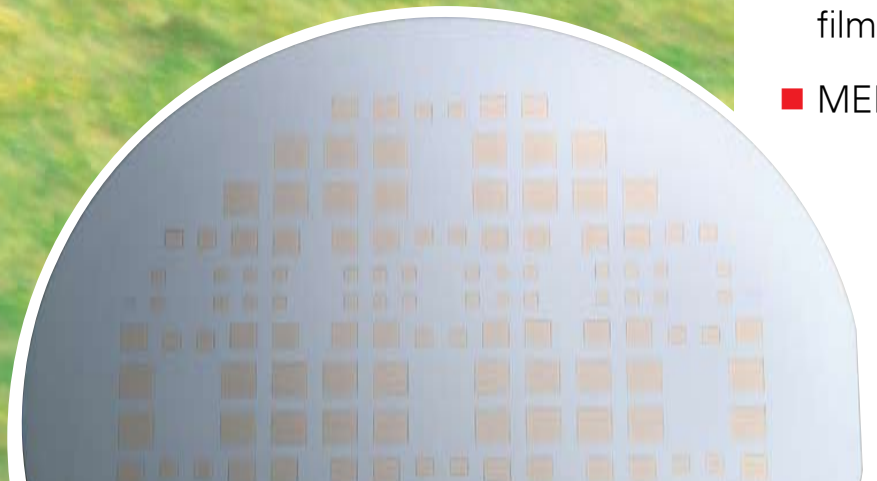

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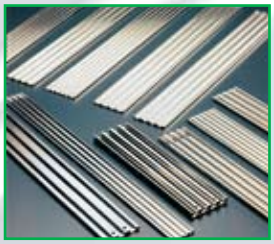
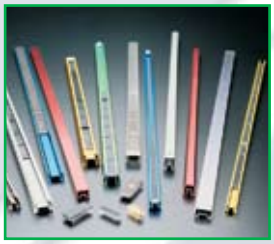
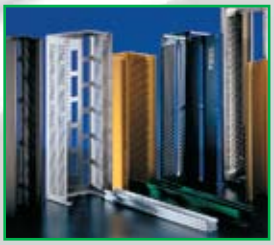

I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines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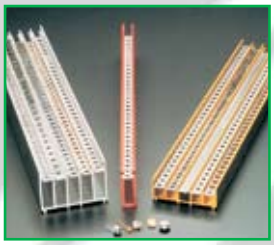
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