MEPTEC Report

Volume 13, Number 2

FALL 2009

A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Quik-Pak, a division of **Delphon Industries**, has announced the appointment of Julie Adams as Worldwide Sales Director. *page 14*

ALLVIA, the first through-silicon via (TSV) foundry, has hired SunSil Inc. to sell and market their products and services in the United States. *page 15*

Amkor Technology has been recognized with the 2009 Global Frost & Sullivan Technology Innovation of the Year Award for its line-up of innovative new products, including through mold via package on package (TMV™PoP), FusionQuad® and flip chip molded ball grid array (FCMBGA). *page 16*

Maxtek announces the introduction of Rapid Prototyping Services. The new services, a result of industry and voice-of-customer research, are designed to support the need for faster validation of IC and package designs and speed the transition to full production. *page 17*

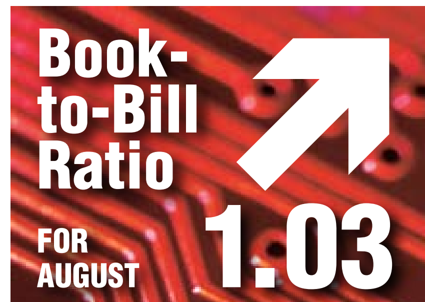
RTI's 2009 Technology Venture Forum comes to the Hyatt Regency San Francisco Airport Hotel in Burlingame, California December 9th to 11th. *page 14*

MEMBER COMPANY PROFILE

Headquartered in Niigata-City, the largest city in northwestern Japan, NAMICS employs approximately 450 people worldwide. Their domestic facilities include their Headquarters and Factory, NAMICS Techno Core (NTC), the Tsukioka Factory and sales offices in Tokyo and Osaka. Their overseas operations include sales offices in San Jose and New York in the United States, Singapore, and Munich.

NAMICS Corporation was originally established in 1946 as Hokuriku Toryo Co. Ltd., a manufacturer of paints and coatings for household and industrial use. In 1958, they successfully developed CERACOAT as their first insulating material for the electronics market. Ten years later they developed silver filled conductive pastes. In 1980, they ceased production of regular industrial paints and coatings and diverted completely into the manufacture of materials for the electronics market. At their 50th year anniversary the company name was changed to NAMICS Corporation. *page 10*

Semiconductor equipment bookings increase 5% over July 2009 level. *page 16*



42nd International Symposium on Microelectronics

Bringing Together The Entire Microelectronics Supply Chain!

San Jose, California
November 1-5, 2009

IMAPS 2009

Planned Sessions Include:

Industry

- Consumer, Portable and Wireless
- Biomedical
- Telecom
- Defense and Security
- Computing and Gaming
- Automotive and Industrial
- Solar and Alternative Energy

Systems & Applications

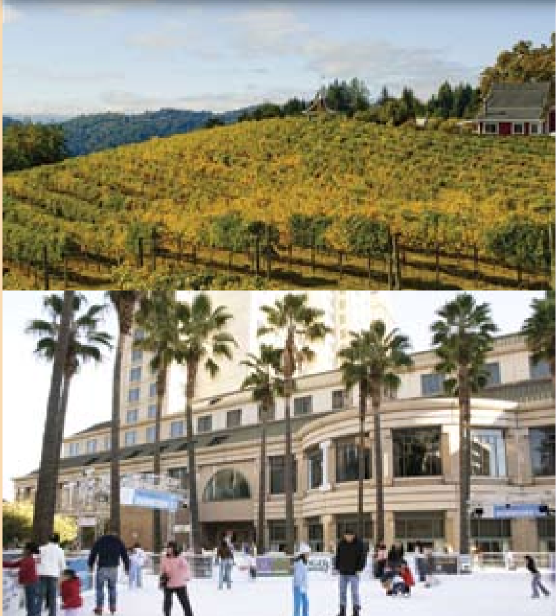
- Thermal Management
- Power Management
- Cost Reduction, Outsourcing and Supply Chain Management
- Electromagnetic Interference (EMI)
- Sensors and Nano Packaging
- Emerging Technologies
- System Packaging
- Microwave & RF Applications
- Electrostatic Discharge (ESD) Protection
- Photonic / Optoelectronic Packaging
- Packaging for Extreme Environments
- MEMS Packaging
- LED Packaging
- Packaging of Compound Semiconductor Devices

Design

- Signal Integrity
- Power Integrity
- Electrical Modeling
- High Performance Interconnects and Boards
- 3D Packaging Approaches
- Embedded and Integrated Passives
- Wafer Level Packaging / CSP
- Advanced Materials

Materials and Process

- Flip-Chip and Wafer Bumping Processes and Reliability
- Underfill/Encapsulants and Adhesives
- Pb-Free Solder Materials, RoHS, Processes, and Reliability
- Design for Reliability
- Package Reliability Testing
- Wirebonding and Stud Bumping
- Ceramic and LTCC Packaging
- Substrate Materials and Technology
- Printed Electronics



Many California wineries are in the San Jose area.

Ice skating in downtown San Jose!

San Jose Museum of Art

www.imaps2009.org

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Council Update

Welcome to the Fall edition of the MEPTEC Report! Our first post-summer event was our *4th Annual Medical Electronics Symposium* which again was hosted by **Arizona State University** at the historic Old Main building on the Tempe campus. This year we teamed up with **SMTA** for a two-day conference; based on the increased attendance over last year, it was a great success. If you missed it, CDs of the proceedings are available – contact MEPTEC for information on ordering or visit www.meptec.org.

Last year we started our series of workshops being held in conjunction with **MEMS Investor Journal**. We are pleased to continue them this year: on October 21st we will hold our *2nd Annual MEMS Testing and Reliability Workshop*, and on October 22nd we offer the *1st Annual Micro Power Technology Workshop*. Both events will be held at the Radisson Plaza hotel in San Jose. See page 8 for more information on these workshops.

MEPTEC's next event will be held on November 19th and is titled *Semiconductor to Solar: Growth Opportunities for the IC Industry*. At our last MEPTEC Advisory Board meeting it was unanimous that we cover the solar/photovoltaic industry, as there are many opportunities for our own industry. **Abhay Maheswari**, former MEPTEC board member and a VP at **Xilinx**, will be the technical chair for this event. He is now VP of Research and Development at **Solaria**, so he brings a wealth of information and perspective from both industries. Long-time MEPTEC Advisory Board member, **Seth Alavi** of **SunSil, Inc.** and **Cliff Tsay**, formerly with **Exar** and now a consultant in the PV/Solar arena, are helping to develop the program. Exhibits and sponsorships are available. See pages 4 and 5 for further information.

Our Company Profile this issue is from MEPTEC Corporate member **NAMICS Corporation**. The company was founded in 1946 as a manufacturer of paints and coatings for household industrial use, and over the years started diversifying into industrial materials, eventually diverting completely into manufacturing materials for the electronics market. Interestingly, NAMICS stands for "Nature and Art, Mutual Prosperity, Innovation, Creativity, and Sensitivity", which describes the essence of their corporate philosophy. See page 10 for their story.

Our Industry Analysis is from **Adrienne Downey** of **Semico Research Corporation** (page 6). In *The "R" Word is no Longer Recession, it's Recovery* Adrienne looks at sequential revenue growth in Q2-09, capacity utilization, capital spending and other factors that are driving the recovery. She concludes with "the companies with the best cash positions that can continue to invest in capacity and new products will win".

The Editorial in this issue continues the economic theme. In *Innovating Through the Downturn*, **Michael Todd** of **Henkel Corporation** (and new MEPTEC Advisory Board member) presents the view that maintaining R&D investment levels during a deep recession may be difficult, but should be a commitment that is essential. He suggests that future success for all companies relies on the continuing technology innovations, no matter what the economic situation. See page 30 for this interesting perspective.

Our first feature article is from **Dan Popa** and **Harry Stephanou** of **Automation & Robotics Research Institute** at the **University of Texas at Arlington**. In *Making MEMS Manufacturable – Tools for Back-End Processes* they describe recent advances in micro and nano technology which have increased the demand for MEMS devices. Their work at ARRI has led to creating a systematic approach to MEMS manufacturing that guarantees high yield and reliable operations for Microsystems (see page 18).

Our next feature article is from **Johannes de Groot** of **Zoran Corporation**. *Thermal Stability and Run-Away Margins of Packaged SOC in Advanced Wafer Technologies* discusses a variety of trends that are putting constraints on package design in SOCs. He describes methodology and components to predict thermal behavior, SOC leakage power and run-away margins. See page 24 for this informative article.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time we hope you enjoy it. Thanks for joining us! ◆

Abhay Maheswari, VP R&D
Solari Corporation

Photovoltaics are a major source of renewable energy today. At first glance these simple PN junction semiconductors have very little complexity. However they are much larger in scale and their application requirements are very stringent. The semiconductor industry on the other hand deals with devices that are ever shrinking and complex. Both have their application spaces which have been clearly defined for many years. However the current boom in the renewable industry has seen significant improvements in renewable technologies and application of integrated circuits as controllers in most PV based systems in parts known as Inverters. Essentially a bridge is being established between the two worlds so that the best of both could be extracted for most efficient PV system yet to come.

In many ways there are system similarities between semiconductors and PV systems. The PV's are very similar to integrated circuits: the interconnects are similar, the packaging of semiconductors resembles the PV modules, the external leads in semiconductor devices that are similar to external cables and junction boxes that connect the system together. In spite of these similarities, there are significant differences. The larger scale PV systems lend to different reliability metrics than IC's. The housing of these PV cells have a set of requirements in the field when they are completely exposed to the environment, as opposed to IC's in packages and PCB's that are enclosed in boxes partially or fully protected from external environments. Hence the test sets methodologies for viable technology in PV applications require a very different focus than integrated circuits, electronic packages and PCBs.

An integral part of PV systems are inverters. This is where ICs are now playing a major role. Other than integrated circuits the key elements that define the inverter's long term viability are many discrete elements, including capacitors. Viability of present inverter technology is questionable today as this part of the PV system has a record low long-term reliability. These components are 10 times less reliable today than the rest of the PV system; however these are essential part of the PV system. There is no doubt that inverter technology and components would need special attention from designers and packagers of integrated and discrete systems with defined tests that mimic applications in field conditions. The current semiconductor industry can contribute significantly to improve system reliability of renewable energy generation systems by improving the reliability and performance of these systems thereby reducing the risk of periodic component failures in the lifecycle of a PV system.

As semiconductor technology went through an upheaval in the last 10 to 15 years and established methods and processes that helped differentiate products for application specific use conditions, a similar approach will be required to better evaluate long term reliability of PV systems. Reforms may be necessary in the standards and methods to address the real concerns of long term viability.

About the Conference

This conference will focus on the basics of PV-based systems as well specific requirements and nuances the industry faces today. It will also focus on specific applications of ICs into photovoltaic applications that are either essential parts of the PV system or would play a significant role in managing performance of PV systems.

Test methods and qualification methodologies established today focus on minimum levels of assurance for long term viability. The advent of new technologies mandate looking at these processes more carefully and challenge existing methods and tests, including materials and constructions in critical use conditions. While some tests may still be valid, there is increasing scrutiny of existing methods which do not project long term reliability of existing systems. The conference will also focus on key learnings, test requirements, and test methods with newer and existing materials, and constructions and processes that drive evaluations of systems as a whole for use conditions they target. ◆

Sessions will include:

Photovoltaic Industry Overview and Current Trends

This session will be geared towards the photovoltaic industry trends in terms technology and capacity. As part of trend analysis, worldwide photovoltaic technology trends, and the growth of photovoltaic compared to other renewable as well as projected growth of these technologies considering current down turn will be discussed. Part of this analysis may show the current capacity and investments in future PV cell capacity, moduling as well other BOM capacity + scaling. Special emphasis on US growth trends will also be made available to attendees. A significant take-away from this session will be an understanding of the impact of government policies in terms of renewable and photovoltaic growth in terms of RPS, incentive programs at the federal and state levels and how the semiconductor industry can be participants and the specific roles they can play.

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MEPTEC PRESENTS

A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

Semiconductor to Solar

Growth Opportunities for the IC Industry

November 19, 2009 • Radisson Hotel • San Jose, CA

Enabling Technologies

The semiconductor industry has always played a major role in terms of materials and technology for photovoltaic. The processes adopted in terms of cost reduction and simplification in photovoltaic production today is better understood in the semiconductor space and more akin to the production processes of PCB as well as semiconductors. This session will focus on all enabling technologies including materials such as crystalline and amorphous Si, and several mainstream thin film technologies such as CdTe and CIGS. The impact of materials, purity and supply potential for the long term will be of key focus in this area. Other areas covered will include reliability assessments, equipment requirements, energy management, etc.

Manufacturing Challenges & Processing for Solar Photovoltaic

This session will address issues related to photovoltaic processing, the associated controls and their impact on efficiency, reliability and repeatability of final product. Semiconductor processes established today, including PCB manufacturing of high performance advanced design rules, mandates critical controls that have been around for a long time. Similar controls can benefit crystalline PV production as well as thin film PV module production greatly. The significance of high volume manufacturing with critical controls to increase yields at a reduced cost, always remains a challenge for the PV industry. The session will focus on key controls and methodologies that are required for high volume production of high performance solar materials as well as modules, so that the solar system cost could be reduced significantly towards grid parity and beyond while reliability and performance could be improved over the system's life expectancy.

Future Trends & Opportunities for the IC Industry

Knowledge already established in IC and packaging industry is directly applicable to the PV solar industry today. There is process knowledge, material knowledge, as well as reliability assessment knowledge that could be effectively transported and implemented at the lowest cost as possible. This session will focus on key areas of limitations that the PV industry is facing today and possible solutions that need to be transported from IC and packaging industry to eliminate those hurdles.

Register online today at www.meptec.org

MEDIA SPONSORS

The "R" Word is No Longer Recession, It's Recovery!

Adrienne Downey
Semico Research Corp.

The Recovery is Here!

Yes, worldwide economic conditions have been tough. Late 2008 and the first quarter of 2009 were brutal, but the semiconductor industry did a good job of reacting quickly this time around and was able to avoid a large accumulation of excess inventory. As inventories were depleted, prices firmed and orders increased. Capacity utilization rates increased from 57% in 1Q09 to 78% in 2Q09. Companies across the industry report that utilization rates will continue to improve in the third quarter, and Semico expects rates to remain high through 2010.

Increasing capacity utilization has translated to increasing revenues. Figure 1 shows the average percent sequential revenue growth in 2Q09 for a sampling of companies in five semiconductor market segments. 2Q09 revenues were strongest for foundries and backend service providers, but even IDMs showed a 19% average revenue increase. Part of the healthy growth was due to inventories returning to healthy levels. In 3Q09 the industry will continue to see improvements. On average, semiconductor companies are expecting a 10-16% sequential increase in revenues in the third quarter.

Test equipment makers as well as packaging and testing companies all expect to see strong revenue growth in 3Q09. Outsourcing orders from IDMs will increase, benefitting backend companies. Amkor and ASE have increased their capital spending projections for the rest of 2009. For LCD driver IC backend provider Chipbond Technology, sales increased 40% in July 2009. Chipbond expects utilization rates in the upper 90% range in the second half of 2009.

On the equipment side, TEL reported rising orders from makers of both memory and logic chips; the company recorded a smaller-than-expected loss in the second quarter. Applied's revenue increased 10% in the quarter ended July 26. The company expects revenues for the current quarter to be up 10-20% sequentially. We think 20% growth is entirely possible, given the huge spending commitments that TSMC has made for the second half of 2009.

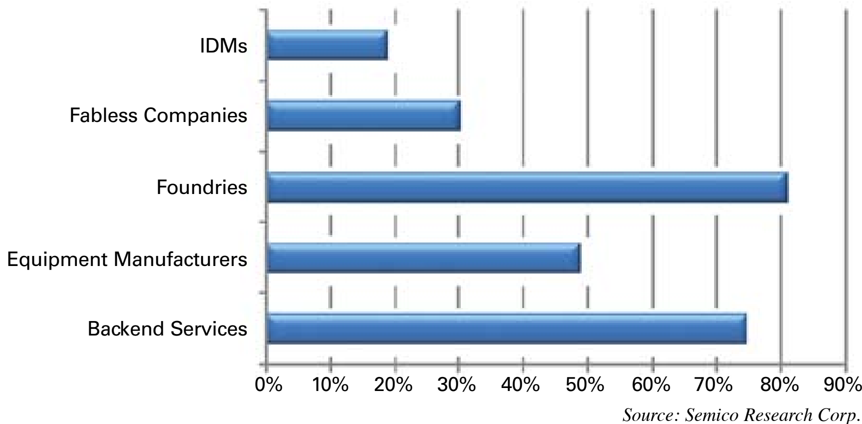

Figure 1. Second Quarter 2009 Sequential Revenue Growth, by Company Type

Capital Spending: Too Little, Too Late?

As shown in Figure 2, capital spending is down 35% in 2009, after declining in both 2007 and 2008. Capital spending includes money spent on fab construction and expansion projects, as well as money spent on new tool sets for existing fabs. The severe decline in capex has resulted in many projects being put on hold or being cancelled altogether. This in turn has reduced the total amount of capacity coming online in the next couple years.

Capital spending is more efficient today due to the continued trend by most companies to utilize foundry capacity and move to a "fab-lite" model. Other

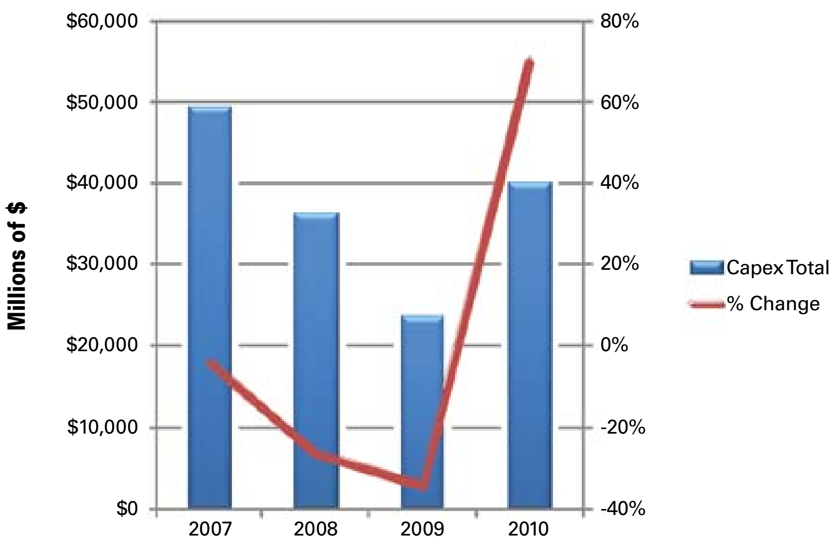

Figure 2. Semiconductor Industry Capex, 2007-2010 *Source: Semico Research Corp.*

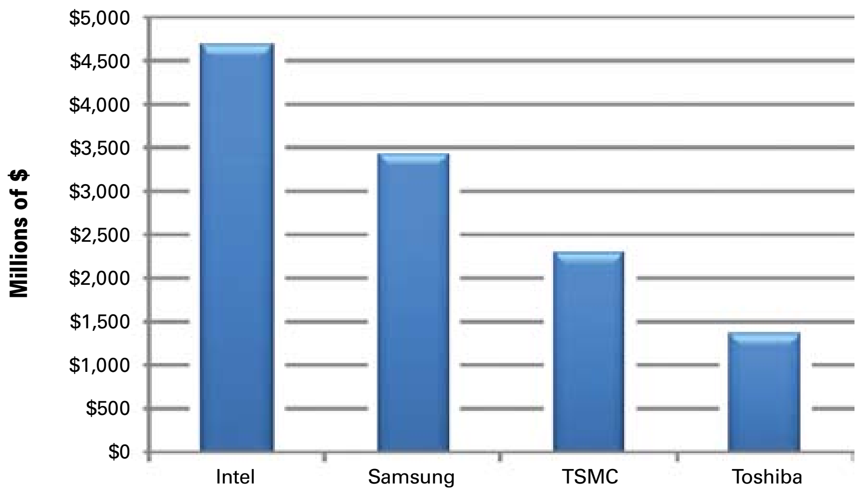

Figure 3. Top Four Capital Spenders in 2009 *Source: Semico Research Corp.*

companies are partnering or consolidating to reduce manufacturing costs. Also affecting capital expenditures and capacity is the closure of fabs by companies going out of business.

However, spending is beginning to increase in the second half of 2009 after a strong second quarter. The capex outlook for 2010 is very positive, continuing the upward momentum from 2H09. Semico forecasts 2010 capex will be $40.1 billion, up 70% from 2009.

Because of the current difficult economic environment, capital investment in 2009 has been slashed by most semiconductor manufacturers and foundries in the industry. As shown in Figure 3, Semico has identified four companies as "big spenders" for 2009: Intel, Samsung, TSMC, and Toshiba. Another twelve companies follow in the $500 million to $1 billion range. The focus of much of this capex is more on improving process technologies rather than adding capacity.

Once again, reduced capital investment during a downturn will soon lead to shortages, increased ASPs and increased revenue.

The capex story at TSMC is particularly interesting. In April 2009, the company stated that 2009 capex would be around $1.5 billion, down 20% from its 2008 spending. By June 2009, Morris Chang, founder and CEO, stated that TSMC's capital expenditures would be $1.9 billion, or flat compared to 2008. Chang said the increase in spending was due to the recovery he saw in the semiconductor industry, based on stronger demand in the second quarter of 2009. By July 2009, Lora Ho, VP and CFO, announced that capital spending will now be $2.3 billion, up

continued on page 9

2nd Annual Workshop on MEMS Testing and Reliability

October 21, 2009 • Radisson Hotel, San Jose, California

MEMS testing and reliability assurance are critical to achieving high production yields and profitability as these processes account for 40 to 70% of the total device cost. According to recent studies, the total world MEMS test equipment market generated revenues of $68.5 million in 2008, at an annual growth rate of approximately 11 percent. While MEMS testing is similar to chip testing in the semiconductors industry, MEMS present further challenges because mechanical, chemical and optical parameters must be tested in addition to electrical properties.

Topics that will be covered at the workshop include:

- Overview of state-of-the-art MEMS testing and reliability strategies
- Wafer-level MEMS testing
- Post-packaging MEMS testing
- Specific tips and techniques
- MEMS test equipment presentations from leading suppliers

Wednesday, October 21, 2009 • 8 am to 5 pm

Register Online Today at

www.memstestreliability2009.com

Co-Produced by MEMS Investor Journal and MEPTEC

1st Annual Workshop on MICRO POWER TECHNOLOGIES

OCTOBER 22, 2009

Radisson Hotel
San Jose, California

According to recent studies and estimates, the market for wireless sensor networks will reach approximately $5.7 billion by 2012. One of the main challenges for this market's development is the emergence of technologies to power all of these wireless sensor nodes. Accordingly, micro power technologies have emerged as a hot technology area that can provide many lucrative investment and development opportunities.

This workshop will ensure that you and your organization are optimally positioned and prepared for business development opportunities in this exciting and rapidly developing technology area.

Topics that will be covered at the workshop include:

- Energy scavenging for MEMS devices and microsystems
- Electrostatic, piezoelectric and electromagnetic energy conversion schemes
- Thermoelectric systems and micro coolers
- Photovoltaic systems
- Micro fuel cells and micro reactors
- Micro combustion engines for power generation and propulsion
- Materials for energy applications
- Micro power ICs and transducers
- Micro battery technologies

Thursday, October 22, 2009 • 8 am to 5 pm

Register Online Today at

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Industry Analysis

continued from page 7

22% from 2008. The increase is due to a positive outlook for demand in 2010 and a "more aggressive technology strategy." Because little was spent in 1H09, TSMC could spend as much as $2 billion in the 2H09.

The economy is emerging from a recession and technology driven markets are attracting consumer dollars again. Based on Semico's supply and demand analysis of leading electronic markets and the related semiconductor content, the dip in capital spending in 2007-2009 and the postponement of so many fab projects could soon create shortage conditions for certain devices, including leading-edge DRAM and NAND, display drivers, LED drivers, touch screen controllers, and MEMS devices like gyroscopes, acceleration sensors. Supplies of CMOS image sensors are already tight from Samsung, Aptiva, and Omni Vision, due to increased demand from notebook makers.

In the memory industry, DRAM prices increased in 2Q09, with some allocation expected in the third quarter. Memory will see steady growth in 2H09, and will be strong for the next two years. Consolidation will continue; Qimonda was the beginning. In Taiwan, the government's proposed Taiwan Memory Company may never materialize, and smaller Taiwanese DRAM makers may not survive. As always in the memory market, continued investment is necessary in order to move to smaller process nodes and remain competitive.

Many executives are cautiously optimistic about the rest of 2009 and are bracing for a "W" shaped recovery. In other words, some executives are preparing for another decline before the industry truly recovers. Semico does not believe this will be a double dip cycle because government incentive programs being implemented all around the world are resulting in increased economic activity. In the US, the Federal Reserve continues to maintain lending rates at near zero.

Electronics are no longer considered a luxury item. Cell phones and new devices such as the netbook are now consumer 'needs'. The companies with the best cash positions that can continue to invest in capacity and new products will win. ◆

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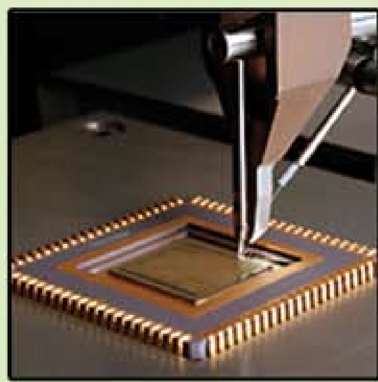

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NAMICS

MUTUAL PROSPERITY TO BOTH MANKIND AND NATURE THROUGH CREATIVITY, INNOVATION AND SENSITIVITY

In 1946, NAMICS Corporation was originally established as Hokuriku Toryo Co. Ltd., a manufacturer of paints and coatings for household and industrial use. In 1958, they successfully developed CERACOAT as their first insulating material for the electronics market. Ten years later they developed silver filled conductive pastes. In 1980, they ceased production of regular industrial paints and coatings and diverted completely into the manufacture of materials for the electronics market. Their sole dedication to this market led to the commercialization of HIMEC® and UNIMEC®, sintering and thermosetting types of conductive pastes respectively. In addition, through extensive research and development they developed the CHIPCOAT® line of products which are high purity insulating materials for ICs and LSIs.

At their 50th year anniversary, the company name was changed to NAMICS CORPORATION. NAMICS stands for

Top: NAMICS Techno Core (NTC) R&D Center. Above: NAMICS headquarters and factory in Niigata-City, Japan. Right: NAMICS product line up of conductive and insulating materials for the electronics industry.

"Nature and Art, Mutual Prosperity, Innovation, Creativity, and Sensitivity" which make up the essence of their corporate philosophy.

Headquartered in Niigata-City, the largest city in northwestern Japan, NAMICS employs approximately 450 people worldwide. Their domestic facilities include their Headquarters and Factory, NAMICS Techno Core (NTC), the Tsukioka Factory and sales offices in Tokyo and Osaka. Their overseas operations include sales offices in San Jose and New York in the United States, Singapore, and Munich, Germany. They are also represented in Seoul, Shanghai, and Taiwan, as well as Denmark, Italy, and France. They also have a factory in Yantai, China where they manufacture insulating materials for electronic components.

In 2008, NAMICS Corporation acquired Diemat Inc., located in Byfield, Massachusetts. Diemat specializes in the development and manufacture of innovative adhesive and sealing materials to serve the electronic packaging industry. Diemat developed and patented new generation materials, the first of which was a lower temperature (300°C) Ag loaded glass adhesive for die attachment. The low temperature glass technology is also available in lead-free compositions.

Diemat also developed and patented a unique family of organic adhesives offering thermal conductivity that is an order of magnitude greater than prior art. Unique polymer compositions and combinations of thermoplastic and thermoset polymers are utilized. These provide "application specific" products with widely ranging properties in the modulus of elasticity, high temperature adhesion, and reworkability.

More recently, Diemat developed a low temperature, solder-glass preform for hermetically sealing optical fibers in optoelectronic packages. This technology replaces the more expensive soldering process, which requires fiber metallization. This low temperature glass technology is also utilized in hermetically sealing lenses for the optoelectronic industry, as well as hermetic sealing of package lids.

With these worldwide operations, NAMICS doubled their sales and workforce within the past ten years. They have become a leading company producing both conductive and insulating materials for the electronics industry.

NAMICS Photovoltaic Business

NAMICS has been developing and manufacturing conductive pastes for photovoltaic applications since 1995. Currently, they are actively expanding their businesses in photovoltaics, taking advantage of their 15-year experience in manufacturing conductive pastes for this market. The electrode materials for solar cells are becoming one of their key product families.

NAMICS supplies two types of pastes for the photovoltaic market; one is a firing type silver paste, HIMEC® Solar, and the other is a thermosetting silver paste, UNIMEC® Solar. The former is widely used for the front electrode of crystalline silicon solar cells. The characteristics of NAMICS HIMEC® Solar are:

1) The electrode can be formed in air at a peak temperature of 650 to 850˚C by rapid firing of several-minutes.

2) The optimal Ohmic contact enables the reduction of series resistance of solar cells by fire-through anti-reflection film which is formed on the surface of solar cells.

3) A fine line and a high aspect ratio of the electrode can be achieved by screen printing.

Solar cells have extremely thin electrodes on their surface, and these electrodes have a role in collecting energy generated by photovoltaics. With the superior characteristics of their pastes, they have succeeded in achieving a high conversion efficiency for crystalline silicon solar cells. HIMEC® Solar includes silver paste for back side electrodes as well.

UNIMEC® Solar silver paste is a thermoset material that cures at a temperature of 180 to 200˚C for about 30 minutes. Since thermal damage to the cells can occur during processes, temperature should be controlled as much as possible in the manufacture of thin film solar cells, such as, amorphous silicon, CIGS (Copper-Indium-Gallium-Selenium) systems, die systems, and organic systems.

NAMICS offers insulating pastes as well as conductive pastes, and they are proud of contributing to the photovoltaic field through developing solutions for a wide range of customers.

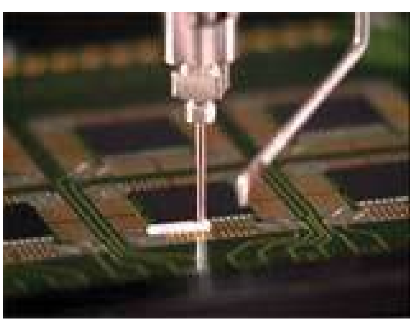
NAMICS Technology

Underfills are materials that protect semiconductors from dust, moisture, vibration, impact, and serve as an encapsulant. CHIPCOAT® is one of their key products, and they have been developing and marketing this UF for the past twenty years. In addition, HIMEC® and UNIMEC® are flagship products of NAMICS that are used in the manufacture of passive components.

New product development is a primary goal to drive growth. Therefore, they are actively developing high quality cutting-edge products to lead the next generation. Based on their three core technologies;

NAMICS' product line up includes (from top)
1 - Solar Paste Products
2 - COF Products
3 - Overcoat Products
4 - HIMEC® Products
5 - UNIMEC® Products

The new NAMICS Techno Core (NTC) Research and Development Center, shown at night, opened in 2008.



NAMICS works closely with raw material suppliers to obtain the optimal resins and fillers that are needed, as well as develop optimal formulating techniques, to meet their customer's current and future requirements for advanced underfill materials.

Materials (insulating & conductive), Processes (composition & dispersion), and Simulation (analysis of materials and structure), they are focusing on the areas of SEEDS, which stands for Semiconductor, Energy, Environment, Display, and System.

Recently, with the increase of environmental consciousness, solar energy is receiving attention worldwide. NAMICS is providing solutions to customers in environmental and energy companies. They offer convenient and ecologically-conscious products to make life better.

In 2008, NAMICS opened their new R&D center, NAMICS Techno Core, to lead change, as well as to create "Only-One & Number-One" (top market share) products.

In order to fulfill customer wants and needs, they continue to nurture the creativity of their employees. In addition, they lead the change from knowledge to wisdom, and will develop new products to actively lead in the next generation.

Collaboration & Innovation

Development of new products takes a tremendous amount of time and resources. In order to strengthen core technologies, they have collaborated with universities and academic institutions. They also utilize this collaboration for the development of new products and technologies for target markets.

An example of a key area of collaboration is the study of the impact of underfill rheology on the reliability of flip chip packages. Flip chip underfills have characteristics of rheology since they are resins. Variation in rheology causes deformation of the substrate depending on the applied temperatures. When a reliability analysis of underfill is made, it is regarded as an elastic body in the FEA (Finite Element Analysis) when temperature cycle testing is conducted. Very little research and few studies have been conducted since the stress reduction behaviors that are inherent to rheology cannot be described. It was also difficult for NAMICS to analyze these behaviors. Reliability analysis is a high priority in investigating the effect of rheology of the underfill materials in flip chip packaging. Working in collaboration with a university and a simulation laboratory, NAMICS investigated the difference between two types of underfill with different transition temperatures of glass (Tg) by elastic and rheological analysis. They found there was a significant difference between the two analytical methods in terms of thermal warpage behavior of packages. Using this information, they succeeded in improving FEA substantially. To be more specific, when analyzing the reliability of flip chip packages, the rheology of the underfill should be considered. NAMICS is now developing new products utilizing this new expertise.

UNDERFILL MATERIALS

Requirements for Capillary Flow Underfill Materials

The most widely used underfill type for flip chips today is capillary flow. In this method the underfill material is dispensed alongside the chip and penetrates between the LSI chip and the substrate by capillary action. In this process, fluidity is extremely important.

In order to obtain optimal dispensability, there are three important properties to consider.

1) Low viscosity

2) Small contact angle with the substrate

3) Filler particle size

In order for underfill to be low viscosity, selection of a low viscosity epoxy resin and hardener system is crucial. In addition, it is also important to control the reactivity of the underfill at the dispensing temperature. Generally a higher dispensing temperature, causes a lower viscosity. Therefore, lower reactivity resin enables dispensing at higher temperatures. On the other hand, an extremely low reactivity resin system is undesirable due to a very long cure time at curing temperatures up to 180°C.

Underfill is usually dispensed in a temperature range between 50°C and 120°C and controlling viscosity and rheology in these temperature ranges is critical.

Surface tension, which provides capillary action, generates only a small shear stress; therefore, it is ideal to use underfills that have characteristics of low viscosity under the low shear stress condition and low yield value.

Filler particles must be small enough to flow into the gap between the chip and the substrate. A filler size of less than 2μm is needed to flow into a gap of 50 μm. Generally, underfills with an average filler size of 0.3 μm are used for gaps of less than 10 μm. Many current flip chip packages have 20 mm x 20 mm chips, gaps of around 50 μm, a bump pitch of 150 μm, and thousands of bumps. In order to underfill these packages without voiding, factors other than fluidity, such as the characteristics of the substrate and chip, and the dispensing conditions must be taken into account.

Current Issues for Underfill Materials

A number of issues are of concern such as lead-free bumps, Low-k Die, large size chips, and narrow pitch/gap. Lead-free bumps and low-k Die are of particular concern.

Currently, the impact of lead-free bumps is being investigated. Compared to eutectic and high lead solder, tin-silver-copper solder has lower C.T.E., higher modulus and greater brittleness. In light of these properties, it is generally better to select resins of relatively high Tg and use high filler content in order to prevent the destruction of bumps during reliability testing.

With the increase of low-k in the dielectric layers of LSI chips, the destruction of low-k layers by stress inside the flip chip packages has become a major issue. Underfills for low-k packages should have low stress and the warpage of packages should be small. It is expected that as the low-k trend expands the underfill is required to provide less stress.

OTHER TYPES OF UNDERFILL MATERIALS

Pre-applied Underfill Materials

Pre-applied underfills are being investigated from a viewpoint of productivity and a requirement for a micro dispensing area in some applications.

Reflow-able underfill is the most promising and is taking the lead in development among pre-applied materials because of their cost effectiveness. The characteristics of this underfill is that it contains flux and cures after solder reflow which ensures connectivity.

Secondary Underfill Materials

Secondary underfill is used for mechanical reinforcement of CSPs and BGAs which are mounted on a substrate. The underfill prevents failure due to dropping or repeated button pressing.

The features required for secondary underfill for mechanical reinforcement are: low temperature quick cure and repair-ability.

A low temperature cure is necessary since some of the parts mounted on the substrates are vulnerable to high temperature exposure. The quick cure is necessary to enhance productivity.

Repairability is also desired, but the trade-off between reliability and repairability is becoming more difficult in the age of lead-free solder. Non-filler type underfills are usually used for this application, but filler containing underfill is occasionally used when higher reliability is required.

UV Cure Type Underfill Materials

This type of underfill has been increasingly used as the underfill for image sensors such as CMOS and CCD. By adding UV curability to the materials, fluidity can be better controlled.

Conclusions

The use of underfill for flip chips and reinforcement materials for CSP/BGA has been rapidly increasing and further growth is expected. In addition, these materials can be expected to grow in terms of market share and technology development, because applications and reliability requirements have become more diversified.

NAMICS works closely with raw material suppliers to obtain the optimal resins and fillers that are needed, as well as develop optimal formulating techniques, to meet their customer's current and future requirements for advanced underfill materials.

For more information please visit the NAMICS website at www.namics.co.jp.◆

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NAMICS Tsukioka Factory
Tsukioka, Japan

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NAMICS Corporation Singapore
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Yantai NAMICS Electronic Materials Co.
Shandong Province, China

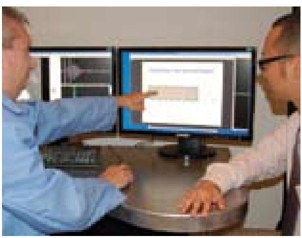
Quik-Pak Names Julie Adams World Wide Sales Director

SAN DIEGO, CA – Quik-Pak, a division of Delphon Industries, has announced the appointment of Julie Adams as Worldwide Sales Director.

Ms. Adams is responsible for directing all sales activities and working with engineering and manufacturing staff to drive business development opportunities and to assure that customer requirements are met. She brings with her extensive experience in strategic sales and development of semiconductor packaging technologies and manufacturing equipment. She has held senior engineering positions at Motorola and Amkor and has spent several years in executive sales positions with RVSI Vanguard and most recently Royce Instruments. Ms. Adams also holds a BSME Degree from the University of Arizona. "We are excited to have Julie as part of our team," says Darby Davis, Delphon Director of Worldwide Sales & Marketing. "She has a long track-record of success in the semiconductor industry and we're confident that she will be successful in expanding Quik-Pak's worldwide sales efforts.

For further information contact Darby Davis, Director of Worldwide Sales and Marketing, 510-576-2220 or Darby@delphon.com.

Effective Acoustic Microscope Imaging of Stacked Die From Sonoscan



ELK GROVE VILLAGE, IL – Sonoscan Inc., has announced that its SonoLab® division is offering a new service that provides greatly enhanced acoustic microscope imaging of stacked die assemblies.

The new service, available immediately, uses Sonoscan's proprietary software developed over the last two years. The new software images die stacks with unprecedented accuracy for internal defect analysis.

Most significantly, it can assign a defect or other feature to a specific layer within the stack, a capability that had been limited due to the thinness and number of layers, until now!

"The merging of the new software with Sonoscan's C-SAM® hardware means that we can now effectively and consistently image the multiple layers in stacked die configurations," said SonoLab Manager Ray Thomas. "In the hands of our experienced applications engineers, this software provides accurate and reliable analyses of stacked die."

More information is available from SonoLab Manager Ray Thomas at 847.437.6400, email rthomas@sonoscan.com.

Amkor Names Stephen G. Newberry to Board of Directors

CHANDLER, AZ – Amkor Technology, Inc. has announced

3-D Architectures for Semiconductor Integration and Packaging

The Practical and Competitive Landscape on the Path to Implementation

9–11 December 2009
Hyatt Regency San Francisco Airport Hotel
Burlingame, California

Industry leaders have been speaking at and attending RTI's conference, *3-D Architectures for Semiconductor Integration and Packaging,* since 2004 and have benefited from the unique opportunity offered by this conference to explore the technology and business implications of the trend toward 3-D integration and packaging. This conference series has helped define this new facet of the semiconductor industry. It offers a unique perspective of the techno-business aspects of this emerging commercial opportunity, combining technology with business, research developments with practical insights, to offer industry leaders the information needed to plan and move forward with confidence. This conference **targets senior-level technologists, managers, and business executives** from the world's leading companies and research institutions, and offers attendees the opportunity to learn from the presentations given by invited industry leaders, from the ample networking opportunities during the conference, and from the expanded exhibit offerings of this year's event.

For more information visit:
http://techventure.rti.org

that Stephen G. Newberry has been appointed as a new member of the Company's Board of Directors. With this appointment, Amkor's Board has been expanded to eight members.

Mr. Newberry, 55, currently serves as president and chief executive officer and as a director of Lam Research Corporation, positions he has held since 2005.

Mr. Newberry joined Lam Research in August 1997 as executive vice president and chief operating officer, and was promoted to the position of president and chief operating officer in July 1998. Prior to joining Lam Research, Newberry was group vice president of global operations and planning at Applied Materials, Inc. During his 17 years at Applied Materials he held various positions of increasing responsibility including assignments in manufacturing, product development, sales and marketing, and customer service. Newberry served five years in naval aviation prior to joining Applied Materials and is a graduate of the U.S. Naval Academy and the Harvard Graduate School of Business.

Mr. Newberry also serves as a director of SEMI, a global semiconductor industry trade association.

More information is available on Amkor's website at www.amkor.com.

First Through-Silicon Via Foundry, ALLVIA, Selects SunSil for Sales and Marketing Support in the U.S.

SUNNYVALE, CA – ALLVIA, the first through-silicon via (TSV) foundry, has hired SunSil Inc. to sell and market their products and services in the United States. SunSil is a global technical sales and marketing company representing leading semiconductor equipment, materials and manufacturing services companies. With significant industry experience on staff, SunSil has two Silicon Valley locations and offices worldwide.

ALLVIA offers services for prototyping and full volume production of both front side and back side TSVs and a full spectrum of facilities, IP and equipment. They recently announced they had secured a next round of funding, bringing the total invested in the company to $25 million, and were using the new funds to build more manufacturing capacity.

"The various compositions of substrate materials make stacking them for 3D integration difficult due to different coefficients of thermal expansion," commented Seth Alavi, SunSil President and CEO. "ALLVIA has solved the problem by putting a silicon interposer between two stacked

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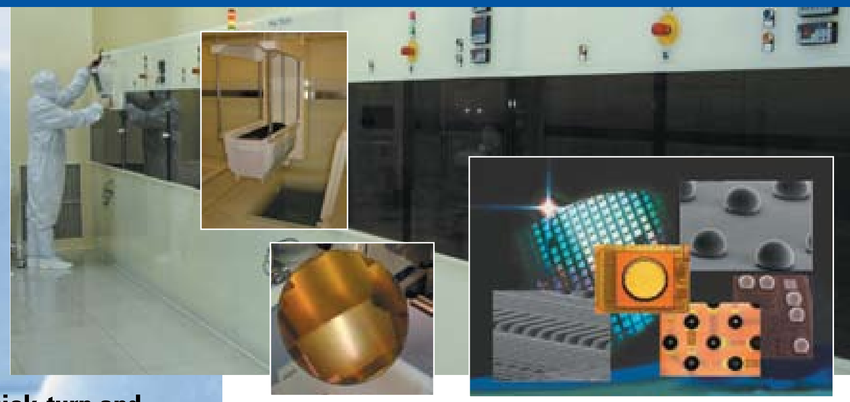

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substrates and connecting them with TSVs. As more and more semiconductor companies are looking to TSVs to solve process problems, we are excited to be representing ALLVIA."

Located in Silicon Valley, ALLVIA is the first Through-silicon via (TSV) foundry and introduced the term "through-silicon via" in both a 1997 business plan and a January 2000 technical article. With the full spectrum of facilities, IP and equipment, ALLVIA offers services for prototyping and full volume production of both front side and back side TSVs to the MEMS and semiconductor industries as well as silicon etching, copper plating, photolithography, CMP, etc. Visit www.allvia.com for more information.

Amkor Recognized for Advanced Semiconductor Packaging and Test Technologies

MOUNTAIN VIEW, CA – Based on its recent analysis of the advanced electronic packaging market, Frost & Sullivan recognized Amkor Technology, Inc. with the 2009 Global Frost & Sullivan Technology Innovation of the Year Award for its line-up of innovative new products, including through mold via package on package (TMV™ PoP), FusionQuad®, and flip chip molded ball grid array (FCMBGA).

FusionQuad represents a breakthrough in lead frame-based plastic packaging, which provides a cost-effective platform for increased lead counts in a standard QFP form factor. FusionQuad applications include a wide range of devices such as hard disk drives, laptop PCs, Ethernet communication, digital television, and data conversion.

"FCMBGA is the advanced and improved version of Amkor's Super Flip Chip (SuperFC®) high performance platform," says Frost & Sullivan Research Analyst, Karthik Kamalakannan. "This technology provides multiple benefits, including improved board space usage, by allowing closer spacing between passive components and the flip chip die resulting in smaller body size and cost savings."

TMV PoP, Amkor's latest offering, is a novel product for next generation package on package applications. It is designed to address challenging 3D architecture requirements in handheld multimedia products enabling higher signal processing and memory densities.

Each year, Frost & Sullivan

North American Semiconductor Equipment Industry Posts August 2009 Book-To-Bill Ratio of 1.03

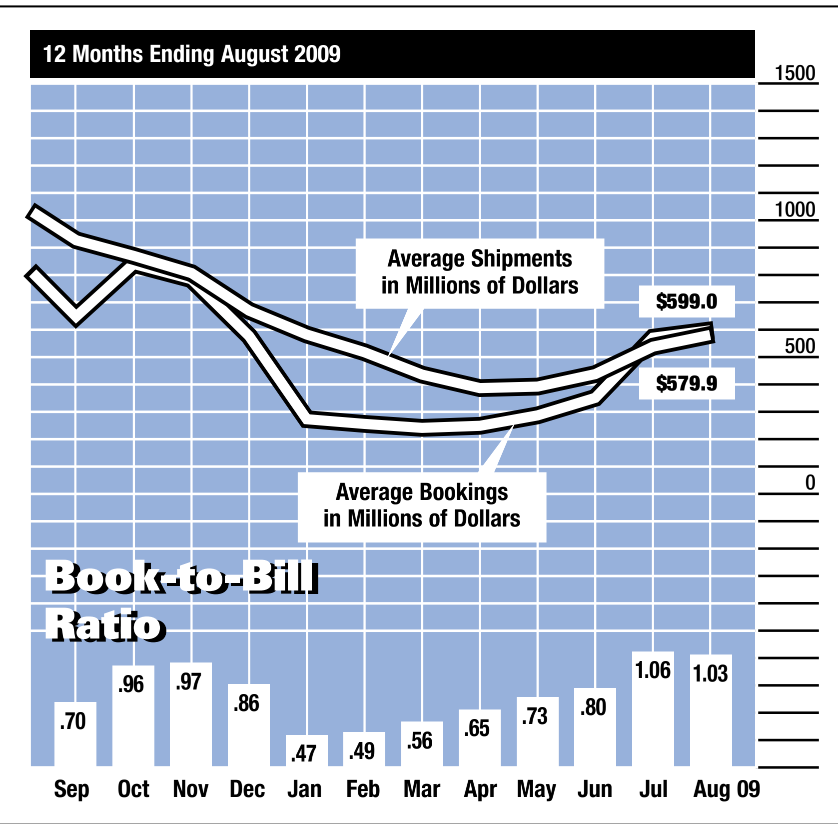
SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted $599.0 million in orders in August 2009 (three-month average basis) and a book-to-bill ratio of 1.03, according to the August 2009 Book-to-Bill Report published by SEMI. A book-to-bill of 1.03 means that $103 worth of orders was received for every $100 of product billed for the month.

The three-month average of worldwide bookings in August 2009 was $599.0 million. The bookings figure is about 5 percent greater than the final July 2009 level of $571.8 million, and about 31 percent less than the $866.8 million in orders posted in August 2008.

The three-month average of worldwide billings in August 2009 was $579.9 million. The billings figure is almost 8 percent greater than the final July 2009 level of $538.0 million, and just over 45 percent less than the August 2008 billings level of $1.06 billion.

"Equipment bookings have increased for five months in a row as market conditions recover from the very low levels reported earlier this year," said Stanley T. Myers, president and CEO of SEMI. "With semiconductor device sales and fab capacity utilization improving over recent months, we expect equipment spending to follow a similar trend during the recovery."

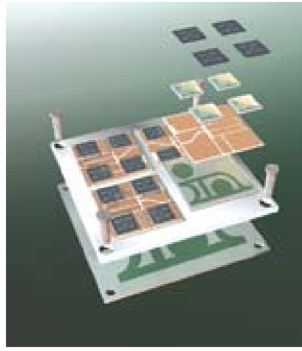
The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



presents this award to the company (or individual) that has carried out new research, which has resulted in innovation(s) that have or are expected to bring significant contributions to the industry in terms of adoption, change, and competitive posture.

Additional technical information on the above referenced packages can be found at www.amkor.com.

Indium Corporation Introduces a Thermal Interface Material for IGBT Modules



CLINTON, NY – Indium Corporation has announced the Heat-Spring® metallic thermal interface material (TIM) specifically designed and optimized for use with Infineon Technologies AG PrimePACK™ IGBT modules.

Many applications call for a TIM that can easily be placed against a backing plate and a cooling solution. Indium's Heat-Spring is a soft metal alloy (SMA) developed as a compressible metallic shim that can be used in IGBT mounting applications.

Heat-Spring has been tested for the latest PrimePACK configurations and has been optimized to reduce thermal resistance below that of other more traditional thermal interface materials.

Because of the increased number of fasteners used in the PrimePACK and its decreased width base plate, the Heat-Spring is ideal for this IGBT module.

Heat-Springs are stable, easy to handle, and require no special mounting apparatus. They are highly conductive both thermally and electrically. Heat-Springs are also made of 100% recyclable and reclaimable metal and are considered a "green" interface material.

For more information visit www.indium.com/TIM or email abrown@indium.com.

Maxtek Adds Rapid Prototyping Services for Faster Design Validation & Time-to-Production

BEAVERTON, OR – Maxtek Components Corporation, a Tektronix, Inc. company, announced the introduction of Rapid Prototyping Services. The new services, a result of industry and voice-of-customer research, are designed to support the need for faster validation of IC and package designs and speed the transition to full production.

For equipment manufacturers in the defense, measurement, medical and communications industries, custom integrated circuits are a frequent and critical part of their next-generation products just as timely delivery for these systems is vital to remaining competitive. With this growing time-to-market pressure, being able to reduce the time it takes to validate IC and package designs and move into the prototype phase of a project is increasingly valuable to system manufacturers and their development programs.

Maxtek's Rapid Prototyping Services were specifically developed to address this need for prototype speed, offering customers a path to rapidly validate their ASIC designs by providing access to advanced interconnect capabilities and a low-cost means of identifying issues – all of which is intended to reduce the design-to-prototype timeline.

For more information call 1-800-462-9835, e-mail technology@maxtek.com or visit www.maxtek.com. ◆

Surface mounted device with delamination (red) along the entire length of several leads. This part would fail per J-STD-020 criteria.

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Making MEMS Manufacturable – Tools for Back-End Processes

Dan O. Popa and Harry E. Stephanou
Automation & Robotics Research Institute
The University of Texas at Arlington

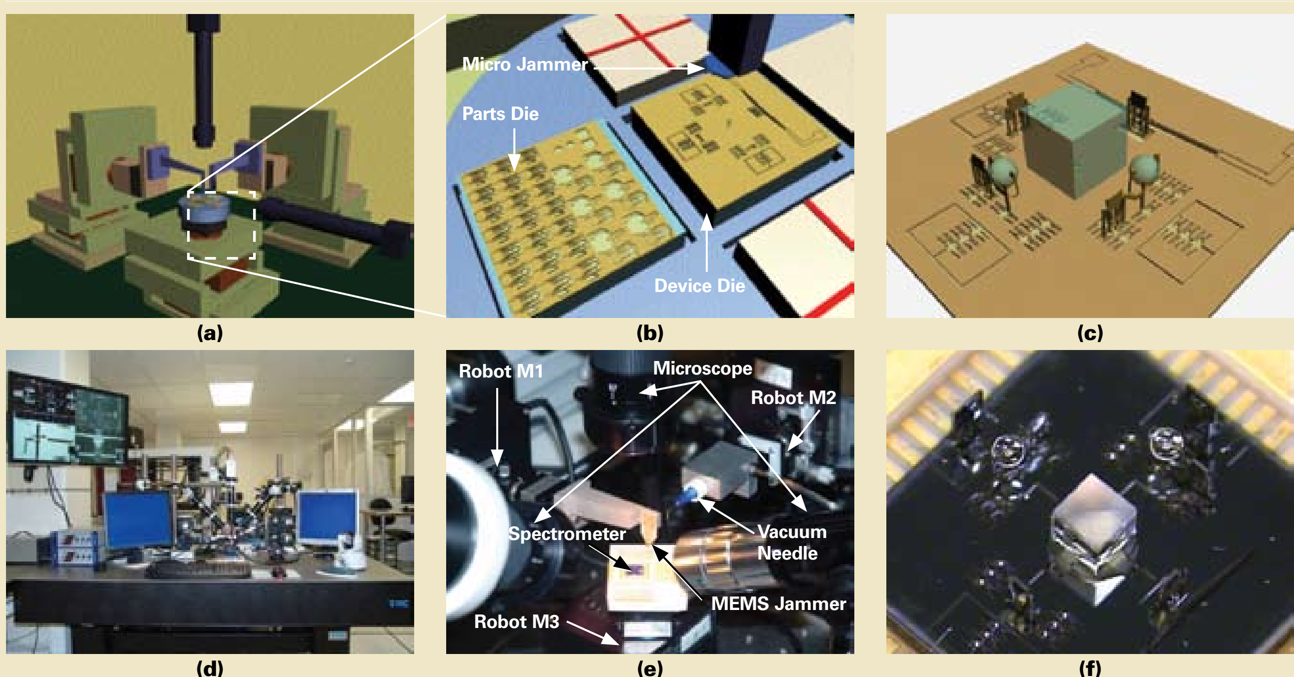

Figure 1: Assembly configuration of microspectrometer; (a) vitual μ³ robotic assembly setup (b) close-up view of the micropart (mirrors, grippers, lens holders) and device dies, (c) assembled MEMS parts and off-the-shelf optical components on the spectrometer substrate. (d) - (f) μ³ assembly cell for actual 1cm x 1cm spectrometer die in class 10,000 cleanroom.

Recent advances in micro and nano technology have increased the demand for miniaturized sensors, actuators, and other non-electronic MEMS. For some consumer applications, such products must be inexpensive, produced in large numbers, and meet appropriate performance criteria for several years of use. Yet in other applications, such as in the defense and aerospace industries, microdevices must operate reliably in harsh environments, for many years, or even decades. Despite increased demands, the path to market for many microsystems is still long, difficult, and fraught with technological challenges.

Recent work at UT Arlington's Automation & Robotics Research Institute (ARRI) aims to create a systematic approach to MEMS manufacturing that guarantees high manufacturing yield and reliable operation for the resulting microsystems. Our new *Texas Microfactory* initiative promotes a unique micromanufacturing methodology combining Design for Automated Assemblability (DfAA), Design for Reliability (DfR), and advanced packaging processes, including wafer-level bonding, 3D interconnects, and fluxless bonding and sealing. In this article, we describe new tools for back-end processes to support DfAA and DfR.

Unlike semiconductor integrated circuits, newer microsystems combine sensors, actuators, mechanical structures, electronics, and optics on a single substrate. Microassembly is an enabling technology that allows building of heterogeneous microsystems with a higher degree of robustness and more complex designs than monolithic fabrication. Whereas at the macro scales, automation is often undertaken after, and often benchmarked against manual assembly, deterministic automation at the MEMS scale requires a more holistic approach. This means that the designs of the assembly cell, part and end-effectors should be considered simultaneously, and that by doing so, we can automate assembly operations in a realistic manner by ensuring higher process yield, lower cycle time and less hardware overhead.

Assembly at the microscale harbors many difficult challenges due to scaling of physics, stringent tolerance budget, high precision requirements, limited work volumes, and so on. These difficulties warrant new robotic hardware, and control and planning software algorithms, different than their macroscale counterparts. Recently, we proposed new modular microassembly equipment, precision metrics for automated assembly systems, and formal conditions ensuring high assembly yields (over 99%). These quantitative tools have been embodied

in software packages switching between open, closed, and calibrated operation in the microassembly cell. Furthermore, a precision-adjusted path planner is implemented to predict the shortest end-effector path that maintains required precision. Simulation and experimental results indicate that the proposed hybrid controller and path planner lead to higher yields at faster cycle times than traditional methods.

As a case study for the proposed DfAA tools, consider the automated assembly of a *microspectrometer*, a complex MOEMS sensor for wide range spectrum analysis and gas detection applications. A microrobotic system – the "μ^3" has been configured at ARRI to carry out general microassembly tasks with parts between 10 μm and 1mm in size (Figure 1). It consists of three robotic manipulators with a total of 19 degrees of freedom, and four high magnification microscopes to provide stereo vision for teleoperation as well as visual servoing.

Automated microassembly of the microspectrometer using the μ^3 poses unique challenges, because multiple heterogeneous microcomponents need to be assembled with a tight mechanical as well as optical alignment. Compliant part and socket designs are used to snap-fit several 2-1/2D silicon MEMS parts onto the substrate. The microparts are fabricated on SOI wafers using DRIE.

Automated assembly of the microspectrometer using μ^3 involves: (i) grasping of four MEMS parts using passive jammer, (ii) maneuvering the parts through collision free paths, (iii) releasing the parts onto their designated compliant sockets. Additionally two spherical lenses and one beamspliter cube are aligned and assembled on the device die. Precise alignment of microcomponents is critical to the mechanical configuration and also to the optical interference path. To ensure high yield we formulate an assemblability criterion and categorize various uncertainties that are associated with microparts and fixtures throughout the microassembly process.

Typically, sequential microassembly requires a high precision micromanipulator and motion control; either by off-line programming with calibration or by online feedback control. The later can be accomplished via a microscope and/or a force sensor integrated with the gripper. However, this results in low assembly throughputs. On the other hand, open loop control does not necessarily ensure high assembly yields, especially in case of complex and sequential processes.

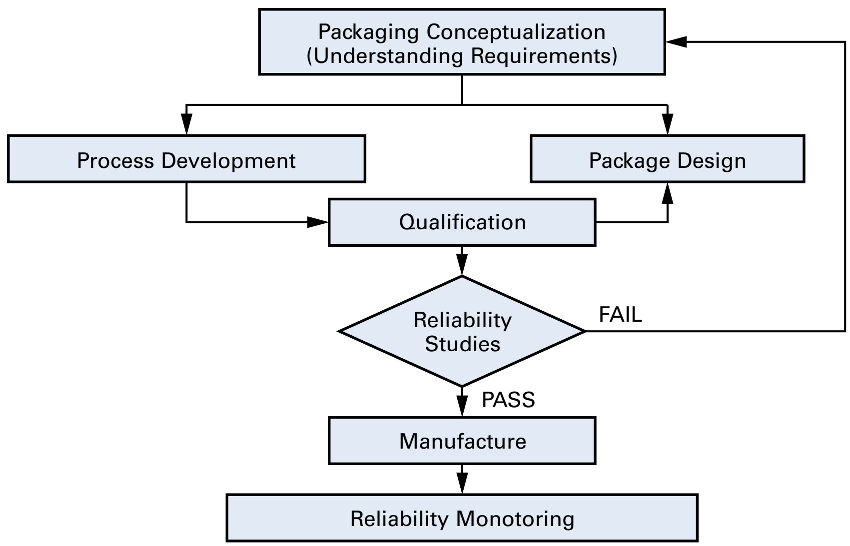

Figure 2: Schematic of *DfR* iteration loop for MOEMS packaging.

A hybrid controller was developed to take advantages of both precision control methods. Experimental results indicate that the hybrid controller achieves 35% more accuracy than pure open loop control, while the assembly throughput is 60% faster than pure closed-loop control. In a simulated production run, a microspectrometer was assembled every 20 minutes with nearly 100% yield.

In addition to microassembly requirements, MEMS and MOEMS products need effective packages to protect them from the damaging effects of the environment. Although MEMS packaging shares many attributes of conventional microelectronics packaging, it is nevertheless, different in several respects, and generally more complex.

Reliability is often not considered as a design factor during product development. Rather, reliability is assessed using life tests, accelerated tests and other techniques after a product has completed its development cycle. The goal of design for reliability (DfR) is to proactively introduce reliability early in product development so that concerns are identified and assessed at every stage, from the conception to obsolescence. We have recently developed a framework for applying DfR principles to MOEMS packaging. Such an approach is desirable for several reasons. First, it reduces the cost and time for product development by departing from the "build-test-rebuild" approach. Second, it provides better understanding of the process input-output relationships, so the practitioner is better able to make informed design decisions. Lastly, this leads to enhanced product performance, reliability and reduced cost.

At the Texas Microfactory, we use a layered approach to implement *DfR* for MEMS packaging, referred to as the "*DfR iterative loop*" (Figure 2). The first abstraction layer in this framework involves packaging conceptualization and definition whereby we sought to gain understanding of the packaging requirements concurrently with the device conceptualization. Decisions are made at this time as to which packaging operations take place at the front end (during device fabrication) and which ones take place at the back end (after device fabrication). Back-of-envelope calculations may be used at this stage to examine the suitability of the packaging solution. It is also important to apply tools such as physics of failure, as well as failure modes and effects analysis (FMEA) in making design decisions that affect the package and device reliability.

The next layers involve detailed package design/process development and optimization. It should be noted that the process development process may be influenced by the package design and vice versa. Package design includes designs for the actualization of packaging functions such as protection from the environment, electrical or optical interconnection. Process development involves packaging process definition in terms of parameter settings, evaluation of alternative processing routes, establishing process windows for parameters and determining process parameters that affect package reliability. Concurrent

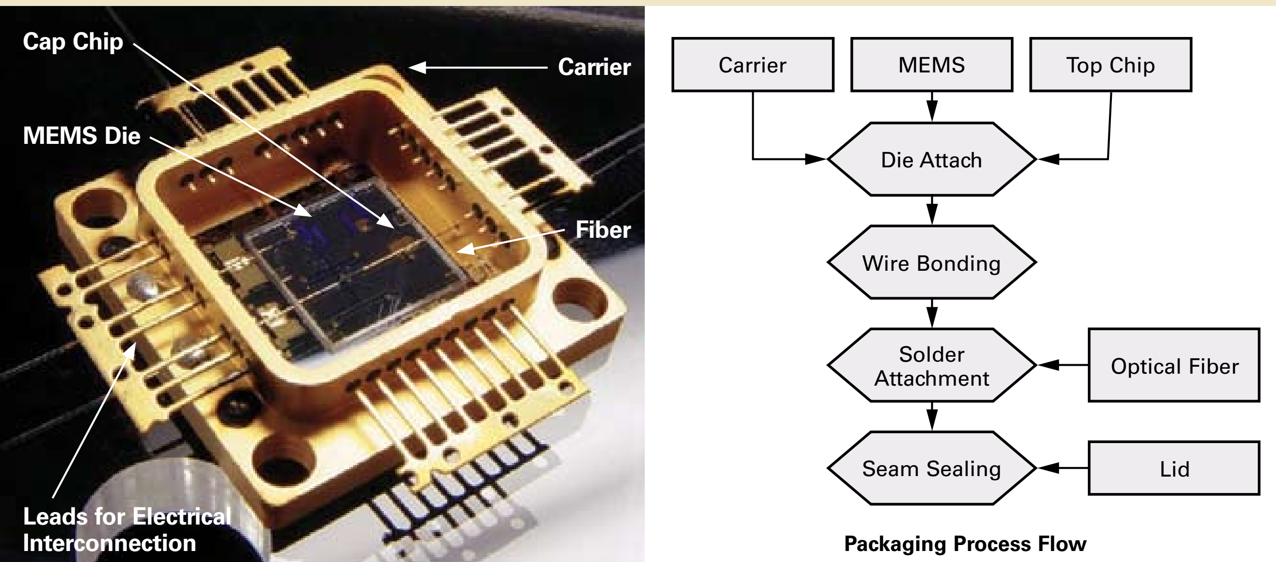

Figure 3: MOEMS application device (optical switch) showing the carrier, optical fibers, MOEMS die, and cap chip (lid not shown).

design, simulation, and reliability testing should be adopted to achieve optimal package design and processes.

The final *DfR* layers involve package evaluation using qualification standards and specifications such as the MIL-STD 883F. Finally, we carry out reliability studies using accelerated tests such as temperature and power cycling tests to examine the long term effect of the package on reliability.

In the context of MEMS fabrication/manufacturing, useful tools in process development and improvement are statistically designed experiments. These are particularly suitable to MEMS packaging because of the low to medium quantities, and higher component costs. As a result, fewer experiments are available for process development. By applying design of experiment principles, we maximize the information regarding the process input/output relationship such as the input factors that affect the process output/response and the sensitivity of the process output to the input variables.

The *DfR* iteration loop is illustrated through a demanding MOEMS application that requires extended shelf lives of over 25 years (Figure 3). The microoptical switch discussed in this paper may be stored in hostile environmental conditions, and the process development allows for a limited number of experimental samples, due to cost constraints and part availability. The expected long life of this device requires hermetic sealing, and the use of fluxless attachment methods to prevent degradation of flux and flux residues.

As a result of the long storage life requirements for the MOEMS switch, and the use of optical components, it is desirable to provide corrosion-resistant hermetic packaging and no organic packaging materials. The device must pass the following tests: hermetic seal, die-carrier shear, die-die shear, wire-bond strength, and a fiber strength test. It was decided to employ corrosion and diffusion resistant package and joining materials, including a custom machined, gold-coated Kovar® metal housing with a lid, In and SnAu preforms and deposited layers. This carrier material was chosen in order to reduce the CTE mismatch to the silicon die.

The silicon die containing electrothermal actuators must be packaged together with 4 optical and 8 electrical interconnects. Because of assembly constraints, the order in which components are added to the carrier is as follows: die & top chip attach, wire bonding, optical fiber sealing, and finally seam sealing of the top lid. The leak routes for this package are the package lid and the fiber-to-carrier attachment joints. Hermeticity of the Kovar® carrier is obtained via lid seam sealing and that of the fiber-to-carrier via fluxless soldering. MEMS die mechanical reliability is obtained through attachment to the Kovar® carrier using a metallic joint.

Sealing of optical interconnections is obtained via trenches microfabricated on the MEMS die via DRIE, and attachment using fluxless soldering. Because of the order of assembly, the melting temperature of the optical solder joints should be lower than the reflow temperature of the SnAu die attach. In addition, this solder joint uses metalized fibers and liquid reflow of the joint through the Au-coated carrier side wall. A good material, with well known solder joint reliability to Au is Indium. These solder joints are formed via hot-plate global reflow, or individually via localized heating by laser energy. In order to reflow all 4 joints simultaneously, a complex fixture is needed. Achieving appropriate indium reflow temperatures with a hot plate requires time, and offers an increased chance for indium-oxide formation. Alternatively, localized heating using a semiconductor diode laser offers advantages such as: simplified fixturing, faster process time, and less chance for indium-oxide formation. Protection of delicate MEMS structures on the die and the vertical axis constraint of the optical fibers are be obtained by using a cap chip flip-chip bonded to the MEMS die.

We applied concurrent simulation and reliability testing to obtain design and process values for the packaging of the MEMS switch. In particular, we used FEA to overcome soldering difficulties associated with laser reflection on the carrier gold surface. Processes that are difficult to model such as the flow of indium solder in the feed-through seals under different ambient conditions were investigated through direct experimentation. The resulting packaging process parameters and package design changes were then tested in pilot production of the first 25 switches, which were then confirmed to having passed the required reliability tests. ◆

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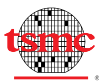

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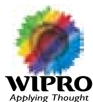

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8:30 a.m.	Show Floor Opens
9:00 a.m.	Research Analyst – Jim Feldhan, President, Semico Research
9:15 a.m.	"The Innovation Imperative" Business Model Doug Grose, CEO, GlobalFoundries
9:45 a.m.	Morning Snack - Sponsored by Tensoft
10:15 a.m.	Research Analyst – Jeff Shepard, President, Darnell Group, Inc.
10:25 a.m.	Energy Harvesting Peter Henry, Vice President & General Manager, Power Management Group, Analog Devices Inc. (ADI)
11:15 a.m.	Research Analyst - Matthew Towers, Founder & CEO, IMS Research/InMedica
11:25 a.m.	Small Footprints SoC Enables Precision Portable Medical Instrumentation Murugavel Raju, AEC Catalog Microcontrollers End Equipment Marketing Manager, Texas Instruments
12:00 p.m.	Lunch on Show Floor - Sponsored by GlobalFoundries
1:15 p.m.	Research Analyst - Mario Morales, Vice President, Global Semiconductor Research, IDC
1:25 p.m.	Opportunities for High Performance Semiconductor Solutions in Cloud Computing Dr. Francis Ho, Senior Director Business Development, Inphi Corporation
2:15 p.m.	Research Analyst - Tony Massimini, CTO, Semico Research
2:25 p.m.	Enabling 3G Wireless Digital Distribution in Emerging Markets John Rizzo, CEO, Zeebo, Inc.
3:00 p.m.	Afternoon Snack - Sponsored by Exar Corporation
3:15 p.m.	Research Analyst - Joanne Itow, Managing Director, Semico Research
3:25 p.m.	Home Networking: Opportunities and Challenges Vinay Gokhale, Senior Vice President Marketing & Business Development, Entropic Communications
4:15 p.m.	Research Analyst - Farah Saeed, Senior Consultant, Energy and Power Systems, Frost & Sullivan
4:25 p.m.	Making a Smarter Grid Robert Dolin, Vice President & CTO, Echelon
5:00 p.m.	Networking Reception on Show Floor

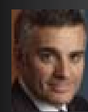
SPEAKERS

Doug Grose
CEO, GlobalFoundries

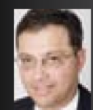
Peter Henry
Vice President & General Manager, Power Management Group, Analog Devices Inc. (ADI)

Murugavel Raju
AEC Catalog Microcontrollers End Equipment Marketing Manager, Texas Instruments Development, Entropic Communications

Dr. Francis Ho
Senior Director Business Development, Inphi Corporation



John Rizzo
CEO, Zeebo, Inc.



Vinay Gokhale
Senior Vice President Marketing & Business

Robert Dolin
Vice President & CTO, Echelon

Epoxy Flux Stealing Tacky Flux's Limelight?

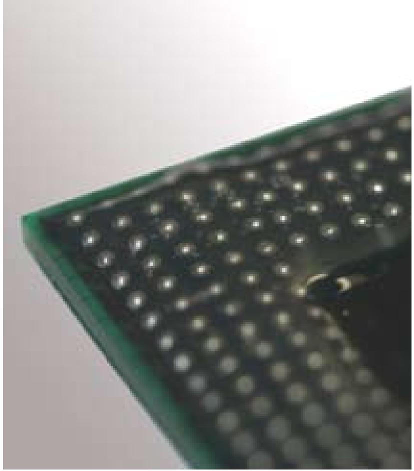
Bruce Chan, Quing Ji, Mark Currie, Neil Poole and C.T. Tu
Henkel Corporation

Technology advance has continued to force the development of newer, better performing underfill systems to enhance the reliability of increasingly smaller devices. Manufacturers not only want materials that perform well, but that are also cost-efficient and easily processed. There have been many attempts to satisfy all of these requirements – some successful for certain applications and some not really on the mark.

To date, the four most commonly used types of underfills are capillary flow materials, fluxing (no-flow) underfills, cornerbond and edgebond systems. Each has particular relevance for specific applications, but some new and older-generation devices may benefit from a ground-breaking underfill material technology called epoxy flux. Part of the class of reflow cured encapsulant materials, epoxy flux is effectively enabling applications for both semiconductor packaging and printed circuit board (PCB) assembly processes.

In another materials development milestone, Henkel has formulated Hysol® FF6000™ – a reflow curable epoxy flux formulation that offers both flux and underfill in a single product. The flux component of the material enables solder joint formation and the epoxy system offers underfill-like. Originally designed for underfilling large format CSP and BGA devices where flow rates and cure times of traditional capillary underfills can limit throughput, Hysol FF6000 has also proven to be an effective material for emerging package on package (PoP) configurations as well as for ball attach processes, just to name a few. In addition to its application versatility, Henkel's new epoxy flux also offers deposition flexibility, as it can be applied via screen printing, dipping, dispensing or jetting.

For PoP assembly, Hysol FF6000 is a promising solution to one of the biggest challenges with these devices. While the level one package assembly follows fairly routine surface-mount procedures, the assembly and subsequent long-term reliability of the level two package is not as simple. Currently, the most common method used is to dip the bottom side spheres of the top package into a tacky flux, place the package and then reflow it. This allows for solder joint formation but, unfortunately, the joints



then remain unprotected and are subject to stresses from shock, drop and vibration. Alternatively, when Hysol FF6000 is used, the second level package is assembled using the same procedure but receives some additional support from the adhesive. The second level package is dipped into epoxy flux prior to component placement. Once the component is placed, the assembly moves through reflow where the fluxing action of Hysol FF6000 enables robust solder joint formation and the epoxy component encapsulates each sphere and then cures. In addition to the added protection afforded by this new material, the in-line processing benefits and cost savings are substantial. Units per hour (UPH) is improved dramatically as subsequent dispense and cure steps are not necessary and costs are reduced through yield improvements and the elimination of dedicated dispensing equipment. In recent testing against other tacky fluxes, Hysol FF6000 offered the best drop test performance, as it was able to withstand the most number of drops before the first failure. This suggests that epoxy flux offers more protection than flux alone.

Similar results were revealed when Hysol FF6000 was evaluated as a ball attach flux. Again, the reliability and strength of the material proved to be more robust than that of water-wash or no-clean tacky flux alternatives. When the shear strength of three solder sphere alloys was tested against four different fluxes (two water washable fluxes, one no-clean flux and Hysol FF6000), the Henkel epoxy flux emerged as the clear winner. With each solder alloy, Hysol FF6000 provided the strongest solder joint. These results clearly indicate that higher reliability can be achieved with Hysol FF6000 as compared to traditional flux formulations.

As mentioned previously, the versatility of Hysol FF6000 is unparalleled. From new package configurations such as PoPs to package-level ball attach and, of course, board- level assembly of large format BGAs and CSPs, Hysol FF6000 offers manufacturers the ability to source a single material for a variety of applications and deposition methods. This latest material innovation from Henkel also reduces costs, improves throughput and simplifies manufacturing processes while enhancing reliability.

For more information on Hysol FF6000 epoxy flux or any of Henkel's advanced electronics material solutions, call the company's headquarters at 949-789-2500 or visit www.henkel.com/electronics. ◆

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Thermal Stability and Run-away Margins of Packaged SOC in Advanced Wafer Technologies

Johannes de Groot
Sr. Director of Operations
Zoran Corporation

Various trends are putting new constraints on package design in particular in the low- and mid-end System-On-a-Chip (SOC) space.

These trends include:

- Increased current density in advanced technology chips
- Increasing relative weight of Leakage Power as opposed to Logic Power as a function of the wafer process corner
- Continuous commoditizing of complex IC functions and the associated pressure on package cost

These trends present a dilemma to design an affordable package that will still guarantee full functionality for the worst-case power scenario. Also, the high leakage behavior of advanced processes has introduced the danger of thermal instability under extreme application conditions in the consumer chips space, which until recently was limited to power applications and very high end processor chips. This triggers the requirement of tools allowing designers, in the early stage of the product cycle, to assess the thermal stability and make trade-off's between process choice, architecture, chip implementation and package choice.

The outline of such a method used at Zoran is presented in this article. Note that the tool requirements to internalize the method are quite modest and can be limited to an advanced spread-sheet program.

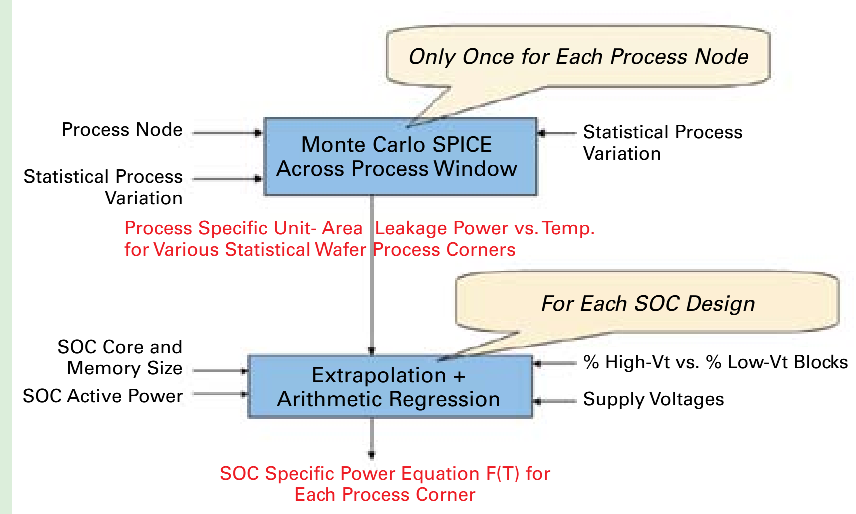


Figure 2. Building an SOC Power equation.

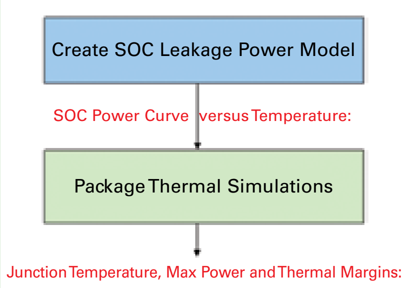


Figure 1. Two-step flow to establish thermal properties.

Methodology and Components to Predict Thermal Behavior

The methodology covered in this article provides a relatively easy 2-step path from early prediction of the SOC Leakage Power to establishing the thermal margins in the actual application, see figure 1.

The first step is to quantify the SOC Leakage Power as a function of junction temperature across the wafer-process window. The resulting mathematical power equations can then be fed into thermal simulations of packaged parts in their target application. This will not only provide the classic parameters like the package thermal resistance (***θ_Ja***), junction temperature ***Tj***, but also the resulting maximum power and even the margins towards thermal run-away conditions. The next section zooms in on how to build the SOC leakage model, and section 4 focuses on the thermal behavior.

Building an Early SOC Leakage Power Model

How do you build a model power-model of a chip that has not even been designed? Early on in the product creation process there is generally a fairly reasonable estimation of the total logic gate-count and required memory size. Since the core-domain is dominating the Leakage Power, we can use this estimate to build a process corner dependent equation for the leakage, add the expected dynamic power (basically all the non-leakage power components), and get the resulting SOC Total Power equation as a function of junction temperature. Figure 2 shows a block diagram on how this is achieved.

For each potential process node a very rudimentary library is build simplifying both the standard cell library as well as

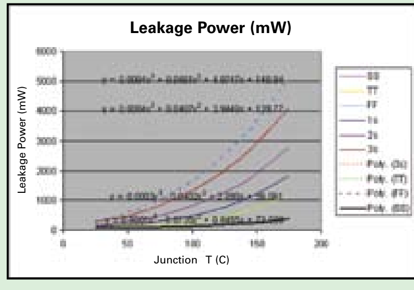


Figure 3. SOC leakage power as a function of temperature for various statistical process corners, 90nm CMOS node.

the total memory macro suite. For each of these cells a Monte Carlo SPICE simulation is run to establish the statistical leakage distribution across the process window. Distributions of various SPICE parameters are established by the waferfab based on actual inline measurements. Basically the output is a leakage model of a per-unit logic/memory area realized in a certain library in a certain process node. This first step only has to be done only once for a specific process node.

The second step is to tailor the model down to a specific SOC. This is achieved by extrapolating inserting the SOC specific core and memory sizes, as well as the estimated percentages of high- versus low-leakage logic blocks and potential voltage over-drive or under-drive conditions. Figure 3 shows an actual prediction of the SOC Leakage Power behavior based on this model.

The bottom curve reflects the Slow-NMOST + SLOW-PMOST process corner (SS), the top curve shows the opposite FAST-FAST process corner. In between are the typical (TT) process and the 1, 2 and 3 sigma fast process corners. The FAST process corner "leaks" an order of magnitude more than the SLOW corner. Figure 3 also shows the regression curves (curve fits) indicating that CMOS core circuitry leakage behaves like a 3rd order polynomial. Note that all physical leakage sources are included like the ever more dominant gate (tunnel) leakage component.

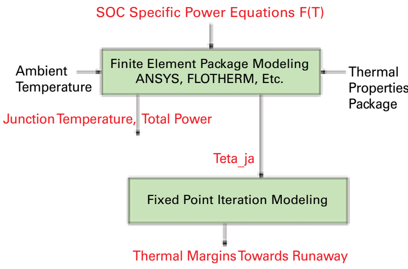


Figure 4. Flow to establish Junction Temperature, Total Power and Thermal Margins.

Now that we can generate these curves and modulate them as a function of design parameters, we now can use them to assess the thermal stability in the actual application, and see how the behavior reacts to changing design parameters.

Thermal Behavior and Run-away Margins

Rather than a set of constant power numbers we can now feed power equations into a finite element thermal package model like ANSYS, resulting in a much more accurate estimate of the thermal equilibrium conditions like junction temperature ***Tj***, as well as the resulting total power number. Note that if the thermal properties of the package are known, a simple iterative spread-sheet program can be used to calculate the junction temperature and total power.

It is important to establish if the chip in the application is thermally stable, and what the margins are, be it in chip power or ambient temperature. A Fixed-Point Iteration method can be used, since the equations involved typically cannot be solved algebraically.

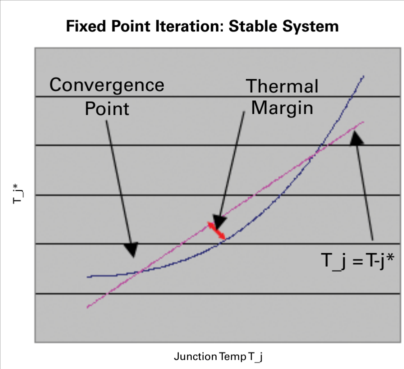
To establish that there is a stable thermal equilibrium, there must be a solution for the following equation:

$$T_j = T_a + P(T_j) * \theta_Ja$$

where:
θ_Ja = Package Junction-to-Ambient Thermal Resistance
P(T_j) = 3rd order SOC Total Power Polynomial
T_a = Ambient temperature
T_j = Junction temperature

This equation is graphically illustrated by figure 5.

Typically the equation has two solutions, the intersections between the 3rd order polynomial and the 45 degree line (T_j = T_j*). The system will stabilize on the lowest point, marked in the graph as "Convergence



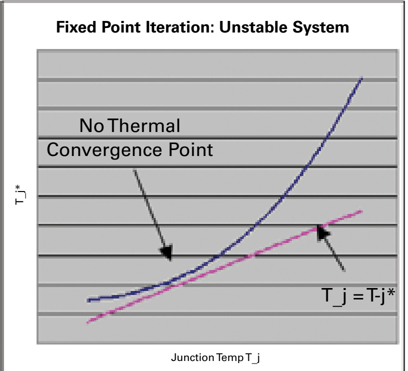


Figure 5. Fixed Point Iteration: A thermally stable and unstable situation.

RESULT FIELDS					
Process Corner	T_junction (C)	Total Power (W)	Leakage Power (W)	Ta Margin to Runaway	Pa Margin to Runaway
SS	115	4.21	0.143	207.9	20.7
TT	121	4.79	0.717	87.6	8.6
TT + 1σ	128	5.48	1.408	51.3	5.0
TT + 2σ	147	7.38	3.312	15.3	1.5
TT + 3σ	THERMAL	RUNAWAY	∞	-14.3	-1.4
FF	THERMAL	RUNAWAY	∞	-31.2	-3.0

Figure 6a. Thermal modeling result non-optimized SOC design.

RESULT FIELDS					
Process Corner	T_junction (C)	Total Power (W)	Leakage Power (W)	Ta Margin to Runaway	Pa Margin to Runaway
SS	114	4.12	0.050	269.7	26.4
TT	116	4.28	0.208	169.7	16.9
TT + 1σ	117	4.41	0.344	129.2	12.8
TT + 2σ	121	4.75	0.684	87.4	8.6
TT + 3σ	125	5.15	1.081	61.3	6.0
FF	131	5.75	1.678	48.8	4.8

Figure 6b. Thermal modeling result after chip optimization.

point". In the right graph, the equation does not have a solution and in this situation there is no thermal stability. The result is thermal run-away and potential burn-out of the chip in the system.

The cross-over point between stability and non-stability occurs when both curves only touch and do not intersect, in other words, both solutions in the left graph merge into a single one. This represents a dangerous situation that the system may appear stable, but a slight change in environmental conditions may trigger thermal run-away. It is easy to see that the red arrow in the left graph represents the thermal margin the system has towards becoming unstable. Via the thermal resistance ***θ_Ja*** of the package this thermal margin can be translated to a chip power margin.

Figures 6a shows an example of the outcome of the analyses described in this article for a chip that has not been designed optimally.

The specific wafer-process corner is depicted in the most left column. For each corner the table shows the estimated Junction temperature, Total Power, Leakage Power, as well as the thermal margins towards runaway for both temperature and chip power. In this example the TYPICAL process condition provide an acceptable junction temperature at 70˚C ambient, and a comfortable thermal stability margin. However, this margin diminishes very rapidly if the process shifts to the FAST corner, resulting in run-away conditions in the extreme cases.

Figure 6b however, shows the exact same chip under identical conditions, where the percentage of High-Vt standard cell block in the core area of the chip is increased from 25% to 100%, effectively replacing the same logic function with low leakage blocks. This change greatly contributes to the thermal stability of the chip: even the extreme FAST (FF) corner is very stable now, although the junction temperature exceeds the 125˚C budget. Similar stability improvements can be achieved by improving the thermal resistance of the package and/or lowering the dynamic power budget of the chip.

Please note that due to the statistical nature of this method one knows what fraction of the population will result in junction temperatures exceeding the budget. An economic choice can be made between eliminating the tail of this distribution at test, versus adding cost to improve the thermal characteristics of the package.

Summary and References

The methodology in this article provides an early view on the thermal behavior of an SOC in actual application environments. It does not only enhances the estimation accuracy of the thermal equilibrium parameters like junction temperature, but also provides insight if there is any danger of thermal runaway, and how thermal margins can be calculated and improved. This method is also very instrumental to assess stability and acceleration parameters in Burn-In or other product qualification stress tests.

The TSMC Taiwan Design Support Group provided the Monte-Carlo SPICE simulation data. ASE Kaohsiung thermal simulation group enabled the option to insert a power equation into the finite element tools. My special gratitude goes to Chang-Chi Lee for introducing the fixed-point iteration method greatly simplifying the process to calculate thermal margins. ◆

Reference: "On the Thermal Stability of High Leakage Devices", Chang-Chi Lee (Calvin) et al. EPTC, 2006.

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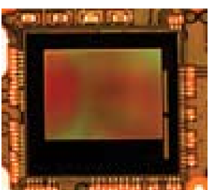

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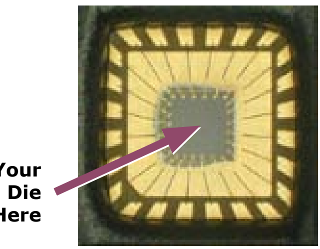

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4	5	6	7	8	9	10
SMTA INTERNATIONAL October 4-8, Town and Country Resort and Convention Center, San Diego, CA						
11	12 COLUMBUS DAY	13	14 **SUNNYVALE MEPTEC LUNCHEON** Lookout Restaurant Sunnyvale, CA	15 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	16	17
18	19	20	21 **MEMS TESTING AND RELIABILITY WORKSHOP** Radisson Hotel	22 **MICRO POWER TECHNOLOGIES WORKSHOP** Radisson Hotel	23	24
25	26	27	28	29	30	31 HALLOWEEN
		6TH ANNUAL INTERNATIONAL WAFER-LEVEL PACKAGING CONFERENCE October 27-30, Marriott Santa Clara, Santa Clara, CA				

NOVEMBER 2009

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
1 DAYLIGHT SAVINGS TIME ENDS	2	3	4	5	6	7
	IMAPS 42ND INTERNATIONAL SYMPOSIUM ON MICROELECTRONICS November 1-5, San Jose, CA					
8	9	10	11 VETERAN'S DAY	12	13	14
15	16	17	18	19 **MEPTEC SOLAR SYMPOSIUM** Radisson Hotel San Jose, CA	20	21
22	23	24	25	26 THANKSGIVING	27	28
29	30					

DECEMBER 2009

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
		1	2	3	4	5
6	7	8	9 **SUNNYVALE MEPTEC LUNCHEON** Lookout Restaurant Sunnyvale, CA	10 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	11	12
13	14	15	16	17	18	19
20	21 WINTER BEGINS	22	23	24	25 CHRISTMAS	26
27	28	29	30	31 NEW YEAR'S EVE		

Innovating Through the Downturn

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Henkel Corporation

Small signs that the economic recovery is beginning are becoming more and more visible, though we will all no doubt be affected by the financial events of the last 18 months for some time to come. While the shape of the recovery is still somewhat uncertain, what is clear is that those companies that stayed the course and remained committed to their technology roadmaps will be well-positioned for growth when market strength returns.

For both manufacturers and suppliers, maintaining R&D investment levels during such a deep recession is a difficult proposition, to say the least, but is a commitment that is essential if companies want to be competitive for the long-term. While many firms have decided to pull back on innovation initiatives, several companies have held firm to their technology commitments, pushing forward with development programs and other strategic investments. Our company, for example, has maintained a consistent percentage of sales reinvestment into R&D and technical service projects throughout the recessionary period, as well as earmarking resources for expansion of development labs in Shanghai, China and Isogo, Japan. Shanghai will see investment to broaden our analytical and development departments for die attach paste and liquid materials and, in Japan, staff will be added to our advanced materials team to enable even more in-depth application and materials design work for future technologies.

Upholding resource commitments such as these throughout the recession has yielded materials advances that will no doubt benefit customers as they design and introduce new technologies to the market. And, as we move out of the recession, it is becoming increasingly evident that continued innovation investment is, indeed, the proper path, as many materials advancements simply would not have been born had resources been reduced. As the old saying goes, "necessity is the mother of invention." So, perhaps, the recession is the mother of innovation!

During this time, for example, development of traditional die attach film products essential for current customer applications has continued, but programs to evaluate next-generation technologies that may potentially replace film are also being evaluated. It's precisely these types of efforts on which many companies would typically scale back during a downturn, but forging ahead has yielded significant progress. Without question, when packaging firms return to full strength, they will require available solutions and won't have the luxury of waiting six to twelve months for development. Take, for instance, the advance of stacked package applications: ultra-thin bondlines will soon be the norm for stacked packages and film will likely not be able to meet the next-generation demands. Current investment in die attach solutions that consistently deposit materials at thicknesses that push far beyond current capabilities will certainly pay off in the long-term, as device manufacturers will be able to meet time-to-market deadlines and maintain competitiveness.

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For applications where exceptionally thin bondlines aren't as critical – leadframe packages, for example – development of a conductive die attach film that offers electrical properties similar to those of silver-filled pastes is underway. This advance essentially delivers leadframe package manufacturers with the same throughput and processability advantages of film-based products.

But industry development initiatives haven't been limited to die attach: work is also being done on a new compression molding technique that enables overmold of a redistributed wafer. Of course, the material requirements are very unique, as the material must be able to withstand all of the downstream processes such as plating and multiple thermal cycles, but there have been excellent results in early trials.

There are also already commercialized materials designed for certain applications that are finding use either in alternative processes or for completely new materials. Taking successful results and applying those to completely different scenarios is also part of the innovation experience. A popular epoxy flux material is a perfect example of this type of "out of the box" thinking. The epoxy flux combines flux functionality and underfill protection into a single system which, in many cases, eliminates the requirement for a subsequent underfill process. It was initially designed for large format BGAs and CSPs, but has also proven to be a remarkably robust material for top level Package-on-Package (POP) devices as well as for sphere attach on BGA packages.

So, innovating through a downturn is most assuredly possible and, in our view, imperative. I'm certainly not suggesting that our company was immune to the effects of the global downturn: we, too, implemented cost-saving measures to ensure the stability of our business, but not at the expense of innovation programs. I firmly believe that future success – for all of us – relies on dedication to fulfilling technology roadmaps and innovation commitments. This isn't always the easiest path forward, but arguably the most beneficial and the electronics industry at large will reap the rewards. ◆

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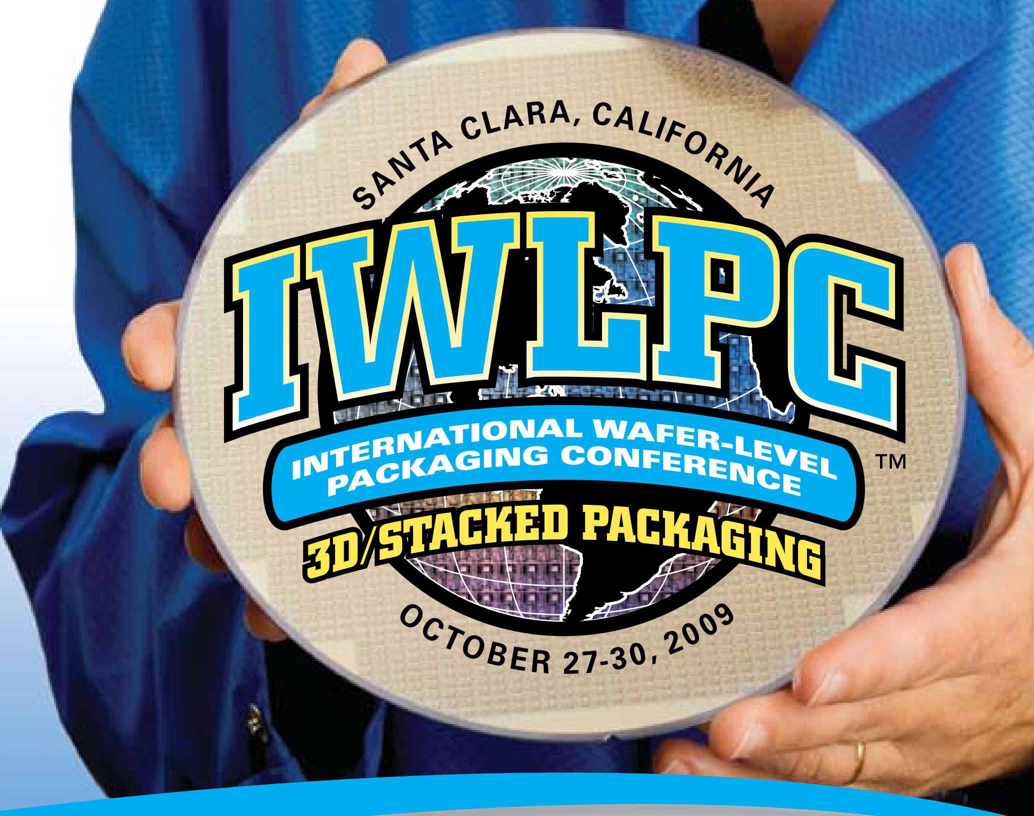

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