MEPTEC Report
Volume 14, Number 1
SPRING 2010

A Publication of The MicroElectronics Packaging & Test Engineering Council

SEE PULL-OUT BROCHURE

8th Annual

MEPTEC MEMS Symposium

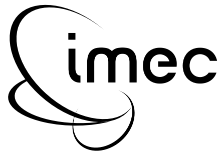
MEMS and IC System Integration: From Sensing to Awareness

A Special One Day Symposium and Exhibits Coming to San Jose, CA May 20th

INDUSTRY NEWS

Asia Pacific Microsystems, Inc. has announced that it has shipped over 2 million MEMS pressure sensor elements to a leading global automotive electronic company. *page 12*

A multidisciplinary research team at the **Nationasl Institute of Standards and Technology (NIST)** has found that an organic semiconductor may be a viable candidate for creating large-area electronics, such as solar cells and displays that can be sprayed onto a surface as easily as paint. *page 12*



Synopsys, Inc. and the Belgian nanoelectronics research center, **imec**, have announced that they have entered into a collaboration to use Synopsys TCAD (Technology Computer-Aided Design) finite-element method tools for characterizing and optimizing the reliability and electrical performance of through-silicon vias (TSVs). *page 13*

Sonoscan has publicly announced Sonoscan Critical Evaluation™ (SCE), a confidential service that acoustically inspects critical electronic components. *page 14*

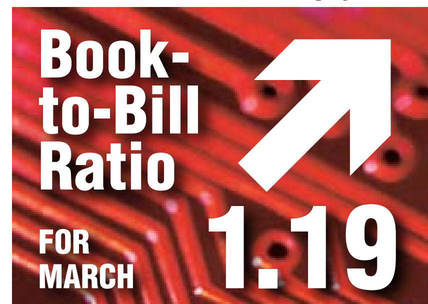
ECTC 2010 - The 60th Electronic Components and Technology Conference will be held June 1 - 4 at the Paris Las Vegas Hotel in Las Vegas, Nevada. *page 20*

MEMBER COMPANY PROFILE

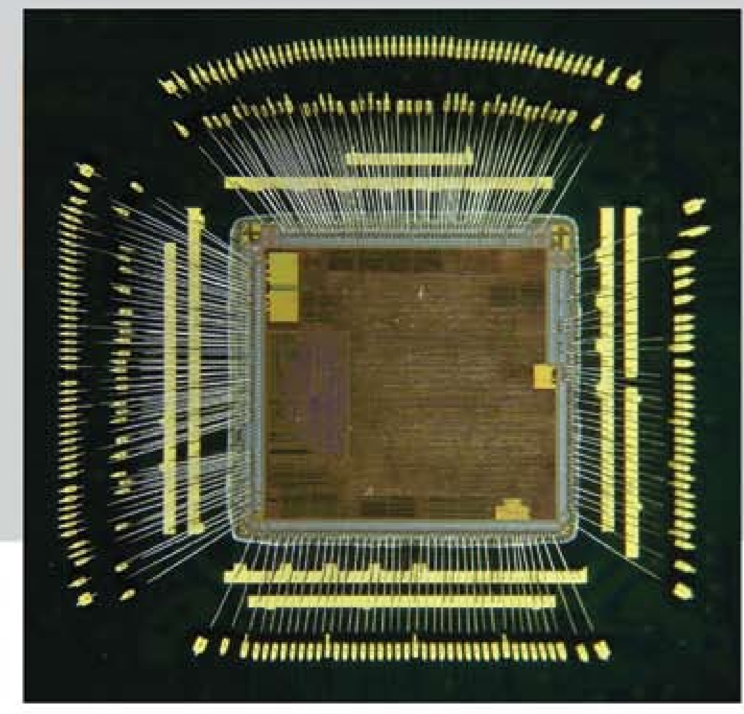
As one of the most diversified technology and manufacturing leaders, Honeywell International serves customers worldwide with aerospace products and services; control technologies for buildings, homes and industry; automotive products; turbochargers; and specialty materials.

In 2009 **Honeywell Electronic Materials** announced a new material that improves the efficiency and power output of photovoltaic (PV) panels. The new product, called Honeywell SOLARC™, is a transparent coating material that improves the light transmittance through the glass that covers PV panels, thus increasing the PV module efficiency and power output. This coating also significantly reduces glare from the glass, allowing the PV panels to better blend with their surroundings. *page 6*

Semiconductor equipment billings increase 423.3% over March 2009 level. *page 14*



Copper Wire



Copper Wire is a lower cost alternative to the traditional gold wire used in semiconductor packaging. Offering clear advantages, copper wire bonding is gaining popularity for products at 25 microns and below, where the majority of wire bond applications lie. ASE's copper wire bonding initiative is geared towards this group of applications. Bonding pad composition and wafer structure are major factors for copper wire evaluation, and ASE is customizing products based in specific customer needs.

www.aseglobal.com

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Council Update

Welcome to our Spring 2010 issue!

Our first event of 2010 was *"From Chip to System: Design Challenges and Solutions"* and was held on February 25 at the Holiday Inn in San Jose. The event explored co-design solutions – bridging the gap from silicon to system, ensuring quality and reliability in the design process, disruptive design solutions, and navigating the design IP minefield. CD's of the proceedings are available; visit www.meptec.org to order.

Our next event will be the 8th Annual MEMS Technology Symposium, *MEMS and IC System Integration: From Sensing to Awareness*. This symposium will cover the many integration technologies that have emerged over the last few years, each with its strengths and weaknesses. The keynote presentation will be **Philippe Kahn**, CEO and Founder of **Fullpower Technologies**, speaking on *"Accelerometrics: The Art of Motion Sensing...Because Motion is Life"*. Kahn is a technology visionary and creator of the first complete camera-phone solution. He has received numerous technology and business awards including the *2002 International Imaging Association (I3A) Leadership Award* and in 1995 was selected as one of Byte Magazine's twenty most important people in the history of the computer industry. You will find a pull out brochure for this symposium in this issue. Details and registration are available on www.meptec.org.

Our Industry Analysis this issue is by MEPTEC member **Jan Vardaman** of **TechSearch International, Inc.** In *"Semiconductor Packaging Expands in the Third Dimension"*, Jan explains that there are numerous approaches to 3D packaging, including SiP, PoP, PiP, CoC, etc. She shows that the adoption of 3D through TSV offers the best in 3D integration. Go to page 4 for this informative piece.

Our Company Profile comes from long-time MEPTEC member **Honeywell Electronic Materials**. Honeywell International is a diversified technology and manufacturing leader, with products that are ubiquitous in our everyday lives: planes, cars, heating and cooling our homes, medication dispensing, and many more. Honeywell's Electronics Materials division is a global leader in the semiconductor materials industry, and serves many sectors of technology. See their story on page 6.

One of our feature articles this issue is from long-time Corporate MEPTEC member company **ASE (US) Inc.** on *"Advanced QFN Package for Low Cost Solutions"*. The article describes ASE's aQFN package, which is an enhanced version of a conventional QFN and is a good solution for electrical components of portable communication devices. See page 9 for details.

Our editorial in this issue is by MEPTEC Advisory Board member **Seth Alavi** of **SunSil, Inc.** Seth wrote this piece as a follow up to our Q4-09 event, *"Semiconductor to Solar: Growth Opportunities for the IC Industry"*. Seth talks about a "technology renaissance" that has occurred over the last 50 years. He suggests that the next wave of technology for our industry just might lie in the solar/PV areana – see page 22 for this interesting piece.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC signs MOU with ASTSA

The Asia Semiconductor Trading Support Association (ASTSA) and MEPTEC have signed an MOU (strategic partnership). The ceremony took place at the 9th Annual Microelectronics and Advanced Packaging (MAP) International Workshop which was held in Fukuoka on November 13, 2009. Founded in October 2006, ASTSA has signed MOUs with a number of semiconductor-related organizations in several different Asian countries since its inception; however, this was the first time that MEPTEC, an organization with a long history of more than 30 years, has entered into an MOU with another semiconductor industry organization. Mr. Joseph Fjelstad, who represented MEPTEC at the signing ceremony commented on the value of the relationship between MEPTEC and Asia after the signing and implied the possibility of global expansion. Mr Fjelstad noted that: "More than 91% of 278 corporate members of MEPTEC are presently located in the US. Although MEPTEC has until now largely operated in the US providing technical forums and information to its members, MEPTEC hopes and plans to actively increase the number of its members in Asia, which is clearly leading production in the semiconductor packaging industry."

Semiconductor Packaging Expands in The Third Dimension

E. Jan Vardaman, President
TechSearch International, Inc.

There are many approaches to 3D packaging. These include versions of system-in-package (SiP) such as stacked die, stacked packages – package-on-package (PoP), package-in-package (PiP), and chip-on-chip (CoC) – in production today as well as versions being discussed for the future such as system-on-package (SOP), 3D fan-out wafer level packages, and vertical side interconnection techniques. While these packaging methods provide many benefits, the adoption of 3D through silicon via (TSV) technology offers the ultimate in 3D integration. Table 1 shows the advantages of various technologies.

Table 1. Advantages of Various Package Configurations.

	Die Stack	Side by Side	PoP	TSV
Advantage	Small, high-density circuits	Extremely reliable High thermal dissipation	Variable memory volume Memory shrink supported	Super small and super high-density
Smaller, high density	Excellent	Fair	Good	Excellent
Thermal resistance	Good	Excellent	Good	Excellent
Reliability	Excellent	Excellent	Good	Fair
Cost	Good	Fair	Fair	Fair

Source: TechSearch International, Inc. adapted from Renesas Technology Corporation.

Stacked Die

Applications for stacked die are typically portable products such as mobile phones, digital cameras, and music players but are also increasingly found in medical, industrial, and aerospace applications. Memory products with stacked die include solid-state drives (SSDs), microSD cards, and USB memory sticks. The die for these applications are typically less than 100 μm, with some companies reportedly with 25μm die thickness in R&D for microSD cards. The highest die stacks in production are reported to be up to 17 (memory die plus a controller) for microSD cards from both Samsung and Toshiba.

Stacked die CSPs are ideal for applications requiring multiple die in a small space, whether driven by form factor requirements or the need for maximum memory capacity. Two or more die are assembled into a stack that is then overmolded into a single, standard laminate CSP package. Typically most of these die are wire bonded, but some stacks contain flip chip die on the bottom. These packages ship in high volume, with more than 2.5 billion stacked die CSPs estimated to have been shipped in 2009. While most of these packages contain only two die, stacked die CSPs with nine or more die are in production. Figure 1 shows ASE's *a*QFN.

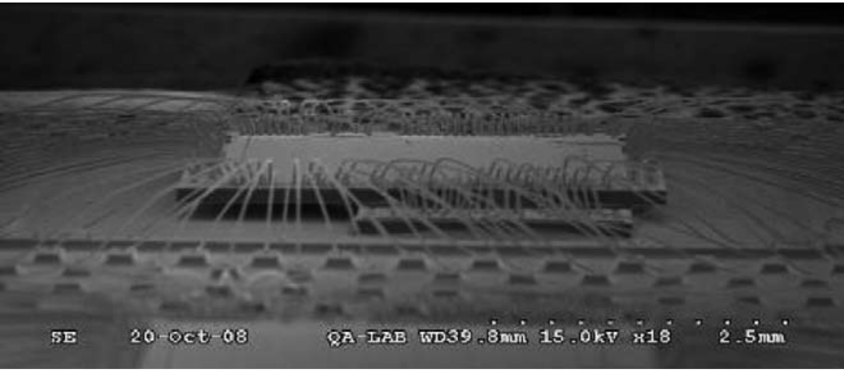


Figure 1. A stacked die in ASE's *a*QFN package. *Source: ASE.*

PoP

Package-on-package offers a different business model from stacked die, in that the memory die which are typically housed in the top package can be separately tested and burned in, if necessary, before they are committed to the stack. Logistics are simpler when the memory can be sourced in a standard package and assembled to the bottom package, and this approach also gives the flexibility to use different types of memory, depending on the application.

The primary applications for PoP continue to be logic plus memory stacks for smartphones, but the technology is also popular in digital cameras, MP3 players, and other multimedia applications. Demand for PoP is driven by integration and miniaturization, business and logistics advantages, and the requirements for standard and efficient interfaces for the high-speed bus between the processor and memory. Amkor leads in production volumes of PoPs. Amkor's bottom, high-density package that enables PoP stacks has been one of the fastest growing new products in Amkor's history[1], and has indicated that it is the fastest growing unit volume packages in the company's history. TechSearch International estimates that more than 220 million PoPs shipped in 2009 and the volumes will continue to grow.

One disadvantage of the PoP compared to the stacked die CSP is height. Substrate thickness and ball pitch/diameter are key factors governing package height. There has been considerable work in both areas, resulting in lower profile packages. In addition some companies have developed new packages. For example, through molded via (TMV™) is a new bottom PoP technology developed by Amkor (see Figure 2). TMV™ is a matrix-molded package with solder-filled openings for the

stacked interface to the top PoP. TMV™ offers improved warpage control, which allows the bottom PoP to be thinner, and it appears to be ideally suited to 0.5mm and 0.4mm interface pitch requirements in emerging JEDEC low power DDR2 (LP DDR2) specifications.[2]

Other companies, including CMK and Dia Nippon Printing have developed bottom package substrates with embedded components that offer a lower profile PoP. While these are not in production yet, several companies including Renesas show the technology on their roadmaps.

Fan-in PoP also addresses constraints associated with the peripheral connections between the top and bottom PoP packages, including large package size and warpage. Instead of peripheral connections, fan-in PoP provides a full array of connection points directly above the bottom silicon by using an interposer substrate on the top side of the bottom package. Advantages of fan-in PoP include a potentially smaller package footprint with less warpage, and a larger die/package ratio.[3] STATS ChipPAC has developed a fan-in PoP, and the Kyushu Institute of Technology has developed a similar solution known as the Dual Face Package. Samsung has developed a fan-in package with blind vias onto the silicon in the bottom PoP. Figure 3 shows a fan-in PoP.

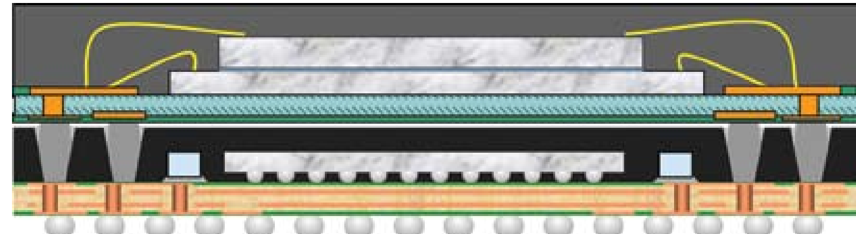


Figure 2. Through Mold Via (TMV™) is a new bottom PoP technology developed by Amkor.

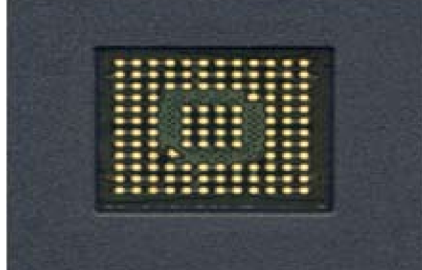


Figure 3. Fan-in PoP. *Source: STATS ChipPAC.*

PiP

Package-in-package is an intermediate solution. It is similar to a stacked die package, except that one of the stacked devices is a memory package – essentially a very thin LGA – that is pre-tested before being assembled and molded into the package. The PiP is also similar to stacked die in that it offers a thin, standard package for board assembly, but it has lower risk than stacked die because the memory package is tested and is only used if it is good. PiP is found in portable products such as mobile phones and digital cameras. The volumes for PiPs are in the tens of millions of units.

CoC

Chip-on-chip (CoC) is the first step in moving to 3D at the wafer level. In this technology the chips are thinned and face-to-face bonded without TSVs. Researchers at AT&T Bell Labs proposed one of the first concepts.[4] Infineon announced a CoC interconnection in 2005 when it introduced the Cu/Sn diffusion solder process called SLID. The first prototype application was for a smart card and included the integration of a memory and a controller, but it was not commercialized. In 2005, Sony introduced a microcontroller and memory CoC for the PlayStation. One of the drivers for the adoption was that Sony was unable to find a way to make the die cheaper by scaling embedded DRAM process technology from 90nm to 65nm. Sony noted that even with the adoption of a single chip DRAM and logic, each with a different manufacturing process, it would take a long time to obtain acceptable yield levels.[5]

TSV: The Ultimate in 3D

Many companies have commented that 3D ICs designed with TSV are the only option. Increased bandwidth is achieved because more data can be passed between the chips. The shorter interconnects enable faster data transfer. Lower power I/O signaling between the stacked die is also achieved because the signals do not have to be driven through packages and boards. Data transfer between stacked die is possible with short vertical interconnect lines that act as on-chip transmission lines and there is less loss and noise, therefore simple, low power drivers and receivers can be used for signaling. 3D integration also provides smaller form factor for systems by creating the option of building in the vertical direction.[6]

Applications for 3D TSV with stacked die include a variety of memory and logic combinations. The timing for mass production for 3D TSV technology depends on several factors. Clearly, there is demand for 3D TSVs, the infrastructure must be ready and how the TSV compares in terms of cost with existing technologies is critical. In many cases, this means wire bonded die stacking. While performance is a driver, cost is a limiting factor. While many DRAM makers have shipped samples of stacked memory with TSVs, the first commercial application for DRAM with TSVs is not expected until 2012, assuming reliability requirements can be met and current technologies are not able to meet the performance needs with lower cost. While many companies in the wireless application space would like to adopt a TSV solution today, the earliest adoption for volume production is expected to be 2012 when foundries have production lines fully qualified.[7]

As companies move from R&D into production the difficult work begins in addressing the issues of design, thermal management, test, and assembly. Different needs and economic factors determine the timing of adoption in each application. Issues in moving to volume production include the installation and qualification of high-volume 300mm production lines, assembly and test capability, the availability of TSV interposers, and reliability data. As the major issues are resolved, the ultimate in 3D packaging will be achieved.◆

1 "Amkor PoPs Cork for Fast Growing Package on Package Solution" Press Release April 18, 2007.

2 M. Dreiza, "Package-on-Package IMAPS Webinar," Jan 2009.

3 F. Carson, "Advancements in 3D IC Packaging", Semicon Japan, December 2008.

4 Y. Los, R. Frye, and K. O'Connor, "Design Methodology for Chip-on-Chip Applications," IEEE Transactions CPMT, Part B, Volume 21, 1998, p. 298.

5 M. Uno, "Chip-on-Chip Offers Higher Memory Capacity, Speed," Nikkei Electronics Asia, February 2007, pp. 28-32.

6 M. Shapiro, et al., "Reliable Through Silicon Vias for 3D Silicon Applications," International Interconnect Technology Conference, June 1-3, 2009, pp. 63-66.

7 E. J. Vardaman and P. Garrou, "3D Through Silicon Via: Infrastructure and Markets," TechSearch International, Inc., January 2010.

Honeywell

ELECTRONIC MATERIALS

Honeywell International is a diversified technology and manufacturing leader, serving customers worldwide with aerospace products and services; control technologies for buildings, homes and industry; automotive products; turbochargers; and specialty materials.

Whether you're flying on a plane, driving a car, heating or cooling a home, furnishing an apartment, taking medication or playing a sport, Honeywell products touch most peoples' lives everyday. Honeywell's brand promise commits to "...building a world that's safer and more secure ... more comfortable and energy efficient ... more innovative and productive."

Damper Flapper

Honeywell can trace its roots back to 1885, when an inventor named Albert Butz patented the furnace regulator and alarm. He formed the Butz Thermo-Electric Regulator Co., Minneapolis, on April 23, 1886, and a few weeks later invented a simple, yet ingenious device that he called the "damper flapper," a predecessor to the modern day thermostat that many people associate with Honeywell. In fact, the company introduced the T-86 "Round" thermostat in 1953, and it became one of the world's most recognizable designs; it remains in production today and adorns the walls of more households around the world than any other thermostat!

Honeywell "Round" Thermostat

Today, Honeywell employs over 120,000 people in more than 100 countries. It is a Fortune 100 company with sales of $31B in 2009.

Honeywell Electronic Materials

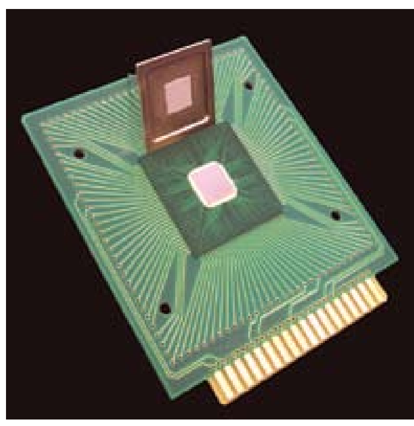
A rich heritage of innovation and experience backs Honeywell Electronic Materials, a strategic business enterprise of Honeywell International. Honeywell is a global leader in the supply of critical materials to the semiconductor industry, enabling customers to develop innovative technologies and overcome manufacturing challenges. Honeywell's expertise in both chemistry and metallurgy and commitment to disciplined quality processes result in the development of superior technologies that are now being introduced to the adjacent markets such as photovoltaic, optoelectronic, LED and printable electronics. With global manufacturing and R&D locations, Honeywell is near to its customers and development partners.

Honeywell serves customers in the semiconductor, photovoltaic, LED, printable electronics and optoelectronics markets with product offerings including advanced electronic polymers, electronic chemicals, sputtering targets and coil sets, packaging solutions for thermal management and electrical interconnect, and precious metal thermocouples for temperature control.

A Focus on Thermal Management and Electrical Interconnect

As microprocessors become smaller and faster, heat dissipation and environmental requirements have emerged as major technology challenges in the supply of electrical interconnect materials. Honeywell Electronic Materials has established itself as a leading supplier of electrical and thermal interconnect products for semiconductor packaging.

Specifically, Honeywell supplies heat spreaders used in both desktop CPU and chipsets, thermal interface materials (TIM1.5 and TIM2) for computing and memory modules, and low alpha Pb and Pb-free soldering material for chip interconnection applications. Packaging materials expertise also includes the production of high purity evaporation charges, electroplating anode products used for under bumping and wafer bumping of flip chips and other electrical interconnection products such as Al wire, Boron Oxide, die attach wire, and pure metals.

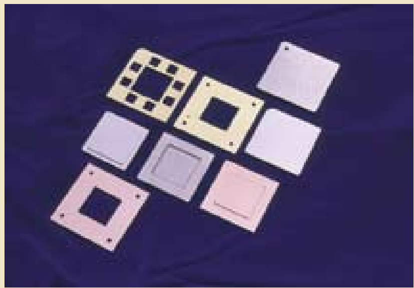


Semiconductor Packaging Materials

PCM45 Phase Change Materials

Honeywell supplies a family of phase change materials that offer industry leading thermal management performance. Known as "PCM45," these phase change materials are available in tape and roll as well as screen printable formats. They consist of a sophisticated thermally conductive material and maintain optimum filler size distribution to achieve maximum packing density compared to conventional phase change materials.

Honeywell PCM45 Phase Change Materials



Honeywell Heat Spreaders and Mechanical Stiffeners

Honeywell Electrical Interconnect Offerings

Heat Spreaders and Mechanical Stiffeners

Honeywell Electronic Materials is a premier supplier of formed and finished components to the semiconductor industry for packaging applications. These components are used in multiple types of packages for thermal management, die protection and mechanical support. Metal finishing on packaging components can be tuned for performance on a wide variety of adhesives.

Electrical Interconnect

For electrical interconnect, Honeywell offers evaporation and electroplating materials for back and underbump metallization and wafer bumping of flipchip die, as well as low-alpha lead products for solder bumping and Pb-free high temperature die attach wire for high power devices and the automotive industry.

In 2009, the company introduced Honeywell Pb-free Die Attach Solder, a lead-free thermal interface material that effectively manages the tremendous heat produced by semiconductor chips in order to improve chip reliability.

Honeywell had been developing lead-free die attach solder alloys for many years to meet the industry's environmental requirements that emerged with the use of lead-free solder at the circuit board level. This new alloy will replace high-lead alloys and provides better thermal management than other proposed lead-free thermal management alternatives such as polymer-based materials.

Demand for lead-free solders is growing, driven in part by regulation. Honeywell's new Pb-free Die Attach Solder is an advanced technology that meets these requirements, but is also cost effective. Lead-based solders are currently used for power/discrete die attach because they have a very good combination of melting temperature, wetting behavior, and mechanical properties. The new lead-free solder alloys are designed to meet these requirements, particularly resistance to melting during board level solder reflow.

The lead-free material is based on Honeywell's metallurgical expertise and long experience as a supplier of die-attach solders. Honeywell Pb-free Die Attach Solder is designed to be used mainly in wire form and compliments Honeywell's large diameter aluminum wire products.

Adjacent Markets: A Bright Future

Later in 2009, Honeywell Electronic Materials announced a new material that improves the efficiency and power output of photovoltaic (PV) panels. The new product, called Honeywell SOLARC™, is a transparent coating material that improves the light transmittance through the glass that covers PV panels, thus increasing the PV module efficiency and power output. This coating also significantly reduces glare from the glass, allowing the PV panels to better blend with their surroundings.

"SOLARC has already demonstrated the highest efficiency of any anti-reflective (A/R) coatings commercially available today," said Dmitry Shashkov, marketing director for Honeywell Electronic Materials. "This is another example of Honeywell applying its materials expertise, developed from 50 years of innovation for the semiconductor industry, to meet the challenges of the PV industry."

Most commercially available PV panels today lose approximately 4 percent of their potential power output due to light reflection from the front surface of the cover glass. In addition to the decreased electricity generation, the glare from the reflection light is considered aesthetically undesirable, especially in residential rooftop installations.

SOLARC coating reduces reflection significantly, resulting in more light reaching the solar cell, which translates into higher electricity output. While use of such A/R coating is relatively low in the PV industry today, it is widely expected to become the industry norm over the next few years, according to the major PV manufacturers.

Honeywell's SOLARC, which is a liquid-based coating, can be used by all common types of PV modules. However, it provides the most benefits to rooftop installations, where space is limited

and any increase in efficiency is critical. Because SOLARC coating reduces glare from the glass, it also contributes to a discreet, blend-in look of residential PV panels that has become very desirable to consumers installing the panels.

The coating is compatible with many coating processes, including spray, roller, curtain, slot-die and spin-on coating. Unlike other commercially available A/R coatings, Honeywell SOLARC does not require mixing of two components prior to deposition, and has at least a six month shelf life.

Demonstrating a 4 percent increase in transmission at 550 nanometers, Honeywell's SOLARC has demonstrated a very good response across a broad solar spectrum that is relevant for PV cell operation, from 350 nanometers through 1,100 nanometers. SOLARC coating has also demonstrated superior durability in a broad variety of accelerated tests designed to imitate harsh environmental conditions to which a PV panel is likely to be exposed during its lifetime.

Furthermore, environmental testing of SOLARC coating has shown that it provides additional protection to the glass, especially under hot and humid conditions that may lead to gradual glass deterioration. The coating has been further optimized to enable anti-soiling and self-cleaning functionality that prevents dust accumulation. This represents another valuable property of SOLARC, as solar panels lose on average 7 percent of their power output due to particulate contamination, according to the California Energy Commission.

Honeywell's SOLARC is based on proprietary technology and is validated by strong internal development processes and recognized industry test methods and laboratories.

The release of SOLARC coating further broadens Honeywell's portfolio of materials for the PV industry, which already includes backing sheet laminates, dopants, solar-grade electronic chemicals, and precision thermocouples.

Also in 2009, Honeywell announced that it developed a new thermal management material that improves energy efficiency of light emitting diodes (LEDs), which are increasingly being used in applications such as street lamps, automotive lighting, flat panel TV displays and computer monitors.

The new product, called Honeywell LTM6300-SP, is a thermal interface material that highly effectively transfers heat generated by LED lamps. As LEDs become smaller, faster and more powerful, more heat is being generated in a confined space, which can threaten to damage the LEDs' performance. If LEDs overheat, they become dim, their color is muted and their lifespans are shortened.

Photovoltaic Module

Because LEDs are semiconductor devices, they require more precise heat management than traditional light sources. Honeywell's thermal management materials are designed to meet this specific challenge, helping to effectively transfer heat in semiconductor applications.

Honeywell is committed to energy efficiency technology, and this newly developed thermal management material, which enhances the performance of energy efficient LEDs, is the first in a series of Honeywell phase change materials being developed for the growing LED segment.

LTM6300-SP was designed for LED backlights for flat panel displays, but the packaging technology can be also be implemented in LEDs used in a wide range of industries, from automobiles to computers. Honeywell LTM6300-SP is a high-thermal-performance phase change material that is superior to silicone-based products, which typically pump out and degrade at high temperatures.

The lighting industry has evolved from incandescent bulbs toward more energy-efficient options such as fluorescent bulbs and LEDs. Demand for LEDs is growing because they have several benefits over traditional light sources, such as lower energy consumption, longer lifespan, and smaller size. They also produce more light per watt than incandescent bulbs, are more durable and faster, and are mercury-free.

LED Stoplights

When used instead of traditional light sources, LEDs also reduce pollution and carbon footprint because they demand less power, which translates into energy savings that result in lower carbon dioxide and mercury emissions.

For more information on Honeywell Electronic Materials products and services, contact them at:

Phone: 509-252-2102
Fax: 509-252-8617
www.honeywell.com

Honeywell
ELECTRONIC MATERIALS

Advanced QFN Package for Low Cost Solution

Andy Tseng and Bernd Appelt, ASE (US), Inc.
Yi-Shao Lai, Mark Lin, Bruce Hu, JW Chen, Louie Huang and Sunny Lee
Advanced Semiconductor Engineering, Inc. (Taiwan)

Advanced QFN (*a*QFN) is an enhanced version of QFN (Quad Flat No-Lead package) with multiple rows of terminals featuring higher number of I/O ports. The thermal and electrical performance of *a*QFN should is superior due to a smaller profile and shorter interconnects. Solder wettability control and board-level thermo mechanical reliability of *a*QFN is greatly enhanced over conventional QFN and similar types of lead frame packages because of the greater standoff of the *a*QFN Cu posts. *a*QFN provides similar I/O numbers as BGA-type chip-scale packages (CSP) but at much less cost since the expensive substrate is replaced by a lead frame. *a*QFN turns out to be an ideal low cost solution for electrical components for portable telecommunication applications such as IrDA, Bluetooth, RFID, cell phone baseband etc. because of its superior thermal, electrical, reliability performances and miniaturized package size.

Recently, Cu wire bonding for IC packaging has been used to replace Au wire bonding in fine bond pad pitch applications to reduce package cost. *a*QFN is one of the packages adopting Cu wire bonding. The overall cost of *a*QFN packages with Cu wire bonding has been decreased significantly by about 10-15% for each individual piece. With such advantages, it is expected that *a*QFN will replace many CSP applications, especially for handheld & PDA devices and related applications.

Introduction

IC packages are demanding to be smaller, lighter, and fine pitch for high performances and multiple operation functions of electronic devices. For such demands, chip-scale BGAs (CSP), wafer-level chip-scale packages (WLCSP), and leadless packages such as quad flat no-lead packages (QFN) are favored packaging choices. CSP shows the best design flexibility by three-dimensional circuit routing within the substrate. WLCSP provides reasonably good design flexibility by circuit routing through the redistribution layer (RDL). However, the electrical and thermal performances for WLCSP are relatively low, and the layout is not feasible for high-power applications with the presence of RDL. Both, CSP and WLCSP, are relatively high in cost. Leadless packages possess the best electrical and thermal performances[1] as well as the lowest fabrication cost among these packages, however, their lead counts are quite low and their design flexibility clearly is the worst.

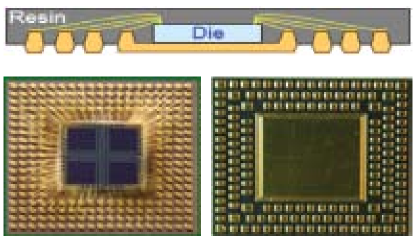


Figure 1. Schematic and package outline of *a*QFN.

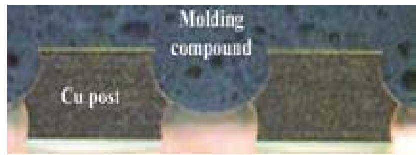


Figure 2. Cross-sectional view of *a*QFN.

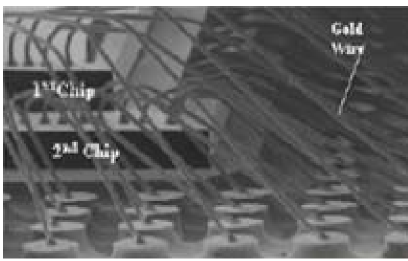


Figure 3. Stacked-die *a*QFN.

In order to expand the application range of leadless packages and to preserve their cost and performance advantages, efforts have been devoted to increasing the number of leads, following the QFN structure in particular (e.g.,[2,3]). The multiple-row QFN does suffer from solder bridging between neighboring terminals when the pitch is small. The low stand-off of QFN solder joints may also raise thermo mechanical reliability risks. To overcome these issues, the *a*QFN package, whose schematic and outline are shown in Figure 1, has been proposed and developed [4, 5].

*a*QFN is an enhanced version of conventional QFN and is capable of providing many more footprints at an identical package size, with the I/O number approaching that of CSP. The unique fabrication process of aQFN consists of double-sided etching of the Cu lead frame to create isolated Cu posts with a relatively high standoff (see Figure 2). The higher standoff leads to enhanced solder wettability control which enables fine-pitch devices as well as improved thermomechanical reliability of the solder joints[3]. This particular packaging structure also offers the possibility of die stacking, as shown in Figure 3. Furthermore, a certain amount of routing can be done through post-to-post wire bonds or within the mother board.

Fabrication Process of *a*QFN

The fabrication process of *a*QFN is composed of two major sections. In section one, NiAu is plated in the pattern of the *a*QFN circuit pattern. The NiAu layer is then used as a photo resist or etching mask for half-etching the copper strip. The half-etched lead frame is shipped to the assembly house for IC packaging. The assembly process follows sequentially with die attach, wire bond, and molding. Clearly, the half-etched lead frame is capable of providing a cavity for the die that enables die stacking with low package profiles, or it avoids excessive thinning of the die, and hence reduces the fabrication risk during the wafer thinning process. The half-etched lead frame also eliminates the possibility of mold flash along the interface between lead frame and tape as in a conventional QFN process. After molding, the Cu lead frame undergoes another etching step down to the compound to form the isolated Cu posts, as shown in Figure 2.

Three packages: *a*QFN, BCC++ and QFN, all leadless packages were modeled. We note that thermal performances are similar among all leadless packages. Slight differences of θ_{JA} among aQFN, QFN and BCC++ come from the thickness of the die pad. Thicker die pads benefit the heat dissipation.

The thermal characteristics of exposed pad LQFP, regular LQFP, CSP and

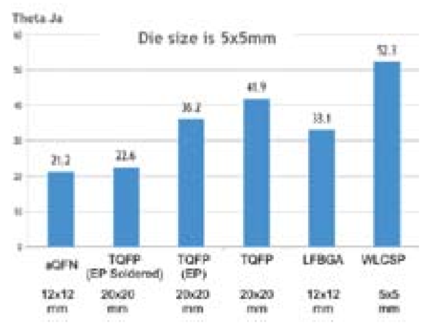


Figure 4. Thermal data of different type packages.

WLCSP, were evaluated via θ_{JA} and are compared in Figure 4. Power dissipation was set to 2W and ambient temperature to 25°C. We note that thickness of die and package does not have a significant effect on thermal characteristics. Clearly from the chart, the thermal performances are similar for packages with die attach paddle soldered to the PCB. CSP has multi-Cu layers which enhance thermal performance. Bare die of WLCSP has the worst heat dissipation.

Performance Comparison: *a*QFN vs. CSP

To demonstrate the excellent performances of *a*QFN over CSP, identical functions are intentionally designed into both *a*QFN and CSP packaging structures, so that thermal and electrical performances of these two structures can be reasonably compared. With the same functions, *a*QFN allows a thicker die (or a lower fabrication risk during wafer thinning process) as well as a smaller and thinner package silhouette compared to CSP (see Table 1).

Comparisons of thermal and electrical characteristics between the two packages are listed in Tables 2 and 3, respectively, in which the thermal characteristics are evaluated under a power dissipation of 1W and an ambient temperature of 25°C. It is clear from the tables that *a*QFN outperforms CSP in terms of thermal and electrical performances, even though the longest trace in CSP is shorter than that in *a*QFN.

The electrical simulation data in the frequency domains are shown in Figure 5.1 (Insertion loss) and Figure 5.2 (Return loss). From both data, the *a*QFN can run above 16GHz (at -0.3dB) and 17GHz (at -15dB) which is a lot higher than CSP packages. Besides the excellent thermal and electrical performances, *a*QFN is also cost-effective compared to CSP because of the absence of the substrate.

	*a*QFN	CSP
Package size	10.4 × 10 × 0.85	13 × 13 × 1.4
Lead count	254	293
Die size	4.6 × 4.4 × 0.28	4.6 × 4.4 × 0.13
Die pad size	5.2 × 5	---
Die attach thickness	0.025	
Terminal/Ball size	0.2 × 0.2	0.3
Terminal/Ball pitch	0.4	0.65
Standoff	0.03	0.3
Substrate thickness	---	0.26

Table 1. Component Dimensions of Packages.

Package Type	Air Velocity (m/s)	θ_{JA} (°C/W)
*a*QFN	0	23.53
	1	17.78
	2.5	15.74
CSP	0	35.72
	1	31.32
	2.5	29.11

Table 2. Comparison of Thermal Characteristics.

Package Type	Trace Length (mm)	R (mΩ)	L (nH)	C (pF)
*a*QFN	Shortest: 0.91	70.4	0.982	0.160
	Longest: 3.31	210.5	3.845	0.329
CSP	Shorter: 2.97	157.2	2.723	0.742
	Longest: 3.00	232.2	5.854	0.953

Table 3. Comparison of Electrical Characteristics.

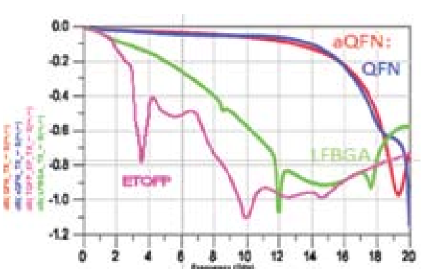


Figure 5.1. Insertion loss of *a*QFN, QFN, TQFP and CSP.

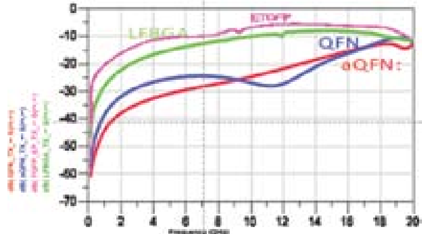


Figure 5.2. Return loss of *a*QFN, QFN, TQFP and CSP.

*a*QFN Package Qualification

A 10.2x10.2mm *a*QFN 246L package has been chosen for packaging qualification under the conditions shown in Table 4. This package passed moisture sensitivity level 2a of pre-condition and also passed TCT 1000 cycles, PCT 336 hours and HTST 1700 hours.

*a*QFN Surface Mount Process Study

Given the lower package standoff (50μm) and fine pitch terminals (0.47mm) of *a*QFN when compared to CSP (200μm solder ball height and 0.5mm pitch), SMT tends to be more difficult. To improve the assembly yield, SMT DOEs were performed and "*a*QFN Surface Mount Application Notes" have been developed to ensure that it has high yield rate in SMT assembly. Some design rules from the application notes are listed in Table 5.

Condition (Package)	Progress
Moisture Sensitivity	Passed Level-2a @260°C
TCT: -65°C ~ RT ~ 150°C	Passed 1000 cycles
HTST: +150°C	Passed 1700 hours
PCT: 121°C 85%RH, 2atm	Passed 336 hours

Table 4. Packaging Qualification Conditions.

Table 6 shows the yield data from five different SMT assembly houses which followed the "*a*QFN SMT Application Notes". The overall yield is 99.3%. The top 3 defect modes are solder bridging (short), cold joints (open) and mis-alignment (placement accuracy).

Conclusions

*a*QFN package is an enhanced version of conventional QFN which is capable of providing many more footprints at an identical package size and with the I/O number approaching that of CSP. It is an ideal solution for electrical components of portable telecommunication devices for its superior thermal, electrical, and reliability perfor-

mances and miniaturized package size. It is expected that *a*QFN will replace many CSP-BGAs.

It has been shown that the electrical and thermal performance of lead frame packages is retained at similarly low costs. *a*QFN outperforms CSP and WLCSP packages electrically and thermally and most importantly in cost.

"*a*QFN Surface Mount application Notes" have been developed and very high SMT assembly yields have been demonstrated at five independent assembly houses.

Acknowledgments

The authors would like to thank Yuan-Ting Chang, Chang-Chi Lee, and Chi-Wei Wu with ASE, Inc. for their support in performing thermal and electrical analyses.

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5. Japanese Patent No. 3,780,122.

6. Courtesy by Mitsui High-tec, Inc.

7. ASE group, "aQFN Surface Mount Application Notes V9 ", 2009-11-12 .

aQFN Package			PCB Land Pad Design			Stencil	
Land Pitch (mm)	Terminal Size (mm)	Land Shape	Land Shape	Copper Pad (mm)	Solder Mask Opening (mm)	Thickness (mm)	Opening (mm)
0.8	0.4	Square	Square	0.43	0.53	0.12	0.48
0.8	0.4	Circle	Circle	0.43	0.53	0.12	0.48
0.65	0.35	Square	Square	0.375	0.475	0.12	0.4
0.65	0.35	Circle	Circle	0.375	0.475	0.12	0.4
0.5	0.3	Square	Square	0.325	0.425	0.1	0.38
0.5	0.3	Circle	Circle	0.325	0.425	0.1	0.38
0.5	0.25	Square	Square	0.275	0.375	0.1	0.33
0.5	0.25	Circle	Circle	0.275	0.375	0.1	0.33
0.47	0.27	Circle	Circle	0.27	0.37	0.1	0.32
0.47	0.245	Circle	Circle	0.27	0.37	0.1	0.32
0.4	0.2	Square	Square	0.225	0.325	0.1	0.27
0.4	0.2	Circle	Circle	0.225	0.325	0.1	0.27

Table 5. Design Rules of Stencil Opening.

SMT Assembly House	X-ray	O/S Test	Yield
	(passed units)/(total units)	(passed units)/(total units)	%
SMT Assembly House 1	9989/9998	9987/9998	99.9%
SMT Assembly House 2	12993/13020	12977/13020	99.7%
SMT Assembly House 3	9982/9990	9952/9990	99.6%
SMT Assembly House 4	14997/15055	14865/15055	98.7%
SMT Assembly House 5	11981/11996	11854/11996	98.8%
Summary	59942/60064	59635/60064	99.3%

Table 6. Yield Data from Five SMT Assembly Houses.

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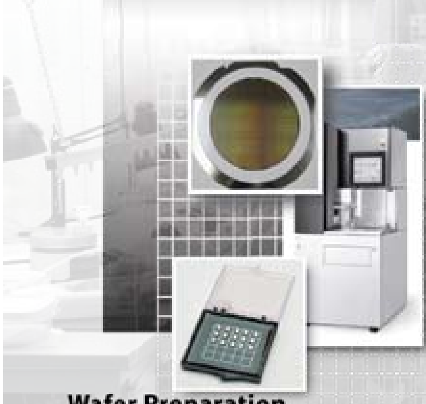

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Editor's Note: A portion of the press release below was omitted in our last issue and is being rerun in its entirety.

IEEE Rayleigh Award to Sonoscan's Dr. Kessler

Dr. Lawrence W. Kessler guiding the latest developments in acoustic microscopy.

ELK GROVE VILLAGE, IL – On September 21 in Rome, Italy, Sonoscan president Dr. Lawrence W. Kessler received the prestigious Rayleigh Award presented by the Ultrasonics, Ferroelectrics, and Frequency Control (UFFC) Society of the IEEE.

Each year a recipient is selected on the basis of achievements in research, education, publications, and technical innovations. Since he founded Sonoscan in 1974, Dr. Kessler has been a conspicuous leader in each of these areas. As the Chief Technology Officer of Sonoscan, he has been responsible for many of the numerous patents that Sonoscan has received over the years.

He has also spearheaded the continuous flow of technical innovations that have grown the utility and versatility of acoustic micro imaging systems into the industry that we have today. In 1975 Sonoscan introduced the first commercially available acoustic microscope, the SLAM (Scanning Laser Acoustic Microscope). In 1984 Sonoscan introduced the reflection-mode C-SAM® (C-Mode Scanning Acoustic Microscope) system, which was the precursor of all modern acoustic microscope systems.

Sonoscan, Inc., 2149 East Pratt Blvd., Elk Grove Village, IL 60007, Phone: 847.437.6400, x240, Email: info@sonoscan.com, Web: www.sonoscan.com.

Honeywell Announces New Thermal Management Materials for Portable Computing Devices

MORRIS TOWNSHIP, NJ – Honeywell Electronic Materials has announced a new printable thermal management material designed to help manage the tremendous heat produced by increasingly powerful semiconductors in portable computing devices such as laptops and netbooks.

Honeywell is a recognized leader in developing thermal management solutions that transfer and dissipate heat, and the new material, Honeywell PCM45M-SP, builds on Electronic Materials' existing line of thermal management materials. As semiconductors become more powerful and smaller, more heat is being generated in the confined spaces where semiconductors are packaged for end-use applications. This tremendous heat can damage the semiconductor or degrade its performance, and it can damage the device as well.

In typical mobile computing applications, chip temperature rises steeply at start-up and remains high during operations. PCM45M-SP is designed to meet these specific thermal management requirements, delivering reliable power cycling performance where other thermal materials would typically fail.

PCM45M-SP can withstand more than 1,000 hours at 150°C without degradation and more than 1,000 temperature cycles. The application is not limited to heat sink design, and the material may be applied to a component, heat sink or thermal spreader in any shape built into the printing screen. Additionally, the enhanced stability of this new material minimizes or eliminates the need for premixing, conserving time and resources.

For more information about Honeywell products visit www.honeywell.com/em.

Simultaneous Double Sided Probing System

WINOOSKI, VT – SemiProbe has announced the installation of a new enabling technology – simultaneous double sided prober. The system will provide test access to a next generation sensors. Previously, double sided probers were used primarily as a part of an emission microscope system which required the device to be probed from either the top or the bottom depending upon the orientation of the emission microscope. These systems were designed to allow probe contact on either side of the wafer, but not both at the same time. New devices with active regions on both sides of the wafer as well as some TSV (Thru Silicon Via) technologies will require individual probe contact on both sides of the wafer at the same time. The new system installed at a leading research laboratory is an enabling technology allowing access to device information never before available thru simultaneous contact with probes on both sides of the wafer.

More information about SemiProbe may be found at www.semiprobe.com or by calling (802) 860-7000.

APM Ships Pressure Sensor Elements to Automotive Industry

HSINCHU, TAIWAN – Asia Pacific Microsystems, Inc. (APM) announced that it has shipped over 2 million MEMS pressure sensor elements to a leading global automotive electronic company. APM provides MEMS foundry services for the piezoresistive sensor elements which are key components for the pressure sensor business. With intensive engineering development and product qualification work with this customer, the first production was launched in May 2009, and so have the additional product families in early 2010. APM is shipping the sensor elements to this first tier customer's plant for module assembly and calibration.

APM is also a key partner to the same customer for the MEMS pressure sensor development roadmap. Early collaboration between the customer's design group and APM's process experts facilitates the turn-key proto-type fabrication and a true "design for manufacturability" model. This type of relationship aids in launching cost efficient, high quality, and high yield products.

APM is a pure-play MEMS wafer foundry founded in 2001. It is one of the leading MEMS wafer foundry service providers with a 27,000 square foot 6-inch MEMS fab comprised of a broad range of MEMS fabrication capabilities. APM, an affiliated company of United Microelectronics Corporation, is ISO 9001, ISO14001 and TS16949 certified.

NIST Studies Spray-On Manufacturing of Transistors

A multidisciplinary research team at the National Institute of Standards and Technology (NIST) has found that an organic semiconductor may be a viable candidate for creating large-area electronics, such as solar cells and displays that can be sprayed onto a surface as easily as paint.

While the electronics will not be ready for market anytime soon, the research team says the material they studied could overcome one of the main cost hurdles blocking the large-scale manufacture of organic thin-film transistors, the development of which also could lead to a host of devices inexpensive enough to be disposable.

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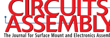

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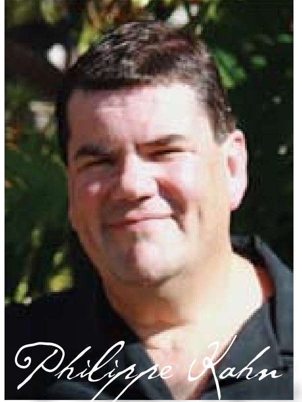
New technologies have life cycles of about 50 years. The semiconductor industry emerged in 1950s, and the market leaders experienced extended periods of high (70%) gross margins. The days of such margins seem to be over, and the number of market segments with significant (>25%/y) growth has shrunk. However, many high growth segments are correlated to MEMS-based devices, which add real-world sensing and actuation to digital logic and memory to create smart, aware systems. From a MEMS perspective, access to advanced custom ICs has become easy and inexpensive, enabling a wealth of new, intelligent, integrated systems.

As high volume MEMS markets have emerged, we have witnessed a trend from discrete sensors to "smart" sensors integrated with electronics, bringing a potential for extending the period of de-commoditized (high gross margin) semiconductor applications through system level MEMS-IC integration. We are now at the cusp of another wave of integration, where multiple sensors can be integrated together with electronics into systems that are significantly more "aware" – providing not just sensing, but gesture recognition, pinpoint location, human activity, and environmental conditions to name a few. Networking all of these sensors together provides yet another level of smart integration.

While first generations of MEMS devices were offered without electronics, with time a lot of effort went towards on-chip integration of electronics. This symposium will cover the many integration technologies that have emerged, each with its strengths and weaknesses.



Symposium Keynote

Accelerometrics: The Art of Motion Sensing... Because Motion is Life

Philippe Kahn, CEO and Founder of Fullpower Technologies

In his keynote presentation Philippe Kahn will discuss the art of motion sensing. Please join him as he reflects on how motion shapes lives and how hybrid sensors hold a special opportunity for the next generation of mobile devices to integrate complex and advanced motion solutions and the necessary software technology. Just like microphones couldn't deliver advanced speech recognition solutions, the best sensors need an advanced motion recognition engine. What is this engine? Kahn will use the MotionX technology platform as an illustration of these advanced software solutions.

Philippe Kahn is a technology visionary and creator of the first complete camera-phone solution. Kahn is presently CEO and founder of Fullpower Technologies, his fourth successful technology company, which specializes in mobile sensing solutions for use in mobile phones and other consumer electronic devices. He holds a master's degree in mathematics and is the author of dozens of patents. In addition Kahn has received numerous technology and business awards including the 2002 International Imaging Association (I3A) Leadership Award and in 1995 was selected as one of Byte Magazine's twenty most important people in the history of the computer industry.

MEMS Industry Group's Members Only event, METRIC 2010

We are pleased to be co-locating with the MEMS Industry Group's Members Only event, METRIC 2010. METRIC will be held the day preceding the MEPTEC symposium, on May 19, with a special reception and panel discussion on May 18. Visit the MIG website at **www.memsindustrygroup.org** for details.

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A limited block of rooms has been reserved at the Wyndham Hotel for a rate of $129.00. The hotel is conveniently located at 1350 North First Street, San Jose, CA in close proximity to the San Jose Airport. Call 408-453-6200 or 800-996-3426 to reserve your room. Be sure to mention MEPTEC in order to secure the special rate.

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The team's work showed that a commonly used organic transistor material, poly (3-hexylthiophene), or P3HT, works well as a spray-on transistor material because, like beauty, transistors aren't very deep. When sprayed onto a flat surface, inhomogeneities give the P3HT film a rough and uneven top surface that causes problems in other applications. But because the transistor effects occur along its lower surface – where it contacts the substrate – it functions quite well.

The simplicity of spray-on electronics gives it a potential cost advantage over other manufacturing processes for organic electronics. Other candidate processes require costly equipment to function or are simply not suitable for use in high-volume manufacturing.

Imec and Synopsys Collaborate on 3D Stacked IC Development

MOUNTAIN VIEW, CA – Synopsys, Inc. and the Belgian nanoelectronics research center, imec, have announced that they have entered into a collaboration to use Synopsys TCAD (Technology Computer-Aided Design) finite-element method tools for characterizing and optimizing the reliability and electrical performance of through-silicon vias (TSVs). The collaboration will accelerate the development of 3D stacked IC technologies.

While considered an emerging technology, 3D stacked IC complements conventional transistor scaling and allows multiple chips to be stacked and integrated into a single package. This technology reduces form factor and power consumption, and increases bandwidth of inter-chip communication by minimizing connections through the circuit board with high parasitic capacitance. As with other innovative technologies, 3D stacked IC introduces a number of new issues that can potentially affect its reliability and performance. The collaborative research to address these issues will take place at imec, where silicon wafers with test structures will be manufactured and tested, and Synopsys' TCAD tools will be used to model the TSVs in the chip stacks to optimize 3D stacked IC performance and reliability.

Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at www.synopsys.com.

Imec is headquartered in Leuven, Belgium, and has offices in Belgium, the Netherlands, Taiwan, US, China and Japan. Further information on imec can be found at www.imec.be.

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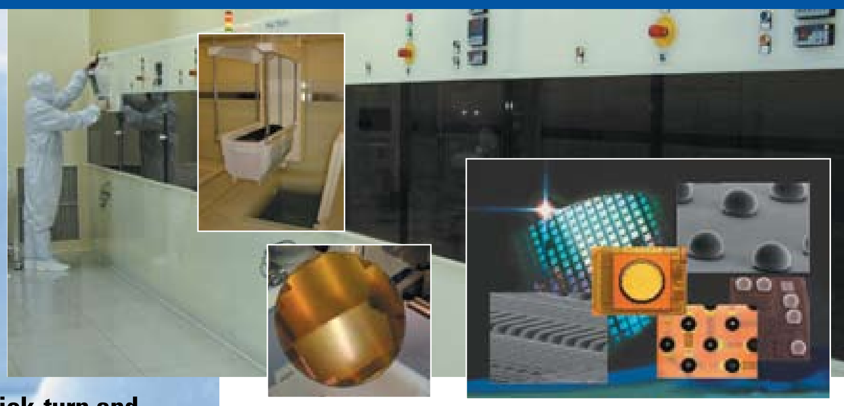

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Amkor Technology Installs Systems from SUSS MicroTec

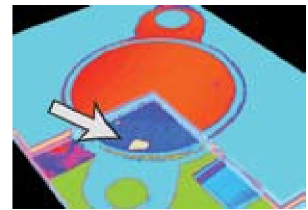
GARCHING, GERMANY, – SUSS MicroTec has received orders for multiple 300mm lithography systems from Amkor Technology Inc. The equipment package includes MA300 Gen2 mask aligner systems and ACS300 Gen2 wafer processing clusters for wafer level packaging, wafer bumping and 3D integration technology. Installations at Amkor's K4 plant in Gwangju, Korea, and T1 fab in Hsin-Chu, Taiwan, are scheduled to be completed in Q3 2010.

"As a contract manufacturer for semiconductor companies worldwide we are committed to bringing leading-edge packaging solutions to market", said ChoonHeung Lee, CVP and CTO, Amkor Technology. "SUSS MicroTec's lithography systems have been an integral part of our success and have set an exceptional track record for process capability, reliability, support and overall cost of ownership for our worldwide operations."

For more information about SUSS MicroTec visit their website at www.suss.com.

More about Amkor is available from the company's SEC filings and www.amkor.com.

Mil/Aero Reliability Inspection for Latent Defects



3-D acoustic image of hybrid device. Arrow indicates internal defect.

ELK GROVE VILLAGE, IL – Sonoscan has publicly announced Sonoscan Critical Evaluation™ (SCE), a confidential service that acoustically inspects critical electronic components such as hybrids, capacitors and plastic-encapsulated microcircuits used in military and aerospace systems. The service became active in mid-2009.

Acoustic Micro Imaging nondestructively images hidden latent defects such as delaminations, cracks and voids – for example, a delamination on the face of a silicon chip. It also characterizes materials such as encapsulants.

SCE handles individual components, hybrid devices, and printed wiring boards. The purpose of imaging is to locate, identify and analyze internal

North American Semiconductor Equipment Industry Posts March 2010 Book-To-Bill Ratio of 1.19

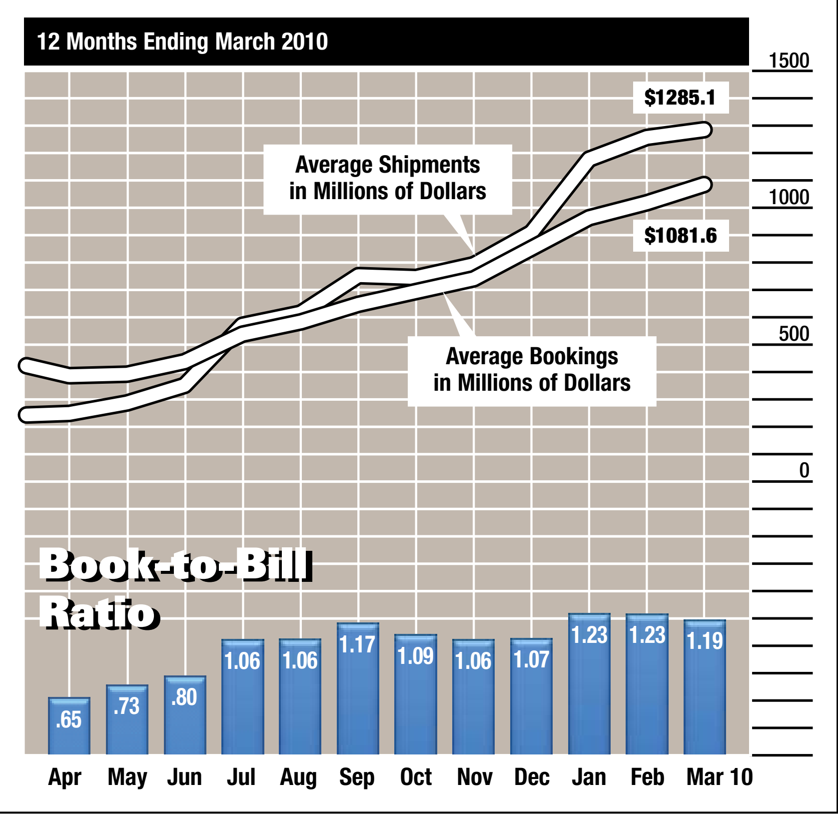
SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted $1.29 billion in orders in March 2010 (three-month average basis) and a book-to-bill ratio of 1.19, according to the March 2010 Book-to-Bill Report published by SEMI. A book-to-bill of 1.19 means that $119 worth of orders was received for every $100 of product billed for the month.

The three-month average of worldwide bookings in March 2010 was $1.29 billion. The bookings figure is up 2.7 percent from the final February 2010 level of $1.25 billion, and is 423.3 percent above the $245.6 million in orders posted in March 2009.

The three-month average of worldwide billings in March 2010 was $1.08 billion. The billings figure is up 6.4 percent from the final February 2010 level of $1.02 billion, and is 146.8 percent above the March 2009 billings level of $438.3 million.

"Bookings have now returned to levels seen in late 2007," said Stanley T. Myers, president and CEO of SEMI. "The steady and consistent rise in bookings and billings shows that the industry is on a well-managed growth path."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



anomalies that can cause electrical failures in service, such as die attach voids in a hybrid device or singulation cracks in a capacitor.

In some applications, the interest is on purely mechanical features in items such as micro spot welds or multi-layer composite materials.

Two groups work together to provide SCE:

- the SonoLab® applications laboratory personnel; and
- hardware engineering, machine shop, software engineering and other Sonoscan departments that give specific support as needed.

Typically client engineers handle their own parts and load them into a laboratory C-SAM® system in a secure, certified room at the Elk Grove Village SonoLab®. Acoustic imaging, according to the client's requirements, is supervised by Sonoscan specialists who apply their expertise in critical areas such as image interpretation and the use of alternate imaging techniques to achieve the component reliability required by the client.

SCE gives the client company's engineers the control they need over testing and evaluation of their parts as well as the in-house resources to meet the full spectrum of challenges that are part of advanced testing of critical components.

For more information contact SonoLab manager Ray Thomas at 847-437-6400 x 245.

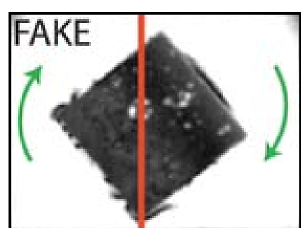
Sonoscan Expands Counterfeit Identification Menu

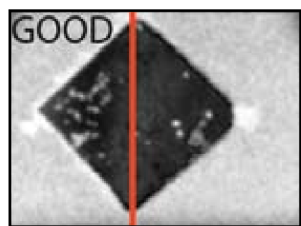
ELK GROVE VILLAGE, IL – SonoLab®, the applications laboratory division of Sonoscan, has recently developed analytical techniques that bring to 25 the number of acoustically detectable features and characteristics used to separate counterfeit plastic IC packages from genuine packages.

"The increase in useful tools is the result of our growing base of experience in separating counterfeit components from genuine parts – often within a mixed lot shipment," said SonoLab manager Ray Thomas. "Our laboratories are seeing more questionable parts because the industry has become much more interested in weeding out counterfeit parts. Ideally, engineers have known genuine parts to which they can compare incoming parts."

Identifying a counterfeit component may be straightforward, he added, but is often more complex. Part of the problem is that counterfeiters are becoming more skilled at making their knock-offs resemble genuine components. Using a greater number of acoustic techniques increases the confidence factor when separating genuine parts from fake parts. Measuring two or three parameters may suggest that a part is genuine or fake, but having a menu of 25 items on hand makes it much easier to make clear distinctions.

For more information contact SonoLab manager Ray Thomas at 847 437-6400 x 245.





In these acoustic images of two D-PAKs, the diamond shape is the die, attached to its rectangular substrate. In the counterfeit D-PAK at top, the die is rotated (arrows) out of its correct position. It is also closer to the lower edge of the substrate than the good die at bottom. The die in genuine D-PAK at bottom is properly centered and aligned, thus indicating that the counterfeit part was manufactured by a different vendor or a different process. In addition, the mold compound shows measurable variation between the two packages.

Surface mounted device with delamination (red) along the entire length of several leads. This part would fail per J-STD-020 criteria.

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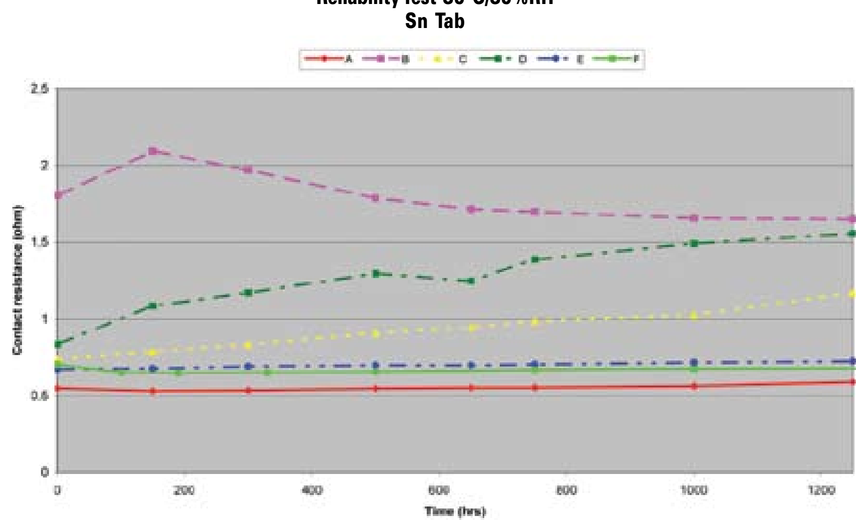
Photovoltaic Modules get a Charge from New Electrically Conductive Adhesives

Tom Adcock, Gunther Dreezen, Hilde Goosens and Anja Henckens
Henkel Corporation

For high reliability applications such as satellite, automotive, medical and telecom products, electrically conductive adhesives are often used as an alternative to traditional solders. Their benefits are many but, for these applications, conductive adhesives deliver low temperature processing, fine-pitch capability and improved thermal cycling resistance. These advantages are arguably compelling, but electrically conductive adhesives have had limited success on common electronic metals such as copper and Sn and, therefore, have been used most often on noble metallizations like gold and silver palladium on ceramic substrates. While conductive adhesives may also provide benefits to the thin film solar cell market and the silicon solar cell segment, their limitations on copper and Sn have slowed their adoption.

To address this limitation, new development work has resulted in the formulation of electrically conductive adhesives that overcome the drawbacks of older-generation systems. Recent work has shown that the unstable contact resistance of electrically conductive adhesives on copper and tin is due to electrochemical corrosion of these metals under elevated temperature and humidity conditions. Based on these fundamental understandings, Henkel has developed a new class of conductive adhesives which exhibit exceptional contact resistance stability on surfaces including OSP copper, Sn alloys and even 100% Sn. The result is a new electrically conductive adhesive product – called Hysol ECCOBOND CE 3103WLV – for use on thin film solar substrates.



Contact resistance stability under 85%RH/85°C conditions of conductive adhesives when bonding a Sn metallized tab onto ITO-coated glass.

To demonstrate the performance of Henkel's new electrically conductive adhesives for thin-film solar cell applications, a test device with indium tin oxide (ITO) terminations was bonded to non-noble metal (Sn) interconnection tabs using the electrically conductive adhesives. Contact resistance measurements were performed and the results of this testing are illustrated in the figure above. The graph clearly shows that the new conductive adhesives designed for compatibility with non-noble interconnects (samples A, E, F) exhibit stable electrical contact between ITO and a Sn termination through 1000-hours of 85°C/85%RH exposure.

All of the other adhesives that were tested were unable to provide a stable electrical contact resistance.

As the electrically conductive adhesives are processed at temperatures significantly below the melting temperature of traditional SnPb and lead-free SnAg solders, the reliability data from this report indicate that electrically conductive adhesives containing new corrosion inhibitors are a viable alternative to solder interconnections for applications requiring low-temperature processing.

These results are very encouraging for the photovoltaic market sector, as manufacturers can now incorporate a low temperature process into their operations without risking any performance sacrifice. Henkel's Hysol ECCOBOND CE 3103WLV is the ideal answer to address the requirements of next-generation solar cell manufacture.

For more information on Henkel's complete line of solar cell adhesives, please call Henkel at 949-789-2500 or visit www.henkel.com/electronics. ◆

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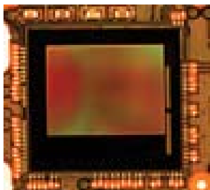

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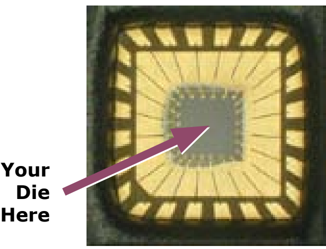

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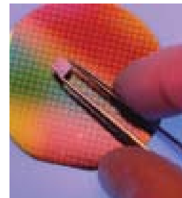

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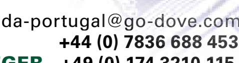

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4 EASTER DAY	5	6	7	8	9	10
11	12	13	14 **SUNNYVALE MEPTEC LUNCHEON** Biltmore Hotel Santa Clara, CA	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	1

MAY 2010

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
2	3	4	5	6	7	8
9 MOTHER'S DAY	10	11	12	13	14	15
16	17	18	19 **MEMS INDUSTRY GROUP METRIC 2010** Wyndham Hotel San Jose, CA	20 **MEPTEC MEMS SYMPOSIUM** Wyndham Hotel San Jose, CA	21	22
23	24	25	26	27	28	29

JUNE 2010

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
30	31 MEMORIAL DAY	1 **ECTC 2010 - 60th ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE** June 1 - 4, Paris Las Vegas, Las Vegas, Nevada	2	3	4	5
6	7	8	9 **SUNNYVALE MEPTEC LUNCHEON** Biltmore Hotel Santa Clara, CA	10	11	12
13	14	15	16	17	18	19
20 FATHER'S DAY	21 SUMMER BEGINS	22	23	24	25	26
27	28	29	30			

Semiconductors to Solar – Packaging Challenges and Issues

Seth Alavi, President
SunSil, Inc.

Almost fifty years ago, semiconductors created a high technology renaissance, which has forever changed the lives of people around the world. Take the mobile phone; in the remote locations where no telephone landlines were available (or practical), a mobile phone tower provided the means of communications. Needless to say, the positive contributions of semiconductors to our daily lives and its impact to the well-being of mankind has been nothing short of spectacular.

Solar and renewable energy sources are the new evolution in the field of electricity production enabling a cleaner, greener and a decentralized source of electricity. Vast regions of the world currently not equipped with centralized energy sources (power plants, power lines & etc), can now benefit from localized energy sources. For the purpose of this article we will focus on Photo Voltaic (PV) solar energy. PV solar energy has the potential to provide 50% of worlds' electricity needs today.

PV devices are simple PN junction semiconductor devices, albeit much larger with at times more stringent reliability requirements. The demanding ambient conditions, such as high heat, stress and humidity, pose a unique challenge to the PV systems. PV modules have been compared to integrated circuit packages – the module being the package, and the cables being the leads and the interconnections.

An integral part of the PV system, the invertors, are comprised of many discrete (ie: capacitors) and ICs. Today's inventor technology is unable to withstand the stringent long term reliability requirements. Hence some believe invertors to be the "weakest link" in the reliability chain, having ten times lower reliability than the rest of the PV system.

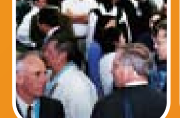
As the semiconductor industry has advanced and matured over the last half century, invaluable experiences in improving long term reliability has been obtained and can be applied to the PV solar industry. A good example, are semiconductors designed for "harsh environments", such as space applications or under the hood of a car in extreme cold or hot conditions. The same approaches and techniques are now rapidly being applied to the PV solar industry.

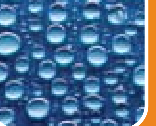
Additional expertise being transferred from semiconductor industry to the PV solar industry include: 1) Low cost manufacturing: key to future competitiveness of solar industry, 2) Optimized assembly processes: for improving reliability & reducing the overall costs, 3) Thermal management: a major factor in modules' long term reliability, and 4) Optimum designs.

Another area of great importance to PV solar industry is Standardization, Technology/Reliability roadmaps and Specifications. Again, semiconductor related organizations, such as SEMI and JEDEC have long been active in setting the standards and promoting uniformly accepted specifications. While other organizations such as SIA or SEMATECH have helped define the technology/reliability roadmaps. These same groups are now becoming more active in the solar related fields and they see the need to assist this "young" industry improve its efficiency and reliability while lowering the costs.

As semiconductor packaging engineers and experts, especially those in North America, we face a shrinking demand in semi related activities and yet a thriving market for solar related projects exists. Hence we are being pulled into the direction of solar at a lightening pace!

Currently there are over 200 companies in Silicon Valley alone researching and manufacturing products related to the solar industry. The buzz in the valley generated from the solar industry is very similar to the buzz generated to the semiconductor industry almost 50 years ago. The excitement is contagious and the future is bright! ◆





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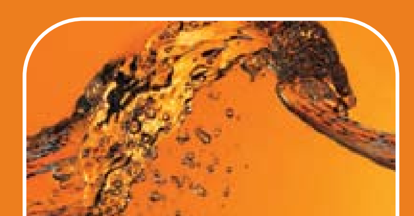

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