MEPTEC report
Volume 8, Number 1
QUARTER ONE 2004
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

SPEL SEMICONDUCTOR LTD. announces the appointment of **Anna Gualtieri** to Vice President of Sales & Marketing. *page 12*

DYNALOY, INC. has announced that it has begun construction of a dramatically expanded new facility for production, warehousing and shipping. *page 14*

ASYMTEK has earned the ISO 9001:2000 Quality Management System certification. *page 14*

CARSEM offers SiP solutions using their MLP (micro Leadframe Package. *page 17*

STATS offers "green" Flip Chip Land Grid Array package for height sensitive wireless applications. *page 17*

TECHNOLOGY

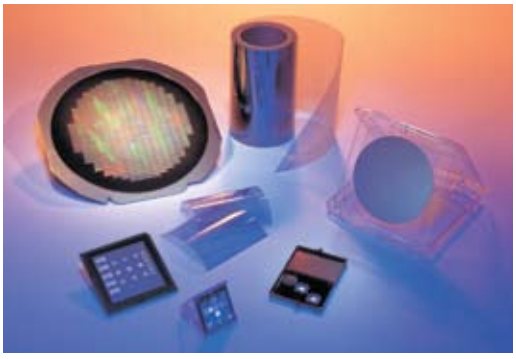
Vada Dean reports on **Celerity Research**'s new wafer sort technology in *"Wafer Sort Meets the Fab Roadmap"*. *page 21*

Charles DiLisio of **D-Side Advisors** discusses the *"New Opportunity in the Value Chain"*, and how SATS firms have an enormous opportunity to capture new

APEX 2004 Exhibition & Conference, co-located with the IPC Printed Circuits Expo, will be held February 24th - 26th at the Anaheim Convention Center, Anaheim, CA.

Courtesy of Sandia National Laboratories

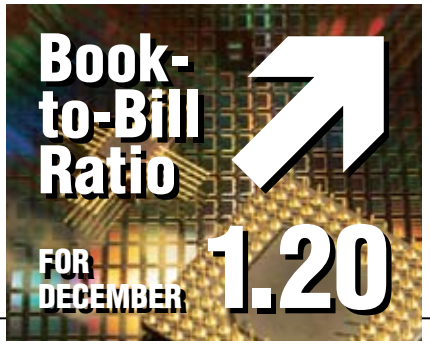
MEMBER COMPANY PROFILE



At the heart of their unique product line is GEL-PAK's proprietary GEL material, an elastomer that provides a tacky surface that securely holds fragile parts in place during transport. The GEL-PAK products provide significantly more device protection than a traditional waffle pack or chip tray and without the need for pockets or cavities.

GEL-PAK has met the growing demands of device manufacturers by offering in-depth product customization and quick turnaround backed up by a worldwide network of sales support. With President and CEO Jeanne Beacham at the helm since her management buy-out in 1997, GEL-PAK, an ISO 9001:2000 certified company continues to develop enabling products designed for applications where process uniformity and optimum protection of devices is mandatory. *page 18*

Semiconductor equipment bookings increase 33% over December 2002 level. *page 16*



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MEPTEC Council Update

Welcome to the first issue of 2004! We made it through a very challenging year in our industry, but it looks as if an economic recovery is truly now a reality. This is indicated in the article by **MEPTEC** Advisory Board member **Jim Walker** of **Gartner Dataquest**. See page 10 for the good news: Worldwide Semiconductor Capital Spending to Experience Double-Digit Growth in 2004. That's what we like to hear!

We also asked Jim and another MEPTEC Advisory Board member from Gartner Dataquest, **Mary Olsson**, what they felt would be a good industry indicator to report on in our Newsletter. They created one specifically for MEPTEC on the semiconductor equipment market quarterly forecast growth indicators. See page 11 for the first report of this indicator to see where we are now, and watch for fu-ture issues and follow it over the year to see if it hits the mark. We appreciate the support Gartner Dataquest has given over the years and continues to provide.

2003, although challenging, continued to be another growth year for MEPTEC. We steadily maintained and grew our membership, but we really stepped up the pace in terms of events. In addition to our monthly luncheons in Sunnyvale, CA and the Phoenix, AZ area, we held our popular quarterly events. As if 20+ events weren't enough, we added our **Executive Level Membership** (ELM) and programs. See Executive Director **Phil Marcoux**'s column and ELM updates on page 4. We've got a whopping 35 events planned for 2004 – visit www.meptec.org for a full listing. Our first event of the year is one you may be attending as you read this issue: our February 19 event on *"SIPs or SOCs – The Multi-Million Dollar Question"*.

Our next quarterly one-day technical symposium is entitled *"Emerging Technologies: MEMS and Wafer Level Packaging – Leading the Charge for Commercialization of Wafer-Level Packaging"*. This event will be held on May 11, one day preceding another important event, the *"Interconnection Investors Conference"*. See pages 5 and 6 for information on these exciting events.

One of the technical articles in this is-sue was a spin-off of one of our 2003 events: December luncheons in both Sunnyvale and Phoenix. **Vada Dean** reported on **Celerity Research**'s new wafer sort technology, and has provided us with an article on the subject (see page 21).

Another contributed article is by **Charles DiLisio** of **D-Side Advisors**. D-Side Advisors is currently participating in several MEPTEC activities. If you're reading this issue at our February 19 event you will have seen Charles give the keynote speech and lead the analysts panel discussion. His article, on page 22, discusses the *"New Opportunity in the Value Chain"*, and how SATS (semiconductor assembly and test services) firms have an enormous opportunity to capture new profit. Visit www.dside.com for more information on the services D-Side Advisors offer.

In the University News column this issue we profile the **University of Florida**. A couple of our Advisory Board members, **Phil Marcoux** and **Marc Papageorge**, are U of F alumnus, and were instrumental in getting this report for us. See page 7 for in-formation on their radio frequency research, among many other things.

We're please to highlight **GEL-PAK** in our Member Company Profile this issue. They have an interesting story to tell (see page 18). They organized in 1980 due to **Hewlett-Packard**'s need to transport highly fragile devices in a secure manner. "Protecting and transporting the critical materials enabling the world's leading technologies" is their main purpose, and they have really proven themselves as leaders in that arena. We appreciate GEL-PAK's support; they are regular exhibitors at our events, and their National Sales Manager, **Pat Kennedy**, is a MEPTEC Ad-visory Board member.

You will see in place of our usual Editorial in this issue a poignant story about the life and death of long-time industry veteran **Bob Hilton**. Bob passed away on December 18 in a tragic boating accident in his native Australia. Two of his very good friends and colleagues, **Mark DiOrio** of **MTBSolutions** and **Maniam Alagaratnam** of **LSI Logic**, put down their thoughts about this interesting man. Bob was on our Advisory Board, and was the recipient of the MEPTEC Packaging Technologist Award in 2000. The award was a wonderful way to honor this great man, especially with a surprise visit by former CEO of **National Semiconductor**, **Charlie Sporck**, who presented the award to Bob during the luncheon ceremony. See page 30 for Mark and Maniam's reflections. To honor Bob, we'll keep his name in a special placement on the Advisory Board list in the front of each issue.

As always, thanks for joining us! ◆

From The Director

Out with Old, In with the New

Of course we all get to do some reminiscing this time of the year. For many of us that means cleaning out our e-mail boxes with the chance to relive events, trips, and accomplishments of the past twelve months. We also do this to free enough memory space for the flood of new emails that we get to help us start the New Year.

The past twelve months for MEPTEC have been some of the most eventful in its entire twenty-five year history. We held four successful symposiums: "Packaging, Assembly, and Testing, in RF Technology" in February; "MEMS and Advanced Packaging Technologies: Synergies and Convergence", in May; "Where the Component Meets the Board", in August; and "Packaging Industry Roadmaps: Overcoming Obstacles and Navigating Solutions", in November.

In August, I had the honor of being named Executive Director. In September we launched a MEPTEC Executive Level Membership, or ELM. Our first ELM event, a lunch featuring Dr. Joerg Borchert, Vice President of Infineon's Secure Mobile Solutions Products Division set the stage for a series of follow-up lunches, a Symposium and an Executive Seminar for 2004 that examine the benefits, challenges, and infrastructure for SIPs (System-in-Package).

Our first ELM lunch of 2004, in January, featured Bruce McWilliams, CEO of Tessera who shared with our invited executives the excitement of Tessera's successful IPO in November.

I'm very pleased that a number of companies signed on as charter Executive Level members and look forward to many new members in 2004. Thanks to ASAT, BESI, Tessera, and UltraTera Corporation for their support. We also formed our Ad-visory Committee for the principal event for the Executive Level members, the Interconnections Investors Conference, scheduled for May 12, 2004 in Santa Clara (see information on page 6).

Our plans for 2004 are aggressive as we continue to try to respond to the wishes of our members. We again have planned to hold four Symposiums. These will be held at our new location, the Santa Clara Westin. Our Q1 Symposium, "SIPs or SOCs, the Multi-million Dollar Question" is scheduled for February 19, 2004. Our Q2 Symposium, "Emerging Technologies: MEMS and Wafer Level Packaging – Leading the Charge for Commercialization of Wafer Level Packaging" will be held on May 11 (see information on page 4), the day preceding our Interconnections Investors Conference.

Get that e-mail from 2003 cleaned out so you have adequate space for all of the announcements from MEPTEC for 2004!

Looking forward to a great year,

Phil Marcoux
Executive Director
MEPTEC

ELM Update

On October 28, 2003 Richard McCarthy, California Seismic Safety Commission, spoke to a group of MEPTEC executives at a luncheon that was sponsored by the State of California and San Jose State University Mr. McCarthy and Prof. Guna Selvaduray of SJSU approach-ed MEPTEC to put this joint session to-gether. Over 20 executives were in attendance.

Mr. McCarthy gave a brief introduction about the role of the California Seismic Safety Commission and history of the seismic threats in our region. He presented to the group issues of earthquake risk reduction for the Silicon Valley Business Community. He is interested in bringing high-tech companies together with the Commission & CDM to help develop legislation to help small businesses lower their earthquake risk in California.

The guest executive for the December 5, 2003 MEPTEC ELM luncheon was Ivor Barber, Director of Product Development for LSI Logic. Ivor spoke about LSI's ongoing investigations and interest in SIP (System-in-Package) as an option for some LSI's new product plans. He provided the group of invited and member executives some very thought provoking pros and cons about his companies use of SIPs. He also told us that they had questions as to who are the best resources for them to use as manufacturers for their products once they decide whether to pursue the SIP path as a compliment to their present SOC technologies.

The first ELM luncheon of 2004 was held on January 12 and featured Bruce McWilliams, CEO of Tessera. Bruce spoke about Tessera's successful IPO in November. The February ELM luncheon featured Charles DiLisio, President of D-Side Advisors, speaking on Understanding Profitability, Value and Growth. Topics covered were the changing semiconductor market, slipping value, and SATS companies as profit centers.

For more information about MEPTEC ELM events and membership, e-mail Kim Barber at kbarber@meptec.org, Phil Marcoux at pmarcoux@meptec.org, or visit the our web site at www.meptec.org. ◆

MEPTECPresents

MicroElectronics Packaging and Test Engineering Council

A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

May 11, 2004 • The Westin Santa Clara, Santa Clara, CA • 9:00 a.m. - 5:00 p.m.
Table Top Exhibits 11:00 a.m. - 7:00 p.m. • Reception 5:00 p.m. - 7:00 p.m.

Converging Technologies: MEMS and Wafer Level Packaging

MEMS – Leading the Charge for Commercialization of Wafer Level Packaging

MEMS industry trends have historically lagged those of its big brother the IC industry, especially with regard to "Moore's Law parameters," such as de-creasing lithographic feature size and die size, and increasing wafer size. However, in packaging, the tables have turned as the MEMS industry is now leading the IC industry towards true wafer scale packaging.

While WLP has long been the ultimate target of many IC packaging roadmaps, it has not yet be-come pervasive. For ICs, it has been argued that WLP fails to meet the ever increasing demands for extreme functionality in very space-constrained applications such as mobile phones. In the case of MEMS, however, the need for WLP is driven by the fundamental need to encapsulate delicate mech-anical components at the wafer level before any assembly processes. Enclosing and protect-ing MEMS in the fab is critical to reducing cost, in-creasing yield, and improving reliability. Wide-spread adoption of WLP is expected to propel MEMS into many cost-sensitive high-volume mar-kets, including mobile telephones, inexpensive medical diagnostics, and consumer electronics.

This one-day conference brings together respected professionals in the fields of MEMS and Wafer Level Packaging to emphasize new tech-nologies, applications, and industry trends. The next decade will see a blurring of the boundary be-tween fab and packaging, and present compel-ling opportunities for the entire value chain, from equipment and packaging suppliers to device and product manufacturers. This is a fantastic opportunity for Advanced Packaging and MEMS professionals to come together and explore syn-ergies that will enable the convergence of these technologies, propelling both into the future.

Sessions will include:

- Technology Overview
- Enabling Technologies
- Assembly Processes
- End User Applications/Future Trends

Some of the topics to be covered

- Trends and Roadmaps
- Low Temp Wafer Bonding/Wafer Bonding Technology
- One-step Electrochemical Processing
- Microprocessing of LCOS
- Display Packaging
- Lab-on-a-Chip
- Thermal Issues
- Hermeticity
- Wireless Sensors
- Chip Cooling
- Pressure Sensors
- Wafer Level Micro Packaging
- Biomedical Issues

REGISTER NOW!

To register by phone, or for more information about this and other MEPTEC events, contact Bette Cooper at 650-988-7125, email bcooper@meptec.org or visit the MEPTEC web-site.

Ask Us About Exhibiting at This Event!

Held at The Westin Santa Clara in conjunction with the May 12th MEPTEC Interconnections Investors Conference

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MEPTEC Presents

MicroElectronics Packaging and Test Engineering Council

The First Annual

Interconnections Investors Conference

For Semiconductor Assembly & Test Services

Wednesday, May 12, 2004 • The Westin Santa Clara, Santa Clara, CA
9:00 a.m. - 5:00 p.m. • Reception 5:00 p.m. - 7:00 p.m.

The First Annual Interconnections Investors Conference will bring to-gether investors, analysts, large end customers and growing semiconductor interconnection companies to gain a better appreciation for the financial opportunities in the Semiconductor Assembly and Test Services (SATS) industry. SATS companies include substrate, package assembly and electrical test suppliers serving what is commonly called the back-end of the semiconductor industry.

SATS companies represent the fastest growing segment in the semiconductor industry. Some have an-nounced that they will double revenues this year and need expansion capital. SATS companies as a group have a largely undeveloped foundation in the world's capital markets.

MEPTEC, the leading industry group representing the SATS and the Semiconductor Interconnection Industry is producing the first Interconnections Investors Conference in Silicon Valley, at the Westin Santa Clara Hotel on May 12, 2004, to introduce these companies to the U.S. Capital Market, and to potential end customers.

Who Should Attend?

The attendees at this Conference will be representatives from large outsourcing companies, institutional and large private investor groups, and capital companies, as well as other companies that serve the semiconductor interconnection industry.

Presenting Companies and Organizations

The Presenters will be leading industry analysts, publicly traded and late stage established SATS and interconnection companies. The selected SATS Presenters will be companies with promising semiconductor interconnection, IP, material, test, and packaging businesses and technologies.

Conference will include:

- Keynote Address by Satya Chillara, Senior Semiconductor Analyst for W.R. Hambrecht and Company
- An Overview of the IC Interconnection Industry
- Understanding SATS Profitability Outlook
- Analyst Speakers
- Presentations by SATS Companies
- Reception

Held at The Westin Santa Clara in conjunction with the May 11th MEPTEC Converging Technologies: MEMS and Wafer Level Packaging Symposium

Register Online at www.meptec.org

MEPTEC *Join Us!*

University of Florida Wireless Interconnect

High-frequency CMOS is changing the future of wireless

Martha Dobson
Editor
The Florida Engineer Magazine
College of Engineering

Electronics engineers at the University of Florida made news around the world in 2000 when they were the first to send a wireless signal across a microchip. Professor Kenneth K. O and his research team from the Silicon Integrated Micro-wave Circuits and Systems Laboratory (SiMICS) placed a radio transmitter and antenna on a standard silicon chip. The radio transmitted a clock signal a distance of 22 mm across the chip to a re-ceiver.

The system, developed for the Semiconductor Research Corporation, was a step beyond placing antennas on processor boards, as is done in wireless LANs. The antenna was on the chip itself, as part of the integrated circuit. The use of RF signals makes transmitting information across a chip less problematic, im-proving speed and accuracy, and eliminating signal distortion.

The wireless chip was a significant breakthrough for UF's Electrical & Computer Engineering department, which has a long history of RF electronics research. The system was the result of O's research into the use of CMOS technology to make faster, better, and cheaper RF integrated circuits. CMOS had been considered a low-frequency, or slow, technology. O's research has shown that CMOS technology can reach frequencies of 5 GHz, even 20 GHz. "Now we are talking about 100 GHz. When I say that we can have 100 GHz circuits, people do not even flinch," O says.

Currently, O and his team are developing the next generation of their single chip wireless system. The new version will be a single-chip radio about 3 mm by 3 mm in size. Called mnode, the chip will include the antenna, the transmitter, the clock that times it, and the power source. It will be disposable and able to communicate up to about 5 meters away.

Dr. O is standing between test platforms for his on-chip antennas. These 3mm antennas can broadcast out to 15m.

The single-chip radio project is being sponsored by DARPA and carried out in cooperation with Motorola Labs, in Plan-

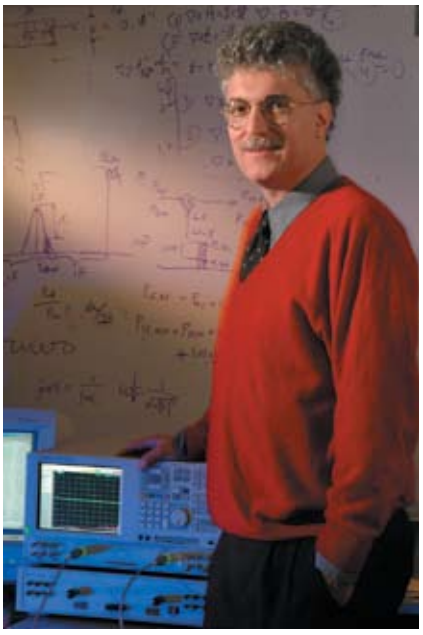
tation, Florida. Two additional factors must come into play to make the chip practical. First, the radio needs a power source. Right now, an external power connection is the likely solution. In the near future, however, the radio may be powered by a thin film battery integrated into the chip. Second, the crystal timing device has to be integrated into the chip. Motorola Lab is working on this as a subcontractor on the 3-year, $3.5 million project from DARPA.

As the devices get smaller and faster, the power supply voltage will also decrease. A disposable radio will need to function at low voltage, so this area is also being studied by the RF team. The team is working on power circuits of .1 to .3 volts, far lower than the 3 volts used by cell phones.

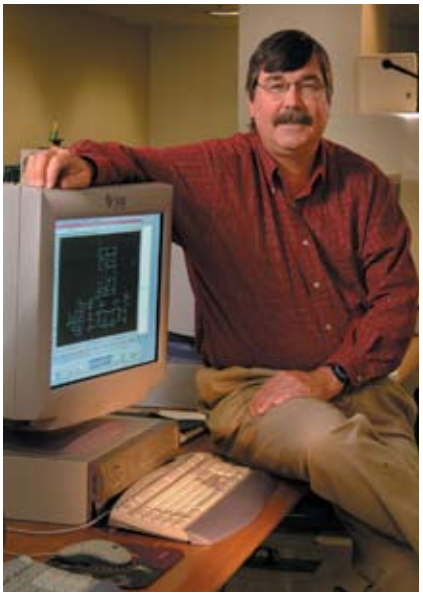
A separate, but highly relevant, research area for the RF team is multi-standard, multi-frequency band radio communications. Radio applications now use different frequency bands, standards, and protocols around the world. Global wireless interconnect will require cross-protocol accessibility and concurrent operations on more than one band. Another research effort, led by Associate Professor Jenshan Lin, is the development of very small, 2 x 2 mm, RF ID tags with the potential to broadcast a distance of up to 10 meters.

The electronics industry is making use of the high-frequency CMOS technology SiMACS has developed. SiMACS students are now working with companies on products that use CMOS, including Texas Instruments, RF Micro Devices, and Intersil. The ECE department has a unique connection with Intersil (now part of Conexant), a Palm Bay spinoff of Harris, which dominates the wireless LAN market. Intersil sponsored a PhD student whose mission was to do their RF CMOS research work as the basis for his dissertation. The collaboration was highly successful, and was an important factor in the company switching its manufacturing of newer generations of radios to CMOS technology.

High-frequency, single-chip systems like those being developed at UF have complex, mixed-signal circuit designs. These systems-on-a-chip (SoCs) will need to be debugged in the design phase and will need expensive RF testing in the production phase. Critical RF and analog circuit nodes in such ICs often are unobservable and uncontrollable by today's test techniques. The inability to observe and control circuit nodes will result in more design iterations, slower time from design to market, and inadequate manufacturing test coverage. Production tests will be difficult, slow, and expensive.



Dr. Eisenstadt is using some some of the advanced high speed testing equipment to characterize performance of mixed signal IC's.



Dr. Fox is with one of the stations used to design mixed signal testing circuits placed in the die lines of integrated circuits.

Without new test developments, the manufacture of complex mixed-signal/RF chips may be possible but testing procedures may make them too costly to sell. The semiconductor industry has a pressing need for improved mixed-signal/RF testing during IC production. The testing solution must satisfy the needs of both production engineers and IC chip designers.

On-chip testing of RF/mixed-signal SoC systems is a new test area. Virtually all existing on-chip test work focuses on digital and analog baseband circuits (typically ADCs). Associate Professors Will-iam Eisenstadt and Robert Fox in ECE's Electronics Circuit Laboratory are ex-ploring new testing techniques to im-prove on-chip observability and controllability in microwave/RF ICs and SoCs.

Eisenstadt and Fox have demonstrated a number of new circuits for embedded test mixed-signal ICs. They include compact signal generation circuits, 5 GHz signal sampling circuits and 5 GHz peak and RMS signal detection circuits. Currently, the research is looking towards using these circuits for on-chip transceiver testing and for oh-chi substrate noise testing.

The research has several goals:

- To create a cost-effective strategy for a built-in, self-test of complex RF/mixed-signal systems.
- To design and qualify embedded test circuits that can be added to a RF/microwave transceiver architecture.
- To demonstrate greatly improved circuit test coverage of RF and analog embedded IC circuit nodes.
- To benchmark these new embedded test strategies with existing analog/RF transceiver test practices and present cost/performance tradeoffs.

Radio frequency research is just a portion of ECE's activity in electronics. ECE's chairman, Professor Mark Law, says, "The electronics area of our department is one of our leaders and a focus area of growth. We hope to build on these success stories in the future." ◆

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Robert M. Fox

FROM WIRELESS INFRASTRUCTURE TO HANDHELD DEVICES

Wireless connectivity is fast becoming the standard for communication. The demand for devices with increased functionality, smaller form factor, and lower power consumption is unrivaled. Developing and manufacturing such a device is a challenge.

From silicon to system level integration, STATS can assist you in identifying a cost effective solution with ideal performance for your wireless application. Our design capability, package characterization, advanced semiconductor packages ranging from super low profile to high density interconnect, immense test capability with vast wireless product knowledge, manufacturing services and robust e-business infrastructure provides you with a competitive advantage in developing and delivering your new wireless product to market on time.

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- Distribution

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Worldwide Semiconductor Capital Equipment Spending to Experience Double-Digit Growth in 2004

Jim Walker
Principal Analyst
Semiconductor Packaging and Assembly Service
Gartner Dataquest

As we begin 2004, worldwide semiconductor capital and equipment spending will see a continuation of strong acceleration in billings and bookings that gained momentum during the second half of 2003.

Worldwide semiconductor capital spending is projected to grow 28 percent in 2004 to $37 billion, up from $28.9 billion in 2003 (see Table 1). Worldwide capital equipment spending is expected to total $29.5 billion, a 36 percent increase from 2003 revenue of $21.7 billion. The worldwide capital equipment market includes wafer fab equipment (WFE), packaging and assembly equipment (PAE) and automated test equipment (ATE).

The semiconductor industry will be firing on all cylinders in 2004. The return of a corporate investment cycle, a PC upgrade cycle, and demand for port-able and wireless products are all contributing to increased growth. These factors, coupled with a broad-based recovery in end-user applications, low inventories and tight manufacturing capacity all are converging to provide for strong growth in all equipment segments.

Although semiconductor demand continues to increase, inventories remain at healthy levels and average selling prices (ASPs) are stabilizing, device manufacturers remained cautious in 2003 as capital spending remained stall-ed near the levels reached in 2002, ex-cept for packaging and assembly equipment.

Thus this combination of cautious investment and rising production has driven utilization rates upward across the board in recent months. Gartner estimates that 2003 will have ended with worldwide utilization around 90 percent and leading edge utilization in excess of 95 percent. This trend should continue through 2004 and well into 2005 as manufacturers become more comfortable by investing heavily in response to increased end market demand and improved profitability.

	2002	2003	2004
Semiconductor Capital Spending	27,393	28,943	37,109
Growth (%)	-38.5	5.7	27.9
Capital Equipment (Including Test)	20,715	21,742	29,544
Growth (%)	-29.0	5.0	35.9
Wafer Fab Equipment	16,203	16,464	2,071
Growth (%)	-31.5	1.6	34.1
Packaging and Assembly Equipment	2,344	2,922	4,023
Growth (%)	-21.6	24.7	37.7
Automated Test Equipment	2,168	2,356	3,450
Growth (%)	-14.9	8.7	46.4

Source: Gartner Dataquest (December 2003)

Table 1. Worldwide Semiconductor Capital and Equipment Spending Estimates (Millions of US Dollars

These high utilization levels will drive the growth in the wafer fab equipment (WFE) market in 2004. The WFE market is projected to grow 34.1 percent in 2004 to $22 billion, up from $16.4 billion in 2003. The industry needs more capacity if it is to continue meeting increased device demand. However, running a fab at high utilization rates leads to high margins and profits, something the industry has not seen much of for the past few years. This can result in semiconductor manufacturers playing a risky game – maximizing profitability on minimum assets while assuming they can wait until the last minute to commit resources for new capacity.

While the front-end fab of manufacturing was dormant, the back-end was not. As in previous industry recoveries, packaging and assembly served as a "leading indicator" of a possible industry turnaround. It showed improvement months before other portions of the semiconductor industry. While the overall semiconductor industry remained flat, the semiconductor assembly and test services (SATS) market experienced positive, double-digit growth in 2002. This was then followed by the growth in packaging and assembly equipment in 2003.

Because advanced packaging demand has been growing significantly in the past year and capacity is tightening, the packaging and assembly equipment (PAE) market will continue on this growth curve. Throughout the year 2003 orders for PAE have increased. Driving this growth has been the demand for CSP and BGA packages, along with the continued transition to flip chip for higher-end, performance-based applica-

tions. The strong demand in Q3 led us to in-crease our forecast to just under 25 percent growth in PAE for 2003 to $2.92 billion. This growth is welcome news after the decline of 22 percent in 2002, which followed the negative 55 percent contraction in 2001. For 2004, we see even more improvement, as PAE reaches over $4 billion in revenue with a growth nearing 38 percent.

After two years of dismal industry conditions and sharply negative market growth, the ATE market is finally poised for an upturn. The entire market sank during 2001 and 2002, and no market segment was left untouched. 2003 mark-ed the turn for ATE market revitalization. Given the improved market de-mand for devices, ATE investment budgets have ramped back up in 2003, providing for the first positive growth in several years, estimated to reach 8.7% for the full year. By 2004, market grow-th will shoot significantly upward and will continue to grow through 2005. Overall, the worldwide ATE market is projected to grow at a compound annual growth rate (CAGR) of approximately 13.2 percent through 2008. However, the ATE market still won't return to its levels reached in the year 2000.

Thus for 2004, global capital spending is expected to increase by 28 percent. However, due to the cyclic nature of the industry, the question will again be: Can orders for new equipment be released fast and early enough to avoid shortages in the device market? While we have seen encouraging increases in the order rate for new equipment in the past few months, the memories of the exuberance of 2000 and the pits of 2001 still remain. There is still a question as to whether the equipment industry can respond fast enough to the anticipated demand for new equipment. However, this industry has proven time and time again that it can rapidly ramp its ship-

Semiconductor Equipment Market Q1 2004 Forecast Growth Indicators

A "where are we now" glance at the electronics industry in the first quarter of 2004 is shown in the table below. This projected outlook is based on several current values/trends and indicators, including government economic forecasts and selective statistical data. Market conditions for electronics vendors and users entered the early stages of an expansion period in 2H 2003. This ex-pansion period is marked by two phases:

Phase I: 2H 2003 to Mid/Late 2004

- Contract pricing improves in volume driven commodity components (DRAM, Analog, and discretes)
- Manufacturing capacity tight in some categories. Lean inventories and solid demand return profitability to the materials and device industry.
- Device vendors expand in a "controlled" fashion
- Cellular phone handset manufacturers report continued strong demand
- Package/Assembly and Automated Test Equipment bookings were strong exiting 2003.
- Worldwide sales of semiconductors rose to $166.4 billion in 2003, up 18.3 percent from the $140.8 billion in global revenue recorded in 2002, according to the Semiconductor Industry Association (SIA) February 2004 report.
- According to SIA the industry recorded an 11 percent sequential revenue increase to $ 48.1 billion in the fourth quarter of 2003 from $43.3 billion in the third quarter, and a 28 percent rise in year-over-year revenue in December of 2003.

Phase 2: Late 2004 through 2005

- Continued end-user demand with spot shortages drives the return of the industry's historical spending patterns. Double digit growth of over 11 percent in semiconductor revenue in 2003 now boosted to over 20 percent in 2004.
- Stronger geographic markets and improved global economies should boost chip sales in the final quarter of 2004, driving revenue above 24.
- PC replacement cycle has begun and includes the following forecast from Gartner Dataquest:

		Growth
2003	**$164.2 Million**	**10.8%**
2004	**$185.2 Million**	**12.8%**

Revenue Growth (%)	2003	2004
	Base	Base
World GDP	+2.5	+3.7
U.S. GDP	+3.0	+4.7
Electronic Equipment*	+3.8	+7.5
Semiconductor	+11.8	+20.1 to 24
Capital Spending	+5.7	+27.9
Equipment Spending	+5.0	+35.9
Wafer Fab Equipment	+1.6	+34.1
Packaging & Assembly Equipment	+24.7	+37.6
AT Equipment	+8.7	+46.4
Silicon Ship (MSI)	+9.1	+15.4

* Production Revenue

Source: Gartner Dataquest

Quarter 1 2004 Forecast Growth Indicators.

Henkel Technologies Promotes Muni to Global Business Manager for Semiconductor Packaging

CITY OF INDUSTRY, CA – Henkel Technologies has promoted Bhavesh H. Muni to a new position as Global Business Manager, Semiconductor Packaging. Mr. Muni will oversee North American marketing and sales for the semiconductor market, and will lead the company's packaging business efforts for this product niche.

Mr. Muni brings to his new position more than 15 years of sales and R&D experience in electronics packaging and assembly. He most recently service as Henkel's Global Marketing Manager for Semiconductor Packaging, where he worked with customers to develop next generation semiconductor packaging and thermal management materials. Mr. Muni holds a M.S. in Polymer Science from the University of Detroit, and a B.S. in Chemical Engineering from Regional Engineering College in Srinagar, India.

Visit www.loctite.com/electronics for more information.

SPEL Announces Anna Gualtieri as New VP of Sales & Marketing

SPEL Semiconductor Ltd is pleased to announce the appointment of Anna Gualtieri to Vice President of Sales & Marketing. In June 2003, Ms. Gualtieri accepted the position and joined SPEL's team. Anna Gualtieri comes to SPEL with over 23 years experience in the Semiconductor Industry. Prior to SPEL, Ms. Gualtieri has spent 17 years at packaging subcontractors. She is also a mem-ber of the MEPTEC Advisory Board.

"Based on her industry experience and enthusiasm, Anna is a welcome addition to SPEL", remarked SPEL CEO Sam Varghese.

SPEL Semiconductor Ltd is an Assembly & Test Subcon located in Chennai (Madras) India. SPEL has been serving the Semiconductor Industry since 1988.

For additional information, please visit the SPEL website at www.spel.com.

Dynaloy Promotes Diane Scheele to Director of Technical Services

Dynaloy, Inc., an international manufacturer of engineered chemical solutions for multiple industries and applications, has an-nounced that Diane Scheele has been promoted to Director of Technical Services, effective January 2, 2004.

"With the product development and technical needs of our business segments rapidly accelerating, Diane's skills and background will continue to be an invaluable asset to us," said Donn Detzler, President of Dynaloy.

Ms. Scheele continues to bring to Dynaloy over 15 years of experience in the development of specialty materials for the automotive, industrial and microelectronics in-dustries. Ms. Scheele has a B.S. degree in polymer chemistry from Penn State University.

For More Information Contact Donn Detzler or Charles Haywood at Dynaloy, Inc., 1535 E. Naomi Street, Indianapolis, IN 46023, Tel: 317-788-5694, Toll-Free (US Only) 800-669-5709, Fax: 317-788-5690, www.dynaloy.com, info@dynaloy.com.

Honeywell Electronic Materials Announces Oliver Shon as New Greater China Sales Leader

SUNNYVALE, CA – Honeywell Electronic Materials has announced that Oliver Shon has joined the organization as the new Greater China Sales Leader. Mr. Shon brings over 20 years of extensive experience in the Chemicals industry. Most recently, he was the General Manager of Ashland Taiwan Co. Ltd. Under Mr. Shon's leadership, Ashland Taiwan Co., Ltd. was recognized as the top-performing region in the Ashland Chemicals group for the past three years. Prior to his tenure at Ashland, Oliver held various leadership positions at Luxchem Polymer Ind. (Malaysia), Arindo Chemical Indonesia and Qualipoly Chemical Corp., Taiwan.

"We are excited to welcome Oliver Shon to Honeywell Electronic Materials. Mr. Shon's industry experience, leadership capabilities and passion to serve customer needs will enable him to make significant impact immediately," commented Rick Widden, Director of Global Sales, Marketing & Business Development for Honeywell Electronic Materials. "Oliver will be focused on strengthening our position in Taiwan and implementing our strategy to support the emerging market in China by delivering outstanding service and value to our customers," continued Widden.

Mr. Shon holds a MBA from Pacific Western University, USA and a Bachelor's degree in Chemical Engineering from the Chenshiu Junior College of Technology, Taiwan.

For additional information, please visit www.electronicmaterials.com.

Nordson/Asymtek China Promotes David Wang and X.Q. Gao

CARLSBAD CA – Nordson/Asymtek China has announced the appointments of Mr. Wang Tian-bo (David Wang) as Regional Sales Manager and Xueqiang ("X.Q.") Gao as Applications and Field Services Engineer, based at Nordson Shanghai in Pudong. Wang and Gao's primary responsibilities are to provide direct support for distributor sales and service personnel in mainland China. Both management moves ensure Nordson/Asymtek customers will receive continued satisfaction through high quality support and service.

Wang brings an extensive global perspective to Nordson/Asymtek, with more than ten years of industry and management experience with Loctite in China and Singapore. As Regional Sales Manager, his priority is to identify new opportunities in the territory to help customers achieve their dispensing goals. Wang received an MBA degree in Engineering from China Europe International Business School (Shanghai CEIBS), and held various key positions in the electronics and automotive industry before joining Loctite. He reports to Glen Gibbs, Asymtek's Asia Pacific General Manager.

In Gao's new position as Applications and Field Service Engineer, he is responsible for field service and applications support in the Nordson Shanghai lab. Prior to his appointment with Nordson/Asymtek, Gao held positions with AMD China, K&S China, and ESE, a local distributor of Nordson/Asymtek

products. Gao received his B.S. degree in Electrical and Mechanical Engineering from the Nanjing University of Science and Technology.

Celebrating 20 years of success in 2003, Asymtek supplies award-winning automated fluid dispensing systems to customers worldwide. Specializing in semiconductor, surface mount, and electronics packaging applications, they are committed to providing total dispensing solutions and local support. Find out more on their Web site at: http://www.asymtek.com.

STATS China Plant Ready for Operations

Shanghai facility offers STATS' industry leading mixed signal test services

SINGAPORE and MILPITAS, CA – ST Assembly Test Services Ltd. (STATS), a leading independent semiconductor test and advanced packaging service provider, today announced that its Shanghai manufacturing facility is ready for operations. Located in Pudong, STATS' new facility offers wafer probe and final test services to cater to the growing mixed signal market in China.

Tan Lay Koon, STATS President and Chief Executive Officer, said, "We have opened in record time our first manufacturing facility in China to meet immediate market demand for mixed signal and high-end test services. With this strategically located facility, we are able to provide our world class products and services to one of the fastest growing semiconductor markets in the world. Apart from supporting indigenous foundries and design houses, this facility also allows STATS to serve existing customers expanding into China on a first-to-market, cycle-time driven basis."

On September 3, 2003, STATS announced that Semiconductor Manufacturing International Corporation (SMIC), China's most advanced pure-play foundry, is utilizing its Shanghai facility to perform initial and final testing of its mixed signal devices. Following the opening, existing engagements with SMIC will be transferred to STATS' Shanghai facility.

First announced in July 2003, this new test facility gives STATS a strategic foothold to participate in China's growing outsourcing business and a geographical base to support its global customers who require turn-key services in China.

Further information is available at www.stts.com

Asymtek Appoints Smart Technology (SmartTec) New Distributor in Europe

CARLSBAD, CA – Asymtek has added a new distributor, SmartTec (smart technology products and solutions), to represent their line of automated fluid dispensing systems in Germany and Austria. As a new system supplier for the electronic industry, SmartTec provides Asymtek's customers with on-site equipment service, training and applications support. The combined long term experience of SmartTec's founders in the electronics

manufacturing industry and their relationships with international suppliers make them an excellent resource for Asymtek's customers.

"SmartTec is well acquainted with dispensing and coating technologies, and has always demonstrated a strong commitment to customer service," explains Michel van de Vijver, Nordson Europe's Sales and Marketing Manager. "We are pleased to have them join our growing team of sales representatives."

For more information about SmartTec, contact their headquarters at 06103-30127-0 or visit www.smarttec.de.

Celebrating 20 years of success in 2003, Asymtek supplies award-winning automated fluid dispensing systems to customers worldwide. Specializing in semiconductor, surface mount, and electronics packaging applications, they are committed to providing total dispensing solutions and local support. Find out more at www.asymtek.com.

Carsem Completes Construction of China Facility

SCOTTS VALLEY, CA – Carsem has announced that they completed the construction of their Carsem-Suzhou Ltd. facility, located in the province of Jiangsu, 50 miles (80 km) west of Shanghai. The new factory is 172K sq. ft. (16K sq. m.) and is located on 430K sq. ft. (40K sq. m) of land in the Suzhou Industrial Park.

The construction started in April 2003 and was completed in January this year. The initial staff was hired during the second quarter of 2003 and extensive training has al-ready begun in Carsem's existing Malaysian factories. The assembly and test equipment to support the manufacture of the MLP (Micro Leadframe Package) Quad and Dual family will be installed during the first quarter of 2004. Customer qualifications will be-gin during the later part of the first quarter and the factory will be in full production by the end of the second quarter of 2004.

David Comley, Carsem's Group Managing Director, stated, "This is a major milestone towards meeting the tremendous growth potential of the China market as well as the rapidly increasing demand for the MLP package family. We have a significant number of key customers that have expressed the need for our MLP assembly and test capability in the China region and we anticipate a very rapid ramp in production volumes this year."

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, Suzhou, China and sales offices across the USA, plus the UK. Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Dynaloy Announces New Facility Construction

Dynaloy, Inc. has announced that it has begun construction of a dramatically expanded new facility for production, warehousing and shipping.

"We have experienced rapid growth in several of our business segments and it became apparent that we would rapidly outgrow our existing facility," said Donn Detzler, President of Dynaloy. "Our microelectronics group in particular is seeing strong growth. Also, we have entered new areas of business and are actively evaluating several acquisitions. The quadrupling of space represented by our new facility will ensure that we are able to meet our customers' needs for years to come."

The new facility will contain state-of-the art production and analytical equipment suitable to meet the needs of Dynaloy's custom-ers in the semiconductor, microelectronics and electronics industries. These will include an ISO Class 8 clean room, specialized monitoring equipment and an advanced inventory-handling system.

Dynaloy anticipates that all operations will be transferred to the new facility by the end of July, 2004.

For More Information Contact Donn Detzler or Charles Haywood at Dynaloy, Inc., 1535 E. Naomi Street, Indianapolis, IN 46023, Tel: 317-788-5694, Toll-Free (US Only) 800-669-5709, Fax: 317-788-5690, www.dynaloy.com, info@dynaloy.com.

Asymtek Achieves ISO 9001:2000 Certification

CARLSBAD, CA – Asymtek announces it has earned the ISO 9001:2000 Quality Management System certification, assuring the highest and most current quality standards for their customers. The certification, based on a comprehensive audit by third party agency Det Norske Veritas (DNV), indicates that Asymtek has successfully revised its quality management system to meet the new requirements of ISO 9001:2000.

Asymtek was assessed and certified as meeting the requirements for design, production, customer service, technical support, sales, and marketing of their automated fluid dispensing systems. "ISO requires that standards are periodically revised to ensure that they are current and satisfy the needs of the global community," explains Martin Stone, Asymtek's Vice President of Operations. "By implementing the necessary internal processes and achieving ISO 9001:2000 status, Asymtek is demonstrating a strong commitment to continual improvement and customer satisfaction."

Find out more on their Web site at www.asymtek.com.

STATS Expands Manufacturing Space in Singapore Facility

Corporate office moves to new location, customer service; assembly and test operations to remain at current facility

SINGAPORE and MILPITAS, CA – ST Assembly Test Services Ltd. (STATS) is moving its Singapore corporate office to a new location, making way for additional manufacturing capacity at its current facility.

Effective November 3, 2003, the move involved close to 200 general administrative and support staff, including sales & marketing, information technology, finance and human resources. STATS' customer service, assembly and test operations continues to be housed at its current manufacturing facility at 5 Yishun Street 23.

STATS' 580,000-sq.ft. facility in Yishun comprises 300,000 sq.ft. of operational space, state-of-the-art manufacturing equipment and a class 10K clean room environment. With the move of its corporate office to a new location, STATS will convert an estimated 45,000 sq.ft. of vacated space for operations purposes.

Dov Oshri, STATS Chief Financial Officer, said, "As we announced at our third quarter earnings, additional production equipment is scheduled to be brought in to support the immediate needs of our customers. We're in a state of readiness to quickly ramp up in response to business de-mand for test and assembly services. With the completion of facilitization works, the equipment can be installed in a relatively short time in step with customer orders and further business growth."

STATS' new corporate office is located at
10 Ang Mo Kio Street 65, Techpoint #05-17/20, Singapore 569059, Main telephone: (65) 68247777, Main fax: (65) 68247776.

Further information is available at www.stts.com

Rodel and Shipley to Change Name to Rohm and Hass Electronic Materials

MARLBOROUGH, MA – Shipley Company and Rodel have announced that they will become Rohm and Haas Electronic Materials, effective February 1, 2004. Rodel and Shipley together comprise the more than $1 billion Electronic Materials business group of Rohm and Haas Company, which delivers innovative material solutions to the electronic and optoelectronic industries.

Pierre R. Brondeau, who heads this business group, said that unifying the Rodel and Shipley names under the parent company name, Rohm and Haas, should make it easier for potential and existing customers to understand the breadth and depth of his business's impact in the global electronics marketplace.

"Our customers will continue to receive the same exceptional advanced technology and service that has established us as a worldwide market leader," said Brondeau. "We remain committed to bringing innovation to the global electronics market and adopting the single Rohm and Haas name will accelerate future growth."

Shipley Company and Rodel make up the more than $1 billion (US) Electronic Materials business group of Rohm and Haas. The organization develops and delivers innovative material solutions and processes to the electronic and optoelectronic industries. Focused on the circuit board, semiconductor manufacturing and advanced packaging industries, its products and technologies are integral elements in electronic devices around the world.

Additional information is available at www.shipley.com and www.rodel.com.

Shipley Company Electronic and Industrial Finishing Division Achieves ISO-9001: 2000 Certification

FREEPORT, NY – Shipley Company, part of the Rohm and Haas Electronic Materials group, has announced that its Freeport, New York, Lucerne, Switzerland and Sasakami, Japan locations have recently achieved certification against the new ISO-9001: 2000 Quality Management System (QMS) standard. The certification of these three sites reinforces Shipley's global commitment to continue to ISO certify its major manufacturing facilities. Other sites with ISO-9001: 2000 certification operate in China, England, Hong Kong, Singapore, and Taiwan.

"We are pleased to continue our ISO certification against the new ISO-9001:2000 standard for our major R&D and manufacturing sites. This achievement is concrete evidence of our commitment to continuous improvement, global customer satisfaction and quality systems," said David Schram, Electronic and Industrial Finishing President, Shipley Company.

ISO-9001:2000 certification provides Shipley the opportunity to publicly validate that processes are in place to consistently produce products that meet customer needs. Its scope is designed around a structured quality management system focused on customers' requirements as related to new product development, measurement, analysis, and improvement.

Additional information is available at www.shipley.com and www.rodel.com.

Asymtek Launches New High-Speed DispenseJet® DJ-9000 Jet

CARLSBAD, CA – Asymtek announces the release of its new DispenseJet® DJ-9000 jet for precise, high-speed delivery of a wide variety of fluids including underfill, surface mount adhesive, encapsulants, conformal coatings, UV adhesives and silver epoxy. Based on the company's award-winning DJ-2100 series, the DJ-9000 is a new generation jet that is faster, easier to clean, and delivers the capabilities needed for today's most advanced production requirements.

Ideal for stacked die and densely packed boards, the DJ-9000 jets in tight spaces as small as 200 micrometers, and creates fillet wet-out widths as small as 300 micrometers on the dispensed side of the die. The DJ-9000 dispenses fluid either as discrete dots or a rapid succession of dots to form a 100 micron (4 mil) diameter stream of fluid from the nozzle. Dot diameters as small as 0.33 mm and shot volumes as small as 3.6 nanoliters can also be achieved. Jetting breaks through many of the barriers of traditional needle dispensing to deliver speed, quality and low cost of ownership, and has proven to be one of the best ways to dispense many fluids. Go to www.asymtek.com for more information .

ASM Announces Levitor RTP Shipment For Implant Anneal to European Customer

BILTHOVEN, THE NETHERLANDS – ASM International N.V. has announced that its subsidiary, ASM Europe B.V. has shipped a Levitor® 4000 Rapid Thermal Processing system for 200 mm wafers to a leading de-vice maker in Europe. The European customer will use the Levitor 4000 to develop implant anneal processes for the 90 nm technology node and will also use the tool for NiSi annealing applications in the temperature range of 200°C to 550°C for future technology nodes.

"The Levitor satisfies the requirements depicted in the ITRS roadmap for critical processes from the present technology node down to the 45 nm technology node," said Ernst Granneman, ASM's Levitor business unit manager. This includes state-of-the-art arsenic and boron-based ultra shallow junctions as well as CoSi2 and NiSi formation. The Levitor 4000 RTP tool's unique concept of heating the wafer distinguishes this system from lamp and susceptor-based systems on the market with respect to process performance, flexibility, low cost per wafer and extendibility.

The process capability of the Levitor in the high temperature regime as well as in the low temperature regime, particularly below 400°C, qualifies the system for development in present and future technology nodes. In addition, the capability to perform spike pro-cesses in the full temperature regime provides solutions not accessible for conventional lamp-based heating systems.

The Levitor 4000 is based on a floating wafer principle where a wafer, confined between two massive hot blocks, is heated through conduction. The gas layer between the wafer surface and reactor blocks self-centers the wafer and keeps it floating without any support. The 0.15 mm thick gas enables uniform, ultra fast heating with rates up to 900°C/s.

For more information, visit ASMI's website at www.asm.com.

Ion-Free Plasma Processing for a Broader Range of Semiconductor Devices

CONCORD, CA – March Plasma Systems has introduced their patent-pending ion-free plasma treatment process. Downstream ion-free plasma enables the cleaning process to be safely used on an even broader range of semiconductor devices.

Advanced memory components with smaller geometries, such as stacked die and other pre-programmed devices, require increasingly smaller wirebonds. Cleanliness is extremely critical as wire contamination can prohibit proper bonding. However, conventional downstream plasma treatment can potentially cause EPROM erasure in such devices. Ion-free processing, in the absence of UV light, enables the cleaning process to be used safely and effectively.

Advanced memory devices may also require cleaning due to epoxy bleed-out. When epoxy is applied to microcircuit devices, a small amount of resin separates from the epoxy. The separated resin enters small crevices on the gold circuitry and spreads to the surrounding bond pads. Ion-free processing allows removal of the epoxy resin without exposure to the direct plasma glow discharge.

With ion-free processing, the ions, electrons and protons are removed, enabling the chemically active radicals and byproducts to perform the work using oxygen as the source gas. An ion-free plasma environment is one in which the part is exposed only to the chemical components of plasma.

March's XTRAK-IFP system is configurable for either direct or ion-free plasma treatment. The system's modularity provides ultimate flexibility to match various manufacturing flow requirements, from high-speed, in-line to standalone configurations where one plasma station supports an island or group of equipment.

A complete review of March's plasma

North American Semiconductor Equipment Industry Posts December 2003 Book-To-Bill Ratio of 1.20

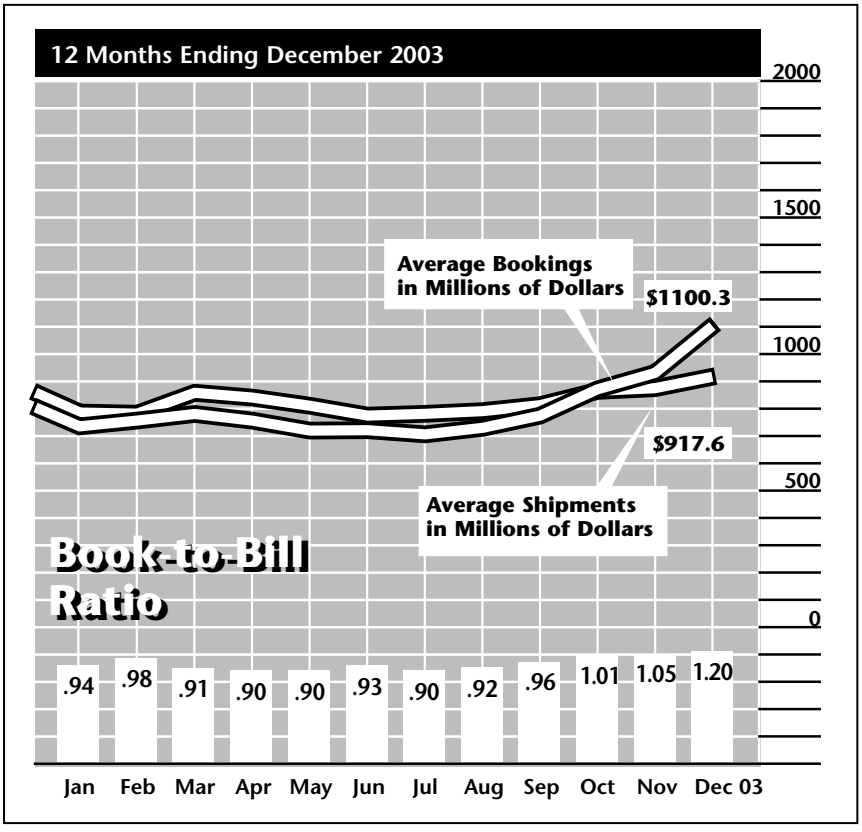
SAN JOSE, CA – The North American-based manufacturers of semiconductor equipment posted $1.1 billion in orders in December 2003 (three-month average basis) and a book-to-bill ratio of 1.20, according to the December 2003 Express Report published by Semiconductor Equipment and Materials International (SEMI). A book-to-bill ratio of 1.20 means that $120 worth of new orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in December 2003 was $1.1 billion. The bookings figure is 19 percent above the revised November 2003 level of $923 million and 33 percent above the $827 million in orders posted in December 2002.

The three-month average of worldwide billings in December 2003 was $918 million. The billings figure is five percent above the revised November 2003 level of $876 million and five percent above the December 2002 billings level of $878 million.

"The December data support the positive outlook for strong growth in semiconductor capital investment this year," said Stanley Myers, president and CEO of SEMI. "Analysts presenting at the SEMI Industry Strategy Symposium in January were in agreement that 2004 is shaping up to be a double-digit growth year for the global semiconductor equipment industry."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

treatment systems may be found on the Web site at www.marchplasma.com.

Honeywell Electronic Materials and Mitsubishi Chemical Corporation Announce New Electronic Chemicals Facility

SUNNYVALE, CA – Expanding its electronic chemicals product line and blending technologies, GEM Microelectronic Materials LLC (GEM3), a joint venture between the Electronic Materials business of Honeywell and Mitsubishi Chemical Corporation (MCC) announced the construction of a new facility in Chandler, Arizona. The facility will provide advanced application specific etching and cleaning chemicals to customers in the semiconductor industry.

A supplier of process chemicals for the semiconductor industry, GEM3 maintains multiple chemical manufacturing facilities in the United States providing products, solutions and services that address most wet chemistry steps in semiconductor manufacturing. GEM3 is able to license innovative technologies from its parent companies (Honeywell and MCC) as well as conduct development work of its own. GEM3 has been increasingly focused on providing application specific products for etch and clean processes for its customers. The Chandler facility will support both product development and volume growth in this area and reinforces GEM3's ability to supply the high-est purity products available with offerings of purities as high as "part per trillion (ppt)."

The ability to selectively and uniformly etch substrates without damaging underlying layers is imperative to wafer manufacturing. GEM3's expertise in this area includes both the development and manufacture of products for customer-specific applications as well as mainstream etchants. Cleaning chemistries are critical for reducing defect densities and improving yields. Recent innovations have created new blends that reduce cost of ownership, are more environmentally friendly than existing chemistries and focus on new materials utilized in the semiconductor industry.

"The Chandler facility will further enable GEM3 to provide the materials that are being requested by our customers to integrate into their specific manufacturing processes," stated Jim Favier, President of GEM3 and General Manager for the Chemicals business segment of Honeywell Electronic Materials. "We are focused and committed to being able to develop and deliver these materials for our customers. This new site reinforces that commitment," concluded Favier. GEM3

expects to complete construction of the facility in Q2 of 2004 with qualified production samples available in the same quarter.

For additional information, please visit www.electronicmaterials.com.

STATS Offers "Green" Flip Chip Land Grid Array Package for Height Sensitive Wireless Applications

High density, lead-free solution

SINGAPORE and MILPITAS, CA – ST Assembly Test Services Ltd. (STATS), a leading independent semiconductor test and advanced packaging service provider, has qualified a new environmentally friendly version of its Flip Chip Land Grid Array (FCLGA) package.

STATS offers a full array of Flip Chip CSP packages including the Flip Chip stPBGA (FCstPBGA) and Flip Chip LGA (FCLGA) which leverage STATS internal wafer bumping capabilities. The FCLGA offers a smaller form factor with increased routing density and improved electrical performance. A lower profile, 0.65mm nominal package thickness is achieved by using a thin core, high density laminate substrate, solder wetable I/Os lands and thinned die, making the FCLGA an ideal solution when electrical performance, form factor, and package height minimization are primary requirements. STATS has also broadened its product offering beyond traditional eutectic tin/lead to include increasingly popular lead-free alloys.

The lead-free FCLGA is targeted at high frequency and/or high data rate applications such as mobile phones, WLAN modules, PDAs, digital cameras, and camcorders which are driving low profile, high performance, environmentally-friendly packaging options. As with all of its flip chip package offerings, STATS provides full turnkey support, including advanced design and simulation support, wafer bumping, wafer probing as well as assembly and test.

Further information is available at www.stts.com

Carsem Offers MLP-SiP (System-in-Package) Solutions

SCOTTS VALLEY, CA – Carsem has announced that they now offer SiP (System-in-Package) solutions using their MLP (Micro Leadframe Package).

SiP is the advanced technology of placing one or more IC's and passive components into a single package. Prior to this announcement Carsem has been providing high volume production SiP solutions using organic (BT) and ceramic (LTCC) substrates in both BGA (Ball Grid Array), and LGA (Land Grid Array) options.

Carsem now has the ability to provide leadframe based substrate SiP solutions utilizing their MLP package family, which are QFN & SON compliant packages per JEDEC's MO220 and MO229 standard's. The MLP-SiP can be as simple as an MLP that contains a single IC and a few passive components in the range of 0201 to 0402 sizes. The more complex MLP-SiP versions contain more than one IC plus MOSFET devices, diodes and passive components including passives that are larger than 0402 in size. Both wire bonding and Carsem's patented FCOL™ (Flip Chip on Leadframe) is used to interconnect the active devices and the recently announced "copper clip" can be used in place of wire bonds on the MOSFET devices. Typical body sizes range from 4x4 mm with 16 leads (lands) to 9x9 mm with custom land patterns. Thickness options range from 0.9mm to 2.0mm.

According to Paul Smith, Carsem's Director of Marketing, "We have been working with several key customers on implementing the MLP-SiP technology and they have been very successful in the introduction of some advanced products that take advantage of this new capability."

David Comley, Carsem's Group Managing Director, stated, "Our MLP and SiP business has shown tremendous growth during 2003. This new MLP-SiP technology allows us to provide our customers with an even greater choice of highly cost effective solutions to help them compete in the market."

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, and sales offices across the USA, plus the UK. Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-

GEL-PAK, LLC

When a company needs to transport small, valuable, fragile devices from one location to another without risk of damage, who do they most likely turn to? GEL-PAK. Working across many industries, GEL-PAK has been creating innovative solutions for the safe handling and shipping of leading edge technologies for over twenty years.

GEL-PAK President and CEO Jeanne Beacham.

Headquartered in Hayward, California, GEL-PAK was born in 1980 out of Hewlett-Packard's need to securely transport highly fragile beam-lead diodes. Since then, GEL-PAK has successfully used their unique proprietary elastomer technology to develop a diverse and customizable line of innovative products for the safe shipping and handling of sensitive devices. At the heart of their unique product line is GEL-PAK's proprietary GEL material, an elastomer that provides a tacky surface that securely holds fragile parts in place during transport. The GEL-PAK products provide significantly more device protection than a traditional waffle pack or chip tray and without the need for pockets or cavities.

With President and CEO Jeanne Beacham at the helm since her management buy-out in 1997, GEL-PAK, an ISO 9001:2000 certified company continues to develop enabling products de-signed for applications where process uniformity and optimum protection of devices is mandatory "Our focus is to continually provide unique solutions for our customer's constantly evolving needs," says Beacham. GEL-PAK has met the growing demands of device manufacturers by offering in-depth product customization and quick turnaround backed up by a worldwide network of sales support. "The only way that we can anticipate our customer's needs," adds Beacham, "is through outstanding customer communication and support."

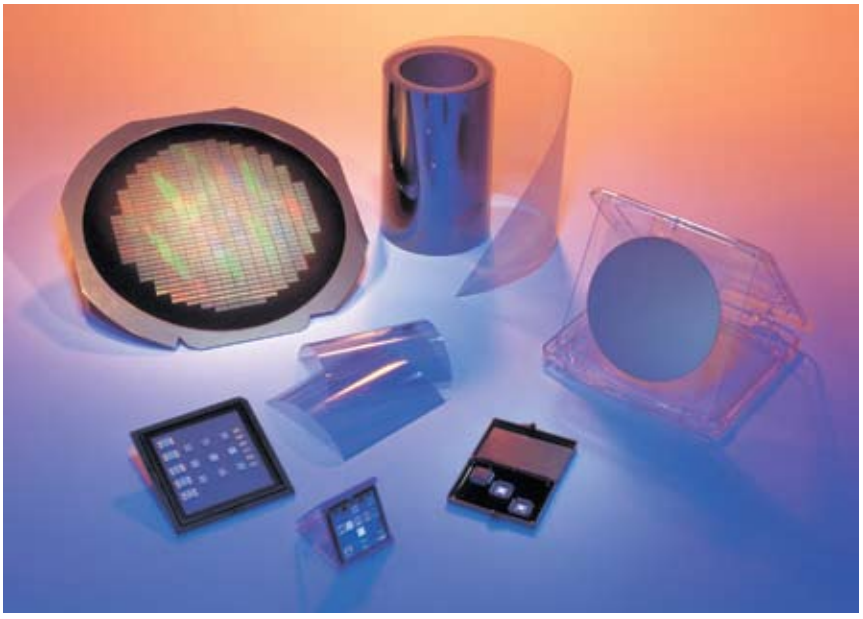
GEL-PAK, an ISO 9001:2000 certified company, works within industries where "clean room" quality is a must.

With over 1,000 active customers, ranging from Fortune 500 companies to small start-up manufacturers and universities, GEL-PAK's one-of-a-kind products are used in a variety of industries for the protection of critical components during transport, processing, inspection, and assembly. Some of the key industries that rely on GEL-PAK products are semiconductor, medical, automobile, data storage, aerospace, microwave, opto-electronics, and telecommunications.

GEL-PAK's extensive family of products have been designed to safely hold and immobilize devices by backside surface contact only, preventing po-tentially damaging contact with the edges or top surface which occur in waffle packs. Devices are held securely after making contact with the GEL surface and will stay in place, even if the carrier is inverted or dropped. All of the products can be customized by optimizing the GEL retention level (the tack or ad-herence of the GEL) based on the size, weight, and surface finish of the customer's device. The carriers are available in transparent, conductive, or anti-static materials as well as having the ability to be personalized with a company logo or a grid for device mapping. The versatility of the GEL-PAK products allow for a range of device sizes to be stored in a single tray or box enabling the user to greatly minimize their chip tray inventory thus reducing

both production control and purchasing costs.

The GEL-Box and GEL-Tray™ product families are ideal for manual applications in which the device may be re-moved with tweezers or fingers. The Va-cuum Release™ (VR) Trays and the Large Format Vacuum Release Carriers are de-signed for more automated environments in which the component may be unloaded manually by a vacuum pen or by an automated piece of equipment such as a die attach or pick-and-place machine. The GEL-Film® material is ex-tremely versatile and is used in a broad range of customer process steps. GEL-PAK products are typically customized to the customer's specifications based on desired size of the carrier, material type, GEL retention level, and automation needs.



GEL-PAK's innovative product lines expand to meet the needs of its customers and their industries.

MANUAL RELEASE PRODUCTS

GEL-Box (AD series)

GEL-PAK's AD Series, the original "sticky box", features an integrated pocketless hinged box system that is ideal for handling, storing, and shipping medical, optical, and other small microelectronic components that can be re-moved manually with tweezers or by hand. This pocketless carrier is also ideal for handling subassemblies, hybrid mod-ules, and packaged devices.

GEL-Tray (BD and CD Series)

The GEL-PAK BD and CD Series "pocketless" chip carriers are available in a 2" tray configuration and are intended for device off-loading with tweezers. The GEL coating is applied directly to the surface of a plastic tray (BD) or glass slide (CD).

Applications for the BD Series include the handling and shipping of GaAs FETs, laser diodes, beam-lead diodes, small thin-film passive devices, high-value medical, and optical filter components.

The CD coated glass slides are designed for high temperature applications such as bonding and reflow with a carrier capability up to 225°C. In addition, CD slides are utilized in a variety of applications where handling of materials for microscope inspection is required.

Inspection of a 300mm Large Format VR Plate during the production process.

VACUUM RELEASE (VR) PRODUCTS FOR AUTOMATION

Vacuum Release™ Trays

GEL-PAK's patented Vacuum Release (VR) technology allows for the safe handling of devices of any size from small transistors and diodes (0.25mm) to large ICs and wafers (300mm). The trays have no pockets, cavities, or compartments and can ac-commodate a wide range of device sizes and shapes on a single carrier. The 2" and 4" VR Tray products are ideally suited for high volume die handling ap-plications associated with automated processing equipment such as Palomar, F&K Delvotec, BESI, Newport, ESEC and Royce.

The vacuum release trays use a thin GEL membrane over a mesh material to hold the devices securely in place. The devices can be "released on demand" by applying a vacuum under the tray which causes the GEL membrane to conform to the shape of the mesh. This greatly reduces the surface contact between the GEL and the device, freeing the device for offloading. Once the tray is in the release mode, devices may be easily re-moved with a vacuum pick-up tool.

GEL-PAK's original "sticky box," the AD Series is designed for manual release systems.

The hold/release mechanism is reversible and the tray returns to its original holding mode when the vacuum is removed.

GEL-PAK Large Format Vacuum Release Carriers

The large format products, based on the GEL-PAK Vacuum Release™ technology, were developed in response to the semiconductor industry's trend to-ward larger, thinner, and higher value wafers and substrates. The carrier system is extensively used for shipping fragile InP and GaAs wafers and can accommodate larger silicon wafers up to 300mm in diameter. They are also used to immobilize partial or diced wafers that are still on a film frame during transport. In this unexpanded form, die edges are extremely sensitive. The large format carrier prevents any damage that is caused by wafer movement during transit.

PROCESS FILMS

GEL-Film®

The GEL-PAK FILM Series is a very versatile product with a wide variety of process applications ranging from front side wafer protection during the delicate process of GaAs or InP thinning to thin

GEL-PAK's Vacuum Release (VR) Trays are designed for automated handling processes.

film head crown lapping. It also makes an excellent protective coversheet for handling fragile wafers, micro-displays, and lenses. The film products are optimized to meet the specific customer pro-cess specifications. GEL-PAK's film manufacturing capabilities enable film thickness' ranging from 1 mil up to 20 mils and with a wide range of tack levels. The films can be constructed on a variety of carrier substrates and with an optional backside pressure sensitive adhesive for mounting applications.

QUIK-PAK DIVISION

In order to expand their range of services within the semiconductor industry, GEL-PAK acquired SPT, Inc. out of San Diego in 2000 and renamed it QUIK-PAK. This separate division of GEL-PAK provides patented "open-cavity" IC plastic packages for prototyping new IC designs. QUIK-PAK allows for new IC designs to be prototyped in a plastic package that is mechanically and electrically identical to the production part.

This method of prototyping is cost effective in that there is no need for expensive ceramic packages or retooling of test boards and sockets. The open cavity technology significantly reduces the overall time to market for new IC designs and revisions because design verification and prototype units are assembled in the same package within a 24-hour period.

QUIK-PAK's open packages range from the smallest SOT up to 304 lead QFP's as well as all BGA style packages. Any IC plastic transfer molded package can be reconfigured to an "open-cavity" format regardless of package style, size, or lead count. The QUIK-PAK packages can be assembled with standard wire bonding techniques, either by the customer or by QUIK-PAK's 24-hour assembly service. QUIK-PAK can also provide an assembled device that is left open (ideal for FIB work) or encapsulated as well as flattened and marked packages.

KEEPING THE FUTURE AND THE CUSTOMER IN MIND

GEL-PAK is committed to exceptional customer service and constantly looks for innovative ways to apply their unique and highly customizable GEL technology to meet their customers' ever changing needs. "We are committed to continuous quality improvement, from initiating quick-turn programs for customers who need fast product delivery to making sure that we are employing ISO 9001:2000 standards of quality," says Beacham. "All of the industries we serve undergo constant evolution and our commitment to pursue new solutions for our customers continues to be the key to GEL-PAK's success."

For more information, please contact GEL-PAK at 510-576-2220 or visit their website at www.gelpak.com. GEL-PAK is located at 31398 Huntwood Avenue, Hayward, California 94544. ◆

Wafer Sort Meets the Fab Roadmap

Vada Dean
Celerity Research

Figure 1. Moore's Law

Source: Intel

The ongoing integration of semiconductors into daily life has caused semiconductor products to become ubiquitous in the de-veloped world. Mobile phones, data networks, entertainment systems, personal computers, automobiles, and even office lighting depend on semiconductors. This pervasiveness of semiconductors has been enabled by the dictum known as, "Moore's Law" (Figure 1). Originally written as a prediction of how the industry would behave technologically and economically, it now governs our roadmaps and investments like a cruel taskmaster. Its prescience and ac-curacy have spawned customers that no longer accept incremental improvements over many years; instead, they expect twice as much for half the price every 18-24 months.

The pace of semiconductor adoption and the demands of "Moore's Law" create daunting engineering challenges. Since more power and more features must be packed into smaller spaces the photolithographic thin-film process has met the challenge by yielding smaller and smaller features at an ever decreasing cost per transistor. Ironically, the semiconductor test process used to validate semiconductor products has been allowed to violate the economic side of "Moore's Law." As chips become more complex the cost of test has risen commensurately (Figure 2). A major contributor to this rising cost trend has been the reliance on mechanical test tooling. As the number of I/O increases so does the number of "spring-like" elements re-quired to interface the wafer with the outside world. The increase in "spring-like" elements requires additional costs in labor, material, and capital.

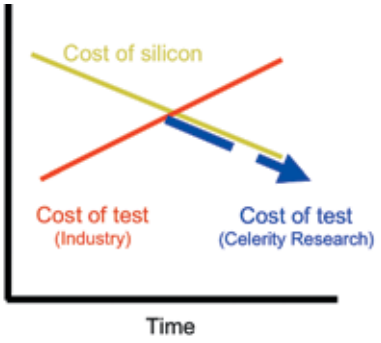


Figure 2. Cost of Silicon Structures vs. Cost of Test

In order to break the cost trend in semiconductor test, Celerity Research has developed products that keep pace with the accelerated output of photolithographic thin-film processes – by using the same processes to fabricate test tooling. Instead of utilizing expensive capital and labor to manipulate relatively small runs of probe cards and their springs, several probe heads are fabricated on wafers. Therefore, the same economic drivers that enable decreasing generational costs for chips now enable generational cost reductions for probe cards.

Utilizing the wafer manufacturing model also allows Celerity Research to innately follow the ITRS roadmap. As wafer manufacturing techniques improve, the processes and design rules governing them migrate to subcontractors. Celerity Research's fabless model readily adopts these changing design rules and makes the latest technology available to test engineers in the shortest time possible. In fact, Celerity Research's existing design rules meet the ITRS requirements through 2007 (Figures 3, 4 and 5) while future development continues to bring the fab roadmap to wafer sort. ◆

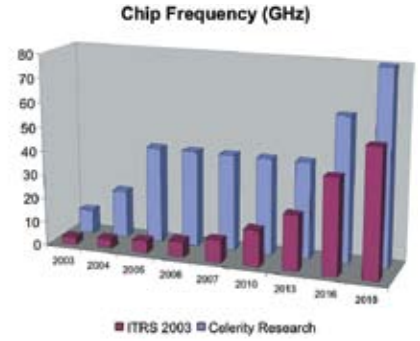


Figure 3. Chip Frequency ITRS vs. Celerity Research

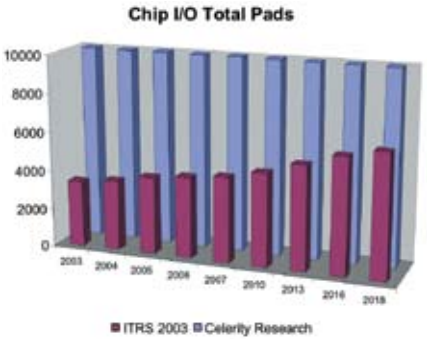


Figure 4. Chip I/O Total Pads ITRS vs. Celerity Research

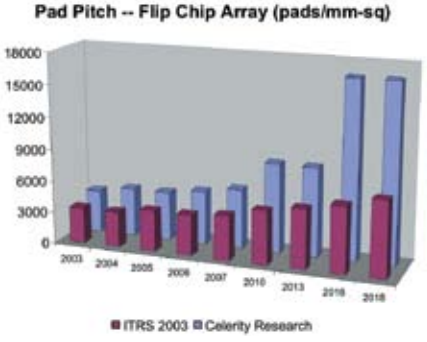


Figure 5. Pad Pitch – Flip Chip Array ITRS vs. Celerity Research

New Opportunity in the Value Chain

At this inflection point in the market, SATS firms have an unprecedented opportunity to capture new profit

Charles DiLisio
President
D–Side Advisors

The semiconductor value chain is well known. It is a mix of captive and independent software, hardware and service vendors and suppliers that stretches from EDA tools through manufacturing to assembly, test and distribution. Players range in size from a handful of engineers designing a new tool to massive IDMs and foundries. This value chain is highly competitive and profitability is a slippery outcome.

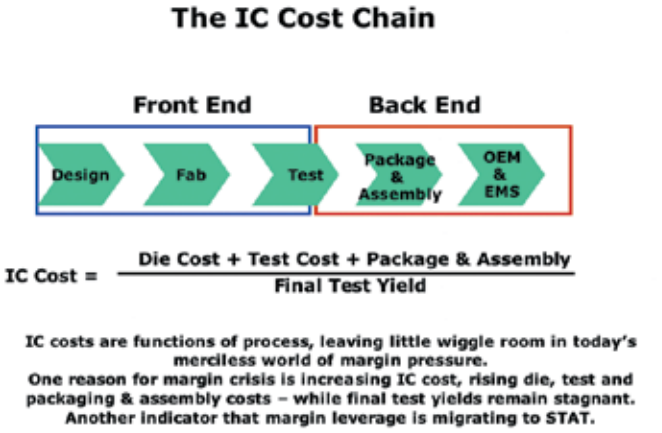
In the 1990's integrated device manufacturers (IDM) followed a two step plan for profitability. First, IDMs and their fabless offspring tried to develop a "platform product". The hope was that their silicon platform would become the foundation around which the company could build derivatives and de-velop extensions, as Intel has done with microprocessors.

The second step was to find volume markets such as the PC, display or cellular phone, to take advantage of the silicon platform where the advantages of Moore's Law (greater performance at lower costs) would greatly expand the end market demand through lower end product prices with greater and greater functionality.

Blindly following the IC manufacturer for platform product, volume markets became the SATS siren song in the new millennium. Volume meant revenue and profits. However to get the volume required SATS companies to make capital investments in test and assembly equipment

Capital investments weren't in the game plan. Few SATS companies perceive themselves as anything other than working to reduce the cost of their expertise. SATS history is as a cost center. In the beginning assembly and test was seen as the labor intensive cost center for IDMs. Now the service is seen as a necessary evil, a cost re-quires to display the chip designer's brilliance. Meanwhile IDMs and foundries continue to coerce SATS companies into lower fees for their expertise and much of this expertise has nothing to do with labor costs.

Three forces affecting the IC value chain have driven SATS firms to lower return on investment (ROI).



Elephant costs, canary returns. By the end of the 1990's boom SATS found themselves investing in an expensive technology curve but not getting the required return.

Suddenly a SATS company experienced the worst of Moore's Law – increasing capital costs and rapidly declining pricing not being amortized over larger and larger volume. New equipment was required to match new generations of new chips and packaging types. SATS firms were caught on the technology treadmill as they follow the lordly manufacturers to new geometry's which re-quire new packaging techniques with ever-finer tolerances

Spider web supply chain. Today's global supply chain provides both a telescopic and microscopic look into the market never before available in the complex world of IC design, fabrication, and delivery. It is a great tool when running contract manufacturing or an original equipment manufacturer (OEM) business.

The growth of the global supply chain has destroyed the relationship SATS firms had built with customers. In the beginning foundries grew as OEMs disaggregated their business models to focus on their core competencies and SATS emerged as a key in pro-duct cost and delivery. Today SATS is integral to the web that is global supply chain; but the SATS have lost huge amounts of customer equity in the process, equity in the form of customer relationships and partnerships. The global supply chain with its telescopic view destroys vendor/partner. Old re-lationships and business partnerships die when procurement has the ability to look globally for advantages in time, delivery and price.

Supposedly the supply chain creates a true capitalistic market where everyone can compete. But the SATS don't win because the supply chain traps them in a spider web of global competition. Stuck and they can't get out.

Mongoose Markets. The end market to-day resembles a mongoose with rapid movement in and out of holes, up, down and around looking fickle, but known to be ruthless. The mongoose keeps moving to forage for opportunities that become present and move on to the next opportunity. Like the mongoose, many end-user markets begin to look more consumer-like with price points that don't require deliberation (i.e under $200), short product cycles and high segmentation to meet specific end-user requirements or one to one marketing.

Three negatives driving today's SATS marketplace:

Elephant costs, canary returns:
Running on an expensive technology treadmill without getting necessary returns

Spider web supply chain:
Trapped in a web of global competition

Mongoose Markets:
Fickle, fast and but ruthless

The movement to a short-cycle consumer-like business model tends to eliminate

volume and long production runs. In addition the IC value chain moves from a learning curve model, where smart players can make money following the learning curve – to an order stocking model where ROI is dependent on the having the product available during it's short lifecycle and at a fixed price-point that leaves little opportunity for entering under the learning curve.

The three drivers effect the entire value chain negatively shifting value from the technology provider to the end user. For ex-ample cellular phones are basically free re-gardless of the technology stuffed inside.

For IC firms higher levels of integration have led to lower system costs, prompting market to grow driven by lower system costs. Good? No! Because, at this point a weird economic inversion occurred. As the consumer became accustomed to newer, better, faster, cheaper – demand, driven by low cost, coupled with splintering markets, lead to higher technology costs. But, the sellers of technology received lower value for their technology because, in our example, the cost of the cellular phone remained zero to the end user.

To regain that lost value semiconductor manufacturers can cram more in a chip. Or rework and update the monolithic methodology. But despite these tactics, the cell phone is free.

In this environment profits have eluded many IC firms, while simultaneously with each chip they ship the value of their technology downstream to the OEM. The good news is that SATS firms can gain big profits in this environment.

Changing Business Models

	Old Business Model	New Profit Model
Design & Process	• Bigger Wafers • Smaller Geometries • Additional Design Tools • High Cost ASICs	• Commodity CMOS Processes • Promiscuous Foundries • Ubiquitous Design Teams • Ordinary FPGAs, ASSP, etc.
Markets	• Big & Deep (PCs, Cell Phones)	• Fragmented & Short-term
Test, Assembly, Packaging	• Cost Center • Necessary/Boring • Submissive to IC Companies	• Value Center • Speeds Time-to-Market • Improves Time-to-Revenue

SATS as a Profit Center

In the market the follower, the SATS, like the medieval vassals can lament that the lordly IDMs and fabless firms are in bad shape and thus their outlook is grim. Or the SATS firms can view this as an inflection point in the market, as a challenge for change. SATS firms have the chance to gain big returns, due to this unprecedented break in the semiconductor value chain.

The positive driver is, why build it in silicon? Why not achieve same functionality using innovative packaging?

Promoting such ideas requires new thinking, especially a new understanding of "The Customer" with a sales shift from IC firm to OEM. No longer a vassal the SATS firm become a true mercenary seeking the greatest return for investors.

Instead of relying on the foundry to send over the monolithics, ASICS or FPGAs, the innovational firms could approach the OEM, asking system question to determine desired functionality, then help design teams to un-derstand how their goal might be achieved through such techniques an multi-chip modules or stack packing. For the OEM the basic financial question is: Why integrate on silicon when you can achieve comparable functionality in the package. Roles reverse as the IC firm becomes a commodity supplier while the SATS delivers the high value-add.

The opportunity is now. 2004 is the year for SATS to leverage this change, capturing the value being lost by the IC firms.

SATS have this opportunity because it offers new flexibility, which until recently was part of the semiconductor company's value proposition. This flexibility results from technology such as flexible substrates that allow the SATS firm to add value, which was once reserved for the IC firm.

One idea is to sell the OEM that they can achieve required functionality using innovative package techniques rather than expensive FPGAs, PLDs or ASICs. The advantages are that innovative packaging techniques will cost less while meeting their need for time-to-market.

Another idea is to emphasize *"good enough"* benefits over traditional build to spec. For example by using packaging the OEM might achieve good enough results to fit the product need. Maybe not the highest functionality possible, but of high value to the OEM because it fills the need quickly getting end product to market faster.

In addition with good enough, real costs are lower in terms of engineering and hardware cost and the OEM can get to market sooner at a lower cost.

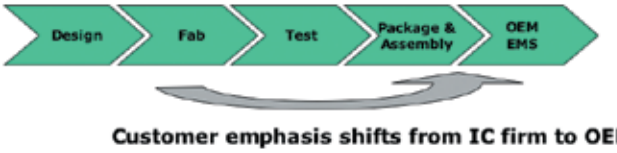
An irony is that this opportunity begins to make SATS look more like an aggressive contract manufacturer rather than a subservient foundry vassal. There is an analogy here in that EMS assembles boards while the SATS assembles chips – and boards are simply a higher level of integration than a modern package. If SATS firms seize the opportunity, the value chain will witness SATS growth into EMS-like strength. If not the EMS may acquire SATS capability.

Today SATS firms have the potential to turn old historic value chain inside out. Savvy executives are realizing that value is now in the hands of SATS not the IC firms. To capture the opportunity, gains profitability SATS firms must:

- Recognize high value of their work
- Stop thinking like a cost center
- Sell their value to end user/OEM not IC firm

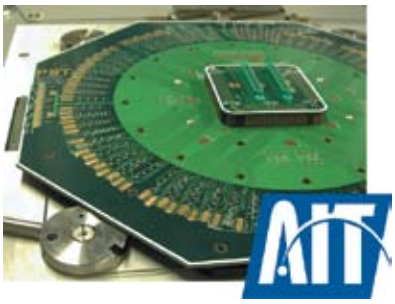
On the other hand, if SATS do not take charge of this opportunity, value creation and profits that go along with it will most

New Opportunities for SATS Emerge in the Value Chain



Customer emphasis shifts from IC firm to OEM

OEMs can achieve required functionality using innovative package techniques to meet their need for time-to-market as consumer demand both variety and low price



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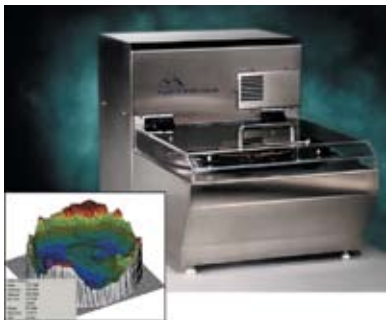

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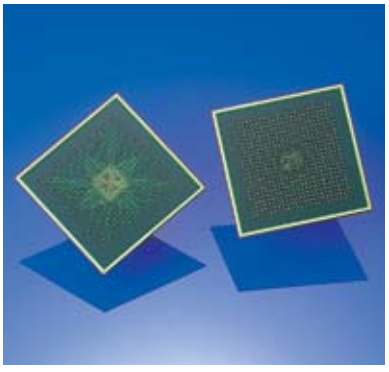

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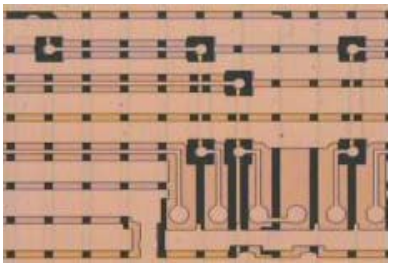

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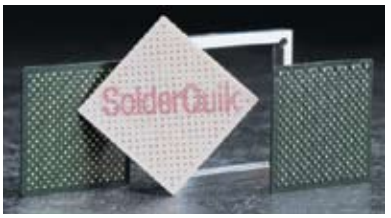

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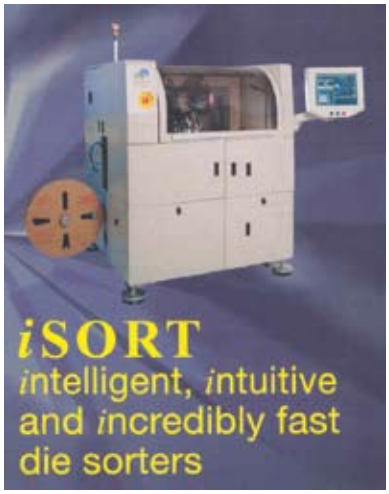

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For more information contact STI California Inc., 46753 Fremont Blvd., Fremont, CA 94539, Tel (510) 657-4691.

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MARCH 2004		1	2	3	4	5 **MEPTEC EXECUTIVE LUNCHEON** Ramada Silicon Valley	6
	7	8	9	10 **MEPTEC EXECUTIVE SEMINAR AND SUNNYVALE LUNCHEON** Ramada Silicon Valley	11 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	12	13
	14	15	16	17 **ST. PATRICK'S DAY**	18	19	20 **SPRING BEGINS**
	21	22	23	24	25	26	27
APRIL 2004	28	29	30	31	1	2 **MEPTEC EXECUTIVE LUNCHEON** Ramada Silicon Valley	3
	4 **DAYLIGHT SAVINGS TIME BEGINS**	5	6 **PASSOVER**	7	8	9 **GOOD FRIDAY**	10
	11 **EASTER**	12	13	14 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley	15 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	16	17
	18	19	20	21	22	23	24
	25	26	27	28	29	30	1
MAY 2004	2	3	4	5	6	7	8
	9 **MOTHER'S DAY**	10	11 **MEPTEC MEMS/WAFER LEVEL SYMPOSIUM** The Westin Santa Clara Santa Clara, CA	12 **MEPTEC INTERCONNECTIONS INVESTORS CONFERENCE** The Westin Santa Clara Santa Clara, CA	13 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	14	15
	16	17	18	19	20	21	22
	23 30	24 31 **MEMORIAL DAY (31st)**	25	26	27	28	29

Bob Hilton:
A Great Packaging Engineer Moves On

One of the greatest packaging engineers of all time passed away recently. Robert Max Hilton (Bob) at the age of 58 met with a tragic death in a boating accident near his home in Australia on December 18th. The details of the accident are not totally clear but what is for certain is that truly one of the greatest packaging engineers of all time has moved on.

Bob Hilton was the Vice President of packaging engineering at National Semiconductor during the 80's and put together a packaging engineering group that has yet to be rivaled. During his tenure at National Bob became the leader in TAB assembly using bumped wafers and bumped tape on bond pad spacing as low as 80 microns and lead counts in the hundreds. National made the first high volume commercially available CSP (TapePak). With Tapepak came the development of a customer application lab specializing in SMT. National implemented a process to preplate leadframes with solder, developed a Sn wafer backing process to eliminate Au eutectic chip attach, cultivated polyimide die attach along with a polyimide passivation process. National also developed and implemented a rapid solidification soft solder process to eliminate voiding and de-signed the first matrix leadframes. They were also the first to convert their high volume assembly production to Cu alloy leadframes and the first to wire bond directly to Cu leadframes in high volume. When package reliability became of an extreme focus, National packaging engineering was the first to define ionics and ionic contamination limits. On the equipment side, National was the first to go to fully automatic wire bonders and auto molding systems and patented the first tunnel die attach concept. And there was one project in particular that Bob Hilton earned notoriety on and that was called Odyssey, which was the first fully automated assembly line for IC packaging.

Bob was an outstanding packaging technologist because he had a thorough understanding of the three basic disciplines required to excel in microelectronic packaging; electrical engineering, mechanical engineering and material sciences. When and where Bob felt unsure of his capabilities he would either hire or associate himself with someone with more expertise in that specific area. As such, Bob built a wide network of employees, suppliers, customers and colleagues in which he would challenge everyone to excel. Regardless of what you did, where you came from or what you looked liked, Bob's only criteria of merit was that you could perform to a very high level

Bob Hilton accepts the 2000 MEPTEC Technologist Award from Charlie Sporck, former CEO and President of National Semiconductor.

of achievement of which many of us never realized we were capable of attaining. Bob's ultimate weapon was his charisma and the ability to make engineers realize that they were capable of achieving more and going beyond the limits of what was perceived by most to be good enough. Bob pushed the envelope of packaging engineering to a new level of excellence.

But for all his past accomplishments, probably his most important was to bring packaging engineering into the 21st Century. Bob Hilton was forcing us as a packaging community to become more involved and aware of electrical performance and designs of the package. Bob's ultimate personal goal was that you would not be able to tell where the silicon stopped and the package started; the package would no longer just be a protector of silicon but would actually enhance the performance of the silicon. A device maker would need to equally consider his packaging design IP with his silicon design IP as his market advantage. In the late 90's MTBSolutions was formed and Bob took the technical charter of the company to break open the packaging bottleneck that many device technologies suffer from. His ultimate goal was to have the package perform to the same level as the chip itself.

Ultimately Bob Hilton achieved his goal. He designed packages that could perform as well as silicon. He developed material sets that would allow the signal to flow through the package unabated. He developed flip chip pro-cesses that ensured the device would perform reliably. Just a few days before he died his packaging dream was realized when ASE Malaysia shipped the first thin film XSP packages to their European customer who clocked the performance at 50GHz.

But in reality Bob surpassed his goal. He had done what we as his colleagues always acclaimed as his greatest strength. He developed an infrastructure of engineers and suppliers that would enable the semiconductor industry to make significant gains in packaging technology now and in the future. He taught us to push ourselves, our suppliers and the systems in which we worked in to go beyond the adequate and to strive for excellence. Bob Hilton would always end his engineering staff meetings with the quote, "Though I shall pass this way but once I shall strive to do the best I can".

Those of you who had the good fortune of working with Bob Hilton will understand the significance of his passing.

Mark DiOrio
President / CEO
MTBSolutions

I first met Bob in 1973, at National Semiconductor in Singapore. He was on his way to Haiti to be Plant Manager at Na-tional's facility. Little did I realize that this chance encounter would lead to a professional and personal relationship that would span 30 years.

I worked with Bob first in Malaysia and later in the Valley. Bob had a profound effect on me and, countless others associated with semiconductor packaging.

He was a dynamic and inspirational leader. He used his candor, wit, humor and charisma in his dealings with people. He was an individual who had a voracious appetite for success in every endeavor he undertook. A consummate team player, he strove for nothing but the best when challenged. This rubbed off on others who worked along side him…. he kept raising the bar, which resulted in many innovations in Packaging. He constantly encouraged people to think 'outside the box' for creative ideas and solutions.

Bob constantly reminded us that "for every problem, there was a solution and where there is a will, there is a way". To many of us, he was a great mentor who enjoyed using his intellect to be creative and solve the many challenges that occurred.

Bob was a great family man who looked forward to spending time with his family in Australia between his business trips. A truly compassionate person, he will be missed but always remembered for the outstanding contributions that he made to semiconductor packaging.

Magazines and Carriers for Process Handling Solutions


Film Frames


Film Frame Magazines


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Grip Rings


Grip Ring Magazines

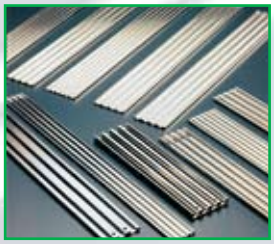

Grip Ring Shippers

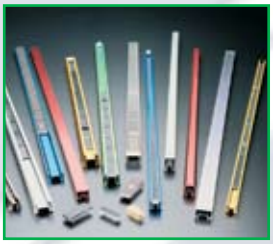

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.


Process Carriers (Boats)

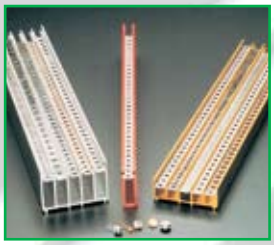

Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines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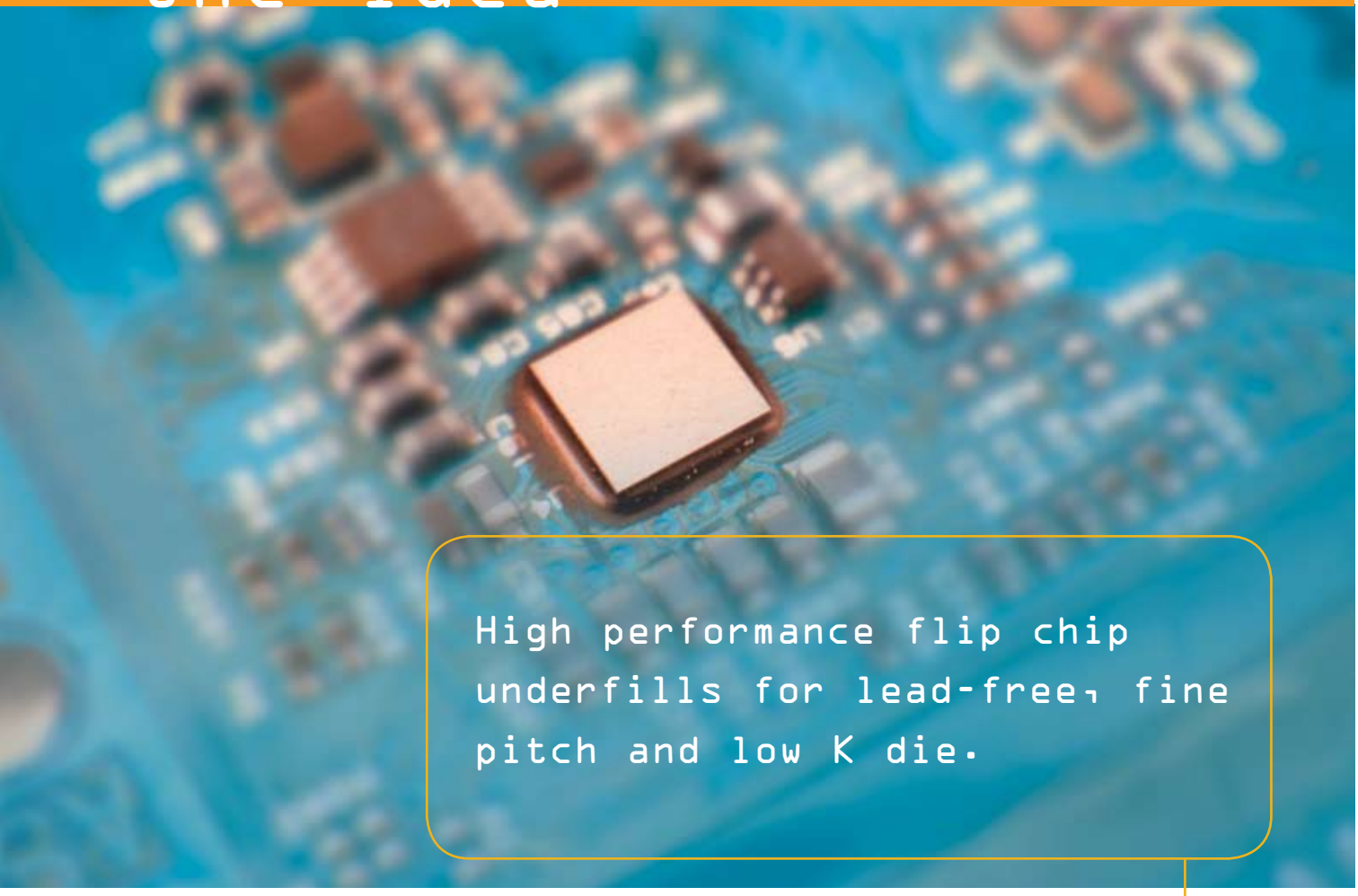

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