MEPTEC report
Volume 9, Number 1
QUARTER ONE 2005
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

HONEYWELL has appointed **Barry Russell** to the position Vice President and General Manager of **HONEYWELL ELECTRONIC MATERIALS**. *page 13*

SEMI has announced that **LUBAB L. SHEET** has been named Senior Director of Nanotechnology. *page 14*

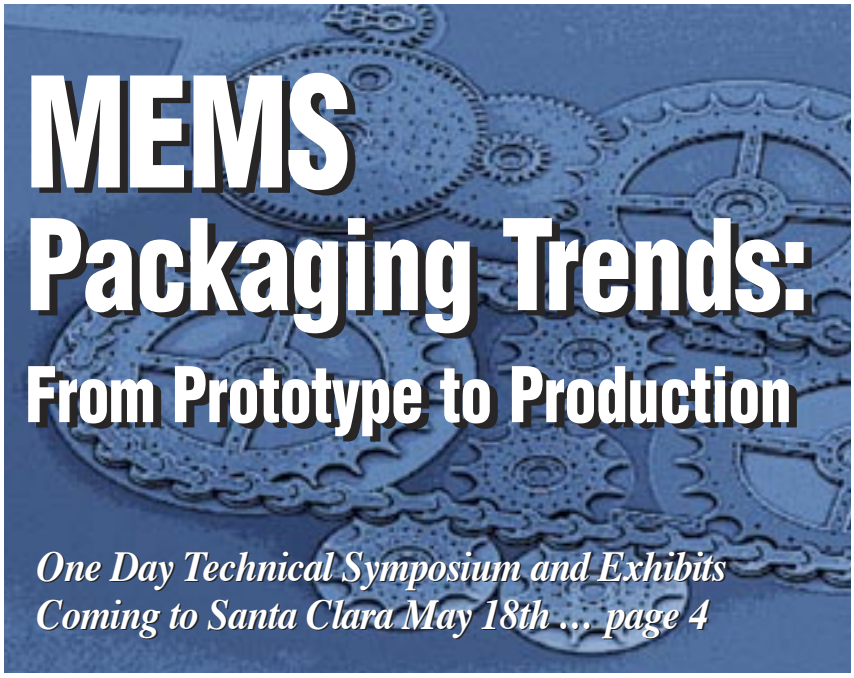
KULICKE & SOFFA INDUSTRIES, INC. has announced the sale of its wedge bonder technology to **ORTHODYNE ELECTRONICS**. *page 18*

TECHNOLOGY

Josh Nickel and **Joe Rosenberger** of **Silicon Bandwidth, Inc.** present *Enabling Superior Power delivery Through a Novel Decoupling Capacitance Platform.* *page 26*

Winthrop Baylies of **Traceability System Architects** discusses *Traceability of Materials and IC Packages to Improve Yields and Quality.* *page 28*

IEEE Wescon D2M - Explore Design to Manufacture Solutions, will be held April 12-14 in Santa Clara, CA. *page 36*



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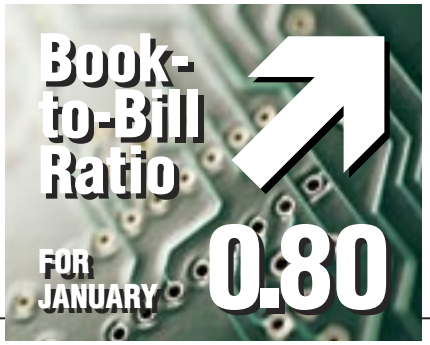
MEMBER COMPANY PROFILE

From their inception, Chip Supply has offered bare die to the hybrid/MCM manufacturers, and continue to ship more bare die than any other processor. Chip Supply is considered the number one value added die processor in the U.S. and is committed to both the manufacturers that supply them silicon and the customers they service.

Chip Supply, Inc., headquartered in Orlando, Florida, occupies five buildings on a campus that houses over 42,000 square feet of which over 10,000 square feet is a clean room environment. Chip Supply has over 125 employees, and is the largest added value reseller of bare die in the world today. Chip Supply also maintains sales offices in key market areas in North America and Europe, and maintains worldwide sales representation. *page 22*

Semiconductor equipment bookings increase 23% above January 2004 level. *page 20*



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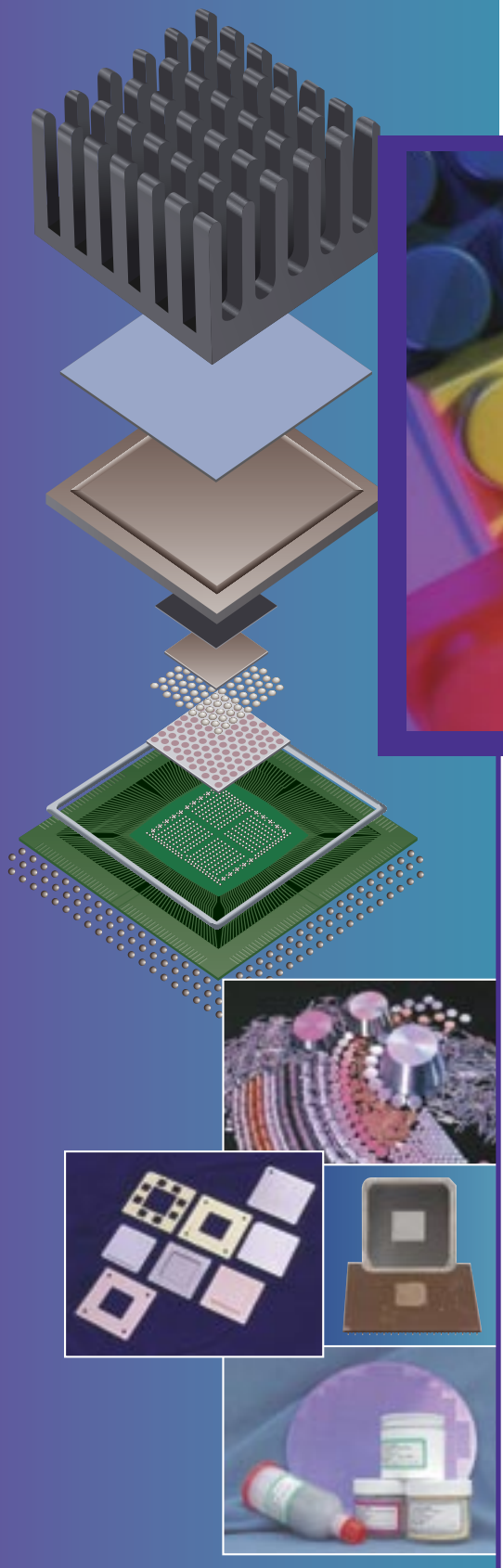
PACKAGING ■ OPTOELECTRONICS

Putting the Pieces Together



Providing the Most Complete Solutions for Your Interconnect Packaging Challenges...

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Honeywell

ELECTRONIC MATERIALS

MEPTEC report

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Welcome to the first issue of 2005! The economic recovery that was merely a glimmer of hope at this time last year seems to have come to fruition. We're glad to report it was a good year for MEPTEC. We steadily maintained and grew our membership, and continued to hold our monthly luncheons in Sunnyvale, CA and the Phoenix, AZ area, as well as our popular quarterly events. We had a cumulative attendance of nearly 2,000 attendees at our various events in 2004, and we plan to continue that trend in 2005.

Our next event will be held on Wednesday, May 18, 2005 at the Westin Hotel in Santa Clara, California. The event, entitled *MEMS Packaging Trends: From Prototype to Production* will be our third event on this topic. This year we'll be discussing, as the title suggests, the factors that will drive the next wave of the commercialization of MEMS. See page 4 for information on this exciting event.

Another event that is in development is part of a continued series that we call our *Educational Network Series*. **MEPTEC** Executive Director **Phil Marcoux** writes about *Launching New Products* in his Letter from the Director (see page 5). Phil's feeling is that with industry recovery comes the sometimes rushed launching of new products and services; that is bound to happen during this time, just following a recession. Phil enlisted the help of a couple of good friends and advisors, **Doug Molitor** and **Charles DeLisio** of **D-Side Advisors**, to facilitate a seminar on the subject of how to successfully launch a product (or service). As an Educational Network Series (ENS) event, the format will be very different than our quarterly one-day technical symposiums as we limit it significantly in size to allow for a high level of attendee participation and interaction. The seminar is planned for late spring; stay tuned for more details coming soon.

As a follow-up look on a couple of past symposiums, see page 6 for a synopsis of our February 16 *The Heat is On: Thermal Management Issues in Semiconductor Packaging*, written by **Jody Mahaffey** of **JDM Resources**, MEPTEC's PR firm. This was one of our most highly attended events ever; it proved to be a truly "hot" topic. In addition, **Julia Goldstein**, editor at **Advanced Packaging** magazine and frequent MEPTEC Report contributor, follows up with a review of our November event on *Innovations in Equipment and Materials for Microelectronics Packaging – Complexity Drives Collaboration* (see page 8).

One of the feature articles this issue is contributed by **Josh Nickel** and **Joe Rosenberger** of **Silicon Bandwidth, Inc.** Josh presented this technology as one of the showcase presenters at our November "Innovations" symposium. Discussing the challenges of power delivery, the authors offer a promising technology in the form of "embedded capacitance". This new technology has been demonstrated to not only enhance system power integrity, but to lower system costs as well. As they so aptly summarize, "… the system is greater than the sum of its parts". See page 26 for this informative piece.

Our other feature article is *Traceability of Materials and IC Packages to Improve Yields and Quality* by **Winthrop Baylies** of **Traceability System Architects** (see page 28). This topic was brought to our attention by **MEPTEC Advisory Board** member **Jerry Secrest**. Jerry felt that packaging and quality engineers would benefit from looking at trace on bonding wire, frames, and molding compounds, and how it can help with quality and higher yields. Mr. Baylies discusses traceability and tracking, standards, and traceability benefits, and how it can improve profits and productivity.

Our Editorial this issue is contributed by **Manish Ranjan** of **Ultratech, Inc.** Manish was also a speaker at our November "Innovations" symposium. We asked him to discuss the challenges in choosing lithography equipment. He discusses technical challenges, imaging and alignment considerations and production yield – see page 38 for this interesting piece.

Our Industry Analysis coverage this issue is contributed by **E. Jan Vardaman** and **Linda Matthew** of **TechSearch International**. In this article they discuss how flip chip and wafer level packaging is one of the fastest

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Issue Highlights

MEPTEC Presents

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MEMS Packaging Trends: From Prototype to Production

Wafer-Level Packaging Enabling High-Volume Applications

Micromachines are here to stay. Over the past few years, we have begun to witness the long-predicted explosion of the MEMS market. High-definition televisions with super-sharp micromirror displays, high-volume consumer electronics with accelerometers for motion detection, and high-end automobiles with gyroscopes for navigation control are just a few of the bold new applications of MEMS. The development of low-cost wafer-level packaging, which was the focus of MEPTEC's MEMS symposium a year ago, has been instrumental in this fantastic growth. But this is only the tip of the iceberg.

In MEPTEC's third annual MEMS packaging symposium, we will explore the new opportunities and driving factors that will contribute to further large-scale commercialization of MEMS. The industry overview session will cover topics affecting commercialization strategy such as emerging standards and technology transfer from lab to market. This will lead into an enabling technologies session discussing recent advances such as wafer bonding, electroplating, and encapsulation. A third session will focus on the evolving MEMS packaging infrastructure – companies striving to provide the "picks and shovels" for the MEMS gold rush. Finally, the new frontiers of MEMS will be explored, as we look at several budding applications which promise to be the "next big thing".

The **2005 MEPTEC MEMS Conference** will bring together a rich variety of professionals from academic and industry circles. We will learn lessons from the recent past, discover the present state of the art, and catch a glimpse into the future of MEMS. It will be an exciting opportunity to network, exchange ideas and perspectives, and discover synergies that will drive the next wave of MEMS commercialization.

Session Topics:

- **Technology and Industry Overview**
- **Enabling Technologies**
- **Assembly and Test Processes**
- **End User Applications / Future Trends**

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MAY 18, 2005 • SANTA CLARA, CALIFORNIA

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From The Director

Launching New Products

In my last "From the Director" column I discussed the wave of innovations that I've observed into our segment of the industry. This gave me cause to think about the many prior successful and unsuccessful product introductions we've experienced and observed.

Just as innovation is the lifeblood of any business, so is successfully introducing the products and services that result from those innovations.

A couple of months ago I received a call from a friend and advisor for last year's Interconnection Investors Conference, Doug Molitor of D-Side Advisors. Doug has been a successful marketing and management consultant to local companies for many years. Over lunch the topic of product launches came up and we both agreed that our industry is in a period where after a recession there's a rush to launch many new products. It's common in this period for companies to launch the products as rapidly as possible in order to strike while the market is hot. Unfortunately, many times this opens the door to poorly planned and executed launches.

With that in mind I asked Doug to present a seminar for our members on how to successfully launch products. He agreed and even prevailed on another advisor and popular speaker, Charles DiLisio, also of D-Side Advisors, to join him.

The seminar "Winning Strategies for new Product Launches" will be held in Sunnyvale at the Ramada Hotel later this spring.

This seminar will be targeted to executive and managers of companies both large and small, including marketing, sales and product development. It will also be geared for marcom, public relations and other related professions.

Some of the topics that will be addressed are:

- Have your recent new product introductions meet expectations?
- Are the new products being given enough to succeed?
- How do you make your new product introductions a world class Global event, rather than a so-so blip?
- Is innovation and excitement equal on both sides of the desk, i.e., in both product development and product launch?

Registration and other details will be available soon. The seminar will be limited in audience size to allow for open and frank discussions and to explore other areas of audience interest.

I hope you take advantage of this educational event. ◆

Phil Marcoux
Executive Director, MEPTEC

MEPTEC Council Update

continued from page 3

growing segments in the interconnection area. They project a need for a great deal of capacity expansion to meet fast-growing requirements. See page 9 for their article entitled *Flip Chip and Wafer Level Packaging on Fast Track*.

We're pleased to profile MEPTEC Corporate member **Chip Supply Inc.** in our Member Company Profile this issue. Founded in 1978 in Orlando, Florida, they formed to fill a niche market by supplying bare die to **Lockheed Martin**. Since then they have grown to occupying over 40,000 square feet of facilities and over 125 employees, and are now the largest added value reseller of bare die in the world. We think you'll find their success story very interesting – see page 22.

For our University profile this issue we take a second look at **San Jose State University** located in the heart of Silicon Valley. We profiled them the first time in the fall of 2001, but wanted to offer an update on some of the changes that have taken place there. Long-time MEPTEC supporter, **Dr. Guna Selvaduray**, Professor and Graduate Coordinator in the Chemicals and Engineering Department, takes a look at the changes during his tenure over the last 20 years. A new area of curriculum at SJSU in the Engineering Department is Biomedical Devices. This is such a growing technology area that it made sense to offer it as an interdisciplinary field, and SJSU is very well positioned to offer it. See page 11 for more details.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for joining us! ◆

Thermal Management for Today's "Hot" Products

Jody Mahaffey
JDM Resources

Everyone wants to know what the next "hot" semiconductor product will be. But for those in the semiconductor industry, it's well understood that the "hot" products are already here... and they just keep getting hotter. Today, high-end microprocessors and graphic chip sets play a huge part in our everyday electronics world. As these devices continue to increase in functionality and performance, the speed and circuit density must also increase and that can create some seriously "hot'" issues for systems designers as well as everyone else in the supply chain.

On February 16, MEPTEC, the Micro-Electronics Packaging and Test Engineering Council held its first technical symposium of 2005 titled "The Heat Is On: Thermal Management Issues in Semiconductor Packaging" to discuss with experts how to manage the heat generated by these high wattage devices. We asked some of the symposium's speakers for an insight into the world of thermal management.

All the presenters we spoke to agreed that the entire supply chain must be involved to produce products that meet the thermal management requirements for today's high speed, high performance products. Put succinctly, "With increases in power density and compaction at the system level, a holistic view is necessary," said Chandrakant Patel, Distinguished Technologist for Internet Systems and Storage Laboratory at HP Labs. Patel presented in the Systems Level Challenges and Solutions Session of the symposium.

Dr. Gerald (Skip) Fehr, Industry Consultant and Session Chair for the Modeling, Characterization and Measurement Session of the symposium stated that, "Everyone must be involved; however, in the end the system designer is usually the one who controls the final design and places the requirements for the system. In this way he can influence the chip design, the package design and the system cooling. He will then work with the chip designer and often times he will also have worked backwards from the board design so the chip designer has various restraints on the chips. The package designer must build a package that meets the system electrical and cooling requirements. Cooling methods are part of the system design. Various package styles and cooling techniques are discussed and picked out. The system designer gets everyone on the same page by his specifications and discussions. This is often a back and forth process with all people involved, such that the most economical design is accomplished. For a large system there are a lot of compromises."

Dr. Roger Emigh, Director, WW Package Characterization at STATSChipPAC and a speaker in the Modeling, Characterization and Measurement Session, stressed the importance of each member of the supply chain's role because if the thermal issues are overlooked by any part of the supply chain, then the job of meeting the thermal management goals will be passed along to another portion of the supply chain.

Although CPUs and GPUs are the most commonly thought of devices requiring special thermal management, there are several other areas where thermal management is crucial to the performance of the end product. Patel told us that other devices such as drivers, power converters and mass storage will all require more thermal management as they scale with CPUs.

According to David Copeland, Packaging Technology Research at Fujitsu Laboratories of America, "Years ago, the power supply provided adequate airflow to cool everything. Then fansinks for the processor increased local airflow but not the system total. Finally dedicated fans and fully ducted heatsinks were required. Now even chipsets and memory have airflow requirements, and some are even getting dedicated fans and/or ducting." Copeland presented in the Device Level Challenges and Solutions Session of the symposium.

Dr. Emigh added that, "Stacked die packaging can also present challenges, not only when you are stacking memory onto a logic chip but when the stack contains die that are generating more than a trivial amount of heat."

But one solution may not meet all the thermal requirements for all different types of devices. As Dr. Emigh pointed out with respect to maximum junction temperature, "A device with a limit of 105°C will present a different challenge as opposed to one that can see 125°C."

Furthermore, Joel Camarda, Industry Consultant and Session Chair for the Systems Level Challenges and Solutions Session of the symposium, feels that the differentiation in thermal management requirement is driven by device performance and lithography density, as not all products require state of the art speed and density. He explained that, "Low density and low speed, even high density but low speed devices, will not create the same thermal concern as when both are maximized. So, the requirement is definitely device type (product) driven. However, I believe there is a lot of commonality in the solutions."

Patel takes the approach that, "Given a portfolio of solutions, a mapping needs to exist to address a variety of devices to avoid over or under provisioning of the heat removal solution."

There are many approaches to managing high wattage devices and their associated problems. According to Dr. Fehr all issues need to be addressed and solved for the high wattage device to work reliably. This includes the electrical (usually current capability and noise issues) as well as other restraints for the device being designed. He believes the most difficult problem to be solved changes with different devices and system designs.

Dr. Emigh believes that the approach depends on the system in which the devices will be used. "In larger system environments, like desktop PCs and server/rack systems, it is mostly a space and cost issue. In smaller, space critical systems, the higher wattage devices can require thermal changes beyond just the package/heatsink and in some cases their heat can cause problems for other devices in the system."

There are many types of thermal management issues, but are these issues currently holding back potential developments in the semiconductor market? Most of those we asked feel that thermal management issues are at least limiting development in many markets. "Power management techniques seem to be motivated by thermal management issues and battery life in case of laptops - so one might conclude that thermal management issues are indeed starting to affect the market. It is not clear that potential developments in semiconductor devices are being slowed down - though in the long term, that might be the case," said Patel.

Camarda agreed saying, "Absolutely, primarily thermal issues are responsible for a major microprocessor supplier to revise their next generation product offering. The higher density integrated circuit structures (90 nm and below) and the thin metallization structure operating at high speeds

create heat. The continued advancement of product performance (to higher GHz values) requires a thermal solution."

Dr. Fehr feels that thermal issues are limiting the power and speed of the mobile devices as space and cooling techniques are limited. But Dr. Emigh pointed out that in the communications and mobile/handheld market, the real issue is cost. He believes that the thermal solutions are readily available but they result in a higher cost or require increased space, both of which are to be avoided as much as possible.

Thermal management issues will continue to play a part in the future cost and capability of semiconductor devices. According to Patel, "Increases in power density at the chip level will necessitate active heat removal means, particularly to continue to maximize the ability of silicon devices and processes. Cost of the heat removal mechanism and the energy used to remove the heat will become central. As an example, the commoditization of computing equipment will result in the cost of computer equipment being secondary to power used by the system itself."

Dr. Fehr noted that, "The packaging cost has become as large as the die cost in many cases. The ability to handle the cooling requirements in a cost effective manner is critical for system costs. Presently there are times when two devices are used in place of one when electrical and cooling requirements are too difficult to solve within the system requirements."

Dr. Emigh added that thermal management will impact the cost of not only the packaging but also the systems in which the devices are used.

Some of our speakers believe that finding solutions to the thermal management issues we see today may well open up new markets in the semiconductor industry or at least prevent new markets from being limited. "More effective and less costly cooling techniques will open up the possibility of using higher power devices in the mobile industry where cooling is often a controlling restraint," said Dr. Fehr.

Dr. Emigh feels that these solutions may not necessarily open new markets but better control of the heat being generated will definitely help allow higher functionality to be built into smaller systems.

To achieve the results needed to solve many of the thermal management issues we see today, thermal modeling and simulation are becoming more and more critical.

Dr. Emigh who is responsible for Package Characterization at STATSChipPac, said, "Software enhancements have allowed much faster and more accurate simulation of the full packaging system, instead of just a small symmetrical section of it. Also, the wider acceptance of CFD tools for package level modeling has improved our ability to provide thermal solution recommendations (heatsinks, PCB enhancements, etc.) much earlier in the design process." Those thermal recommendations help reduce the learning cycle time, and ultimately the cost, which is very important at every stage of the supply chain.

Dr. Fehr added, "Enhancements in thermal modeling and simulation are a major help in the design phase. The accuracy, ease of design input and speed of the program are critical in choosing how much modeling and simulation is done. It allows a system designer to look at various alternatives in the system design and determine if there is a lower cost alternative."

But Patel maintains that, "Better fundamental understanding of the subject of thermal management is a prerequisite to any enhancement in modeling and simulation software. My own experience indicates that a better fundamental understanding can enable a more expedient approach than any

particular enhancement. As an example, a higher level thermo-fluidic representation of a heat dissipating source in any software enables expedient and accurate analysis. Users must come up with such techniques, publish, and drive the simulation industry, not vice versa. Once a higher level approach is recognized, the enhancements can be market driven, e.g., the software manufacturer can make it part of the tool."

Throughout the supply chain, thermal management issues continue to be addressed and overcome so that we can continue to make the better, faster, cheaper products that the world expects. ◆

MEPTEC Presents Materials and Equipment Innovations

Julia Goldstein, Technical Editor
Advanced Packaging Magazine

San Jose, CA – MEPTEC featured 29 suppliers in their most recent symposium, "Innovations in Equipment and Materials for Microelectronics Packaging – Complexity Drives Collaboration." This report highlights some of the new product and process developments.

Materials Technology

Dan Tracy of SEMI began by discussing the global packaging materials outlook, noting that revenue in 2004 from array package substrates will outpace that from leadframes for the first time as the industry continues its transition to substrate-based technologies. SEMI has forecast a 10 percent revenue growth for packaging materials in 2004. The global market for organic substrates, dominated by laminates, is expected to grow from $2.3B in 2003 to $4B by 2006. Growth in both mold compounds and solder balls will naturally be driven by the move toward "green" products, with advanced resins and lead-free solder balls increasing significantly.

Not surprisingly, all of the solder presentations and several others featured lead-free solutions. Bow Electronics has developed a process for producing high precision copper spheres that can be coated with gold, tin, or other metals for use as a replacement for high-lead solder balls. Nippon Micrometal Corporation described their lead-free solder balls, claiming optimum reliability with a silver content of 1.2 percent, based on temperature cycling data. This material has much less silver than the 3.8 to 4.0 percent found in common tin-silver-copper (SAC) alloys.

Amitec Ltd. presented their advanced core-less organic substrate, which combines thick and thin film technologies and includes a low K dielectric that enables finer lines and spaces while maintaining 50-Ω impedance. Amitec is not the only company using low K dielectrics. Daisho Denshi's solution replaces standard epoxy resin with a low K film that provides a flat surface with high adhesion strength and allows precise plating of metal traces down to 10 μm lines and spaces with good impedance control.

Two competing companies presented their die attach solutions to the problem of paste bleeding onto adjacent wire bond pads. The general trend in the industry is toward films instead of pastes. Lintec Advanced Technologies presented a new film that can be used for both dicing and die bonding and can be stored at room temperature. Ablestik Laboratories has formulated a B-stageable paste with a two-step cure that achieves fillet control comparable to films plus the ability to fill in substrate topography such as via holes. Target applications include QFN and DRAM board-on-chip (BOC) packages. For stacked die packages, B-stageable pastes could be used for direct substrate attach of the bottom die in a stack, while films are probably preferred for the remaining die.

Equipment Technology

Keynote speaker Mark Stromberg of Gartner Dataquest discussed the packaging and assembly (P&A) equipment market. Growth has slowed, and while the overall SATS market is expected to show about 15 percent growth in 2005, Stromberg's forecasts showed a 14 percent drop in revenue for P&A equipment next year followed by another decline in 2006. Capacity utilization has softened and should continue to decline over the next two years.

Despite the gloomy equipment industry forecast, innovation continues. For example, the industry is focused on solutions driven by the move toward lead-free solder. Surfect presented a plating tool that can deposit multi-layer metal structures for precise binary or ternary alloy bumping. The wafer remains in a stationary cell during the entire process, providing a sequential deposit without moving the wafer. SUSS MicroTec discussed their collaborative effort with IBM on a new lead-free flip chip process, called C4NP. A borosilicate glass template is filled with molten solder of any composition, the resulting solder balls are then transferred to a wafer, and the template is cleaned and reused. The process has been demonstrated with balls as small as 25 μm diameter with a 50 μm pitch. Klaus Ruhmer of SUSS described the new process as, "The greatest thing for us since the mask aligner."

Wafer level packaging requires new approaches to inspection. RVSI has streamlined inspection with a tool that combines several steps into one, examining wafer surface defects, probe marks, bump metrology and 2D and 3D bump inspection for flip chip wafers. Phoseon discussed their novel infrared imaging tool designed for MEMS applications. The infrared light source can see through silicon to inspect wafer-to-wafer bonding and alignment with 0.5 μm accuracy.

The trend toward film die attach has impacted throughput, and ASM Pacific Technology presented one possible solution, an after press station to complete die bonding off-line. Stacked dies are briefly bonded on conventional equipment, and then the new tool bonds multiple die at once, providing a longer cure time and reducing voiding. Datacon discussed a two-step bonding process for wafer level packaging, where chips are aligned to a wafer in a die bonder and then permanently bonded in a specialty chip-to-wafer bonder using thermocompression.

Xsil has a laser micromachining tool that can create through-die vias with very high aspect ratios. One potential application is for stacked packages, to decrease the number of wirebonds needed for a multiple-die stack. A separate Xsil tool is designed to dice thin silicon wafers without the damage typically induced by saw cuts. They typically work with 75 to 100 μm wafers but have diced wafers as thin as 20 μm.

About half of the companies featured in the equipment presentations were winners of the Advanced Packaging Awards at SEMICON West in July, but most of these companies discussed technologies other than those for which they won the award, demonstrating that they have more than one new product to showcase. Perhaps some of the new innovations presented at the MEPTEC symposium will show up in the 2005 awards. ◆

Flip Chip and Wafer Level Packaging on Fast Track

TwinMOS Twister module with wafer level packages.

E. Jan Vardaman and Linda Matthew
TechSearch International, Inc.

Flip chip and wafer level packaging is one of the most dynamic and fastest growing sectors in first level interconnect arena. TechSearch International projects a compound growth rate of more than 28 percent in this market between 2004 and 2009. Although many companies have added capacity for solder bumping and wafer level packaging, demand is projected to outstrip supply. The analysis for wafer bump capacity shows that in 2007 additional capacity will be required if demand continues to grow as projected. With a forecasted demand of 22 million 8-inch equivalent wafers (Flip Chip and WLP) in 2007, TechSearch projects a need for capacity expansion to meet the requirements.

Drivers for Expansion

The drivers for flip chip continue to be performance, on-chip power distribution, pad limited designs, and form factor requirements. High performance logic suppliers such as ASIC, field programmable gate array (FPGA), DSPs, chipset, graphics, and microprocessor makers are expanding their use of flip chip in package (FCIP). Applications such as watch modules and automotive electronics are included as flip chip on board (FCOB) packaging solutions. An increasing number of devices, from diodes to DRAMs, are packaged at the wafer level. WLPs are also growing in volume for a variety of low lead counts (≤ 100 I/O) applications – including analog devices such as power amplifiers, battery management devices, controllers, memory, and integrated passives. Most of these devices are relatively small in size, and thousands can be fabricated on a single wafer. While the shift to flip chip and WLP did not materialize in high volume for DDR2 DRAM, performance requirements will necessitate a shift in interconnect methods from wire bond to bumps (flip chip or wafer level package) for DDR3. Gold bump demand continues to be dominated by LCD driver ICs, but an increasing number of gold stud bumped devices are also shipping.

New Developments

The expansion of flip chip technology continues to spark innovation and new developments. New bumping technologies continue to be introduced for the flip chip market. These include the copper pillar bump and pyramid bump.

The introduction of low-k dielectric materials on the inner layers of the die resulted in the need for changes in package assembly materials and processes for both flip chip and wire bond. Assembly challenges of copper/low-k devices are primarily mechanical, due to the very weak dielectric. Potential problems include cracked diffusion barriers, copper diffusion into the low-k polymers, and cracking of the low-k materials. Low-k polymer materials with high expansion coefficients and low thermal conductivity can also increase the stress and further extend any existing damage to barriers, as well as increase the probability of electromigration of the copper lines. On a positive note, issues with low-k dielectrics have resulted in a greater cooperation in the design, fabrication, and assembly of ICs and improved communication between the industry groups.

Legislation in Europe banning lead and other materials deemed harmful to the environment by 2006 currently provides an exemption for high-lead flip chip bumps, however a number of companies are moving to adopt lead-free bump compositions. Assuming that all wireless and consumer products, hard disk drives, graphics chips, and DDR3 memory use lead-free bumps, 57 percent of the total solder bump demand for 2006 will be lead free.

Barriers to Expansion

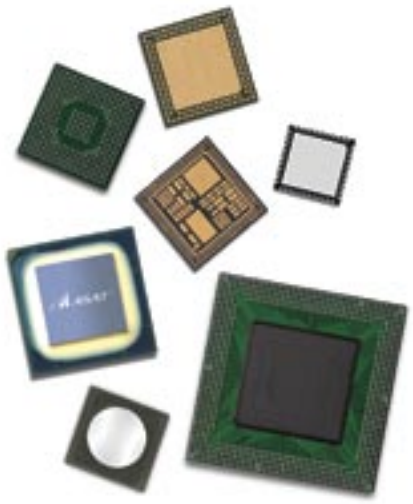
Historically, the barriers to the expanded use of flip chip technologies have been the availability of low-cost bumping services, difficulties with underfill, low-cost substrates, and flip chip bonding and mounting equipment. Substantial improvements over the last four years have removed or reduced many of these barriers. Developments in the infrastructure include the introduction of new, low-cost methods for wafer bumping, an increasing number of subcontract assembly services with growing capacity, and bumping for 300mm wafers. With substantial price declines for wafer bumping and assembly services, one remaining barrier is the price of laminate substrates. In many cases this price represents more than one-half the cost of the flip chip package. While there are more suppliers today than in the past few years, the industry is not mature and the yields for many designs other than microprocessors are still low. Flip chip substrates should be considered in two entirely different markets from a substrate application perspective. Substrate prices for PC microprocessors have declined to approximately $2 per part – based on high volumes (hundreds of millions of units) and substrate design simplification. Graphics processors and chip sets will follow the same price trends as volumes increase. Other flip chip applications with large body sizes, high performance, and low unit volumes do not share the same price structure. Substrate prices are the major component in the price of the flip chip PBGA at high pin counts, but are expected to decline over the next year, depending on volume and design.

More than two dozen companies offer flip chip assembly – both FCIP and FCOB. Almost 20 companies offer flip chip bonders and mounters – each suited for a particular application. Bump inspection systems from at least eight companies are available. Improvements in equipment for flip chip assembly have enabled the technology by allowing the user to select the equipment that provides the required trade-off in accuracy and speed.

The anticipated growth in the flip chip market is finally becoming a reality as a result of performance and form factor drivers coupled with infrastructure developments.

The future for flip chip is bright.

Profit From Our Experience



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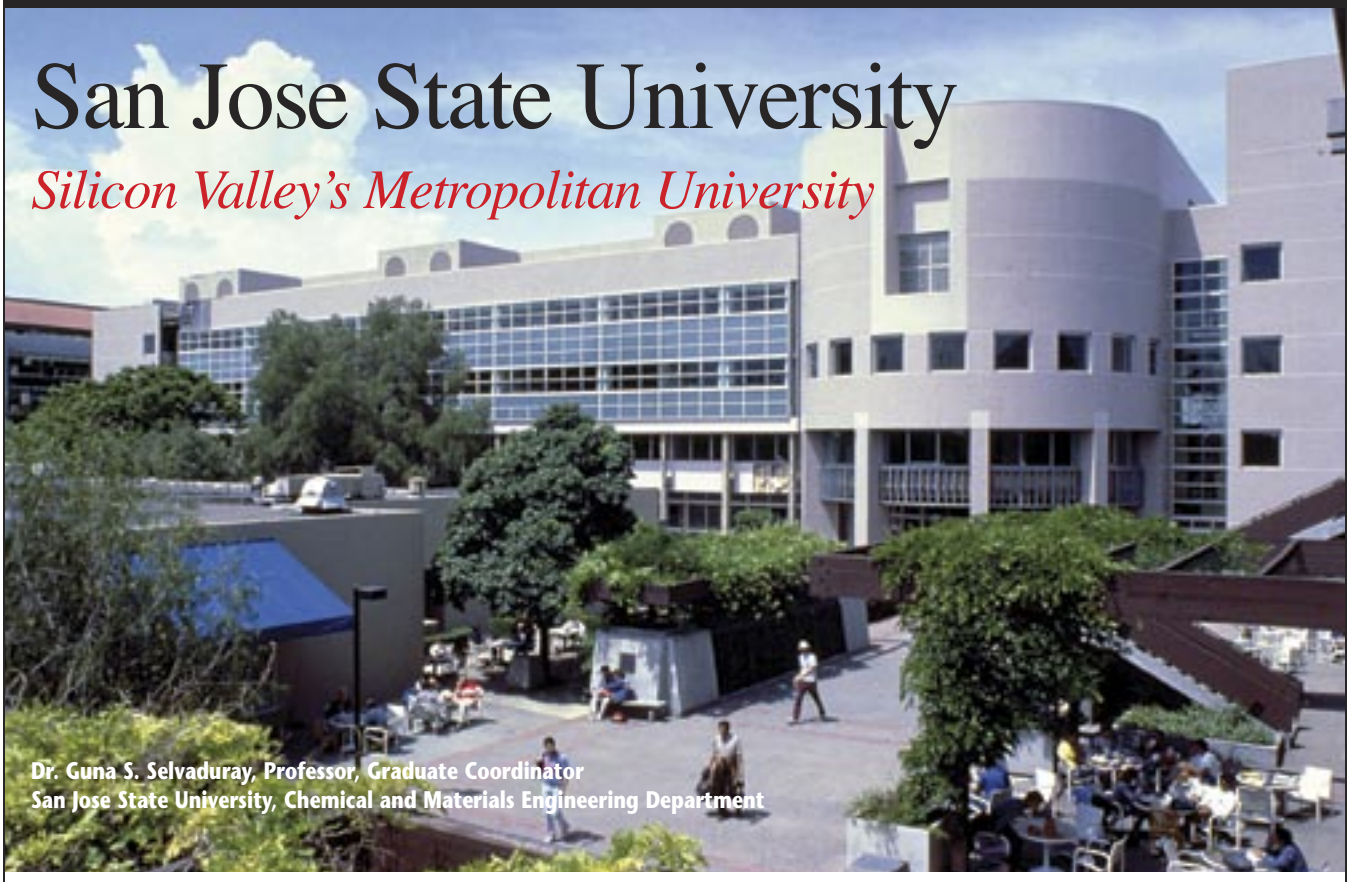

Dr. Guna S. Selvaduray, Professor, Graduate Coordinator
San Jose State University, Chemical and Materials Engineering Department

Over the last 20 years San Jose State University has undergone a significant amount of change – all for the better. Twenty years ago the university still had city streets running through it, leading to a notion of a fragmented campus. There were, of course, a myriad of other issues as well. The fact that downtown San Jose was also somewhat dilapidated did not help the university at all.

And then, changes started happening. One of the early changes was the closure of the city streets running through campus. This played a major role in instilling a sense of a cohesive campus. At around the same time, in August 1988, the new Engineering Building was completed, and had a major effect in propelling SJSU's College of Engineering to prominence.

More recently, the new Martin Luther King Jr. Library was completed in August 2003. This joint city-university library, the first of its kind in the entire USA, was completed ahead of schedule and under budget. It is a state-of-the-art facility and is the largest public library west of the Mississippi.

One of the transformations that SJSU has been going through is developing its identity as Silicon Valley's Metropolitan University, in addition to being the CSU System's flagship, especially for engineering. The university today blends very well with the rapid pace of urban redevelopment that has been going on in downtown San Jose, with the university community contributing significantly to downtown's economic well being. Before the end of 2005 the new San Jose City Hall, which will be only half a block away from campus, is expected to be completed. This is expected bring new vibrancy to the area and to the university as well, including greater collaboration between the City and the University. The City of San Jose, in its strategic plan, identified SJSU as a major partner in its efforts for continued economic development.

SJSU's College of Engineering Building.

SJSU's Martin Luther King Jr. Library, completed in August 2003, is a joint city-university library, the first of its kind in the entire USA. Completed ahead of schedule and under budget, it is a state-of-the-art facility and is the largest public library west of the Mississippi.

SJSU has eight colleges, with the College of Engineering being one of the most prominent ones. The College has six departments offering education programs that lead to degrees in twelve different disciplines, both at the BS and MS levels. A major effort that has been ongoing for more than 15 years is the development of interdisciplinary curricula and concentration areas that reflect the needs of the industrial base that surrounds SJSU.

The Master of Science in Engineering (MSE) Program was originally developed more than 15 years ago, and offers concentrations in a variety of

SJSU's educational philosophy emphasizes a hands-on practical education, based on a sound understanding of engineering fundamentals.

areas, including engineering management, electronic materials and devices, environmental systems, manufacturing systems, and microelectronic packaging. "Special concentrations" to further tailor the curriculum to suit a particular student's needs are also possible.

The MSE Program is built on the premise that competent engineers need both breadth and depth. All MSE concentrations require students to take engineering management, systems engineering, and engineering mathematics to meet the breadth requirement. Students also are required to complete a project or thesis that has industrial relevance. In addition to a project report or written thesis, students also must present their project/thesis verbally and be able to "defend" it. Typically, the breadth requirement and the project or thesis, jointly, account for approximately 50% of the curriculum.

A well defined set of classes for each concentration area is usually developed by one or more faculty members who are experts in that area, in consultation with an industrial advisory board. Typically the concentration area will consist of approximately 4 courses, with the students having the flexibility to take an additional one or two electives. Combined, these account for the other 50% of the curriculum.

The latest concentration area that is being developed is Biomedical Devices. Current projections predict significant growth in the biotechnology industry sector worldwide, with the ensuing demand for a well-educated and trained workforce capable of fueling both basic research and product and process development. In addition, what is known as Silicon Valley actually has a significant number of companies that develop and manufacture a variety of biomedical devices. These companies are also expected to grow significantly in the future.

Biomedical devices are also a critical part of the improved health maintenance capabilities being developed. This is an inherently interdisciplinary field that encompasses not just biology and biochemistry, but also several fields of engineering such as materials science and metallurgy, mechanical engineering and design, electrical engineering and signal processing, and ergonomics. As such, SJSU's College of Engineering is very well positioned to develop and offer this curriculum, which can serve its surrounding industrial community.

The curriculum was developed in close consultation with industry leaders and builds upon the College's vast engineering expertise. Four new courses are being developed. These are: Physiology for Engineers, Biomedical Devices, Biomechanics, and Regulatory Requirements. One existing course on Biomaterials is being revised. Other courses, such as Engineering Management and Engineering Mathematics are also being revised to make the contents more relevant to the biomedical device industry.

SJSU's educational philosophy emphasizes a hands-on practical education, based on a sound understanding of engineering fundamentals. Development of written and oral communications skills and teamwork skills are seamlessly integrated into the curriculum. This includes writing a variety of reports, making presentations using appropriate software, and mandatory team project participation. The concentration area coordinator for this new concentration area in Biomedical Devices is Dr. Guna Selvaduray (gunas@email.sjsu.edu) who may be contacted for further information, including entry and application requirements. ◆

SJSU's College of Engineering website: www.engr.sjsu.edu/coe/

MSE Program website: www.engr.sjsu.edu/ges/

Honeywell Appoints Barry Russell VP and General Manager for Electronic Materials

MORRIS TOWNSHIP, NJ – Honeywell has announced the appointment of Barry Russell as Vice President and General Manager for Honeywell Electronic Materials.

In this role, Russell is responsible for Honeywell's entire Electronic Materials business, which is one of the top five suppliers of materials to the semiconductor industry, developing and manufacturing a broad line of products used in the production and packaging of integrated circuits. He reports to Nance Dicciani, president and CEO of Honeywell Specialty Materials.

Russell joined Honeywell in 2000 from CFM Technologies, a Pennsylvania-based company that manufactures and markets materials, capital equipment and technology to the semiconductor and flat panel display industries. Prior to working for CFM, he was business manager in FMC Corp.'s Specialty Chemicals Group, responsible for electronic materials and fine chemicals product lines.

For the past two years, Russell ran Honeywell's Specialty Additives business as global segment leader. In his previous Honeywell positions, he was global segment leader for Performance Chemicals and was marketing director for Specialty Chemicals, where he worked in the electronic chemicals area, among others, to develop global growth strategies, while also developing strategic alliances with business partners worldwide.

Russell earned a bachelor's of science degree in chemical engineering from the University of Akron, Ohio, and an MBA from the University of North Carolina.

Carsem Announces New General Manager for M-Site Factory

SCOTTS VALLEY, CA – Carsem has announced that Mr. T.L. Soo recently joined the company as the new General Manager of the Carsem M-Site factory. Mr. Soo is replacing the former General Manager Mr. Ian Ee, who after 13 years as the GM will retire at the end of January. Mr. Soo reports directly to Carsem's Chief Operating Officer, Mr. S.W. Woo.

Mr. Soo has over 20 years of experience in the semiconductor and electronics industry. Prior to joining Carsem he was the General Manager at Fairchild Semiconductor in Petaling Jaya, Malaysia, and prior to that he was the General Manager of Operations at Asteria Industries, which is an Electronics Manufacturing Services (EMS) company. He has also held various engineering management positions at Motorola and Siemens and holds an MBA from Henley Management College.

S.W. Woo stated, "I am very pleased to have T.L. join our company. His extensive experience in both the semiconductor and EMS industry will provide a broad vision and will add new dynamics to the growth of Carsem."

Carsem, Inc. sales headquarters is located in Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Rohm and Haas Electronic Materials Names Chris Milton GM of Circuit Board Technologies Europe

MARLBOROUGH, MA – Rohm and Haas Electronic Materials has named Chris Milton to the position of General Manager, Europe, for the company's Circuit Board Technologies business. He will succeed Jean-Pierre Robic, who will focus on the Microelectronics business as General Manager, Microelectronic Technologies, Europe.

"As European circuit board manufacturers focus more on high-specification and specialty boards, we are challenged to develop and provide new materials and equipment technologies to help them in that objective. Chris has the skills, leadership qualities, and business development experience necessary to meet that challenge," said Patrice Barthelmes, President, Rohm and Haas Electronic Materials Europe, and President, Rohm and Haas Electronic Materials Circuit Board Technologies. "We are pleased to have Chris join the Circuit Board Technologies team."

Milton joined Rohm and Haas Electronic Materials (formerly Shipley) in 1996, where he most recently served as European Strategic Business Director for the company's Packaging and Finishing Technologies business. Since joining Rohm and Haas Electronic Materials, he has held several senior positions in business development and marketing within the organization. Prior to that, he held a variety of management roles in the mechanical engineering, chemicals, and plastics industries in the UK and Germany. In his new role, Milton will be responsible for developing new markets and growing the Circuit Board Technologies business in Europe. Milton is a graduate of Oxford University and has an MBA from Cranfield School of Management in England.

Additional information is available at http://electronicmaterials.rohmhaas.com.

Silicon Bandwidth Names Lavi Lev to Board of Directors

Industry leader accepts board position

SAN JOSE, CA – Silicon Bandwidth, Inc., a leading innovator of high-performance, low-cost interconnect solutions for computing and communications platforms, has announced that Mr. Lavi Lev has accepted nomination to its Board of Directors.

In his twenty-plus years in the semicon-

ductor industry, Mr. Lev developed system-on-a-chip and microprocessor solutions for many devices, from consumer electronics and personal computers to workstations and supercomputers. Author of more than fifteen patents in areas as diverse as CAD techniques, digital and analog circuit design, and advanced Internet technologies, he earned a Bachelor of Science degree in Electrical Engineering from Technion, Israel Institute of Technology. Mr. Lev was previously Executive Vice President and General Manager of Cadence Design Systems, Inc., San Jose, CA.

Silicon Bandwidth's President and CEO Ajit Medhekar said, "Lavi is a highly-regarded leader over and above his many achievements in high-tech. His sound judgment in making business decisions helped guide an industry giant like Cadence through a period of exceptional corporate growth. He is a remarkable talent."

For more information, please visit www.siliconbandwidth.com.

SEMI Expands Nanotechnology Emphasis

Lubab L. Sheet named Senior Director of Nanotechnology

SAN JOSE, CA – SEMI has announced that Lubab L. Sheet has been named senior director of nanotechnology and will spearhead expanded efforts to clarify and exploit new technology and market opportunities for the organization's global membership.

Together with the launch of a comprehensive market study, a global executive conference and standards development activities, the newly-created position confirms the increasing emphasis SEMI will place on nanotechnology-related information, public policy, services and events.

"Semiconductor equipment and materials companies have long been working on nanoscaled manufacturing processes. Yet, as an industry, we need better understanding about the future of nanotechnology in microelectronics and business opportunities in other sectors," said Lam Research President and Chief Operating Officer Steve Newberry, who is a member of the SEMI International Board of Directors and chairs the board's Nanotechnology Working Group.

In July, SEMI and IEEE signed a memorandum of understanding to support their respective programs to create nanotechnology and MEMS (micro-electromechanical systems) standards. In November, SEMI hosted the inaugural NanoForum conference in Austin, Texas, with over 400 international delegates from multiple industries. SEMI NanoForum 2005 is scheduled for October 3-6, 2005 at the San Jose Marriott (CA).

In cooperation with the Semiconductor Industry Association (SIA), SEMI has also launched a comprehensive market study on nanotechnology applications in the electronics industry. "Global Nanoelectronics Markets and Opportunities," to be available in the third quarter of 2005, will provide definition of the rapidly-emerging global nanoelectronics markets and offer a global perspective of requirements and opportunities for equipment and materials suppliers.

Effective immediately, Sheet reports to SEMI Executive Vice President Paul Davis and will coordinate the association's global services in nanotechnology. Previously, she served as the research development director at SEMI. Prior to her employment with SEMI, Sheet was the vice president of content and co-founder of SemiSales, a management consultant for Rose Associates and a member of the Silicon Development Group at Applied Materials, Inc. She has a bachelor of science in materials science from San Jose State University and an MBA from Santa Clara University.

For more information visit the SEMI website at www.semi.org.

Silicon Border Awarded Development Grant from Mexico to Re-establish Chip Manufacturing in North America

Federal and state investment and expanded exclusivity agreement signal progress for semiconductor-focused science park planned in Baja California

SAN DIEGO, CA – Silicon Border Development announced it has finalized agreements with the Mexican federal and Baja California state governments for a development grant and an expanded exclusivity agreement for a specialized science park that will establish a strategic alternative for cost-effective and centralized semiconductor operations in North America.

"This dual support from our North American neighbor is important in establishing momentum and moving to the next step in our development roadmap," said DJ Hill, chairman of Silicon Border. "We are excited to tap the tremendous synergy that is possible between the U.S. semiconductor industry and the Mexican manufacturing community to increase the stability and success of the global high-tech supply chain."

The federal government of Mexico and the State of Baja California are jointly providing a grant to Silicon Border Development to develop the high-technology park in Mexicali, capital city of Baja California. The amount of the grant was not disclosed, but a portion comes from Mexico's federal Prosoft program, formed to support technology development throughout the country.

"The continuing collaboration among federal and state government and private enterprise is a reflection of Mexico's growing role in a technology-driven global economy," said Governor Eugenio Elorduy Walther of Baja California, Mexico. "The State of Baja California is a leading region for technology development efforts energized by President Fox, and we welcome the opportunity to host a world-class center for advanced semiconductor operations that will strengthen the foundation of high-tech industry."

The expanded agreement with the State of Baja California grants Silicon Border an additional 24 months of exclusivity for the development of a technology-focused park, including commercial land use and access to mission-critical water, electricity and gas in a 15-square mile area just two hours from San Diego.

Silicon Border is a 10,000-acre high-technology science park catering to the specialized needs of the semiconductor and other capital-intensive technology sectors. Planned for development along the U.S.-Mexico border in Mexicali, Silicon Border enables a cost-effective and competitive manufacturing alternative in North America for emerging and global companies. Improving upon the world's leading technology parks, the park's 15 square miles of world-class infrastructure and education will support the stringent requirements of the semiconductor, flat panel display, telecom, optoelectronic and biotechnology industries. More information about Silicon Border is available online at www.siliconborder.com.

Kyocera Receives DSCC Certification

For its Assembly Technology Division

SAN DIEGO, CA – Kyocera America, Inc. announced that it has received DSCC (Defense Supply Center, Columbus) Level Q Transitional Certification for Assembly and Test, per MIL-PRF-38535, FSC 5962, allowing Kyocera America to perform assembly and test services for defense applications.

Kyocera America has been a DSCC QML approved vendor for many years, but with this new certification, Kyocera America will be a DSCC Qualified Manufacturer

(QML) 38535.

The Assembly Technology Division of Kyocera America, Inc., located in San Diego, CA., offers state-of-the-art wirebond and flip chip turnkey assembly services for prototype, quick turn, as well as volume, commercial and defense-grade requirements. Besides being QML certified, Kyocera is ITAR registered, and both ISO 9000-2000 and ISO 14,000 certified.

Advanced Interconnect Technologies Qualifies its High Reliability SOIC Packages for Next-Generation Automotive and Power Applications

Provides industry's first fully qualified Hi-Rel narrow body SOIC packages with a MSL 1, 260° C rating and zero delamination

SINGAPORE – Advanced Interconnect Technologies (AIT) has announced the qualification of a new family of High-Reliability (Hi-Rel) narrow body SOIC packages. This qualification allows AIT to provide its customers with zero delamination after MSL 1, 260°C pre-conditioning testing which improves the overall reliability of the end product significantly. This milestone helps AIT's cost conscious customers get unlimited floor life and cost savings on packaging and shipping of units, while ensuring the highest levels of robustness during the critical reliability stress tests.

AIT has leveraged industry partnerships to ensure the world's best materials are used in design process in order to attain the highest qualification levels during the reliability testing process. Leading supplier Samsung Techwin helped AIT in the qualification of this package by developing special PPF leadframes with modified surface roughness which adds mechanical bonding and an optimized plating condition.

This qualification brings AIT another step closer to achieving the world's most robust SOIC package with a set of bill of materials that are defined as Green and Pb-Free ready.

"This industry milestone fully reinforces AIT's mission to provide the market with superior green packaging solutions that offer the highest degree of robustness and reliability," said Mike McKerreghan, chief operating officer at AIT. "Working with quality material suppliers such as Samsung Techwin are key factors in the development of packages that meet the ever increasing demands for reliability."

AIT's fully qualified SOIC packages are now available. Pricing is based on volume and configuration.

For more information about the company, its products and services please visit www.aithome.com.

ITC Review Phase of Patent Litigation

SCOTTS VALLEY, CA – Carsem has announced that the International Trade Commission (ITC) is now in the final review phase of the investigation related to a complaint filed by Amkor Technology, Inc. on November 17, 2003. The complaint accused Carsem of infringing a total of 21 claims of Amkor's United States Patent Nos. 6,433,277, 6,455,356, and 6,630,728 by making, using, selling, offering for sale, and importing into the U.S. Carsem's MLP (Micro Leadframe Package) products.

On November 18, 2004 the Administrative Law Judge Honorable Charles E. Bullock issued an Initial Determination that Amkor's asserted claims were invalid, not infringed or both, and that no violation of Section 337 of the Tarriff Act of 1930 occurred. There were four claims found to be infringed but those same four claims were found to be invalid. There were also four other different claims that were found to be valid but Carsem was found to have not infringed. The result of this is that no exclusion order has been imposed on the importation of Carsem assembled MLP products into the United States and Carsem and its customers remain free to import.

On February 1, 2005 the ITC issued a Notice that it will conduct a complete review of the Administrative Law Judge's Initial Determination and extended the deadline for completing the investigation to March 31, 2005.

Carsem, Inc. sales headquarters is located in Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Carsem Receives Excellent Achievement Award from ELMOS Semiconductor

SCOTTS VALLEY, CA – Carsem has announced that they were recently presented with an Excellent Achievement award from ELMOS Semiconductor.

Mr. Dieter Bitterhoff, Manager of Assembly and Off-Shore Operations at Elmos, presented the award to David Comley, Carsem's Group Managing Director, for recognition of Carsem's achievement of excellent assembly performance for automotive products for 2003 and 2004.

Mr. Bitterhoff stated, "Carsem has provided outstanding performance over the previous period and an excellent customer service with prompt and pro-active support."

The member of the Board for Production of Elmos, Mr. Reinhard Senf, further stated, "Carsem is also our strategic partner in regards of our planned move into the MLP, SiP and power MLP package family."

Mr. Comley, stated, "I am very proud to have received this award from Elmos. The automotive electronics industry is very demanding and our team of engineers and support staff have done an outstanding job in partnering with the Elmos organization. We look forward to supporting Elmos well into the future."

ELMOS Semiconductor AG is a developer and producer of customer specific system solutions based on silicon. For more than 20 years, roughly 90 percent of the turnover is achieved with ASICs for automotive electronics. ELMOS is listed on the TecDAX 30 of the German Stock Exchange. Web site: www.elmos.de

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Sweden's PartnerTech Selects F&K Delvotec Bondtechnik GmbH as New Business Partner

F&K Delvotec has announced that PartnerTech in Sweden has selected F&K Delvotec Bondtechnik GmbH as a business partner for die and wire bonding systems for multi-chip component handling, in their new contract manufacturing services (CMS).

"We are pleased to be PartnerTech's supplier of choice and having gained their confidence in the development of their new CMS Business activity", says Joseph Flynn, F&K Delvotec's Sales & Marketing Manager Europe. "We look forward to working with PartnerTech to jointly guarantee state-of the-art technology and quality for their products. Our cooperation with PartnerTech is a very important step into the contractor manufacturing business in Europe".

The strategic decision to work closely with F&K Delvotec to support a wide range of customer needs today while being ready to serve new and emerging market demands with requirements for superior bond qual-

ity, productive throughput, flexibility and reliability provided by F&K Delvotec convinced us of this supplier", says Luciano Pasquariello, Technical Program Manager at PartnerTech.

PartnerTech develops and manufactures products under contract for leading companies, primarily in telecommunications, IT, the engineering sector and medical technology. The company (www.partnertech.com), which has approximately 1,300 employees, reported revenue of more than SEK 1.3 billion in 2003 and is quoted on the O list of the Stockholm Stock Exchange.

F&K Delvotec Bondtechnik GmbH is a leading manufacturer of die and wire bonding equipment. With subsidiaries in Europe, North America and Asia and a base of several thousand installed systems F&K Delvotec is the leading suppliers' preferred back-end partner for complex tasks in the semiconductor and electronics industry. F&K Delvotec's products cover the entire range of die bonding, wire bonding and bond test equipment.

More information about F&K Delvotec is available under www.fkdelvotec.com.

BE Semiconductor Industries NV Announces Restructuring to Improve Operational Profitability

DRUNEN, THE NETHERLANDS – BE Semiconductor Industries N.V., a leading manufacturer of assembly equipment for the semiconductor industry, has announced a restructuring of its operations focused principally on a workforce reduction at its Dutch packaging and tooling manufacturing operations in Duiven and Brunssum of 81 employees, or approximately 10% of total fixed headcount worldwide, as part of a plan to address the current downturn in the semiconductor industry. In addition, Besi will phase out the use of approximately 50 temporary workers at the Duiven facility. A component of the restructuring will be the closing of Besi's tooling facility in Brunssum, the Netherlands in the first half of 2005. The personnel terminations are expected to occur in the first quarter of 2005. Besi intends to take a restructuring charge in the fourth quarter ending December 31, 2004 to cover the estimated costs of this workforce reduction which is not expected to exceed € 5.6 million. Furthermore, in the fourth quarter, Besi expects to incur a charge of up to € 1.7 million relating to the write down of certain inventories and work in progress, which would have the effect of reducing gross margins for the fourth quarter by up to 5.5 percentage points.

In commenting on the restructuring plan, President and Chief Executive Officer Richard W. Blickman noted: "Ongoing economic uncertainties and industry over-capacity is resulting in customers delaying scheduled deliveries, capacity investment and the funding of strategic programs. We currently forecast that our sales for the fourth quarter of 2004 will decline by approximately 20% as compared to the third quarter level. We have taken the difficult, but necessary, steps to realign our operations in response to reduced demand. The restructuring also is consistent with Besi's plans to reduce exposure in high cost geographies and to rely more on low cost manufacturing regions. However, we continue to believe that the fundamental factors affecting demand for semiconductors and semiconductor assembly equipment remain positive over the long-term."

The Company expected to report final fourth quarter and year 2004 results on February 8, 2005.

BE Semiconductor Industries N.V. designs, develops, manufactures, markets and services die sorting, flip chip die-attach, molding, trim and form, singulation and plating systems for the semiconductor industry's assembly operations. Its customers consist primarily of leading U.S., European, Asian, Korean and Japanese semiconductor manufacturers and subcontractors.

Honeywell Opens New Electronic Materials Manufacturing Facility in Arizona

State-of-the-art plant to increase capability for the production of customized chemicals for advanced semiconductors

MORRIS TOWNSHIP, NJ – Honeywell has announced that its Electronic Materials business has opened a new, 40,000-square-foot manufacturing facility in Chandler, Arizona, boosting Honeywell's capabilities to supply both straight and advanced, customized electronic chemicals for the semiconductor industry.

The state-of-the-art facility significantly increases Honeywell's production capacity in Chandler for electronic chemicals, which are used by a broad range of manufacturers to build integrated circuits.

With the opening of the Chandler facility, Honeywell now has three of the newest electronic materials facilities in the United

States. The other two are Honeywell facilities in Bryan and Mansfield, Texas.

The new Chandler facility increases Honeywell's capability to manufacture application specific wet-etch and cleaning chemistries. These chemicals are customized to perform specific operations such as cleaning, which removes organic, metal and particle contaminants during semiconductor manufacturing while leaving other critical materials untouched.

Other new products include wafer-thinning materials that thin the wafer substrate on which chips are built, helping to better dissipate the massive heat produced by today's high-powered semiconductors.

One of Honeywell's strengths is high-purity and ultra-high-purity chemical production that is critical to high-end semiconductor manufacturing processes. Honeywell's technology is capable of producing chemicals into the part per trillion (PPT) purity level.

The opening of the new facility follows Honeywell's acquisition in November 2004 of Mitsubishi's 40 percent stake in GEM Microelectronic Materials, which gave Honeywell sole ownership of the venture, which supplies electronic chemicals. Construction of the Chandler facility had been started as part of the joint venture. Also in 2004, Electronic Materials acquired a product line and manufacturing facility in Thailand that expanded Honeywell's capabilities in chip packaging, specifically in the area of thermal management.

For additional information, please visit www.honeywell.com.

Carsem Receives Outstanding Supplier Award From TouchSensor Technologies

SCOTTS VALLEY, CA – Carsem has announced that they were presented with an Outstanding Supplier of the Year Award for calendar year 2004 from TouchSensor Technologies, LLC.

The award was presented by Greg Poissant, TouchSensor's Director of Quality, during a ceremony held at TouchSensor on February 10, 2005 and was based on Carsem's commitment to Quality, On-time Delivery and overall Customer Satisfaction.

Mr. Poissant stated, "Carsem was selected among 15 suppliers because of their dedication to providing an excellent product and world class delivery"

Rick Flowers, Carsem's Vice President of North America Sales, stated, "I am very pleased that TouchSensor chose Carsem for this prestigious award. This award reflects our commitment to providing our customers with quality services and building strong partnerships. We look forward to working with TouchSensor well into the future."

TouchSensor designs and manufacturers touch-sensistive user-interface panels based on its patented Field-Effect technology. Companies choose TouchSensor's custom panels for their leading-edge designs on appliances, fitness machines, drink dispensers, and industrial products. A private company founded in 1996, TouchSensor was named a 2003 KPMG Illinois High Tech Award winner. The company's headquarters is located outside Chicago in Wheaton, Illinois. Web site: www.touchsensor.com

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, Suzhou, China and sales offices across the USA, plus the UK. Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Kulicke & Soffa Sells Wedge Bonder Designs to Orthodyne Electronics

WILLOW GROVE, PA – Kulicke & Soffa Industries, Inc. has announced the sale of its wedge bonder technology to Orthodyne Electronics located in Irvine, California. The sale includes both the design of wedge bonding machines and the licensing of intellectual property.

Jack Belani, K&S senior vice president, Wire Bonding Division and Corporate Marketing noted that "Since wedge bonders represented less than 1% of our sales last year, it makes more sense for us to focus our R&D resources on our major product lines including ball bonders and test products. We will, however, continue to sell refurbished machines and support our installed base with spare parts and service. Additionally, we will also sell our existing wedge bonder models for a period of approximately 2 years, during which time Orthodyne will continue to develop and enhance their product portfolio with K&S's technology. We are pleased to be working with Orthodyne, whom we believe is well positioned to continue to serve the marketplace with Wedge bonders."

Gregg Kelly, president of Orthodyne notes, "Wedge bonding equipment is our company's primary focus. The new technology and designs purchased from K&S will enhance our product offerings and allow our engineers to create new, best-in-class machines that have their roots in both K&S and Orthodyne designs. We look forward to extending our leading market position as we focus on wedge bonding solutions for our customers."

Kulicke & Soffa's web site address is www.kns.com.

Introduction of New UV LIGHT SOURCE GRANDE for Large Substrates Over 18 Inches

OAI expands its successful Light Source System to accommodate new displays

SAN JOSE, CA – OAI announces the expansion of its successful line of UV Light Sources to handle larger substrates over 18" x 18". The new UV LIGHT SOURCE GRANDE (LSG) combines all the technical features of OAI's standard Light Sources with the latest most innovative design and engineering to meet the demands of its customers in today's ever changing markets. Collimating mirrors are used instead of collimating lenses when the substrate size is 18" or more. The LSG systems have collimating half angles of less than 2 degrees combined with exceptional uniformity. LSG is now available in 5 and 8 kW with constant intensity controllers.

The new LSG is installed and being used successfully in the United States, China and Taiwan. Applications include UV exposure of substrates for displays and for multisubstrates under one exposure. The LSG combined with OAI's alignment system is used in Fodel™ applications.

OAI is a leading manufacturer of precision equipment used in the semiconductor, MEMS, and compound semiconductor industries for 30 years.

Located in Silicon Valley, OAI can be contacted via email: sales @oainet.com, phone: 408-232-0600 or fax: 408-433-9904.

Carsem Opens Taiwan Sales Office

SCOTTS VALLEY, CA – Carsem has announced that they recently opened a sales office in Taichung, Taiwan. In addition, Mr. Max Lee joined Carsem as the Account Manager for the Taiwan Region.

Mr. Lee reports directly to Gerry Blackholly, Carsem's Director of Asia Sales, and he will be responsible for all sales related activity for the Taiwan Region. Lee has over 5 years of experience in the semiconductor industry. Prior to joining Carsem he worked for Lingsen Precision Industry and Silicon Application Corp., both based in Taiwan.

Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Cobar Solder Products Announces New Low-VOC Flux Technology Ideal for Lead-Free

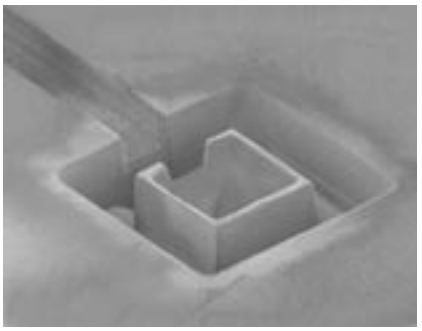
LONDONDERRY, NH – Cobar Solder Products announces the introduction of 94QMB9 a low-VOC soldering flux ideally suited for lead-free soldering in wave and selective soldering systems. It evaporates more readily than VOC-free formulations and thus reduces preheating time and the potential for oxidation and splatter, which allows for maximum equipment through put and energy savings.

Cobar's 94QMB9 is an innovative no-clean flux containing DI-water and alcohol. This flux technology features a proprietary, non-ionic activator system that exhibits the functionality of a block-polymer. Its reactivity is released and boosted beyond a threshold activation temperature. 94QMB9 withstands the higher temperatures required for lead-free soldering while maintaining its wetting characteristics. Its robust formula takes advantage of the latest advances in synthetic materials and delivers the wetting performance needed in demanding lead-free soldering applications.

Cobar Solder Products is the U.S. subsidiary of the Cobar Group, a multi-million dollar corporation with operations and distributors in all major areas of the world. Cobar is a recognized leader in lead-free and VOC-free soldering materials.

For more information, particularly with regard to lead-free soldering, visit www.cobar.com, or contact Cobar Solder Products, 53 Wentworth Avenue, Londonderry, New Hampshire 03053 USA, Tel. (603) 432-7500, Fax (603) 432-7519.

JPSA Laser Announces UV Laser Micro-machining for Medical Device Manufacturing



HOLLIS, NH – J P Sercel Associates (JPSA Laser) offers precision UV laser micromachining services – with micron-scale features and sub-micron tolerances - for a variety of medical device manufacturing applications. Typical applications include micro-fluidics, sensors, nozzles, micro-screens, particle traps, MEMS, MOEMS, micro-dicing, biosensors (lab-on-a-chip), micro-vias, photoablation, photo-machining, micromachining of plastics, ceramics, hard dielectrics, glass and metals, non-destructive high-resolution marking, micro-lithography to 1 micron resolution, high speed drilling, selective material ablation, doping, annealing and more. Materials processed include polymers and plastics, ceramics, glass materials, metals, semiconductor materials, diamond and precious metals, and others. JPSA Laser's core capabilities include expertise in UV materials processing at 355nm, 351nm, 308nm, 266nm, 248nm, 193nm, and 157nm wavelengths.

JPSA Laser's contract manufacturing facility houses state-of-the-art UV excimer and DPSS laser workstations. The applications laboratory is also equipped with a host of diagnostic equipment for laser process development and characterization. JPSA engineers have developed F2 laser, optics, calorimetry, and beam delivery technology, allowing JPSA to offer comprehensive testing of VUV optics and materials processing services at 157nm. Most of the JPSA laser systems are equipped with state of the art air bearing motion stages to ensure high precision and accuracy.

JPSA Laser's core capabilities include exJPSA products and services include UV excimer and DPSS laser micro machining systems, UV and VUV laser beam delivery systems, UV laser materials processing development, optical damage testing, and excimer laser refurbishment services. For more information, visit www.jpsalaser.com, or contact the company at 17D Clinton Drive, Hollis, NH 03049 USA, Tel. 603.595.7048, fax 603.598.3835.

Carsem Increases High-Density MLP Options

SCOTTS VALLEY, CA – Carsem, a leading provider of turnkey packaging and test services to the semiconductor industry, has announced that they have increased the number of package size options of the High-Density MLP (Micro Leadframe Package) family. Carsem MLP's are QFN (Quad Flat No-lead) and SON (Small Outline No-lead) type packages that are compliant to JEDEC's MO220, and MO229 standards.

The High-Density MLP uses a leadframe strip that achieves the very high unit densities used in Carsem's advanced saw-singulation concept. However, because of the efficiency of the High Density mechanical-singulation designs, the throughput is significantly higher when compared to the sawn version and therefore a more cost effective solution. There are two designs of the High-Density MLP, one has the leads on two sides of the package, MLP Dual High-Density (MLPDH), and the other is the MLP Quad High-Density (MLPQH), which has leads on all four sides of the package. Earlier this year Carsem began shipping production volumes of the MLPDH with a 2x3 mm body and 6 leads (3 per side) as well as the MLPQH with a 3x3mm body with 12 leads (3 per side) and 16 leads (4 per side). The additional option for the MLPDH is a 5x6 mm body with 8 leads and it has the same footprint as an 8 lead SOIC. The additional options for the MLPQH are a 4x4mm with 16 and 20 leads, a 5x5 mm with 32 leads and a 7x7 mm with 48 leads. The High-Density MLP is currently only manufactured in Malaysia.

According to Paul Smith, Carsem's Director of Marketing, "One of the advantages of the High-Density MLP is that it gives us a tremendous increase in our throughput and capacity which provides our customers with a very cost effective solution for products that run consistently high volumes. Another advantage is that the leadframes

have been designed to incorporate the use of strip-testing, which will further improve the throughput and enhance yields for the final test portion of the process."

Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Kyocera Expands Flip Chip Assembly

To offer 12-Inch wafer dicing services

SAN DIEGO, CA – Kyocera America, Inc. has announced that it has expanded its flip chip assembly operations to include 12-inch (300mm) wafer dicing. This new capability will increase Kyocera America's wafer dicing capacity by 30%, improving throughput times and yields after dicing.

"We have added a 12-inch wafer dicing machine to support increased semiconductor trend towards 300mm wafer production," said Yasihiro Takai, General Manager, Assembly Technology Division. "It can be used on Si, SiGe and InP wafers, and will be especially helpful when working with semiconductor start-up companies that are going directly to 300mm technology."

Kyocera worked very closely with Disco, the manufacturer of the machine, to develop a special wafer-cleaning feature.

The Assembly Technology Division of Kyocera America, Inc., located in San Diego, CA, offers state-of-the-art wirebond and flip chip turnkey assembly services for prototype, quick turn, as well as volume, commercial and defense-grade requirements. Besides being QML certified, Kyocera is ITAR registered, and both ISO 9000-2000 and ISO 14,000 certified.

Carsem Offers Remote Access Test Development

SCOTTS VALLEY, CA – Carsem has announced that they now offer the ability to access Carsem's ATE (Automatic Test Equipment) systems via a direct VPN (Virtual Private Network) connection and a Carsem secured terminal client server. The high security link allows customers direct access to any of Carsem's tester platforms

North American Semiconductor Equipment Industry Posts January 2005 Book-To-Bill Ratio of 0.80

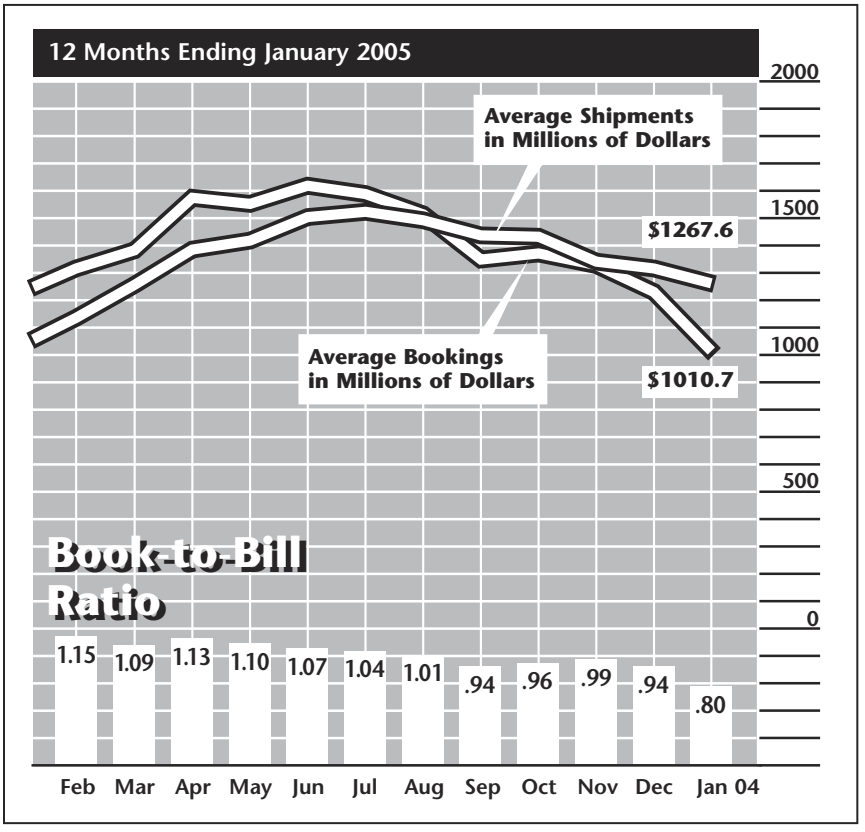
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.01 billion in orders in January 2005 (three-month average basis) and a book-to-bill ratio of 0.80 according to the January 2005 Book-to-Bill Report published today by SEMI. A book-to-bill of 0.80 means that $80 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in January 2005 was $1.01 billion. The bookings figure is 18 percent below the revised December 2004 level of $1.24 billion and 18 percent below the $1.23 billion in orders posted in January 2004.

The three-month average of worldwide billings in January 2005 was $1.27 billion. The billings figure is four percent below the revised December 2004 level of $1.32 billion and 23 percent above the January 2004 billings level of $1.03 billion.

"The three-month average bookings figure for new semiconductor equipment is now at the lowest level since November 2003," said Stanley T. Myers, president and CEO of SEMI. "Total bookings declined sharply in January and are now about 37 percent below the cyclic peak observed in June 2004."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

for the purpose of doing real time test program debug, product engineering and device performance analysis.

The capability provides customers with the ability to work remotely with the Carsem factory staff in performing test program development efforts and product engineering support on a wide variety of tester platforms including Credence, Eagle, LTX, and Teradyne systems. It also gives the ability to achieve a collaborative effort to resolve device specific test issues on a real time basis, which significantly improves time-to-market and reduces cycle times. In addition, Carsem recently established a dedicated test development lab at their S-site, which currently has a Credence ASL-1000 tester but will expand over time to include a wide variety of ATE systems based on customer demand.

According to Allan Calamoneri, Carsem's Vice President of Test Business Development, "One of the advantages of this remote access is that it allows us to establish direct tester links and communication between our customer's engineer and the Carsem test team which streamlines the product introduction process and learning curve dynamics associated with ramping products into production volumes. Another key advantage is that it maximizes the utilization of limited high cost capital resources."

Carsem, Inc. sales headquarters is located in Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Silicon Wafer Shipments Experience Double-Digit Growth for the Third Year in a Row

2004 revenues increase by 26 percent

SAN JOSE, CA – Worldwide silicon wafer area shipments increased by 22% in 2004 when compared to 2003 area shipments according to the SEMI Silicon Manufacturers Group (SMG) in its year-end analysis of the silicon wafer industry. Revenues also grew by 26 percent in 2004 compared to 2003.

Silicon wafer area shipments in 2004 totaled 6,262 million square inches (MSI), up from the 5,149 million square inches shipped during 2003. Revenues grew to $7.3 billion from $5.8 billion posted in 2003. Fourth quarter silicon area shipments declined 9% from the prior quarter though were 7% higher than the fourth quarter of 2003.

"2004 was a very robust growth year for the silicon wafer suppliers as both units and revenue grew at over 20 percent," said Makoto Tsukada, chairman SEMI SMG and general manager of Shin-Etsu Handotai Co., Ltd. "Even though 300 mm wafer shipments were over 15 percent of the total shipments by the fourth quarter and total wafer shipments surpassed the 2000 peak, total revenues in 2004 for silicon wafers were below the 2000 level. As a result, wafer manufacturers remain cautious investing in new production capacity."

The Silicon Manufacturers Group acts as an independent special interest group within the SEMI structure and is open to SEMI members involved in manufacturing polycrystalline silicon, monocrystalline silicon or silicon wafers (e.g., as cut, polished, epi, etc.) not including reclaimed wafers. The purpose of the group is to facilitate collective efforts on issues related to the silicon industry including the acquisition of market information and statistics about the silicon industry and the semiconductor market.

For more information, visit SEMI at www.semi.org. ◆

Chip Supply, Inc.

When performance counts, you need the professionals at Chip Supply. No matter what you are designing; from portable consumer products to aviation electronics to medical imaging systems, Chip Supply can deliver the appropriate electronic interconnect solution to meet your performance goals.

Chip Supply adheres to MIL-STD-883 and MIL-STD-750 inspection flows. Both can be done on our automated equipment or manually as shown above.

Chip Supply was founded in 1978 in Orlando, Florida. A pioneer, making bare die available, Chip Supply was formed to fill a niche market by supplying to Lockheed Martin at a time when the hybrid industry was just getting started and customers had limited avenues to acquiring devices in bare die form. From their roots in the military electronics marketplace, Chip Supply has amassed a wealth of technologies in the electrical interconnect area that empower its customers in a wide range of markets and applications.

Headquartered in Orlando, Chip Supply occupies five buildings on a campus that houses over 42,000 square feet of which over 10,000 square feet is a clean room environment. Chip Supply has over 125 employees, and is the largest added value reseller of bare die in the world today. Chip Supply also maintains sales offices in key market areas in North America and Europe, and maintains worldwide sales representation. Their customer base ranges from military and aerospace markets to the increasingly prominent medical market. Customers for bare die continue to emerge in all markets as the need for smaller form factor devices intensifies.

From their inception, Chip Supply has offered bare die to the hybrid/MCM manufacturers, and continue to ship more bare die than any other processor. With the ability to select from over 25 of the world's leading semiconductor manufacturers they have a diverse

Chip Supply uses automated equipment in the assembly area for die attach and wire bonding requirements.

Chip Supply test services include digital and mixed-signal testing and hot and cold temp wafer probe.

product offering covering discrete, analog, digital, memory and mixed-signal devices and can offer their customers a complete solution to their active component needs. Companies like Texas Instruments have entrusted their bare die sales operations to Chip Supply by utilizing their "Master Die Distributor" designation. Under this agreement, Chip Supply essentially serves as the post-wafer fabrication processor for the semiconductor manufacturer, leaving the marketing and administration of the die program to Chip Supply.

Customer Service/ Quality Assurance

Chip Supply is considered the number one value added die processor in the United States. They are committed to both the manufacturers that supply them silicon and the customers in which they service. Customer service is number one with Chip Supply. The goal is not just to meet the customer's expectations, rather exceed them. In an effort to achieve that goal Chip Supply holds quarterly company reviews and issues an annual customer satisfaction survey. At the top of their concern is the quality of products and services that the customer receives. Chip Supply chooses to only work directly with their semiconductor manufacturers. This choice allows them to verify the pedigree of the material and ensure an open line of communication concerning their purchases.

Also important to Chip Supply is their ability to remain at the forefront of their business in regards to quality. Chip Supply's Director of Quality Assurance, Jim Wolbert, sits on several committees. He is actively involved in Jedec-JC13 and is the Chairman of the TC47/ PT62258 project team for International Standardization for Bare Die. A note worthy detail about Mr. Wolbert; he was recently presented, by the Die Products Consortium (DPC), the Industry Achievement Award for his leadership in developing international standards for semiconductor die products.

Production and Assembly

Chip Supply receives material from their manufacturers in both singulated die and wafer form. The material received in wafer form is diced using one of three wafer dicing systems that are fully automated. These systems can handle wafers up to 8 inches in diameter. Chip Supply's saw operators are all very experienced and highly knowledgeable about the ways in which to handle wafers. Known for their expertise, Chip Supply's die inspectors are some of the best in the industry. All of their inspectors are required to be certified per MIL-STD-883 Method 2010 and MIL-STD-750 Methods 2072 and 2073. After inspection devices will be prepared for shipment, sent to the lab for testing or assembled into a custom package as required by their customers. Assembly capabilities exist in both the custom military packaging as well as ball grid array devices. Both single chip and multi-chip configurations are offered.

Technicians monitor dicing of wafers in clean room dedicated to saw operations.

Custom Packaging

Military packaging, Tape Automated Bonding (TAB), and custom Chip Scale Package (CSP) design and assembly are just some of the many ways Chip Supply can empower unique solutions across their customer base. To supplement the manufacturers standard test, they offer both digital and mixed signal test capabilities, hot and cold wafer probe, environmental screening and failure analysis.

Chip Supply offers non-standard interconnect solutions to a wide range of markets and applications. To the military marketplace, Chip Supply offers hermetic packaging in any number of traditional mil packages, both metal and ceramic. Some examples of the packages they assemble are LCC, Cerdip, Flatpack, QFP, Cans and more in pin counts to meet any application. Programs that require now obsoleted packages and/or devices can now turn to Chip Supply, a QML certified facility, to extend the life of their programs without costly board revisions.

Also available through Chip Supply is Tape Automated Bonding (TAB) and Tape Carrier Packaging (TCP). These offerings are for die products that make use of the flex tape carrier as the interconnect to other active circuitry. Both are considered easily testable and in some cases can be used for assembly processes, such as FlipTAB, in MCM's. Using a variation of the FlipTAB process Chip Supply can offer customers modules in vertical stacks.

In applications where bare die may not be the best solution, Chip Supply can offer significant form factor reductions by utilizing Chip Scale Packaging (CSP) and Wafer Level Chip Scale Packaging (WLCSP). Chip Supply's standard process for manufacturing CSP consists of attaching a bare die onto a laminate (BT) substrate, wire bonding the bond pads to the substrate, transfer molding, ball attach and marking. This process provides their customers with a packaged device only slightly larger than the bare die and simplifies electrical test and burn-in. The use of CSP provides protection of the bare die and simplifies user assembly. This process also enables Chip Supply to offer multichip modules (MCM) in ball grid array packaging.

WLCSP is a process where by the bond pads of the die must be redistributed into an X/Y matrix and attaches solder balls to the new bond pads. This rather simple process is limited to bare die whose number of bond pads, when redistributed into a usable pitch matrix, will fit into the periphery of the die. When this cannot be accomplished, CSP is used.

Chip Supply is empowering customers by providing electronic interconnect solutions. From processing, testing and supplying unencapsulated die, to designing, fabricating and testing Custom Packaging Solutions, they can provide the right interconnect approach to meet both performance and budget demands. For more information about Chip Supply please email them at sales@chipsupply.com or call (407)298-7100. ◆

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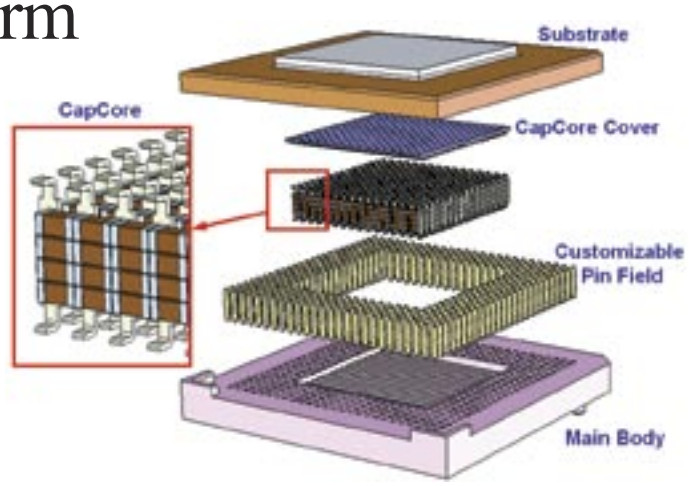

Figure 1. Anatomy of the CapCore interposer. The capacitor core at the center is customized for a checkerboard array of power-ground pins.

Moore's Law has proven to be as relentless as innovation itself. With processing power and data rates perpetually rising, the increased burden placed upon the power management system establishes critical limitations on the device's physical size and efficiency. These limitations, while not insurmountable, pose a more complex set of power and signal integrity challenges. These challenges must be dealt with aggressively if one intends to properly balance performance with size.

Power delivery (PD) system and signal performance limitations manifest themselves with increased bit error rate (BER), increased distributed noise coupling, and core voltage (VCC) droop. They result in suboptimal processing frequency, reduced semiconductor yields, and, in extreme cases, complete device malfunction.

To maintain core power stability the system must provide enough decoupling with an adequately low-parasitic path to the switching semiconductor. To be fully optimal, this capacitance must effectively complement the voltage regulator module (VRM) to provide a "fast" power transient response to the semiconductor without destabilizing the VCC level. Overcoming this challenge requires detailed analysis and simulation of the decoupling on the entire PD system.

Unfortunately, in assessing this bewildering "forest" of system decoupling, designers appear to limit their perspectives to the "trees" of component optimization. Design for PD continues to be encumbered by component-based methodologies and post-design piecemeal solutions. Both tradition and design inertia inhibit system advances in comprehensive chip-package-connector-board co-design.

For example, system engineers continue to trivialize decoupling strategy using legacy and "brute-force" tactics, such as populating the printed circuit board (PCB) with numerous decoupling capacitors (decaps) and employing exotic via technologies. Not only are these approaches ungainly and inelegant, they are highly inefficient from the perspective of system architecture and PCB real estate. More importantly, the inductance of most substrate-PCB stackups imposes a limitation on the power supply transient response attainable through PCB decoupling.

From the business perspective, increasing the PCB decap count to attain lower power impedance is often rationalized with the excuse of the negligible costs incurred in their procurement and assembly. This something-for-nothing illusion, as we will show, overlooks their effect on system total applied cost. In fact, it is only recently that system designers have been forced to confront the coupled problem of VCC stability and transient switching noise from a system performance and cost perspective. Thus, some of the more forward-thinking designers and visionary system engineers have sought out alternative methods to accomplish the task.

One promising response is embedded capacitance. This technology essentially capitalizes on the layered structure of boards and substrates and offers enhanced "built-in" capacitance. Similarly, substrate buildup technology continues to improve, allowing more power-ground plane pairs for capacitance. Despite their technological progression, however, they still lack the raw density of discretes or custom-designed capacitors. Moreover, cost sensitivity to layer count places an upper bound on the stackup complexity and consequently the possible capacitance. Clearly at the PCB level, the lack of semiconductor proximity marginalizes the gains incurred by continually adding more decaps.

Capacitance on substrates with fully populated pin arrays is costly and limited in performance by required access distance, especially on the top sides. More ideal still is on-die capacitance, but this too is limited by physical space and prohibitive costs.

Recognizing the inadequacies of these aforementioned approaches to current and next-generation PD design, Silicon Bandwidth set out to improve decoupling effectiveness by simplifying the PCB and integrating the system's mid-frequency capacitance directly into the PCB-substrate core power path, in a sense utilizing the "third dimension" in the system stackup.

This new platform, named CapCore™, can be designed into substrates, interposers, or sockets. It can be surface mounted or compression fit to standard PCB technologies, including Welltech™[1,2]. It is a robust and highly versatile technology, offering improved core power delivery, lower transient noise, improved system performance, and lower system cost. As we have demonstrated in several forums [1-3], CapCore enables superior power delivery and simplifies current systems to provide a compelling performance and cost advantage to applications.

CapCore's primary implementation for present customers is within a footprint-compatible interposer. This interposer solders between the PCB and substrate. It provides multiple levels of decoupling between adjacent power-ground pairs, and configures to custom "checkerboard" or "random" pair-

ings of powers and grounds.

An example of a custom CapCore designed for a checkerboard core power array is shown in Figure 1, distributed on a 1 mm pitch. The capacitor core provides four 0402 package size chip capacitors soldered between each lead. The substrate rests over the covered "capacitor core" array arranged within a customizable pin field. These components are combined and assembled creating a complete interposer. A prototype is shown in Figure 2.

CapCore's versatility extends to the signal pins. As mentioned, these pins are customizable for specific signal integrity needs. Pin grid array (PGA) solutions, while simple and inexpensive, suffer from mismatched impedance making them appear "inductive". Such discontinuities increase signal jitter and BER budgets, potentially exceeding acceptable design limits. However, additional interposer length is practically transparent to the system interconnect when it provides controlled-impedance channels to the high-speed signals. We therefore offer a coaxial version of the interposer with a shielded main body and insulated signal pins. The prescribed ground pins are simply shorted to the shielded insulator body, while the ground solder connections, as in the PGA case, fit directly into the PCB-substrate footprint. We have designed the signal channel impedances from 30 to 50 W [3].

Naturally, the introduction of an additional "component" inevitably triggers apprehension. Is the extra component cheaper than the eliminated decoupling capacitors?

Unfortunately, this question misleads the actual "cost equation" by oversimplifying the system as a prescribed set of materials and components. Specifically, it overlooks a number of first- and second-order system factors such as architecture efficiency, layer count, and processor performance.

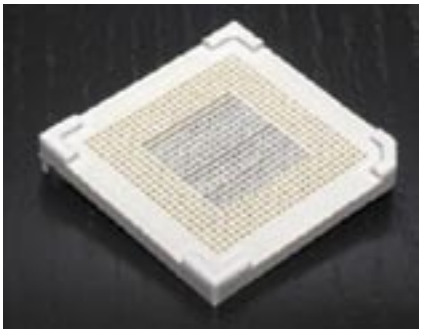

Figure 3. Custom built "UniCap" modules provide substantially higher capacitance and minimal inductance.

Put simply, the cost premiums incurred from the additional decap assembly and the exotic PCB via technology (applied to lower the core power path inductance and increase PCB decoupling effectiveness) understate the effective system costs incurred by the increased complexity. The cost equation must also properly factor in additional supporting layers, space, design rules, and architectural enhancements.

Customers realizing these issues have identified several key values CapCore provides to their system and architecture: closer VRM placement, reduced bus sizes, and smaller PCBs with higher yields. De-crowding the PCB also has immeasurable benefits to the design cycle, as it relaxes stringent routing and layout rules for traces and components.

Finally, and most compelling, is higher microprocessor processing frequency resulting from PD improvements. Core voltage instability limits the maximum processor clocking frequency. Reducing these fluctuations in the core allows higher maximum operating frequency [4,5]. Through several customer partnerships, we have shown improvement in VCC droop with the addition of CapCore to the existing system [1-3]. This results in improved semiconductor yield to higher "bins." The additional processor performance can in turn be sold at a premium. Customers recognize this enormous advantage that offsets the cost of the interposer and premiums incurred from more complex fabrication techniques and increased layer counts.

Custom designs and prototypes are now under development and expected for testing within a month. Further enhancements include UniCore™, which is essentially a custom "through" capacitor designed to match the substrate core power footprint and fit within a very thin interposer between the substrate and PCB. Collaborative customer research shows that this provides a superior performance improvement in terms of droop reduction to the leaded CapCore interposer. A cross-section of this technology is shown in Figure 3. The alternating power-ground can be customized for "random" configuration, but thus far we have only designed the UniCore for checkboard array applications.

In conclusion, we have demonstrated that CapCore enhances system power integrity while maintaining high-speed signal integrity. It is more than an additional component with additional cost; it enables simpler, lower-cost PCBs, architectural advantages, improved microprocessor performance, and lower system cost. Our customers have recognized these advantages and in collaboration we are together demonstrating lower system costs with reduction and relocation in PCB and substrate decoupling capacitors and improved PD performance. We summarize the achievement as "the system is greater than the sum of its parts." ◆

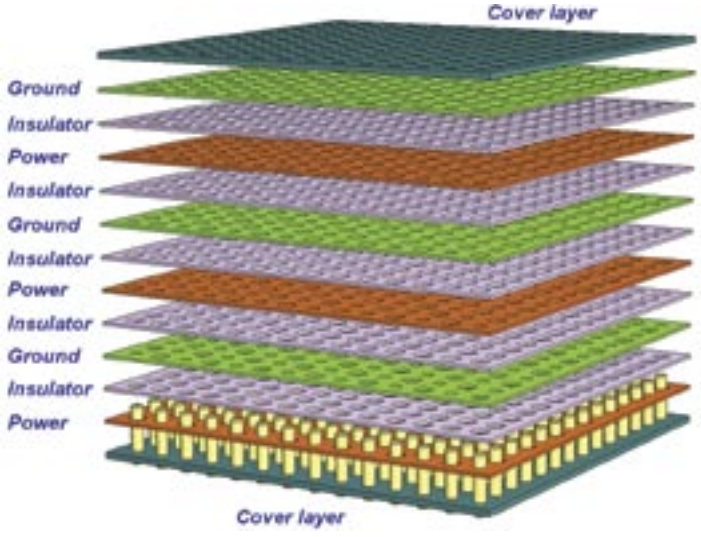

Figure 2. Photograph of CapCore prototype for application with checkerboard core power-ground arrangement.

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Traceability of Materials and IC Packages to Improve Yields and Quality

Winthrop A. Baylies, Co-founder
Traceability System Architects

Yield enhancement is a holy grail in the semiconductor industry. Historically this quest has focused on Wafer Fab performance, in the face of plummeting feature sizes, lithographic challenges, and the vagaries of new bulk and film materials. But it is performance of the delivered semiconductor device – with its high-density interconnects, increasingly complex package materials, and arcane testing procedures – that ratifies the manufacturing practices employed across the entire semiconductor supply chain. Yield enhancement techniques, properly executed, underpin historical device performance improvements that are evident all around us – from ubiquitous "memory sticks" (bye-bye floppies) to ultra-light laptops to "cool" iPods and industrial-strength computing "farms".

Over ten years of AEC/APC symposia have focused on automated equipment control and automated process control. Yield enhancement is one ultimate goal of these activities – for many diverse reasons, not the least being reducing costs, increasing market share, and developing new markets. Final assembly operations are critical factors affecting yields of delivered semiconductor devices. These operations' complexity now approaches those of Wafer Fab areas. Enhancing final device yield requires the presence of both product tracking and sophisticated product traceability systems.

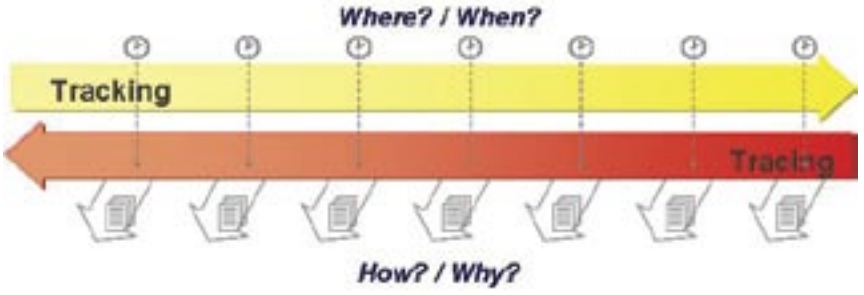

Figure 1. Tracking vs. Tracing.

Traceability and Tracking – How They Work

Tracking – is the time-sequential knowledge of a product's progress. You know where it is now and what to do next. It is an in-line tool for control of product flows and inventories. It is the skeleton or underpinning of a comprehensive, useful product tracing system. It is data about where and in what lots the components of a part originated, then to what processes it was subjected, its test results, its ultimate field deployment and final disposition.

Traceability – is defined in the Merriam-

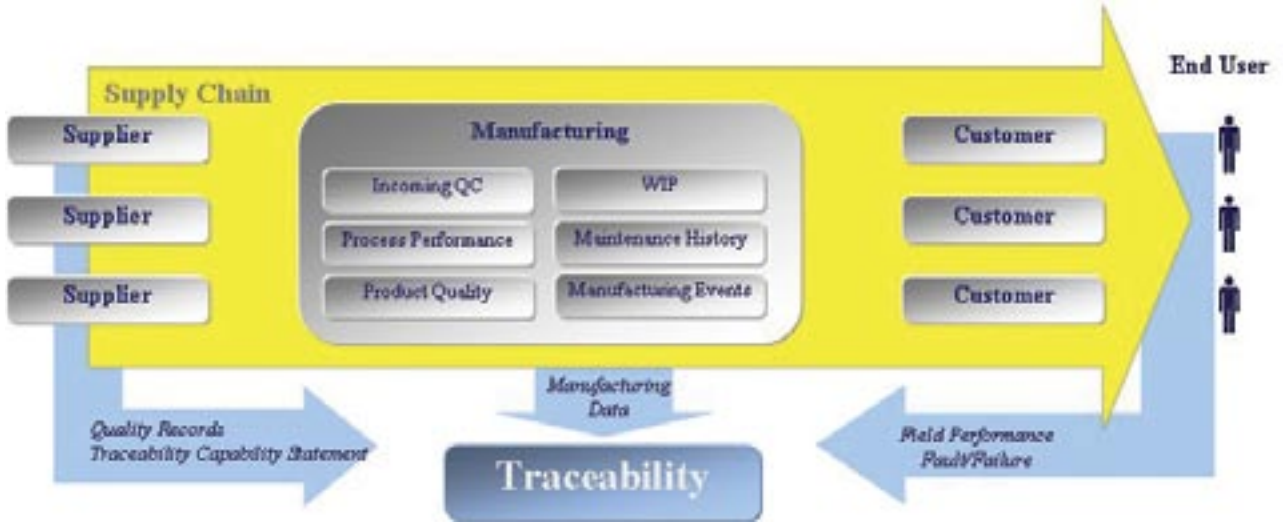

Figure 2. Traceability System Model.

Webster Dictionary as "to discover by going backward over the evidence step by step". It is the comprehensive understanding of what impacted a product's quality during its life-history. You know how it was made and why a failure occurred. Traceability is an off-line tool for detecting failure causes from product life history data. It is the life-history of all elements of a product's instantiation, including:

- Supplied materials
- Processes and procedures
- Metrology and test
- User experience

Doing Traceability

A traceability system draws data from three principal sources (see Figure 2). First are suppliers' quality records and traceability capabilities, which should support item-level traceability. Here, "item" examples include an individual wafer, a leadframe, a packaging substrate, etc. Ideally, each item has a unique ID, often a simple "license plate" number, with which the supplier's data may be linked. Historically, this limitation often was the weakest link in the Traceability chain. Today, such data may contain individual test data, statistical multi-lot information, or both. It is often electronically dispatched.

The second principal source is in-house manufacturing data. Historically, this has been the richest source and will include Incoming QC, Process Performance, Product Quality, WIP, Tool Maintenance History and Manufacturing "Events" such as excursions beyond normal control limits. Today, managing the torrent of data is a major Traceability challenge, on which more later.

The final and often most important source is deployment data from both immediate customers and the ultimate end-users. Historically, this included both field performance and fault/failure analyses. Today, this may be the most important source for diverse reasons – regulatory, customer satisfaction, competition, product planning, etc.

A typical product data flow example is shown in Figure 3. Here, the Product Genome™ comprises an individual product's life history, from supplied parts through system assembly and customer usage. Automatic tracing software formats product data for a structured data base – enabling creation of unique Product Genomes. Notably, that example also includes "rework" cycle(s), in this case for cleaning of shipping containers which contacts a shipped product.

In Final Manufacturing, two elements are critical to product tracking. One element involves the process steps at which a product's ID must be transferred from one form to another, for instance from Wafer to Wafer Frame, Wafer Frame to Die to Strip and Strip to Die to Package (Figure 4). The other element is the underlying data

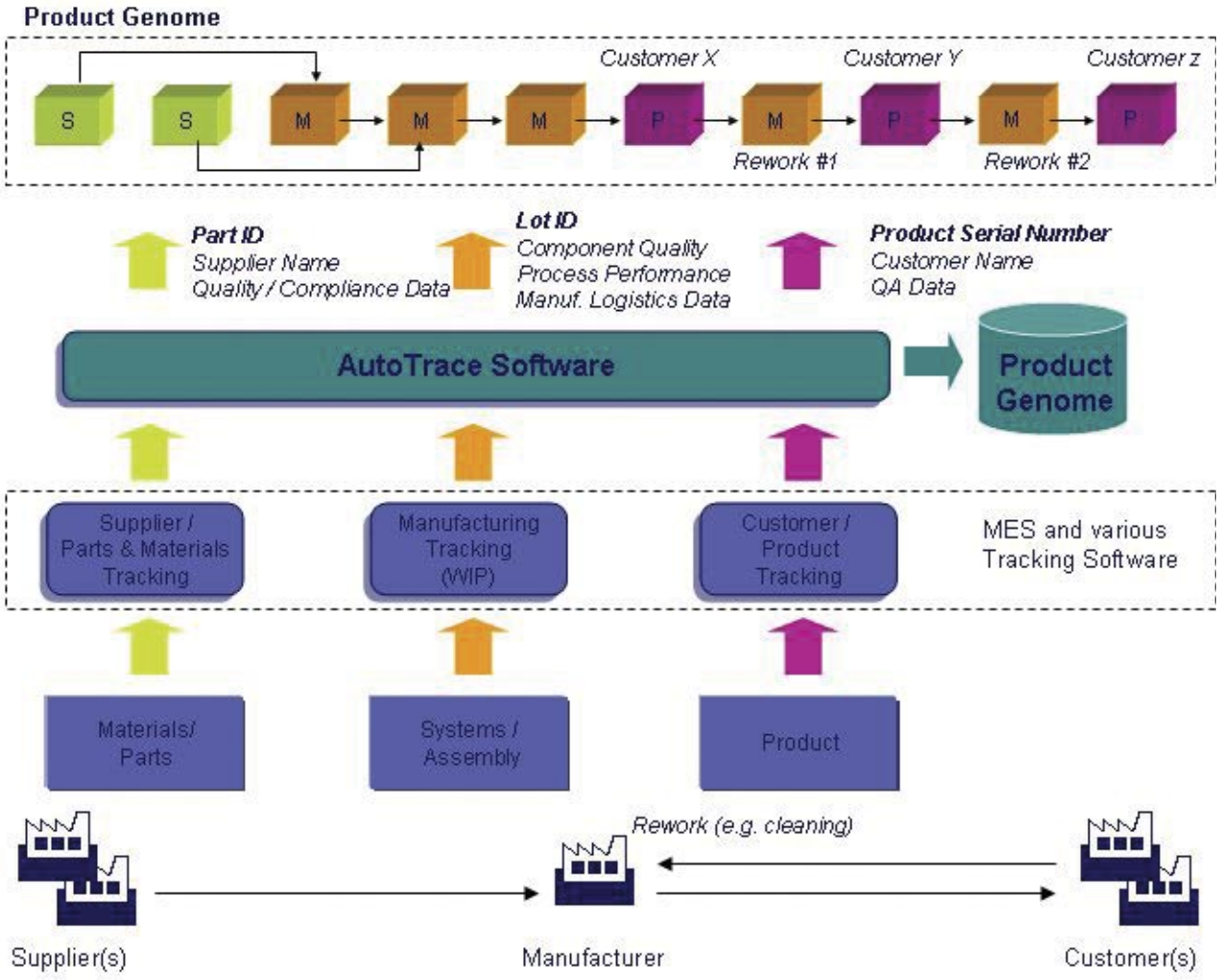

Figure 3. Product Data Flow Example.

format, for example Wafer Maps and Strip Maps (Figure 5).

Intense SEMI Standards international activities support Track and Trace initiatives in Final Manufacturing. SEMI's International Traceability Committee has developed specifications for ID marking symbologies, ID message content and ID mark location on wafers, strips and die. Today, all 300 mm virgin wafers contain an ID (SEMI Specification T7) at the same location, enabling traceability from within the wafer-making line to shipments of microprocessors. SEMI's International Information and Control Committee has developed, and continues to work on, standards such as:

- SEMI G81 – Map Data Items
- SEMI G84 – Strip Map Protocol
- SEMI G85 – Map Data Format
- SEMI E90 – Substrate Transfer
- Draft Doc 3754 – Device Tracing Data, Device ID Data, Substrate Layout Data

Various data elements in SEMI E90 are shown in Figure 6. Implications for both product tracking (where/when) and traceability (how/why) are clear.

Lastly, the relationship of device tracking elements, from a wafer to a finished cell phone, and the demands this makes on product tracking and traceability systems are shown in Figure 7.

When these elements are well coordinated, the complex task of reporting substrate layout information can be reduced to its basic elements, as shown in Figure 8.

Obviously, a traceability system's architecture will enhance or diminish the system's usefulness. Carefully detailing

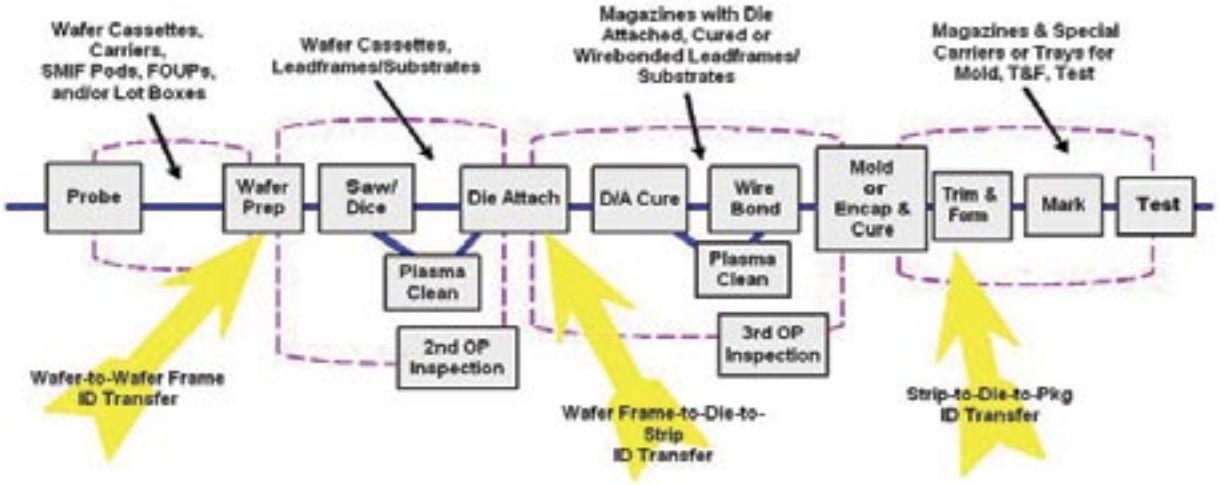

Figure 4. Material ID Transfer in Final Manufacturing.

Source: G. Michaud

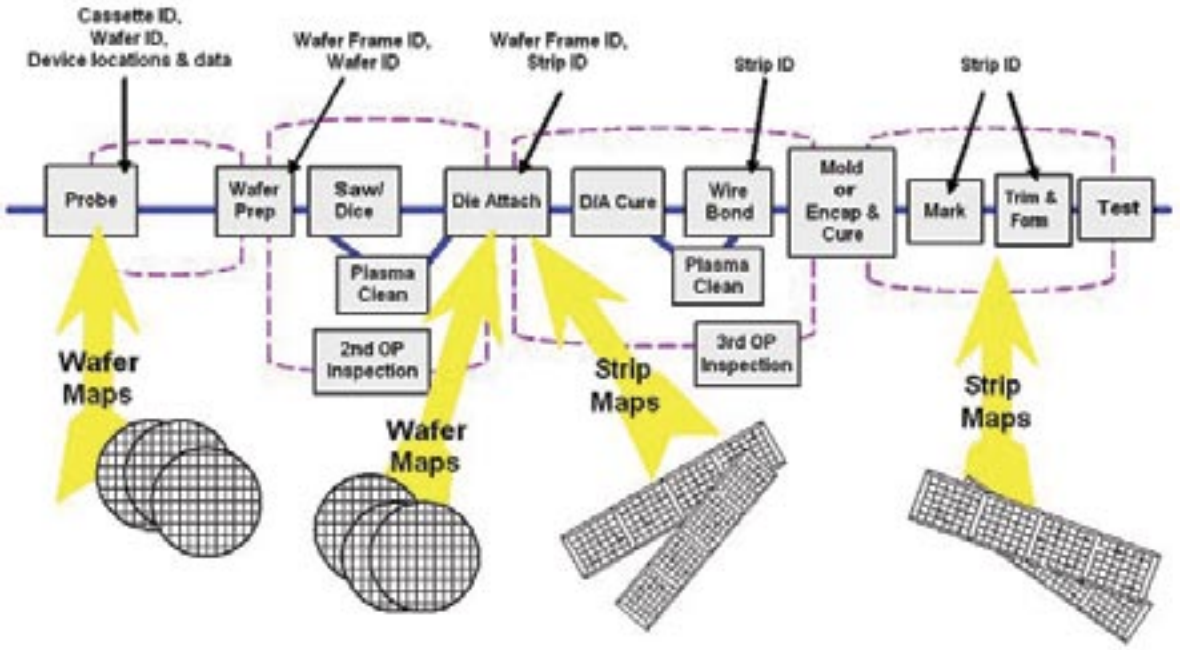

Figure 5. Device Traceability Formats in Final Manufacturing.

Source: G. Michaud

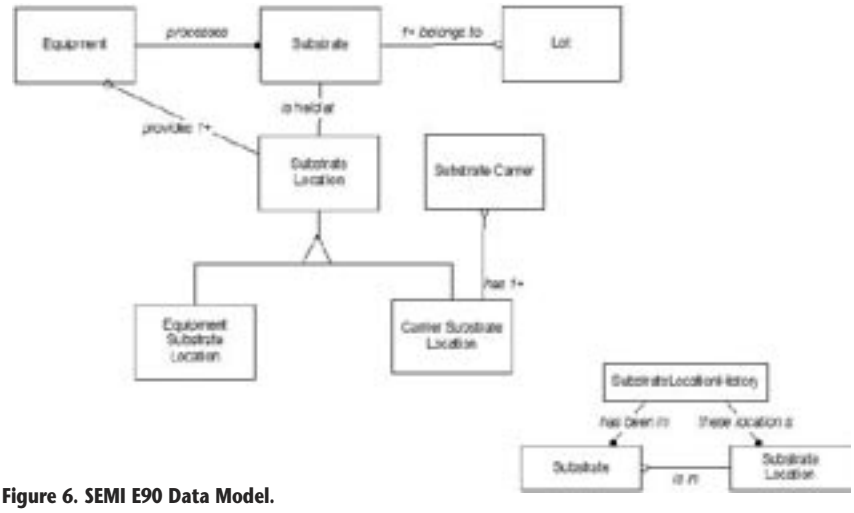

Figure 6. SEMI E90 Data Model.

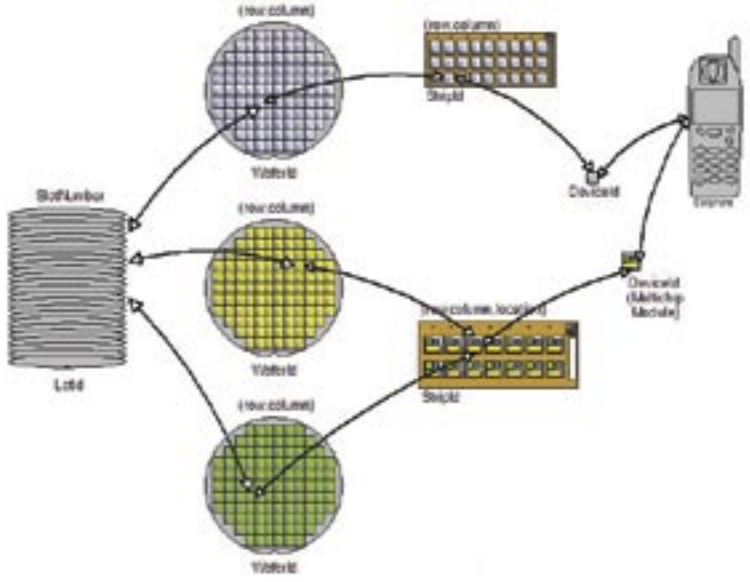

Figure 7. Device Tracking Elements. Source: D. Huntley/Kinesys

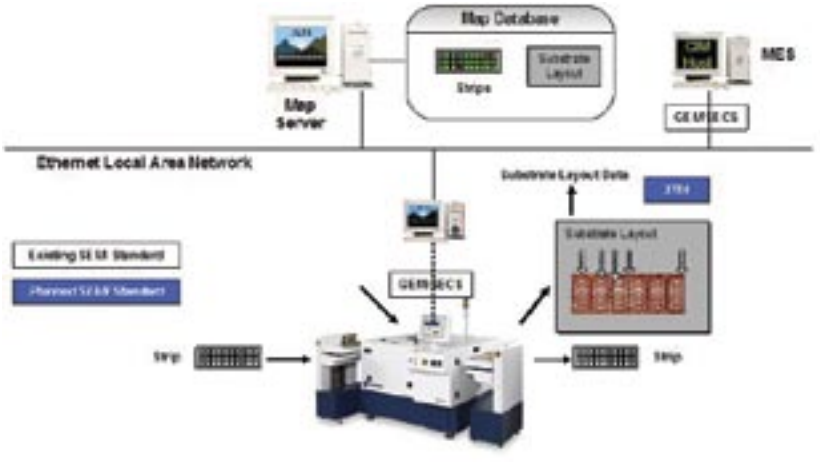

Figure 8. Substrate Layout Reporting. Source: D. Huntley/Kinesys

the architectural requirements is a vital first step in developing a broad-based, functional, responsive and efficient traceability system.

Traceability Benefits

Traceability is long-loop yield enhancement. It links in-house yield management and quality operations with those of your suppliers, your customers and your customers' customers. This structured framework should be designed to support full serial number traceability across all products. Enhanced yields will reflect increased product quality across many levels, including supply chain control of incoming Final Assembly materials such as lead-frames / packages / strips, substrates, bonding materials, etc.

Traceability is a crucial enabler of Root Cause Analysis – determining the why and how a product "event" occurred, and what other similar events may be in the product pipeline from final test to in-patient installation. This in turn provides the key to "Event Containment", its twin – "Event Recall" and most importantly the development of an Event Containment Strategy.

Conclusion

Increased reputation, improved profits and substantial time savings – all these benefits derive from the active, constant scrutiny embodied in a fully effective, properly architected Traceability System. Only recently have such tools emerged from development; they are now proving their value. ◆

Winthrop A. Baylies, *co-founder of Traceability System Architects, is a specialist in international semiconductor, flat panel display, computer disk drive and general gauging technologies. He graduated from Harvard with a BA in Physical Sciences. His career includes over 20 years of management in the Electronics industry, including President/CEO of Solid State Measurements and BayTech Group, and Vice President of Technology Development Group, Inc.*

In 2000, Win co-founded SEMI's MEMS Advisory Group. He co-chairs SEMI's MEMS Wafer Specification Standards TF, is currently facilitating a Wafer Survey and, with MIT, a MEMS-Wafer Bonding Experiment expected to lead to a Wafer Bonding Model.

Win is active in high-technology associations: SEMI: a former director and chairman of its Standards Committee, a current member of its International Standards Committee, co-chairman of the N.A. Traceability Committee, chairman of the Wafer Dimensions Subcommittee, working closely with counterpart groups in SEMI's Japan and European organizations.

A former chairman of ASTM F1 Committee on Electronics, Win received the ASTM Award of Merit and was elected an Honorary Fellow of the Society. He co-chairs SEMI's North American Traceability Committee, is a technical architect on SEMI's North American FPD Committee, and co-chairs the NA/FPD Substrate Standards Subcommittee. He has authored numerous technical articles, test methods, international round robin tests and related research reports. ◆

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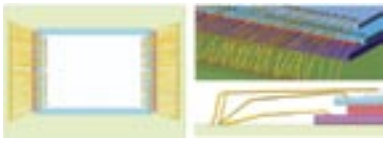

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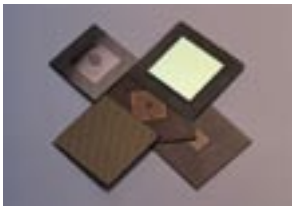

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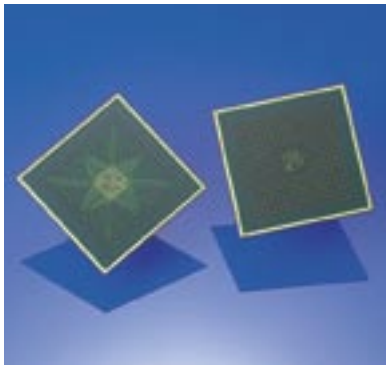

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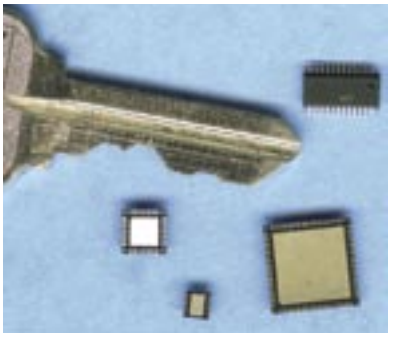

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24	25	26	27 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley	28	29	30

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1	2	3	4	5	6	7
8 MOTHER'S DAY	9	10	11 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley	12 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	13	14
15	16	17	18 **MEMS PACKAGING TRENDS SYMPOSIUM** The Westin Hotel Santa Clara, CA	19	20	21
22	23	24	25	26	27	28

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5	6	7	8 **SUNNYVALE MEPTEC LUNCHEON** Ramada Silicon Valley	9 **SOUTHWEST MEPTEC LUNCHEON** Dobson Ranch Inn Mesa, AZ	10	11
12	13 **TECHNOLOGY VENTURE FORUM** Wyndhan Buttes Resort, Tempe, Arizona	14	15	16	17	18
19 FATHER'S DAY	20 **IMAPS FLIP CHIP 2005** Marriott Austin at the Capitol, Austin, Texas	21 SUMMER BEGINS	22	23	24	25
26	27	28	29	30		

Cost Effective Production Challenges Drive Lithography Equipment Selection

Manish Ranjan
Ultratech Inc.

Advanced packaging technologies continue to gain acceptance due to electrical, thermal and form factor advantages. The manufacturing transition to advanced technology nodes, such as 90 nm and 65 nm, has resulted in an accelerated adoption of flip chip technologies. Advanced packaging enables true performance advantages for the high-end logic devices fabricated at these technology nodes. As flip chip technology gains mainstream acceptance, device manufactures and wafer foundries are adopting traditional front equipment for their wafer bumping line. This adoption has been driven by the realization that the production criterion and yield characteristics for the wafer bumping line are very similar to those in front-end wafer manufacturing.

Tool selection plays a key role in eliminating the bottlenecks associated with advanced packaging lithography. Device manufacturers and wafer foundries are demanding systems that deliver superior technical performance and overall cost savings, thereby lowering the cost of wafer bumping. By providing a very high economic value to the customer, 1X stepper technology has established itself as the defacto lithography standard for volume production of flip chip devices. The key challenges witnessed during advanced packaging lithography are discussed in the following sections.

Technical Challenges During Advanced Packaging Lithography

Photolithography plays a critical role during advanced packaging. The height of the bump and its location relative to the bond pad are defined during this process step and are crucial to maintaining high yields. Typical bump heights range from 20 to 100 microns with image features ranging from 15 x 15 to 500 x 500 microns square. The imaging and alignment considerations, along with the wafer-edge processing and process yield requirements are discussed below.

Imaging Considerations

Successful imaging for advanced packaging processes requires the ability to expose both thin and thick resist films. Unique lithography requirements include broadband exposure, large depth of focus and high-aspect-ratio capability.

A 1X stepper projects an aerial image that can be focused at various depths within a thick photoresist film. This enables steeper sidewall angles and overall higher image quality, regardless of the photoresist type or thickness being used. This is especially critical for thick photoresist used in straight wall electroplating applications. In addition, 1X steppers can be optimized for larger-geometry features while retaining the depth of focus capability over large exposure fields. Ultra-thick photoresists also require a large exposure dose for high-aspect-ratio lithography. For this reason, it is advantageous to utilize a 1X stepper with a broadband exposure system to maximize the illumination intensity at the wafer plane. 1X steppers illuminate a small area on the wafer during each exposure and therefore are able to control the illumination uniformity to a much tighter degree. This results in improved CD uniformity and more consistent resist side wall profiles. Improved CD performance and a more consistent resist sidewall profile lead to more accurate bump heights – increasing the overall product yield.

Alignment Considerations

1X steppers provide site-by-site and enhanced global alignment (EGA) capability, which ensures high alignment accuracy during the exposure process step. In addition, this advanced alignment capability compensates for run-out errors, array and step rotational errors and orthogonality errors witnessed with large area masks utilized by contact and proximity aligners. Another factor affecting alignment is the mask or reticle. 1X steppers utilize quartz reticles, which are wafer-size independent and enable placement of multiple layers on a single reticle, resulting in significant cost savings. 1X reticles do not come in close contact with the product wafer, and the use of a pellicle strategy eliminates the need for cleaning – in turn, eliminating the need for additional mask-cleaning equipment.

Production Yield

One of the most important factors in the selection of any lithography tool is the ability to print defect-free images on a wafer, thereby eliminating the lithography tool as a yield detractor. By the time a product wafer reaches the wafer-bumping process step, it is worth many thousands of dollars. Therefore, any incremental yield loss during the photolithography process sequence creates a significant financial impact. Implementing 1X stepper technology eliminates incidental wafer-to-photomask contact along with any associated yield loss. The use of enhanced global alignment also contributes significantly to improving process yields by reducing alignment errors and improving the quality of the image being exposed. Stepper technology provides superior imaging performance and significantly improved CD control, resulting in high overall product yields. In addition, the high level of process automation provided by stepper technology minimizes operator intervention and provides a robust process window.

Summary

As flip-chip and wafer-level packaging techniques achieve industry acceptance, device manufacturers are faced with several manufacturing challenges, including equipment selection. By utilizing catadioptric 1X stepper technology, customers can address both current and future advanced-packaging lithography technology requirements. The market-specific options developed on this platform represent the most cost-effective approach to satisfying the technology demands. ◆

Magazines and Carriers for Process Handling Solutions


Film Frames


Film Frame Magazines


Film Frame Shippers


Grip Rings


Grip Ring Magazines

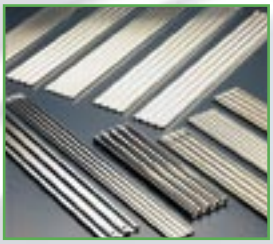

Grip Ring Shippers

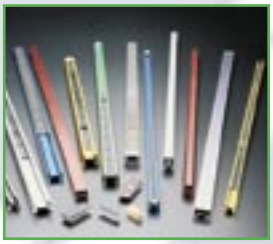

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.

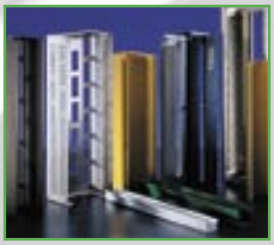

Process Carriers (Boats)

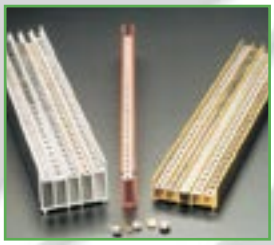

Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines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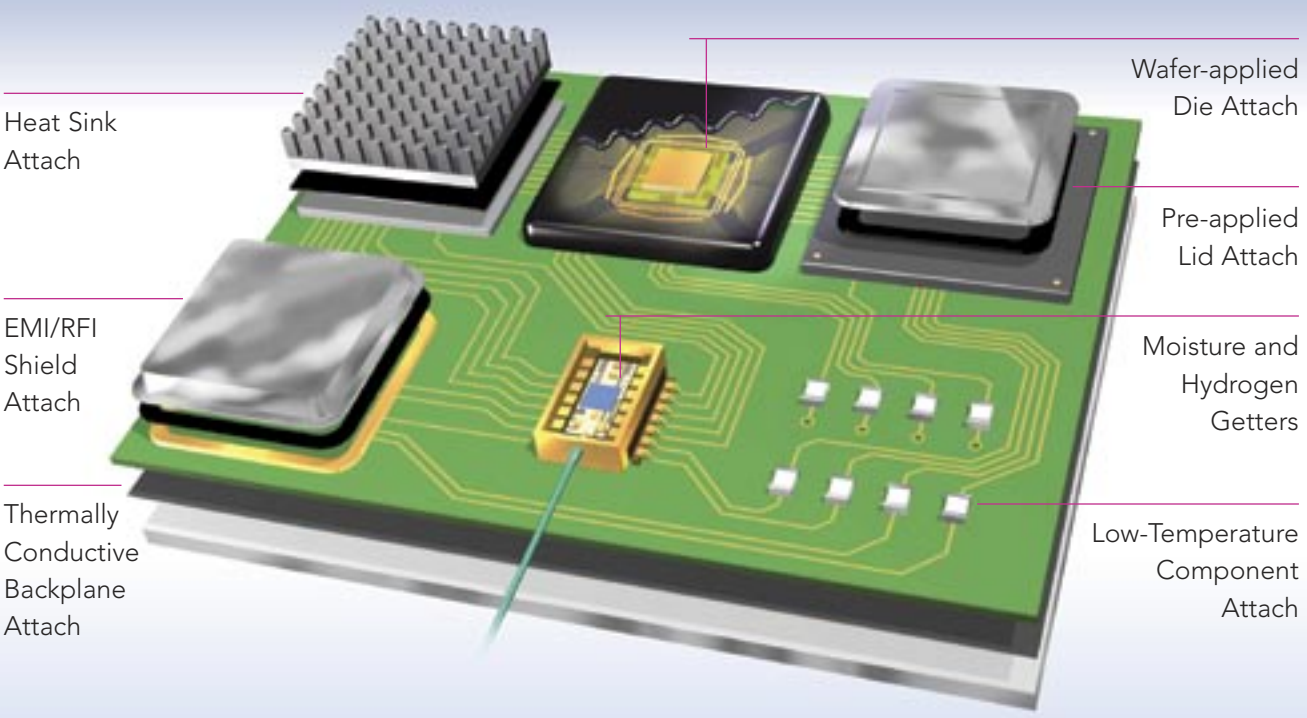

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