MEPTEC report
Volume 9, Number 2
QUARTER TWO 2005
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

CARSEM expands their manufacturing space dedicated to test services operations at their S-Site facility in Malaysia. *page 18*

SIX SIGMA is celebrating 15 years of business this year in which it has serviced over 20 million components. *page 20*

KYOCERA's Copper Bonded Silicon Nitride Ceramic Substrate achieves 5,000 cycles of temperature cycling test. *page 20*

CORWIL TECHNOLOGY CORPORATION adds high volume 12 inch wafer dicing services to address 300mm wafer diameter market. *page 24*

TECHNOLOGY

Joe Fjelstad of **SiliconPipe, Inc.** discusses *3D IC Packaging and Interconnection Technologies – Pathways to Performance*. *page 28*

Jim Davis of **Kinesys** and **Jerry Secrest** of **Secrest Research** present *Navigating E142: SEMI's Specification for Substrate Mapping*. *page 31*

SEMICON® West2005

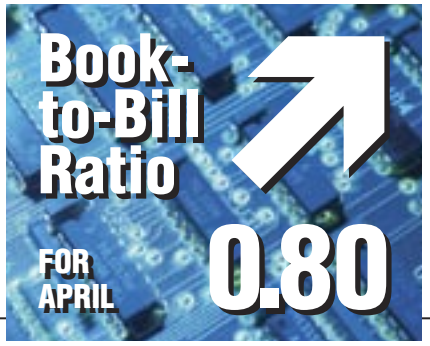
SEMICON West 2005 will be held July 11th through July 15th at the Moscone Center in San Francisco. *page 13*

MEMBER COMPANY PROFILE

Profound has signed a cooperation agreement with a local prestigious university research lab in which both parties will co-develop alternative lead-free alloys and soldering materials, as well as pursuing a more advanced production technology.

Profound Material Technology Co. Ltd. is located in the southern part of Taiwan in the city of Kaohsiung. Profound's factory is ISO9001:2000, QS9000 and ISO14001 certified. With the advantages of its consistent product quality and quick lead-time, Profound has become a qualified solder ball supplier to numerous world-leading assembly houses, IDM, IC test/design houses and rework companies. Profound has sales representatives throughout Asia, US and Europe, which allows them to deliver quality services globally. *page 26*

Semiconductor equipment bookings increase 1.5% above March 2005 level. *page 24*



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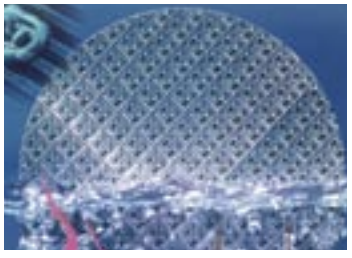

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MEPTEC Council Update

It's hard to believe that it's that time again: summertime, and that of course means Semicon West, when thousands in the industry converge on Northern California to see the latest and greatest technology in the semiconductor industry. This year of course SEMI has moved the entire show back to San Francisco, integrating the Final Manufacturing segment of the show into the rest of the event. Although San Francisco may cause some inconvenience to attendees in terms of traffic, parking, high hotel prices, etc., SEMI's feeling is that in the end, by reuniting the Wafer Processing and Final Manufacturing segments in a single venue, it will make it easier for attendees to maximize their participation and enjoyment of the show.

As in every issue, we offer a summary of MEPTEC events held recently. MEPTEC Contributing Editor **Jody Mahaffey** presents a follow-up on our May 18 *"MEMS Packaging Trends: From Prototype to Production"*. In addition, **Julia Goldstein**, editor at **Advanced Packaging** magazine, follows up with a review of our February event on *"The Heat is On: Thermal Management Issues in Semiconductor Packaging"*. See page 6 for both of these summaries.

Our next event will be held on Thursday, August 25, 2005 at the Hyatt San Jose Hotel in San Jose, California. The event, entitled *"Semiconductor Packaging Strategies: Improving Costs, Productivity and Total Service to Customers"*, came about as most of our events do: during discussion at one of our very active Advisory Board meetings. We're pleased that **Joel Camarda** of **Camarda Associates**, an industry veteran and long-time MEPTEC Advisory Board member, is heading up the event as Symposium Technical Chair. See page 5 for information on this exciting event.

One of our feature articles this issue is contributed by **Joseph Fjelstad** of **SiliconPipe, Inc.** on *"3D IC Packaging and Interconnection Technologies – Pathways to Performance"*. Joe presented this technology at the March MEPTEC luncheons in both Sunnyvale and Phoenix. Joe discusses an IC packaging technology that is brilliant in its simplicity. Always the philosopher as well as superb technologist, Joe sums up his article by quoting a 13th century philosopher monk who observed, "It is vanity to do with more that which can be done with less." See page 28 for this informative and innovative article.

Our other feature article is *"Navigating E142: SEMI's Specification for Substrate Mapping"*, co-authored by **Jim Davis** of **Kinesys** and **Jerry Secrest** of **Secrest Research** (and MEPTEC Advisory Board member). The push for the E142 came from the industry's move towards more complex packaging and the need to integrate maps for many different processes. It also offers some solutions to implementing the standard. Our thanks goes to Jim and Jerry for sorting out and explaining this new standard (see page 31).

Our Editorial this issue is contributed by one of our May MEMS Packaging symposium speakers as well as session leader, **Joe Mallon** of ***memvent***. Joe discusses *"The MEMS Packaging Problem; the MEMS Packaging Opportunity"*. This editorial came out of Joe's presentation at the symposium where he offered a past, present and future look at the "problem" that MEMS packaging presents. Joe points out that the definition of a "problem" is the "…difference between an existing and a desired state of affairs", which looked at a different way can also be defined as an opportunity. He summarizes his thoughts by pointing out that increasing emphasis in the industry on MEMS packaging is needed if the full benefits of the technology can find their way into the marketplace. See page 38 for this introspective piece.

Our Industry Analysis coverage this issue is contributed by MEPTEC member company **Gartner Dataquest**. The article is co-authored by **Jim Walker** and **Mary Olsson**, both long time MEPTEC Advisory Board members, as well as **Dean Freeman** and **Bob Johnson**. They look at *"The Changing Mar-*

continued on page 4

Issue Highlights

From The Director

China and Customer Satisfaction

If you missed the May MEPTEC luncheons in Sunnyvale and Phoenix featuring Ed Pausa of PriceWaterHouseCoopers you missed an excellent presentation on China's impact on the semiconductor industry. But don't despair, PWC has made the entire report that was produced by the PWC staff available publicly. A copy of the complete report is at www.pwc.com/techforecast/pdfs/chinasemis_web-x.pdf.

I don't have the space to list all of Ed's comments but one point worth repeating is that PWC feels that even with the vast number of plants installed in China already, they don't foresee this creating a high oversupply risk in the near-term. Longer term is a different story. If China succeeds in establishing domestic sources of material supply then we can expect significant oversupply, which will result in significant industry volatility. I guess for those of us who have been part of this industry for so long our comment to this will be, "It never changes!"

How does a smaller producer or user of semiconductors prepare themselves for this ongoing volatile property of our industry? Periodic vacations to as many of the world's sunny beaches helps tremendously, but only for a short time.

A possible longer term fix might be found in MEPTEC's upcoming Symposium "Semiconductor Packaging Strategies: Improving Costs, Productivity, and Total Service to Customers." Several industry veterans, led by MEPTEC Advisory Board member Joel Camarda, have assembled several panels on topics including design for low cost and easy manufacturing, reducing material costs, and packaging options for more density and speed.

The Symposium will feature a panel of experts to debate the contentious issue of "who owns packaging research and development". This issue arises from the disappearance of vertically integrated companies of yesteryear who happily churned out packaging innovations, many of which are today's industry standards. Although a few remain, their internal packaging efforts have been severely cutback. While we might expect the assembly contractors to take on the responsibility, they resist due the thin R ad D budgets they have to maintain.

I continue to appreciate your support for MEPTEC and encourage you to spread the word so we can bring more folks the benefit of these high quality programs. ◆

Phil Marcoux
Executive Director, MEPTEC

MEPTEC Council Update

continued from page 3

ket Dynamics of Semiconductor Equipment", and point out that the semiconductor equipment industry has enjoyed strong growth since its inception in the early 70s. In the mid-1990s however, things began to change. See page 10 for the rest of the story…

Our Member Company Profile this issue highlights **Profound Material Technology Co. Ltd.** Profound has become a qualified solder ball supplier to many world class semiconductor service suppliers, IDMS, and test and design organizations. Profound is located in Kaohsiung, Taiwan, and are ISO-9001:9002, QS-9000 and ISO-14001 certified. See their story on page 26.

Our "University News" section this issue is not really about a classic academic institution, but it is about a similar type of research institution that works with academia and industry alike on electronics research. **RTI International** – formerly known as Research Triangle Institute – is best known for its breakthrough developments in thermoelectronics (see page 15). Their research dates back to the mid 1960s when IC technology was still in its infancy. They are headquartered in North Carolina, and recently expanded their capabilities in their semiconductor research and development efforts. RTI and MEPTEC have also formed a recent alliance in helping each other promote their events, especially in the area of thermal management.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at the Semicon West show, or another of the many events where we'll be distributing this issue, we hope you enjoy it.

Thanks for joining us! ◆

MEPTEC Presents
MicroElectronics Packaging and Test Engineering Council

MEPTEC Join Us!

A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

Semiconductor Packaging Strategies:

Improving Costs, Productivity, and Total Service to Customers

Packaging-Assembly-Test manufacturing does not necessarily follow Moore's Law, but nonetheless continues to provide more bang for the buck, in cost, product performance, cycle time, and predictability of supply. Learning how to understand and take advantage of these trends is of the utmost importance to all involved in semiconductor manufacturing.

In this one day symposium, MEPTEC will invite key factory managers, process specialists, logistics managers, and technology gurus from integrated device manufacturers (IDMs), assembly and test sub-contractors, fabless semiconductor companies, and service providers to discuss how they have improved costs, efficiencies, and total service to customers.

Sessions will include:

- Cost Reduction and Process Automation
- "Super Factory" Management
- Package R&D—Who Owns It?
- Global Logistics

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HYATT SAN JOSE

Thermal Management Symposium Draws Crowd

Julia Goldstein, Technical Editor
Advanced Packaging Magazine

Thermal management is a hot topic, as shown by the sold-out exhibit tables and at-capacity crowd at MEPTEC's February symposium, "The Heat Is On: Thermal Management Issues in Semiconductor Packaging." While MEPTEC's focus is on packaging, the symposium covered everything from the chip to the system.

Keynote speaker Greg Chrysler (Intel) outlined the challenge of ensuring that thermal management issues don't become a barrier to increasing transistor density and maintaining Moore's Law. Professor Kenneth Goodson (Stanford University) showed a 2001 ITRS chart suggesting the industry would run out of thermal solutions in 2005 or 2006 as total power exceeded a certain level, but this is fortunately not the case. Cameron Murray (3M), co-chair of iNEMI's Technology Working Group for thermal issues, discussed the 2004 roadmap. Heat flux is projected to increase from 20 to 40 W/cm2 today to 60 to 190 W/cm2 by the year 2018. Murray stated that technological solutions exist to cool such high-density chips, only not at a cost the consumer market can bear.

Chrysler explained one solution at the chip level is to use strained silicon, where buried oxide or SiGe layers create strain in the silicon and affect its electrical properties, reducing leakage current and the amount of power that must be dissipated. There is also a trend toward designing chips with multiple cores. David Copeland (Fujitsu) described how optimizing the separation between cores could lower the maximum temperature of hotspots during operation and greatly reduce junction-to-case thermal resistance.

Another issue Chrysler brought up is that cooling systems are getting bigger as heat flux is increasing and more functionality is being placed in a box. Minimal space for airflow is a problem. Goodson proposed a concept of replacing traditional heat sinks with a "dream heat sink" that is no larger or heavier than the chip. Research begun at Stanford on microfluidic cooling, where fluid would be pumped through micromachined channels located over hotspots, could provide a solution in the near future. While Goodson's research may be years away from a commercial product, fluidic heat sinks are a reality. Marlin Vogel (Sun Microsystems) presented results of a project in which vendors competed to design prototype heat sinks for microprocessors. Solutions included an embedded heat pipe design by Aavid Thermalloy and an oscillating heat pipe with a fin-shaped vapor chamber by TS Heatronics.

In his discussion of market opportunities, Jim Walker (Gartner Dataquest) mentioned heat sink development, as well as moving toward integrated thermal design and modeling software. David Stiver (Flometrics) spoke about the need to move from an entirely supply-chain based approach to focusing on the "design chain," where chip design, substrate design and electrical and thermal modeling are integrated into the manufacturing process. He discussed work of the JEDEC JC15.1 subcommittee toward generating thermal measurements and modeling standards that can be used throughout the industry. Jesse Galloway (Amkor) discussed thermal design for System in Package beyond layout considerations, and gave an example where splitting a ground plane helped keep heat generated by an ASIC from affecting nearby memory chips. Solectron made extensive use of simulation in a project requiring adopting an indoor antenna to be able to function in an outdoor environment. Robert Raos explained how simulation tools were used to predict internal air temperature and optimize the thermal design.

Roger Emigh (STATS ChipPAC) showed how modeling of heat flow could be used to determine how effective a heat sink would be for a given package configuration and aid in package selection. For example, heat can more easily be dissipated into a heat sink on a lidded package than an overmolded package. Package selection can be critical, as Chris Schaffer (International Rectifier) noted in his discussion of voltage regulator modules and field effect transistors. Power density requirements have made the traditional SO-8 package the limiting factor in heat dissipation, requiring advanced packages such as QFNs and custom discrete packages with copper layers to efficiently transfer heat to the PCB and heat sink. Joseph Walters noted that Nvidia uses similar solutions in their graphics modules.

Another aspect of packaging Walker mentioned is materials and interfaces. Goodson described Stanford's research into using aligned carbon nanotubes to produce thermal interface materials with thermal conductivity approaching that of diamond. Jonathan Harris (CMC Interconnect Technologies) emphasized that processing is as important as materials selection, showing an example where co-firing of a tungsten thick film on aluminum nitride eliminated interfacial layers and resulted in a much higher thermal conductivity than firing the two materials separately.

As several speakers noted, a critical area for system-wide thermal management is network power for the Internet. Chandrakant Patel (Hewlett-Packard) discussed the need for dynamic provisioning of cooling resources in a data center, where temperature is continuously monitored and parameters such as fan speed are adjusted as workload varies. The dynamic provisioning concept can be taken down to the chip scale, where micromechanical spray cooling is directed at chip hotspots and flow can be adjusted, depending on whether the chip is idle or active. ◆

The Maturity of MEMS

Jody Mahaffey
JDM Resources

In 2002 University of Michigan Professor Joe Giachino was quoted in a Mechanical Engineering article saying that MEMS (MicroElectroMechanical Systems) was entering its "teenage years". Now, three years later, the question is, "Has MEMS grown up at all?"

Maturity for MEMS seems to be com-

ing along more slowly than many other technologies. According to Marlene Bourne, Vice President of Research and Principal Analyst at EmTech Research (a division of Small Times Media), the commercialization timeframe for MEMS is approximately five to seven years. Customization and packaging constraints are the major factors in the longer than usual development cycle, but it is getting better. "Ten years ago packaging constituted 70-90% of the total cost for MEMS products," says Bourne. "Today because of Wafer Level Packaging (WLP) solutions and use of CMOS processes, that percentage has dropped to 30-50% on average. Between that and the fact that cell phones and other consumer products are now beginning to integrate MEMS at a higher rate, the market is definitely evolving."

Ms. Bourne's research figures show just how much MEMS are growing with actual revenue for MEMS being $5.3 billion in 2003, with just over $7B being forecast for this year and growing to around $10B in packaged MEMS chips by 2009.

There are many reasons why MEMS is taking so long to mature. MEPTEC, the MicroElectronics Packaging and Test Engineering Council, brought together leading experts in the MEMS fields to discuss this topic in its one-day technical symposium "MEMS Packaging Trends: From Prototype to Production" which was held on May 18th, 2005 in San Jose, CA.

Even though it may be moving slowly, the MEMS industry isn't standing still. This past year in particular has seen significant growth in the area of MEMS. A few of the speakers from the MEPTEC symposium agreed to give us some insight into the changes they have seen in the MEMS market over the past year.

Joe Mallon, President of *memvent*, was Session Chair for the MEMS Packaging, Assembly and Test Challenges Session of the event and also a speaker in the MEMS Technology and Industry Overview Session. He believes that the most significant change over the past year has been the growing importance of MEMS devices for gyros in military aerospace, automotive and consumer applications.

Another Session Chair and speaker, John Heck, Research Scientist for Intel sees the rapid growth of MEMS in the high volume markets of consumer electronics and wireless communications in the past year as a significant step for MEMS.

Dr. Thomas Kenny, Professor at Stanford University, agrees saying that, "Some commercially successful products, and the transition to more standard manufacturing is really helping MEMS along. The DLP projectors and televisions are great examples of a large-volume opportunity that is enabled by MEMS." Dr. Kenny presented an afternoon keynote at the symposium.

Packaging has been and continues to be the single most significant hindrance to the maturity of MEMS. Unlike most other devices, each MEMS device requires its own unique packaging approach.

Heck believes that high-volume markets have been slow to adopt MEMS technology because of the high cost of this non-standard packaging. "MEMS have actually been commercialized in several niche fields for a long time now, most notably as inertial sensors and pressure sensors in automobiles," says Heck. "Since these products are essential to the safety of modern automobiles, the high cost of packaging was tolerated. However in other fields, such as consumer electronics, price is the name of the game. The technology to put acceleration sensors in laptops, cell phones, and video games has been around for a long time, but only recently has the cost come down

enough that it is reasonable to consider adding these functions to such devices."

According to Dr. Siamak Akhlaghi, Project Manager for Micralyne, Inc. and speaker in the Enabling Technologies Session, "Probably the biggest issues relate to the challenges of packaging MEMS-based products, which may account for more than 80% of the price of the final product. At Micralyne, we serve customers who are developing products in such industries as drug delivery, medical devices, automotive, defense, optical communications, mobile telephony and digital printing. It is a significant challenge to develop packaging solutions for each in a cost effective fashion."

Another speaker in the Enabling Technologies Session, Markus Wimplinger, Director of Technology for EV Group stresses that it is important for designers and developers to keep packaging issues in mind from the very start of designing a device.

In most cases there are no standard processes for packaging MEMS. Dr. Wan-Thai Hsu, Chief Science Officer for Discera, Inc. and speaker in the End User Applications Session says that this creates a whole set of problems in itself, affecting equipment throughput and other manufacturing processes.

Due to the very nature of MEMS products, packaging will likely remain one of the biggest issues in product maturity. Wimplinger explains, "The packaging issues for MEMS are significantly different as compared to other products, as the MEMS package has to fulfill a broad variety of functions for the device. For other, traditional devices, the package only performs a function of protecting it in a mechanical and electrical sense. For MEMS devices, the package is, in most cases, an integral part of the device. Beyond protecting the moving parts, in many cases it serves as the interface with the environment it is working in, e.g. it connects the pressure sensor to the environment it is supposed to measure. For image projection chips it serves as the transparent window that allows the image to be projected on the wall. Besides being the interface, in many cases the package must also maintain a very specific environment inside the package. Maintaining that environment is a critical parameter to keep the device functioning."

Packaging is such a major issue in MEMS that Mallon believes that in conventional IC's, the package is commoditized and driven to minimum cost while for MEMS devices, often the MEMS die becomes commoditized and the package adds value.

But packaging isn't the only issue holding MEMS back from full commercialization. Overall market perception may be playing a strong role in its slow maturity.

Reliability has been an ongoing issue with MEMS. According to Heck, "Many people have had the impression that MEMS cannot be made reliable due to stiction, wear, or shock-resistance. That misconception has been proven wrong by the inertial sensors in our cars made by Analog Devices and Bosch, the DLP video projection chip from Texas Instruments, and the FBAR duplexers in cellular phones from Agilent."

Igal Ladabaum, President and CEO of Sensant Corp. was a presenter in the End User Application Session. He says that, "Another common misconception with regard to the MEMS industry is the analogy that it should take off like the integrated circuits industry. This thinking emerged in the early days because MEMS fabrication shares many materials and techniques with integrated circuit microfabrication. The fact is that MEMS are specific enough that there are no microprocessor or memory equivalents, for example. The MEMS industry can be compared to the ASIC industry at best, and even then, ASIC's only have a small set of packaging variants. MEMS are application specific, and so far, only a handful of "break-out" applications have materialized."

Wimplinger believes that in some cases the assessment of the market potential for MEMS isn't realistic. "There are many great MEMS devices but for some of them, the market estimations in regards to volume are way to optimistic. Also the target selling price vs. production cost has to be watched closely. MEMS will become true high volume if they are used in mass market consumer devices (cell phones, other portable devices all the way to appliances such as the coffee maker). In order to enter that market, pricing requirements have to be met."

Getting the monetary backing to develop MEMS also seems to be difficult. Aklaghi explains, "Since the MEMS industry is relatively immature (as compared to the semiconductor industry), it lacks many common manufacturing and packaging standards. This encourages products to be developed on a "one process-one product-one package" basis and, as a result, the advantages related to potential economies of scale are relatively limited. This makes it relatively expensive to develop products, which, in turn is exacerbated by the lower than expected investment in MEMS related products. Fortunately, over the past few years the industry has been maturing and availability of venture capital has been increasing."

Mallon adds that, "Current VC financing requires a big, quick, market hit to work. Many important smaller applications find it difficult to attract financing."

Even with all these problems, MEMS keeps pushing forward to enable new markets. Some of the important applications being enabled by MEMS could include sensor networks. According to Heck, "As wireless communications become cheaper and operate on lower power, a huge market for sensor networks will open up. Monitoring buildings, factories, and homes is currently very expensive, because wires need to be run everywhere. But as these sensor networks begin to become widespread, they will make use of sensors based on MEMS technology to measure everything from vibrations, to light, to chemicals in the air."

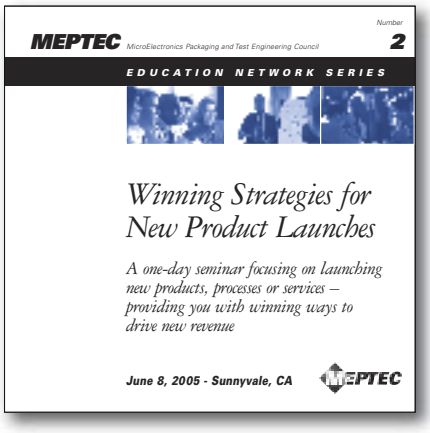
Heck also pointed out some other interesting new applications to watch for. "MEMS accelerometers are now being used in laptops to sense a drop and shut off the hard drive before the computer hits the ground. Accelerometers are beginning to appear in cell phones so you can flick your wrist to navigate through menus, rather than pressing those tiny buttons that give you finger cramps."

As MEMS continues to mature, we can expect to see them in many more everyday consumer products such as toys, cameras, laptop computers and biomedical products. Aklaghi says his company has several new MEMS-based products being developed for different markets. "The target markets are quite varied but most are looking at solutions which are smaller, faster and less expensive as compared to the incumbent solutions - which is really the promise of MEMS overall."

For MEMS to really succeed and mature, it needs to provide advantages over other existing technologies. According to Heck, "MEMS have proven to reduce cost and/or enhance functionality of many products in a way that cannot be substituted by any other technology."

Kenny believes that overall, MEMS has been more successful than most people realize. "MEMS will always be the hidden, en-abling element of bigger systems."

Apparently MEMS technology has matured past the "teenage years" but may still have a long, hard road ahead. Maybe we can consider this the "college years" where we learn more about the technology every day and it is quickly becoming a mature and useful addition to our society. ◆



Product Launch Overview: Launching New Products or Services Is Critical To Success

On June 8 at the Ramada Inn in Sunnyvale, MEPTEC held a unique one day seminar focusing on launching new products, processes and services, in an effort to help provide members with winning ways to drive new revenue. The following is an excerpt from the seminar proceedings, and describes much of the Product Launch section of the seminar:

New products, processes and services are the lifeblood of your business. They are the signpost for growth, drivers of new revenue and are a significant indicator of corporate viability. Success in bringing new products to market has a direct impact on the image and valuation of your firm. Cutting costs does not increase revenues; selling new products do. Success in selling new products is the road to growth. But, if the product is poorly launched – poorly received by the market – then revenue will lag and competition or substitute technology will slam shut the window of opportunity. When that happens growth slows and the bottom line suffers. The globalization of business has changed the landscape making old launch methods ineffectual and obsolete. New product introduction strategies are required. Ask yourself these three questions:

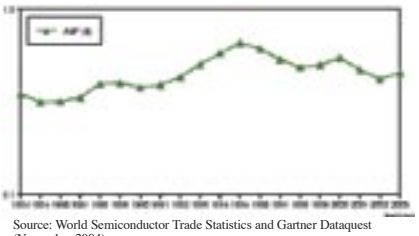
1. Have recent new products or services met revenue expectations?
2. Does your product introduction process drive sales?
3. Is your existing launch process world-class?

If the answer is "no" to any of them read on: To launch a new product you want to get it rapidly out into the market. You need satisfied buyers whom you can use to promote the product's adoption by a wider audience. The classic strategy for new technology lies in finding those customer segments which are early adopters. Once the new product has been launched and is widely accepted by the early adopters, then target multiple vertical markets where the more conservative customers will be easier to sell.

The seminar also included an interesting discussion on "Maven Marketing", and was taught by Charles DiLisio, President of D-Side Advisors. A "maven" is described in this context as the "go-to guy" in a company to get information on new emerging companies or technology; he or she most likely works for the CTO or directly for the CEO; they are the person who looks for ways to integrate existing products and services into an entirely new product, and is the person who can integrate ideas across the company's functional group. This person can be of great assistance in helping sales and marketing develop new non-traditional target markets, or niches that may not have been considered. He or she can help sales and marketing to provide a system solution, not just make a sale.

A CD of the proceedings is available. Contact bcooper@meptec.org or call 650-988-7125 for more information. ◆

The Changing Market Dynamics of Semiconductor Equipment



Source: World Semiconductor Trade Statistics and Gartner Dataquest (November 2004)

Figure 1. ASP Inflection Point for Semiconductors

Jim Walker, Mary Olsson, Dean Freeman and Bob Johnson
Gartner-Dataquest

The semiconductor equipment industry has enjoyed strong growth since its inception. From 1972 through the mid-1990s, the industry achieved a compound annual growth rate (CAGR) of 15 to 17 percent. This strong growth made the industry one of Wall Street's "darlings" because of its high profit-to-expense ratios, which in turn were a result of the industry's potential for strong growth. However, in the mid-1990s, an inflection occurred in the growth curve. Beginning in 1994 and 1995, the industry CAGR for semiconductor revenue dropped from a range of 15 to 17 percent and has been reset to about 10 to 12 percent. The semiconductor equipment industry has subsequently also been dealing with a slowdown in growth.

What was the cause for this reduced growth? With the exception of 2001, unit demand continued to increase. New fabs were being added at a significant clip. The growth of the fabless industry was one of the hot topics in the marketplace. Why then, was there a drop in the revenue CAGR?

The answer to this question is partly related to the average selling price (ASP) of semiconductors. In mid-1995, ASPs also had a similar inflection point that correlates very well with the inflection point in the revenue CAGR (see Figure 1). So now the question becomes "Why did the ASPs begin to decline?"

While pricing pressures are always one of the major drivers of market dynamics, several other issues have played a significant role over the past 10 years. These include:

- Consumerism
- Increased competition
- Capital markets
- Fewer buying centers
- The shift of semiconductor manufacturing to Asia/Pacific
- The pace of technology

All of these issues have played and will continue to play a role in the market dynamics for semiconductor equipment manufacturers.

Consumerism

The growth of consumer electronics has led to significant growth in unit volumes for chips. However, due to the extreme low-cost desires of the consumer marketplace, it has also led to a decline in ASPs. This will only continue in the future, as consumer semiconductors will account for more than 50 percent of semiconductor revenue in 2013. Early in the semiconductor industry's history, the mantra was, "If you can make it, they will buy it." The industry blossomed on the productivity gains it helped provide to businesses.

Over time the business environment began to saturate and during the 1990's shifted to a market driven by replacement cycles. Unit growth remained strong as companies sold to consumers at increasing rates. However, the consumer market has characteristics different from the business market. Lifestyle enhancement drives the consumer market, and productivity is not as important. Price points drive purchases. As a result, margins came under pressure as consumers looked for the best deal. A good recent example of this is how quickly the price of DVD players dropped to a price at which they were affordable to nearly everyone. The price of electronic goods began to erode; as a result, semiconductor ASPs began their decline.

The early industry mantra no longer applies. The industry has migrated from a supply "push" to a demand "pull" market, which is driving an environment of increasing price sensitivity to suppliers. Thus, margin pressure is rising, the price premium segment of the market is shrinking on a relative basis, APSs are declining, and the long-term revenue growth trend is defunct.

With the revenue growth trend broken, the supply chain has begun to feel pricing pressure. To meet consumer price points, all participants in the supply chain must look at their margins. The issue of price points vs. margins hit silicon suppliers especially hard in the 1990s. The pricing pressure also affects semiconductor equipment manufacturers and industry material suppliers.

Increased Competition

By the mid-1990s, competition was significant because of the efforts by South Korean/Taiwanese to improve market share and by the rapid emergence of the fabless/foundry model. The capability to design and manufacture a semiconductor without needing to build your own fab led many fabless companies to enter the market, which dramatically increased the level of competition.

In the early 1990s, the number of fabless companies in the marketplace rose dramatically. The rise of the foundry model, with manufacturing capabilities less than a generation behind that of the integrated device manufacturers (IDMs), made it simple for a company to design and produce devices for the semiconductor market. This rapid rise of the fabless companies, along with a growing number of dynamic random-access memory suppliers, led to greater competition, which in turn led to pricing wars for market share dominance. The

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expanded competition and the trend toward consumerism are two key issues driving ASPs down. Until further consolidation of silicon device providers occurs, little relief for ASPs is likely in the future.

Capital Markets

Much of the recent historical growth in the semiconductor market was the result of new entrants – mainly memory or foundry companies – funded by offerings in the public capital markets or government incentives. However, the long downcycle has reduced the attraction of semiconductor ventures to capital markets. Thus, there will probably be few new major entrants into the industry. Also, semiconductor manufacturers must generate sufficient cash themselves to fund new capacity. This will drive the trend for more joint ventures and partnerships for both semiconductor manufacturers and semiconductor equipment manufacturers as they look for new ways to deal with the reduced capital investment levels.

Fewer Buying Centers

Now, as the industry continues to mature, fewer buying centers are available for sales by semiconductor equipment manufacturers. Foundries, the move to 300 millimeter (mm), alliances and research consortiums have all led to fewer locales where semiconductor equipment can be tested and then sold to the market. "Copy exact "or "copy smartly" policies have created an environment in which one toolset is sold not just to one company, but also to any company associated with a particular consortium. Overall, these factors have made it easier to sell into the industry, yet they have limited the number of opportunities while requiring vendors to be in on the ground floor during the R&D cycle. Companies can no longer afford to wait out the R&D process and then rush in when production tools are needed. Thus, the trend has been adoption of the foundry model and creation of multi-company alliances and consortiums.

Shift of Manufacturing Centers

Since the 1980s, the semiconductor manufacturing centers have been shifting their locations. As a result of government incentives, inexpensive capital allowed the industry to move from the Americas and Europe to Japan, then South Korea and Taiwan. There has been a great deal of discussion about whether China will become the next semiconductor manufacturing power. Although China would like to become a semiconductor power, it has yet to offer sufficient tax incentives, such as those that led to the booms in Japan, South Korea and Taiwan. Thus, for at least this cycle, China will not wrest significant market share from other semiconductor manufacturing centers. North American companies have led spending in absolute terms for 20 years, but Asia/Pacific companies have led in terms of spending relative to revenue. Asia/Pacific's market share has increased dramatically, from nearly 5 percent in 1990 to over 30 percent today.

Historical spending patterns provide clues about what to expect in the next cycle. Although companies based in the Americas have retained their leadership in absolute spending for the past decade, Asia/Pacific companies have aggressively maintained their spending above other regions. From a company headquarters' perspective, North and South America will, for the first time, drop below the Asia/Pacific region in terms of total spending in 2004. This trend is expected to continue as more companies turn fabless and look to the Asia/Pacific foundries to provide the manufacturing capability needed to drive industry growth.

Impact on Semiconductor Equipment Suppliers: Industry Profitability Is Low

With manufacturing shifting to Asia/Pacific and chip ASPs in decline, how have semiconductor equipment manufacturers performed during the past 10 years? The net profits during this time were disappointing for a growth industry. If we take the average percentage of profit, the industry has run a deficit of 1.8 percent. Fortunately, from a dollar perspective – the total net profit as a percentage of the total revenue – the picture is a bit brighter; the industry averaged 3.3 percent during the 10-year period. However, since 1998, the equipment industry has not been positive, with the exception of 2000, in which net profit was 10 percent. The rest of that time, the range was between negative 1 percent and negative 27 percent; 2002 and 2003 had negative 27 percent and 16 percent, respectively.

Considering now the distribution of the top 32 semiconductor equipment companies, the number that are profitable is a bit surprising. Thirteen have a negative 10-year average. Of those 13, seven average greater than negative 10 percent.

What can the future bring?

With the birth of consumerism and slower growth in the mid-1990s, the market dynamics of the semiconductor industry have involved shrinking margins for manufacturers as a result of declining ASPs caused by increased competition. While 300 mm may improve capital efficiency, sufficient capital is still a barrier to market entry for smaller semiconductor companies. Semiconductor companies have reacted to these changing business dynamics by finding methods to reduce costs by joining forces for development and manufacturing. This has taken the form of joining consortiums, establishing alliances and moving to foundries for manufacturing; such actions have resulted in the consolidation of buying centers.

These industry changes have created a significant financial impact on the semiconductor equipment companies during the past 10 years. Of the 32 companies measured, 19 have a positive percentage of net income when averaged from 1994 through 2003, whereas 13 have a negative 10-year average, and eight are running at more than negative 5 percent.

From a business perspective, having a negative cash flow for an extended time without going broke is difficult. With the industry decline in ASPs and pressure on margins, companies operating in the red will need to press hard to return to profitability. However, the industry's cyclical nature means some of these vendors will likely need to either merge or fade away because they will not have returned to profitability before the next slowdown begins. Unfortunately, the upcycle will be shorter than initially anticipated, so which companies are "healthy" enough or have enough cash to weather the anticipated slowdown remains to be seen. ◆

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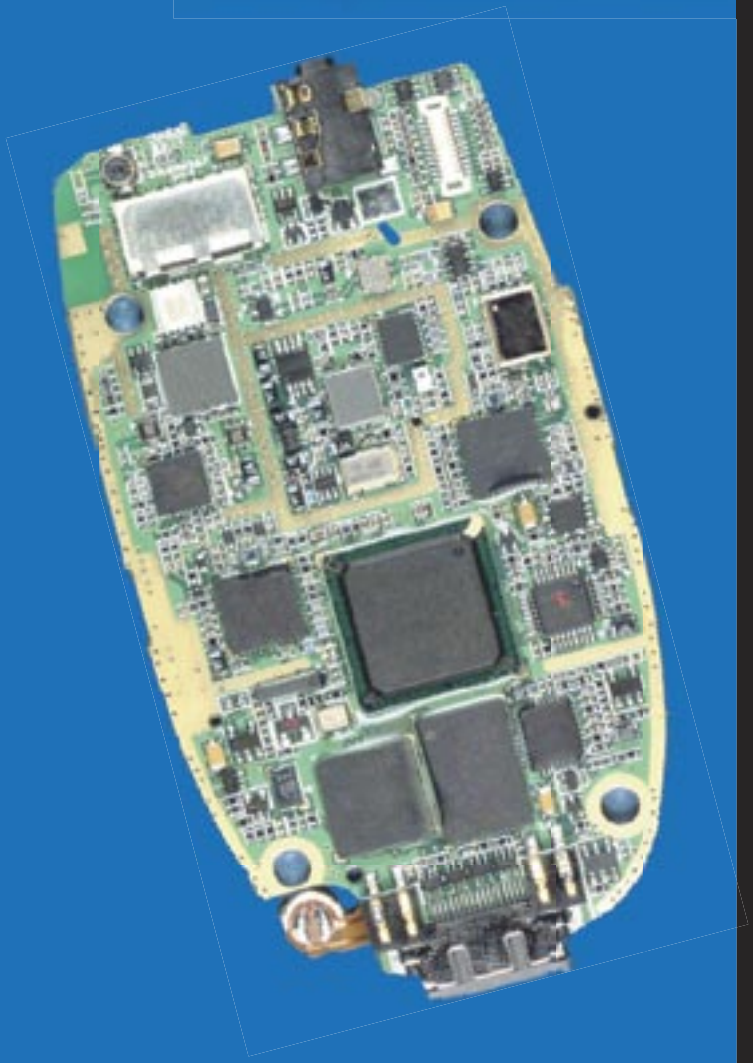

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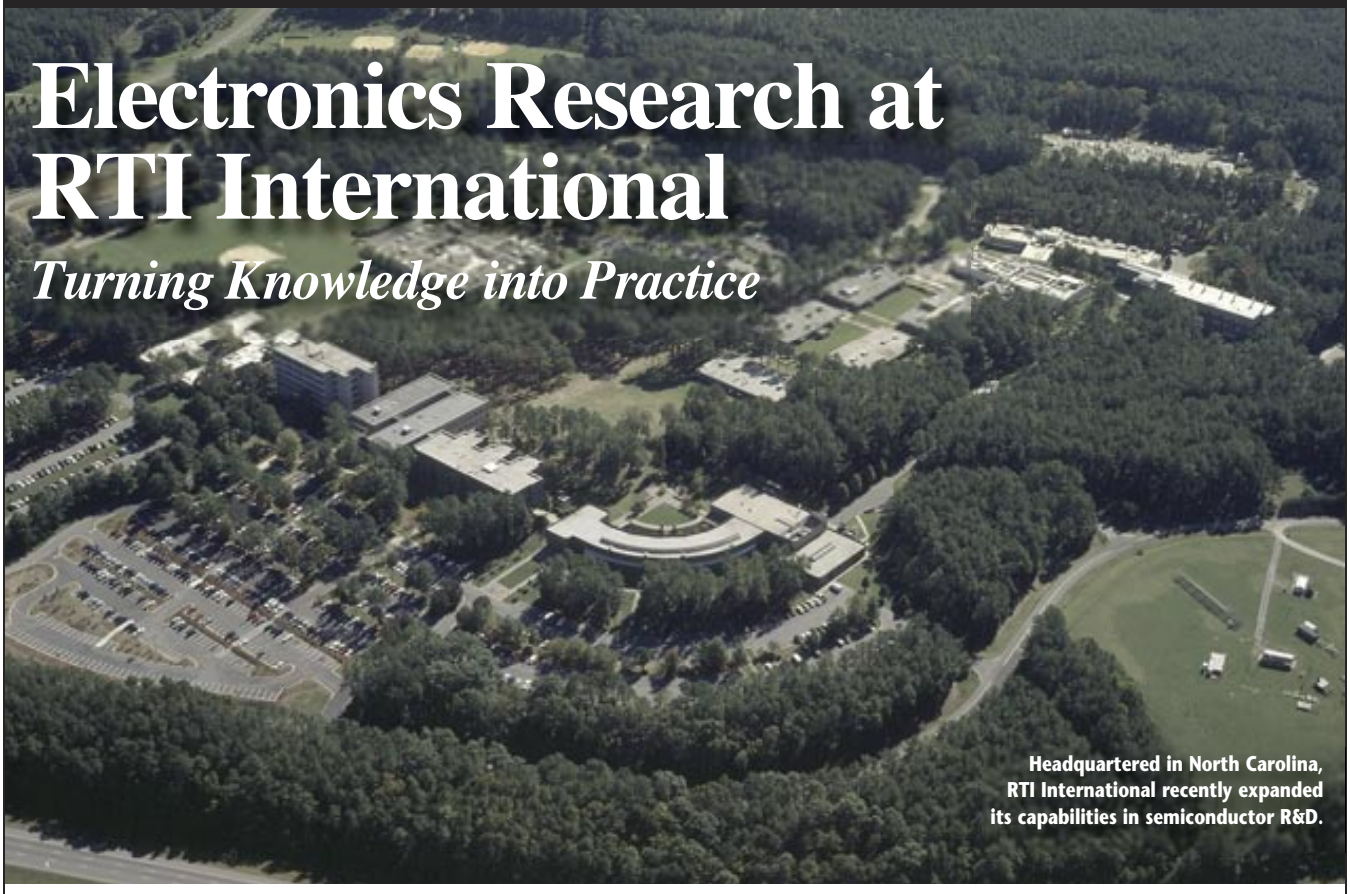


Headquartered in North Carolina, RTI International recently expanded its capabilities in semiconductor R&D.

To members of the semiconductor industry, RTI International—previously known as Research Triangle Institute – is surely no stranger. Perhaps best known for its breakthrough developments in thermoelectrics announced in the October 2001 issue of Nature, RTI's experience in electronics and semiconductor theory and research dates back to the mid-1960s, when integrated circuit technology was in its infancy. Over the years, RTI has built a long and distinguished record in reactor and process development, materials growth, surface preparation, and surface analysis.

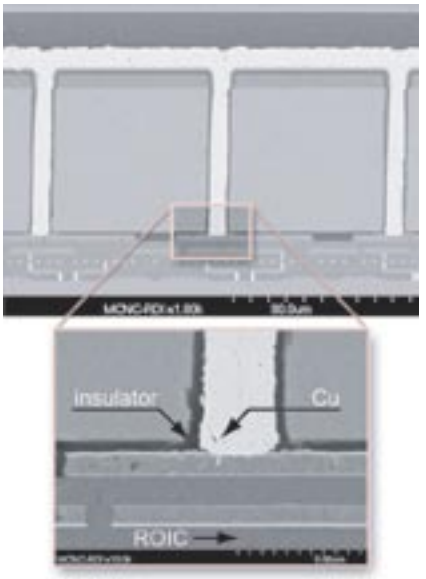
Just this year, RTI again made the news by dramatically expanding its capabilities in semiconductor R&D. RTI recently acquired the MCNC Research and Development Institute, adding more than 60 experts in microfabrication, signal electronics, and communications protocols to its electronics research staff.

RTI's engineers conduct basic and applied research on new materials, device technology, device manufacturing, and device reliability. Achievements include developing novel ways to integrate dissimilar materials – especially active semiconductors – using wafer-bonding and through-wafer interconnect technologies. As an extension of our work in the analysis and fabrication of novel materials, RTI has developed a number of innovative solutions for meeting various electronic packaging and assembly requirements, including ultra fine-pitch flip chip bumping, fine-pitch flip chip assembly, fluxless soldering and assembly using plasma-assisted dry soldering (pads) technology, MEMS packaging, and reliability testing.

3-D Vertical Interconnect Technology

One example of RTI's cutting-edge R&D is its work in vertical interconnect methods. RTI's 3-D interconnect technology increases integrated circuit (IC) performance while reducing weight and volume. RTI has demonstrated vertical interconnects with diameters as small as 4μ and up to 10:1 aspect ratios.

RTI is bringing the benefits of this technology – improved processing speed, less power consumption, lower cost, and smaller footprint – on a joint project sponsored by the Coherent Communications, Imaging, and Targeting (CCIT) program managed by Defense Advanced Research Projects Agency's (DARPA's) Tactical Technology Office. Working with Lucent Technologies' Bell Labs and the New Jersey Nanotechnology Consortium, RTI is devel-



Cross-sectional scanning electron micrographs of RTI's 3-D interconnects are fabricated in thinned layers of Si mounted on read-out IC chips.

oping light-weight, high-resolution, high-speed microelectromechanical systems (MEMS) to create a spatial light modulator (SLM). This MEMS-based technology will be the basis for a scalable prototype system that can digitally manipulate optical beams of light via micro-mirror arrays. The technology will provide an alternative to the adaptive optics used in current communication systems, which are too heavy to use in advanced, mobile platforms. Specifically, the technology is expected to increase communication speeds in the multi-gigabit-per-second range and will provide aberration-free 3-D imaging.

For this project, RTI's interconnect technology will enable the vertical integration of a MEMS mirror array with the necessary electronics. While the MEMS technology is being developed for CCIT and other military applications, it may have the potential for commercial applications such as health care and astronomy.

RTI is also applying its 3-D interconnect technology to new infrared detector systems to be used in high-performance military and space surveillance applications. This project, sponsored by the DARPA's Microsystems Technology Office, requires 3-D architectures and circuits to enable massively parallel signal processing for high-resolution infrared focal plane arrays (FPAs) necessary for the strategic and tactical systems of the future.

RTI's 3-D interconnect technology allows the detector arrays to be integrated with multiple layers of ICs by means of insulated and metallized vias (vertical holes) etched through the body of the IC chips. The resulting multi-layer structure offers short interconnect paths, enables significantly higher inter-layer bandwidths for more demanding signal processing requirements, and reduces noise for improved signal dynamic range. Incorporating this unique 3-D technology will ultimately improve the performance of the infrared sensing systems by significantly increasing processing capability and signal integrity.

AC-Coupled Interconnect Technology

RTI is working with North Carolina State University (NCSU) to develop the next generation of packaging technology, AC-coupled interconnects (ACCI), which produces a higher density interconnect than commercially available flip chip bumping. ACCI leverages an array of non-contacting structures for capacitive multichip coupling, instead of using the traditional wire- or solder-based "ohmic" contacts.

ACCI addresses the needs of future spaceborne electronic systems that will require high-bandwidth, low-power interfaces between chips and modules. This innovative technology also provides greater reliability than traditional interconnect approaches, and it achieves the signal density required by the 2003 International Technology Roadmap for Semiconductors (ITRS) in 2016. By enabling denser packaging, ACCI supports faster processing and lower voltage requirements.

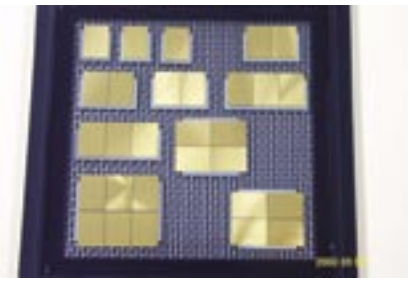
ACCI requires less protection against electrostatic discharge than direct coupled interconnects, because an overglass dielectric protects the input gate. In addition, because the physical structures required for ACCI are not very different from those made today, the manufacturing process can be left entirely unchanged in most implementations of this technology.

Joint development of this technology with engineers at NCSU reflects typical productive collaborations between RTI and other research organizations.

Fine-Pitch Bumping for High-Energy Physics and Advanced Medical Imaging

Most commercial flip chip applications are for devices with I/O pitches of 150-250μm. However, there are growing niche markets for fine-pitch wafer bumping for devices with I/O pitches of 100μm and less. The associated wafer bumping, handling, and assembly of these devices becomes considerably more difficult compared with most commercial applications. In many cases the sensor wafers are thinned prior to bump processing, and have contacts on both sides. RTI is providing world-class development and prototyping assembly to meet these needs.

For example, in the field of high-energy physics, several new experiments require large numbers of pixilated sensor devices to be mounted to read-out integrated circuits (ROICs), which make up the detectors that track collision events. The pixels in these detectors must be very small (50-100μm pitch) to provide adequate spatial resolution for particle tracking. Because the pixels and their electrical interconnections are arrayed over the entire area of the device, solder bumping is the natural choice for the integration of detector elements to read-out and support electronics.



RTI is using ultra fine-pitch flip chip bumping to fabricate these single- and multi-chip detector modules with extremely high I/O density.

In the field of advanced medical imaging, pixilated detectors are being utilized to directly detect the charge deposited by each primary x-ray photon to create a high-resolution x-ray image. RTI is working with CERN in Switzerland to develop high-density X-ray imagers. These advanced imaging systems are made possible through rapid developments in deep sub-micron complementary metal-oxide semiconductor (CMOS) technology and require RTI's dense interconnection technologies. ◆

About RTI International

Founded in 1958, RTI is an independent, nonprofit organization dedicated to conducting research that improves the human condition. RTI is headquartered in North Carolina and maintains laboratory and office facilities throughout the U.S. and overseas. RTI conducts innovative R&D and offers a full spectrum of multidisciplinary services across numerous areas of study in the physical, life, and social sciences. Funds to support RTI's work come from clients in government, industry, and public service.

RTI's electronics R&D spans thermoelectrics; radiation-hardened electronics; sensors and actuators; organic, macro-, and optoelectronics; biomedical and environmental electronics; display technologies; signal electronics; analytical and microfabrication services; and 3-D integration and advanced electronic packaging.

RTI has extensive experience meeting the needs of commercial clients, including commercialization and technology transfer of processes developed at RTI, as well as assistance with contamination control.

For more information on semiconductor research at RTI, including potential collaborative opportunities, visit www.rti.org/electronics or contact Ken Williams, Director, Center for Materials and Electronics Technology, at 919-248-1801 or ckw@rti.org.

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To learn more about the Expo and Supplier Tracks, visit the event website at **www.fsa.org/suppliers_expo/usa**

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Carsem Doubles the Size of Their Test Operation in Malaysia

SCOTTS VALLEY, CA – Carsem has announced that they are expanding the manufacturing space dedicated to the test services operation at the Carsem S-Site facility. The current expansion from 40,000 sq. ft. to 66,000 sq. ft. is in the final phase of completion and, by the end of 2005, the area will be increased to 96,000 sq. ft. Combined with the current 14,000 sq. ft. test operation at the Carsem M-site this will bring the total area for wafer probe and final test services from the current 54k sq. ft. to 110k sq. ft.

Mr. David Comley, Carsem's Group Managing Director, stated, "The turnkey test services segment of our business is growing at a significantly faster rate that any other segment and we see this trend continuing for quite some time. Carsem is fully committed to providing our customers with the test infrastructure and engineering support services they require in order for them to meet their competitive demands."

Carsem is a member of the Hong Leong Group with factories located in Ipoh, Malaysia, Suzhou, China and sales offices across the USA, plus the UK and Taiwan. Carsem, Inc. sales headquarters is located at 269 Mt. Hermon Road, Suite 104, Scotts Valley, CA 95066, phone (831) 438-6861, fax (831) 438-6863, web site: www.carsem.com.

Premier Acquires Austin Test Operations From Cirrus Logic

TEMPE, AZ – Premier Semiconductor Services, LLC/LP has announced that it has acquired Cirrus Logic's Austin-based semiconductor test operation. As part of the transition, Cirrus Logic's test operation's employees become Premier employees and form the basis for Premier's new Austin test facility. Included in the transfer will be such equipment assets as testers, handlers and probers.

From this test site Premier will continue to serve Cirrus Logic, along with providing test, test engineering development, wafer probe/sort, and burn-in services to other customers. Customers will benefit from the site's current capabilities and capacity, along with many other backend services that will be offered for a total turnkey solution.

According to Premier's Chief Executive Officer David Loaney, "This acquisition will serve to further solidify our partnership with Cirrus Logic as it extends the relationship to include local test development in addition to the current backend processing agreement already in place. This acquisition allows us to further expand Premier's already extensive service offerings and capabilities to current and potential new customers."

In addition to electrical test, test engineering development, wafer probe/sort and burn-in services mentioned above, Premier also provides the following services: programming, solder ball attach and rework, tin/lead conversion to or from Pb free, hot solder dip & retinning, solderability testing & restoration, IC recovery from boards, fine & gross leak test, lead inspection, automated lead conditioning, tape and reel, bake & dry pack, ink & laser mark, demark & blacktop, and more. With multiple domestic facilities, Premier is conveniently situated for a fast and accurate alternative to expensive in-house, back-end processing.

For a complete list of services and locations, or for more information, visit our web site at www.premierS2.com.

Rohm and Haas Announces Senior Management Changes

PHILADELPHIA, PA – Rohm and Haas Company announced several management changes for its leadership team, prompted by the retirement of Stephen Robinson, Vice President and Business Unit Director for Architectural and Functional Coatings, at the end of April.

Luis Fernandez, currently Vice President and Business Unit Director for Plastics Additives, will succeed Robinson as head of the global Architectural and Functional Coatings business. During his 20 years with the company, Fernandez, 42, has worked in Latin America, Europe and North America for a number of the company's coatings and plastics businesses. Fernandez holds a B.S. degree in Chemical Engineering from Universidad Iberoamericana in Mexico and attended the Wharton School of the University of Pennsylvania.

Patrice Barthelmes, currently Vice President and Business Unit Director for Circuit Board Technologies, will succeed Fernandez as head of the Plastics Additives business. Barthelmes, 47, joined Rohm and Haas in 1999 after 16 years of experience with firms such as Air Liquide, Sanofi and SKW Biosystems. Barthelmes holds a B.S. degree in Chemical Engineering from INSA, Toulouse in France, and a M.S. degree in International Management from IMD Business School, Lausanne in Switzerland. He will continue to be based in Paris, and retains his responsibilities as General Manager for Rohm and Haas France.

Sam Shoemaker will become Business Unit Director for Circuit Board Technologies and Regional Director for the company's Asia-Pacific region. Shoemaker currently has regional business responsibilities for Circuit Board Technologies and Packaging and Finishing Technologies. Shoemaker also heads strategic planning for the Asia-Pacific region. Shoemaker, 43, joined the company in 1984. He holds a BA degree in Chemistry from the University of San Diego.

Raj Gupta, Chairman, President and CEO of Rohm and Haas, had the highest praise for Robinson, who will be 55 when he retires at the end of April. "I consider Steve to be a good friend and an outstanding contributor to our company's success." Robinson joined Rohm and Haas in 1996 after having distinguished himself as a highly capable executive during a 23-year career with Monsanto. He first served as Director of Strategic Planning and Licensing for the company, then was chosen to lead the company's Microelectronic Technologies business. He has been head of the Architectural and Functional Coatings business since early in 2004.

Additional information about Rohm and Haas can be found at www.rohmhaas.com.

BE Semiconductor Industries Announces Consolidation of its Dutch Fico Operations

DRUNEN, THE NETHERLANDS – BE Semiconductor Industries N.V. has announced the further consolidation and integration of its Dutch Fico molding, trim and form and tooling operations at its Duiven, the Netherlands facility. The consolidation involves the termination of 32 employees that is expected to occur in the third quarter of 2005 and the integration of production and administrative personnel. Besi intends to take a charge in the second quarter ending June 30, 2005 to cover the estimated costs of this workforce reduction which is not expected to exceed _ 1.7 million.

In commenting on the announcement, President and Chief Executive Officer Richard W. Blickman noted: "We have taken the difficult steps of restructuring and consolidating our Dutch trim and form, molding and tooling operations over the past six months in order to improve the productivity of our manufacturing capacity. By means of the current workforce reduction and the restructuring announced in December 2004, we will have reduced our overall headcount

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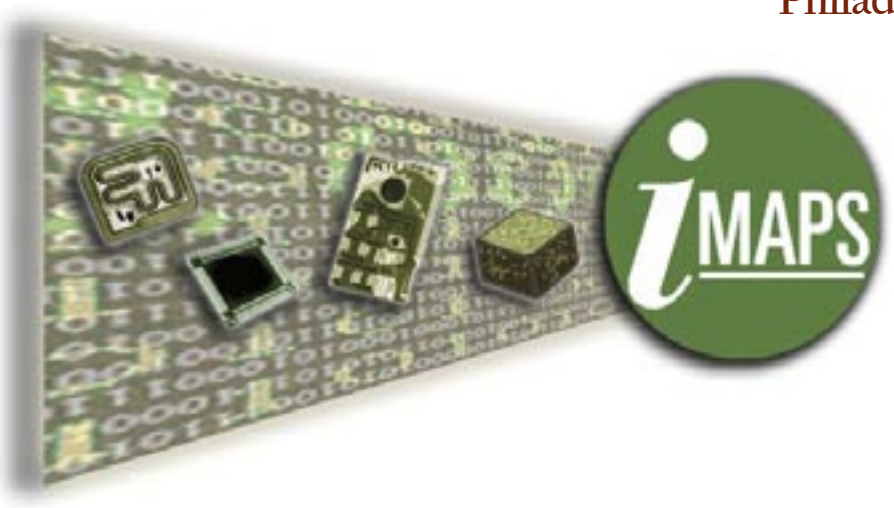

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by 113 or 10% and our Dutch personnel by approximately 33%. The restructuring is consistent with Besi's plans to reduce its manufacturing presence in higher cost geographies and to rely more on lower cost manufacturing regions for certain equipment and tooling production, particularly China and Malaysia."

The Company expects to report final second quarter 2005 results on July 28, 2005.

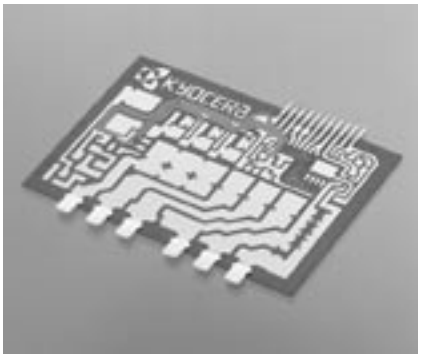
SIX SIGMA Celebrates 15 Years in Business and 20 Million Components Processed

MILPITAS, CA– SIX SIGMA, a leading provider of column attach, robotic solder dip, BGA reballing, and failure analysis services for the electronic component packaging industry, has announced that it is celebrating 15 years of business this year in which it has serviced over 20 million components. "May marks two significant milestones for Six Sigma. Without our customers' continued support, we could not have met these milestones, " remarked Six Sigma's president, Russ Winslow. "We thank our customers for helping make Six Sigma an industry leader in robotic solder dip, column attach, and BGA reballing, services.

SIX SIGMA began operations in 1990 providing robotic hot solder dipping (lead finish) services and related testing for the semiconductor and printed circuit board industries. Today, SIX SIGMA's services include solder column attach, BGA ball attach, and BGA reballing services. Components processed by SIX SIGMA are in applications that vary from the most sophisticated missile guidance systems, to the engine controllers in commercial airlines, to automobile passive restraint systems. SIX SIGMA is now a recognized leader in semiconductor lead finish - processing millions of high-reliability semiconductor components each year.

In addition to recently achieving DSCC commercial laboratory suitability status for hermitic testing, SIX SIGMA continues to provide it's customers new services that meet changing demands. Two new services are now available from SIX SIGMA. Solderability.com is their internet based ordering and reporting system for solderability tests. Additionally to meet the market driven demand for lead-free components in commercial products and tin whisker mitigation in high reliability applications, SIX SIGMA offers component lead finish conversion services to meet industry demand to convert component package interconnect from tin/lead alloy to lead-free alloy and visa-versa.

For more information visit the company website at www.sixsigmaservices.com or call (408) 956-0100.



Kyocera Copper Bonded Silicon Nitride Substrate Achieved 5000 Cycles of Temperature Cycling Test

SAN DIEGO, CA – Kyocera announced its Copper Bonded Silicon Nitride Ceramic Substrate achieved 5,000 cycles of air to air temperature cycling test with a condition of -60 to +175 degrees centigrade without any failure. Its base ceramic substrate is Kyocera Silicon Nitride (Si3N4) with 850 MPa of flexural strength and 5.0 MPam1/2 of fracture toughness. This Silicon Nitride is much stronger compared to other ceramics, for example, Alumina (Al2O3) with 274 MPa of flexural strength and 3.3 MPam1/2 of fracture toughness and Aluminum Nitride (AlN) with 400 MPa and 2.7 MPam1/2. Copper is bonded on the Silicon Nitride substrate by an active metal bonding (AMB) method using Silver-Copper-Titanium brazing metallization. Active Metal Bonding is a stronger method of adhering copper to ceramics when compared to conventional copper bonding methods without metallization, typically using a copper oxide process. The AMB copper bonded Silicon Nitride substrate is much stronger, mechanically than conventional copper bonded Alumina and Aluminum Nitride substrates. Kyocera AMB Silicon Nitride technology is suitable as a substrate material for use in power microelectronics applications in automotive, aerospace and other harsh environment.

San Diego-based Kyocera America, Inc. designs, manufactures and assembles a broad range of microelectronic packaging solutions and optoelectronic components for the telecommunications, wireless, optoelectronic, semiconductor and specialty products markets based on advanced ceramic and plastic material technologies.

RTI Introduces the First Truly Flexible QFN Socket for FA and Engineering/ Production

MORGAN HILL, CA – The RTI 900-113X pogo pin sockets are designed to meet most low pin count failure analysis and engineering test requirements for QFN, LLP, QFP, BGA, LGA, LLP and other types of small packages. Several lid styles are available including a screw-down FA lid for micro-probing, a dual-latch lid and dual-latch clam-shell lid for engineering, and several other special purpose lids. The sockets are designed for bench test, liquid crystal analysis, ESD testing, back-side emission, micro probing, characterization, and low volume engineering and production testing. Options include multiple center ground pads and heated sockets for liquid crystal testing. Mini-DUT cards and many types of fixtures are available for almost any type of FA, engineering, or production application. The 900-113X sockets are priced midway between burn-in sockets and full production sockets.

For additional information, visit RTI's web site at www.testfixtures.com or contact Bill Robson at 408-779-8008.

STATS ChipPAC Expands Flip Chip Portfolio with 300mm Wafer Bumping

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced it will offer 300mm electroplated wafer bumping services in the third quarter of 2005 to complete the Company's full turnkey service offering for advanced flip chip applications. In addition, STATS ChipPAC has expanded solder alloy choices for its current flip chip offering and enriched its design, simulation, and characterization capabilities for high end flip chip packages.

To address growing demand for advanced flip chip applications, STATS ChipPAC will offer 300mm wafer bumping service to Taiwan Semiconductor Manufacturing Company (TSMC) customers in the third quarter of 2005. Using consigned equipment, this electroplating bumping technique is well suited for fine-pitch flip chip applications as it provides superior bump quality, higher yield, finer bump pitches and higher temperature resistance than other wafer bumping methods.

STATS ChipPAC has a strong flip chip

portfolio encompassing single die, multi-die, multi-package and thermally enhanced solutions which provide significant size and performance advantages over traditional packaging approaches. STATS ChipPAC's Flip Chip packaging configurations include Ball Grid Array (BGA), Chip Scale Packages (CSP), Land Grid Array (LGA), Quad Flat No Lead (QFN), Wafer Level CSP (WLCSP), and System-in-Package (SiP) modules as well as next generation three dimensional (3D) packages.

The new 300mm wafer bumping capability complements STATS ChipPAC's current capability which comprises low cost printed wafer bumping on 200mm wafers with redistribution (RDL) and repassivation. STATS ChipPAC has also added ultra low alpha Hi Pb composition to its standard offering of Eutectic and lead free (Pb free). The addition of Hi Pb alloy is particularly important to semiconductor companies with devices requiring high temperature stability, very high reliability, and resistance to electromigration. STATS ChipPAC has already qualified the assembly process for Hi Pb bumping in the fourth quarter of 2004 and has now achieved high volume manufacturing.

SiliconPipe Demonstrates 10G Sidewinder Performance

SiliconPipe proves its technology

SAN JOSE, CA – SiliconPipe has successfully demonstrated its copper interconnection technology by sending a 10Gbps signal through a backplane channel consisting of two standard connectors and 30 inches of trace. The test setup, nicknamed Sidewinder, delivered an eye-opening 60% timing margin at the receiver, utilizing industry standard NRZ signaling and a very low 100 mVp-p signal voltage.

This demonstration was done in cooperation with PHY IC technology from Aeluros. The Aeluros AEL1002 device provides an industry-leading solution for XFP applications, and is rated to transmit an 800 mVp-p signal across 12 inches of printed circuit board and one connector. The remarkable channel efficiency of SiliconPipe's technology made it possible to double the operating distance and adds two connectors while significantly reducing power consumption. More detailed testing is planned on the Sidewinder to ascertain full channel parameters and determine the upper limit of its performance.

"This demonstration gives potential adopters a "proof-of-concept" that can't be denied," says Kevin Grundy, President and CEO of SiliconPipe. "We have moved from the theoretical to the applied, and the concepts work even better than predicted by the computer simulations. Soon we will be demonstrating more SiliconPipe interconnection solutions to arm designers with low power alternatives to signal integrity problems."

Leading edge package assembler NextGen built the Sidewinder demonstration system under a SiliconPipe license. Sidewinder uses an Aeluros SERDES chip and two standard connectors from ERNI.

For more information about SiliconPipe, please visit the company's website at www.siliconpipe.com.

Perfect Cost of Ownership for Telecom Card Production

Muehlbauer, a worldwide provider of technologically innovative security solutions in a market segment termed by the company as the "TECURITY-market", launches the new combined milling & implanting system CMI 3010plus for Smart Card production.

Combined solutions meet the future demands of the market. Thus, Muehlbauer is introducing a new combined milling & implanting line for the production of GSM/UMTS and prepaid telecom cards. This system includes the single process steps milling, implanting, lamination, and plug punching. Freely programmable parameters, e.g. for the new milling head and the hot or cold implanting process, offer highest flexibility and reliability.

The CMI 3010plus can handle all common chip types as well as new flip chip-mounted module tapes. A fast and easy change over to another module variant is guaranteed by a subtle module tape transport. Optionally, Dual Interface cards can be produced, too.

The punching of different plug formats allows a wide range of applications in one compact solution, such as Mini-VISA or Mini-SIM cards. Operation is only done by one user, helping to save personnel and footprint costs for a better cost of ownership than many other types of equipment.

With different in- and output possibilities, the CMI 3010plus reaches a very high autonomic production time with a throughput of up to 3,000 cards per hour depending on card material and cavity size.

Information on Muehlbauer is available on the Internet at www.muehlbauer.de.

Next-Generation Stud Bumper Among New Technology To Be Exhibited by Kulicke & Soffa at Semicon West

WILLOW GROVE, PA, – Kulicke & Soffa Industries, Inc. will demonstrate its new advanced Stud Bumping Machine as well as a new web-based, on-line wire selection software tool during Semicon West to be held in San Francisco, CA from July 12 to 14. Kulicke & Soffa will be exhibiting in booth 7301, Level 1 of the Moscone Center.

Designed for the growing flip chip market, the ATPremier™ High-speed Stud Bumper incorporates new hardware and software technology to provide greatly reduced cost-of-ownership compared to existing stud bumping products. Offering the fastest bumping speeds in the market along with the smallest footprint, ATPremier maximizes the use of resources and clean room space. Currently, the ATPremier bonds 36 standard bumps/second at 60 μm pitch.

In addition to the ATPremier, Kulicke & Soffa will introduce its new on-line gold bonding wire selection tool called WirePRO™ during Semicon West. This new web-based software program was developed to provide customers with a faster, more convenient tool in the selection of bonding wires for specific applications. Accessible through K&S' corporate web-site, www.kns.com, this new software program will be offered as a free, value-added service to all front-end semiconductor companies and packaging assemblers around the world.

To set-up a private meeting with K&S marketing personnel during Semicon West or to get more pre-show insights into Kulicke & Soffa's new technologies, please contact Mark Sullivan at msullivan@kns.com.

AT Premier
New Stud Bumping Technology

Honeywell Announces Availability of Wafer Thinning Materials for Semiconductor Manufacturing

MORRIS TOWNSHIP, NJ – Honeywell has announced the availability of "wafer thinning materials" as part of its product portfolio for semiconductor manufacturing.

The materials will be produced at Honeywell's new Electronic Materials manufacturing site in Chandler, Ariz., which opened in February of this year, as well as at Honeywell's Seelze, Germany facility.

"I am pleased to announce the availability of our new wafer thinning materials because it demonstrates delivery on that plan and our commitment to provide customized, application-specific solutions to our customers," said Barry Russell, vice president and general manager of Honeywell Electronic Materials.

In addition to wafer thinning materials, Honeywell will be producing other advanced wet chemicals. These solutions represent Honeywell's commitment to providing customized, application-specific product offerings to its customers with unsurpassed lot-to-lot consistency, rooted in core Six Sigma methodologies.

Honeywell Specialty Materials, based in Morristown, NJ, is a global leader in providing customers with high-performance specialty materials, including fluorocarbons, specialty films and additives, advanced fibers and composites, customized research chemicals, and electronic materials and chemicals.

NanoForum 2005 to Explore New Markets, New Opportunities

SEMI® announced that NanoForum® 2005, an international conference for leaders in nanotechnology and the semiconductor industry to explore commercialization of nanotech applications, will be Oct. 5-6 at the Marriott, San Jose, Calif. NanoForum is the only global nanotech conference that leverages the technical and manufacturing expertise of semiconductor equipment, materials and service suppliers.

Building on the success of last fall's inaugural NanoForum in Austin, Texas, NanoForum 2005 will explore expanding opportunities for nanotechnology in 10 major markets, as well as the latest technological developments for producing nano devices. Markets to be addressed include medical, biotechnology, automotive, consumer, energy, industrial controls, defense, aerospace, information technology and telecommunications. Technology topics include materials, metrology, deposition, surface conditioning, etch, implant, planarization, diffusion and annealing.

For more information about NanoForum 2005 or to enlist as a corporate sponsor, call Terry Berke at SEMI, 512-241-4070.

SEMI Expo CIS Gathers Scientific and Business Experts from the Semiconductor Community

BRUSSELS, MOSCOW – The 12th annual SEMI Expo CIS will be held in Moscow on 26-28 September. Equipment and materials suppliers, semi-conductor manufacturers and representatives of downstream segments will meet at the National Moscow Hotel and the New Manege Exhibition Hall for the three day event, which includes the Industry Strategy Symposium (ISS Moscow) on 26 September, the Market Conference on 27 September, a conference dedicated to MEMS/MST on 28 September, a table-top exhibition and the Technical Symposium on 27-28 September.

For the first time this year, SEMI Expo CIS will host a one-day conference dedicated to MEMS. The MEMS/MST Conference will cover MEMS market status and trends, MEMS development in Russia, design and equipment for MEMS manufacturing, applications and commercialization. Presentations will include EU Commission programs with regards to MEMS, the role of universities in the development of the MEMS/MST in Russia, and in the field of applications, the development of MEMS or MST for several industry segments, such as the biomedical industry and the automobile industry.

Now in its second edition in Russia, the Industry Strategy Symposium (ISS Moscow) will address four major themes in semiconductor manufacturing processes: innovation, manufacturing, applications and fabless.

The Market Conference will provide an industry update and address the core theme of "How to do business in Russia".

Semiconductor Process Technologies, Photovoltaic, Power Electronics, AEC/APC and FPD will be the main topics at the Technical Symposium, together with a review of the latest developments in SEMI Standards.

The Technical Symposium will be held at the New Manege together with the product exhibition. The exhibition serves as a communication platform for local and worldwide companies doing business in the semiconductor industry and related fields.

An optional tour to St. Petersburg from 29 September until 1 October will include a visit to the IT and MST Centres at the St. Petersburg Electro Technical University.

For registration and further information, please visit the SEMI website at www.semi.org or contact SEMI offices in Moscow at 7.095.931.96.47 or in Brussels at 32.2.289.64.98.

SEMICON West 2005 Highlights Innovations for Manufacturing in New Emerging Technologies Hall

SAN JOSE, CA – Innovation will be on display July 12-14 at SEMICON West 2005 when the Moscone Esplanade is transformed into The Emerging Technologies Hall (ETH), an exciting new expo destination that integrates leading-edge technology exhibits and compelling jury-selected technical presentations.

The ETH showcases advances in semiconductor, nanotechnology, MEMS/Microsystems, Electronic Design Automation (EDA) and e-manufacturing technology. It is also the venue for the Technical Innovation Showcase, a platform for 23-jury selected companies to present unique emerging solutions with the potential to address critical challenges in semiconductor manufacturing.

The ETH reception, sponsored by Microsoft, on Tuesday July 12 from 5:30-7:30 p.m. will bring together technologists from across the industry to network and discuss the exciting innovations.

ETH exhibitors range from start up companies trying to break into the semiconductor manufacturing industry leveraging nanotechnology to well-established leading companies that are extending their reach into new markets. For example Lam Research will present products for MEMS/Microsystems manufacturing and Microsoft, a first-time SEMICON West exhibitor, and its partners will debut e-manufacturing technologies, including advanced equipment process control, remote diagnostics, and in-factory diagnostics to increase fab productivity and reduce fab costs.

MEMS exhibitors will show silicon based MEMS manufacturing technologies and companies in the nanotechnology area will spotlight nano materials, metrology and nano imprint lithography innovations.

SEMI has teamed with Silicon integration Initiative (SI2) to highlight electronic design automation (EDA) and design for manufacturing (DFM) technologies. These technologies are critical in bridging the device design and device production communities for both IDM and foundry markets.

More information about SEMICON West is available at www.semi.org/semiconwest.

CORWIL Technology Corporation Adds 12 inch Wafer Dicing Capability

CORWIL high volume dicing services now addresses 300mm wafer diameter market

MILPITAS, CA – CORWIL Technology Corporation, the leading U.S. based provider of contract integrated circuit (IC) assembly services, has announced the addition of 12 inch (300 mm) wafer diameter dicing capability. CORWIL added the equipment necessary to saw the latest technology wafers in December 2004 to become the first U.S. based subcontractor with the 300 mm capa-

North American Semiconductor Equipment Industry Posts April 2005 Book-To-Bill Ratio of 0.80

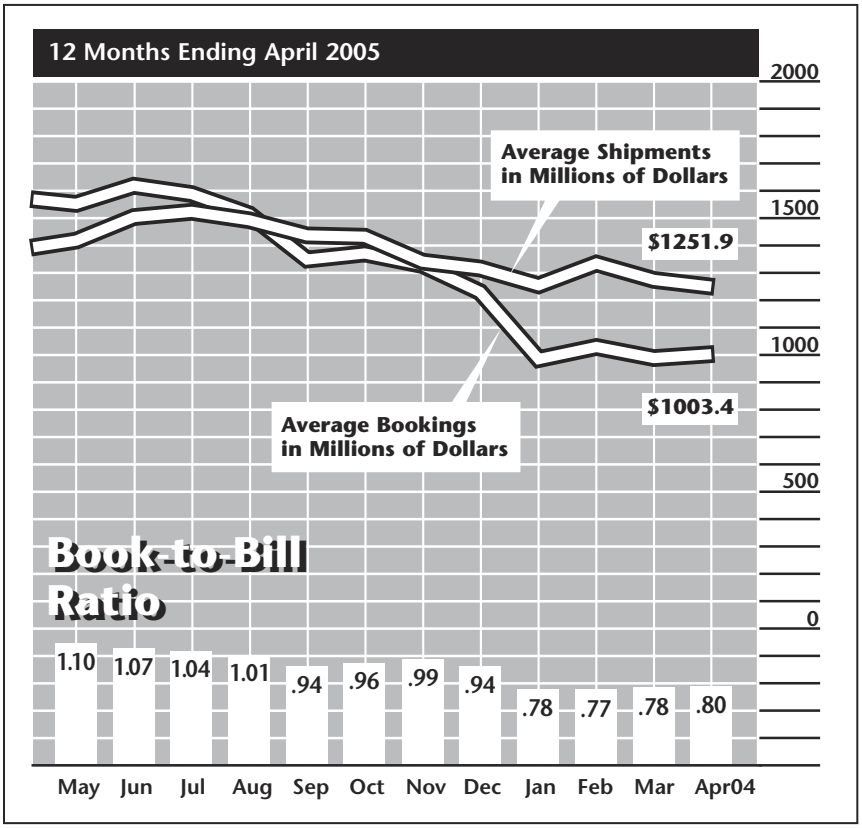
SAN JOSE, CA – North American-based manufacturers of semiconductor equipment posted $1.00 billion in orders in April 2005 (three-month average basis) and a book-to-bill ratio of 0.80 according to the April 2005 Book-to-Bill Report published today by SEMI. A book-to-bill of 0.80 means that $80 worth of orders were received for every $100 of product billed for the month.

The three-month average of worldwide bookings in April 2005 was $1.00 billion. The bookings figure is 1.5 percent above the revised March 2005 level of $988.4 million and 37 percent below the $1.58 billion in orders posted in April 2004.

The three-month average of worldwide billings in April 2005 was $1.25 billion. The billings figure is 1.6 percent below the revised March 2005 level of $1.27 billion and ten percent below the April 2004 billings level of $1.39 billion.

"A minor decrease in billings and a commensurate increase in bookings slightly raises the book-to-bill ratio," said Stanley T. Myers, president and CEO of SEMI. "However, we are in a stasis period, where we have yet to see a significant change in business for North American based providers of new semiconductor manufacturing equipment."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



Data compiled for SEMI by the independent financial services firm of David Powell, Inc.

bility. Both bumped and non-bumped wafers are being processed in CORWIL's new fully automatic, dual spindle, Disco system. The 12 inch wafer dicing capability is integrated into CORWIL's high volume wafer dicing, pick-and-place and die inspection services, state-of-the art wirebond and flip-chip IC assembly services, and wafer thinning and polishing services.

The new 12 inch wafer dicing equipment is integrated into CORWIL's modern new facilities in Milpitas, California. CORWIL has been one of the leaders in wafer dicing and IC assembly since 1990 and provides services to hundreds of semiconductor companies. CORWIL's full assortment of IC assembly services includes quick-turn prototype and production volumes of ball grid array (BGA) substrates, all ceramic packages, molded plastic packages including QFN/MLF assembly as well as flip chip, Chip-On-Board (COB), Multi-Chip-Module (MCM) and RF Module assembly. CORWIL has been ISO9001:2000 registered for nearly a decade and is QML certified (Qualified Manufacturers List) by the U.S. government agency responsible for aerospace and defense purchases of semiconductors.

Corporate headquarters are located at 1635 McCarthy Boulevard, Milpitas, California 95035; web site: www.corwil.com.

Twenty New Fabs to be Built in China by 2008 Says SEMI Report

New market research study details china semiconductor, equipment and materials trends and forecasts

SAN JOSE, CA – In 2004, new semiconductor equipment sales in mainland China reached US$2.73 billion; used/refurbished equipment sales are estimated at US$180 million; fab materials sales totaled US$391 million; and the packaging materials market reached US$781 million, according to the China Capital Equipment and Electronic Materials Market Outlook, a comprehensive new market research report that is now available from SEMI.

China's semiconductor manufacturing is a relatively small share of the world total, but the number of new fabs and packaging plants are increasing relative to other market regions. The report indicates that twenty new fabs are expected to be built in China between 2005 and 2008, with many of the projects to be equipped with used and refurbished equipment.

Furthermore, the number of silicon wafers consumed in China increased dramatically, while the first 300 mm fab began pilot production in 2004.

The 115-page report provides more than 70 tables, numerous figures and extensive commentary based on 130 in-depth interviews conducted with both domestic and international companies, including semiconductor manufacturers, foundries, packaging subcontractors, equipment makers and materials suppliers.

The report identifies important semiconductor market trends and forecasts for the markets in China for equipment, fab materials, packaging materials, indirect materials.

The report is available for purchase from SEMI for $3,000 (SEMI members/single user), and $4,000 (non-members/single user). A company-wide site license is available for $7,500 for SEMI corporate member companies and $10,000 for non-members.

For more information or to order the report, call SEMI Global Sales and Services at 1-877-746-7788 (U.S. toll-free) or 1-408-943-6901. ◆

Profound Material Technology Co. Ltd.

Profound Headquarters

Profound Material Technology Co. Ltd. is located in the southern part of Taiwan in the city of Kaohsiung. Profound's factory is ISO9001:2000, QS9000 and ISO14001 certified. With the advantages of its consistent product quality and quick lead-time, Profound has become a qualified solder ball supplier to numerous world-leading assembly houses, IDM, IC test/design houses and rework companies. Profound has sales representatives throughout Asia, US and Europe, which allows them to deliver quality services globally.

Products

Currently Profound Material offers the following products:

- Solder balls Eutectic & Lead Free
- Patented compact BGA/CSP/Wafer ball attach systems
- Machinery spare parts
- Bar solder
- Water soluble flux

Solder Spheres

Since establishment, Profound has taken an aggressive approach to address the common problems with solder ball quality such as rough surface, dark ball (caused by oxidation due to its metallic characteristics), diameter/sphericity accuracy, mixed ball sizes, etc. Take oxidation for example; to tackle this issue Profound developed a proprietary smelting and forming technology which extends the ball's resistance to oxidation without any side effects to its overall performance before and after reflow. Diameter/sphericity accuracy is one of the big concerns to customers, so in addition to improving it's forming technology early last year they introduced the 3rd generation sieving management system which can eliminate out of specification spheres to a significant level, compared with their competitors.

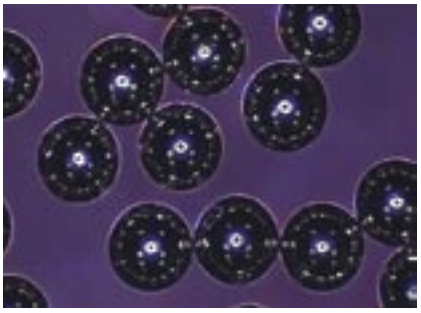
All out-going shipments must also pass an internal shake test where samples are randomly selected and poured into a shaking tube for three minutes of continuous vibration. Only when the result shows acceptable brightness data are they released for shipment.

Profound offers a wide range of solder ball alloys in order to meet customer's one-stop shopping demand:

1. Leaded alloys: Commonly requested Eutectic Sn63/Pb37 and Sn62/Pb36/Ag2.
2. Lead-free: Profound has the appropriate licenses in place to manufacture and ship SAC305 (Sn96.5/Ag3/Cu0.5), SAC405 (Sn95.5/Ag4/Cu0.5), Sn95.5/Ag3.8/Cu0.7, Sn96.5/Ag3.5 and many others to the worldwide market.
3. High-lead: Profound provides high-lead solder balls such as Sn10/Pb90
4. Special alloys: Profound accepts special requests for making specific solder ball alloys like Sn63/Pb34.5/Ag2/Sb0.5/Ni0.01, etc.
5. Diameters: Profound manufactures solder balls from 0.2 through 0.89 diameters and is a specialist in manufacturing small diameter balls from 0.1mm to 0.4mm solder balls.

All solder balls are packaged in ESD containers and filled with inert Nitrogen to keep out moisture and prevent oxidation.

The transition from lead to lead-free materials brings new challenges due to the higher melting point characteristics. Profound began working with their major customers early on to make sure that the move to lead free was a smooth transition. At this time most of its customers have already completed the qualification process of the Profound lead free balls.



Good solder balls show a smooth and shiny surface.

Shaking Test Device

Profound's Solder Ball ESD Containers

Production Facility

"Manufacturing solder balls is a highly competitive business hence having stable product quality, an efficient production facility, effective logistics management with good customer satisfaction is key to our success" Chihmin Chou, Profound's Associate Vice President said. During the last two years, there have been a lot of new suppliers entering the market, with some offering very low prices in order to capture market share. Although solder balls are a critical part of the BGA/CSP packages and can impact the whole package's lifespan, it's very low percentage cost of the package makes it impossible to justify price vs. quality as a trade-off.

Production Facility Follows Green Wave

Profound's soldering materials are produced and packaged in a 10k class clean room. Because management cares about the potential toxic dangers that can be harmful to front line operators, all toxic materials and liquids were banned at all production workstations beginning in the 2nd half of 2003.

"Our production lines are highly automated and not labor intensive. However, experiences are really important. Nevertheless we are very concerned about the health care of those who have high chances to be exposed to dangers in there job performance" said Chou.

Think Tank Alliance

Concerning the costs and limitations when developments are 100% done in-house, Profound has signed a cooperation program with a local prestigious university research lab in which both parties will co-develop alternative lead free alloys and soldering materials as well as pursuing a more advanced production technology. "It's absolutely a great investment because now we have very outstanding academic research staff and world class lab equipment to help substantiate our ideas before putting them into mass production" said Chou.

Water Soluble Flux and Bar Solder

To provide the best combination of soldering materials and also to fully utilize its worldwide sales channels and expand its revenue stream, last year Profound released its water soluble flux and bar solder product lines. Formulated by using a unique chemistry for superior solder joints, the flux also features non-corrosive, non-conductive and is non-reactive with other fluxes with minimal moisture absorption. Its bar solder is available in various alloys.

Patented Compact BGA Ball Attach Systems

Profound has recently introduced its compact BGA/CSP ball attach systems. These ball attach systems are quite different than the commonly available ones mainly due to its small size and flexibility. Some of its key features are.

- Compact size: Its BU570 system is 75cm X 25cm X 30cm and weighs 38KG
- Easy change over
- Easy to use
- Easy to maintain

Because of the compact size and flexibility of its systems, Profound has been able to target the rework and SMT markets which have lower volumes, but a larger variety of packages. Another strong point besides the physical size is its reasonable price structure. These systems are patented in the US, Japan, China and Taiwan.

"Based upon our initial survey we found that compact-sized ball attach systems are rarely found in either the US or European markets," Chou said, "so we are seeing a lot of interest in these systems since their introduction."

BU570 Ball Attach System

Desoldering Air Knife

Compact Reflow system

Ball Attach Related Products

Profound provides related products for ball attach, including desoldering air knife, PCB chip mounter and BGA/CSP reflow systems. These products are designed for small to medium volume producers and offer maximum flexibility and are cost effective.

"The sales of our solder ball business keeps hitting record highs, plus with the introduction of the new Ball Attach Systems, Water Soluble Flux and Bar Solder product lines, we are definitely on a rapid growing path. We predict BGA packaging still has at least 10 years of lifetime growth" Chou summarized.

For more information, please contact North America agent Cumulative Technologies at 408-969-9918 or email, hal@cusjca.com.

Visit Profound material's web site at, www.profound-material.com.tw. ◆

Profound's University Partner

Bar Solder

3D IC Packaging and Interconnection Technologies – Pathways to Performance

Joseph Fjelstad
SiliconPipe, Inc.

In the hierarchy of electronic interconnections, the IC package is the first gatekeeper of electronic system performance. With the relentless doubling of transistors every 18-24 months in accordance with Moore's Law, packaging technology has been pushed to its very limits and, in fact, has often become more an impediment to rather than an enabler of IC chip performance. The responsibility for this clogging of electronic "arteries" is multifaceted just as is the case in the human physiology. Some of it is due to heredity and genetics (design approach) and some is due to diet and exercise (materials and interconnection methods). Fortunately, electronic packaging, unlike human physiology, can be changed with much greater ease but it still requires adherence to good practices. Today, cost and performance are the primary watch words of IC packaging and, while reliability is still important, the concept of "application specific reliability" which has infiltrated certain facets of product development mindset for IC packaging, has robbed the IC package of one of its more noble ancestral attributes in order to keep pace with the apparently more important demand for lower cost. However, if one reconsiders, IC packaging design and manufacture, there exists possibility to create IC packages that sacrifice nothing in terms of performance and reliability while staying on course relative to cost targets. Simplicity is the very heart of this seemingly impossible task.

This article briefly reviews the IC packaging technology challenge from its beginnings to today and then describes some of the novel ways in which IC packages are continuing to evolve to meet the cost, performance and reliability needs of today's and tomorrow's electronic products.

Background

Over the years, the development of IC packaging technology has largely paced the development of the IC but even so, its evolution has been marked by significant differences in thought and approach from the very beginning, starting with simultaneous development of the integrated circuit by Fairchild and Texas Instruments in the early 1960s. Each company chose, from the onset, different packaging technologies for their respective products. Fairchild's first IC products were packaged in the familiar TO can format using an 8 lead configuration, while TI introduced both its IC and a new packaging format called the "flatpack"[i] which was also arguably the first surface mount package as well. Except for a period of relative stability during the era of the through hole mounted device and the iconic dual-inline-package or DIP, there has since been an explosion in IC packaging options to address the growing complexity of ICs and cost sensitivity of customers.

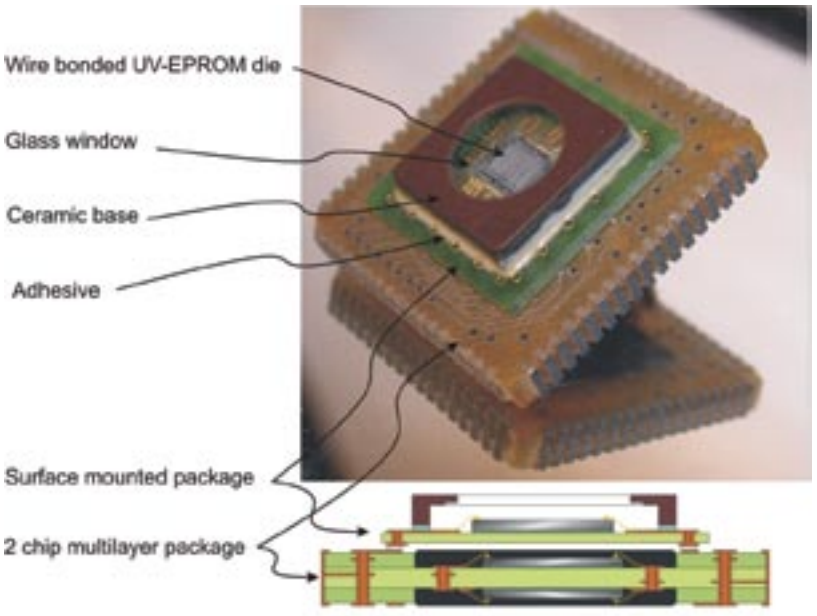


Figure 1. Example of a 1985 vintage organic laminate package with elements of stacked chip and stacked package technology as well as double sided assembly.

There have been several packaging technology eras since the halcyon days of the DIP all of them developed with the same cost and performance objectives in the face of increasing complexity. For example, surface mount technology in the late 1970's marked the beginning of "smaller, faster, cheaper" movement. Then when increases in I/O exceeded the practical assembly capabilities and impacted the performance of peripherally leaded surface mounted leadframe package structures, area array packaging technology and the emblematic BGA entered into mass production in late 1980s. The demand for more mobile products in the 1990s quickly accelerated miniaturization of IC packages for certain ICs such as memory down to the level of the chip itself and CSPs rapidly rose into prominence. At the same time, with the explosion in transistor count on high end CPU chips, the BGA became much more complex and soon required hundreds to thousands of I/O.

Entering the Second Millennium and the Third Dimension

The new millennium ushered in a new era of multi chip packages, reminiscent of the MCM of the early 1990s but with some new twists and due to maturity in process technology, significantly lower cost. In addition, stacked packaging which had been relegated to specialty, often military, products earlier, surged in popularity among designers needing to increase functionality in a small space. These latter generation IC packages are a vital new part of the electronic interconnection family and there use is expected to see continued growth. A review of some of these creative options should help illuminate both their present and future value.

Actually, the concept of the multi chip package is not new. Hybrid circuit technology from it inception was largely predicated on the interconnection of multiple small ICs and passive components in a ceramic package. Even the use of organic laminates to create multi chip packages also has early

roots. Figure 1 shows photos of a multi chip package developed in 1985. As can be seen the device has analogous elements of both stacked ICs and stacked IC packages. Often, such structures were simply place holders until an application specific IC could be created. Moreover, because of a lack of known good die (KGD), die yield was not always predictable and assembly processes were also less than perfect.

Today's version of multi chip packaging has been re-titled variously as system in package (SiP), system level integration and miniaturization (SLIM) and as volumetric system miniaturization and interconnection (VSMI). Regardless of term used, the objectives are fundamentally the same: increase performance and lower cost without sacrificing yield or reliability. It is not and easy challenge. Managing multiple suppliers and mixing technologies places significant stress on the assembly infrastructure but the benefits frequently outweigh the drawbacks. This condition has brought to the table another alternative contender, the system on a chip (SOC), which some espouse as the ultimate solution. It is not clear that there will be a clear winner as the arguments which can be made for all solutions can be most persuasive depending on the challenge faced. And with evolution, the new challenges continue to appear.

Even with all of the innovations of the past, there is always room for improvement relative to the current state of the art. Innovation tends often to be draw into and then from the vacuum created by new challenges that did not previously exist. Presently the realm of gigahertz data rate interconnections and communications between IC chips is one such area.

The Challenge of High Speed Interconnections

Simplicity, in thought, in design and even in life itself, is a concept that has echoed throughout history from the ancient Greeks to modern times. Einstein admonished us that: "Things should be made as simple as possible but not simpler". So it is also that simplicity, when properly executed and applied to IC packaging, will yield the commonly sought objectives of higher speed, lower cost and greater reliability. It will also yield those objectives with greater facility. But is it truly possible?

A new IC packaging concept has been recently introduced, targeted to significantly simplify the design and manufacturing process, while simultaneously offering the potential for much improved electronic performance. The concept builds on a idea first employed for improving the density of wire bonded IC packages such as pin grid arrays (PGA) in the mid 1980s. This technique is generally referred to as a tiered wire bond pad IC package structure. (See Figure 2) The method successfully addressed I/O density problems in applications where on chip pad pitch density exceeded the feature size limitation and routing capability of standard IC packaging technology. In contrast the new proprietary, patent pending packaging technology[ii] takes the earlier tiered contact concept further extending it to the I/O terminations on the package surface. The result is a stair stepped or "wedding cake" like IC package structure. (See Figure 3)

The advantages of the simplified method are significant in all of the prescribed areas including, cost, performance and reliability. A point based evaluation of the concept relative to such commonly applied metrics relative to IC packaging will make clearer the benefits of the new approach.

Looking first to cost, it is noted that cost is reduced because of the reduction in the number of manufacturing steps and especially the elimination of plated vias. This follows earlier work in the creation of the "off the top" OTT™ package, which was designed for direct interconnection between one or more IC using the top surface of the IC package to bypass and obviate the need for plated vias in critical path signals.[iii] The simple structural elements of the package also allow for improved manufacturing yields. Electrical testing cost should also be greatly reduced, if not eliminated, because the circuits are only on one side (though a ground layer may be provided on the second side of each layer if desired) and they can thus be easily examined visually for shorts and opens and non-uniformities which could affect electrical performance. Moreover, because each layer only has as much material as is required for the circuitry used, there is less waste, especially in volume manufacture. Qualified materials and equipment to accomplish assembly exist today and can be used with little, if any, modification. Finally, an added advantage is available in that individual layers can be inventoried for creating custom packages, including mixed pitch I/O if desired, on a moments notice.

Turning to performance, one finds that the same plated vias which add cost and consume routing space can also be an impediment to electrical performance. By eliminating plated vias from the package, signal performance is significantly improved. In fact, complex field solver analysis, more frequently now required for characterizing critical signals as they pass through the package, is not needed. Moreover, differential pairs, common to most of today's high speed circuit designs, can be designed such that they have virtually zero skew and so that cross talk can be almost completely eliminated. If this were not enough benefit, the clarity of the signal channel has yet another benefit that is not commonly recognized and that is power savings. A clear channel means that much lower voltages are required for reliable signal transmission. For example, in one application of an embodiment of this general type of package, which was designed to demonstrate that capability of direct and via less signal transmission, the total power required was *less than two percent* of the anticipated requirement.[iv] Finally, because of the versatility of the method, substrates of differing material types can be used when and where required so higher cost materials that are often desirable of high speed signals can be used sparingly and mixing of I/O pitch on a package is also possible. (see Figure 4) This approach also opens up routing channel opportunities to internal I/O terminations.

Reliability is the last item on the list. Once more, obviating the need for plated vias, which are often the "Achilles Heel" of interconnections, will help to improve overall package reliability. Presently under study, but not yet proven, is the expectation that the periphery I/O of the package having longer

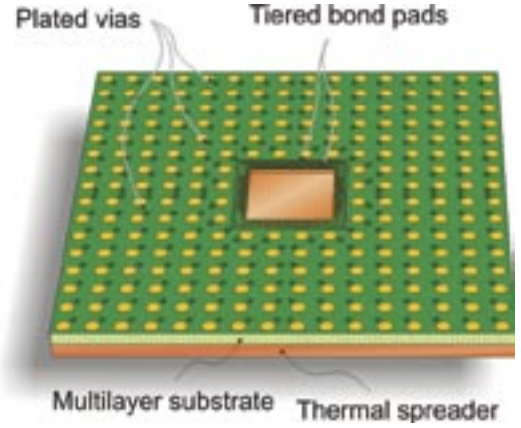


Figure 2. Standard approaches to IC packaging require plated vias which are subject to reliability concerns, add processing cost and negatively impact performance.

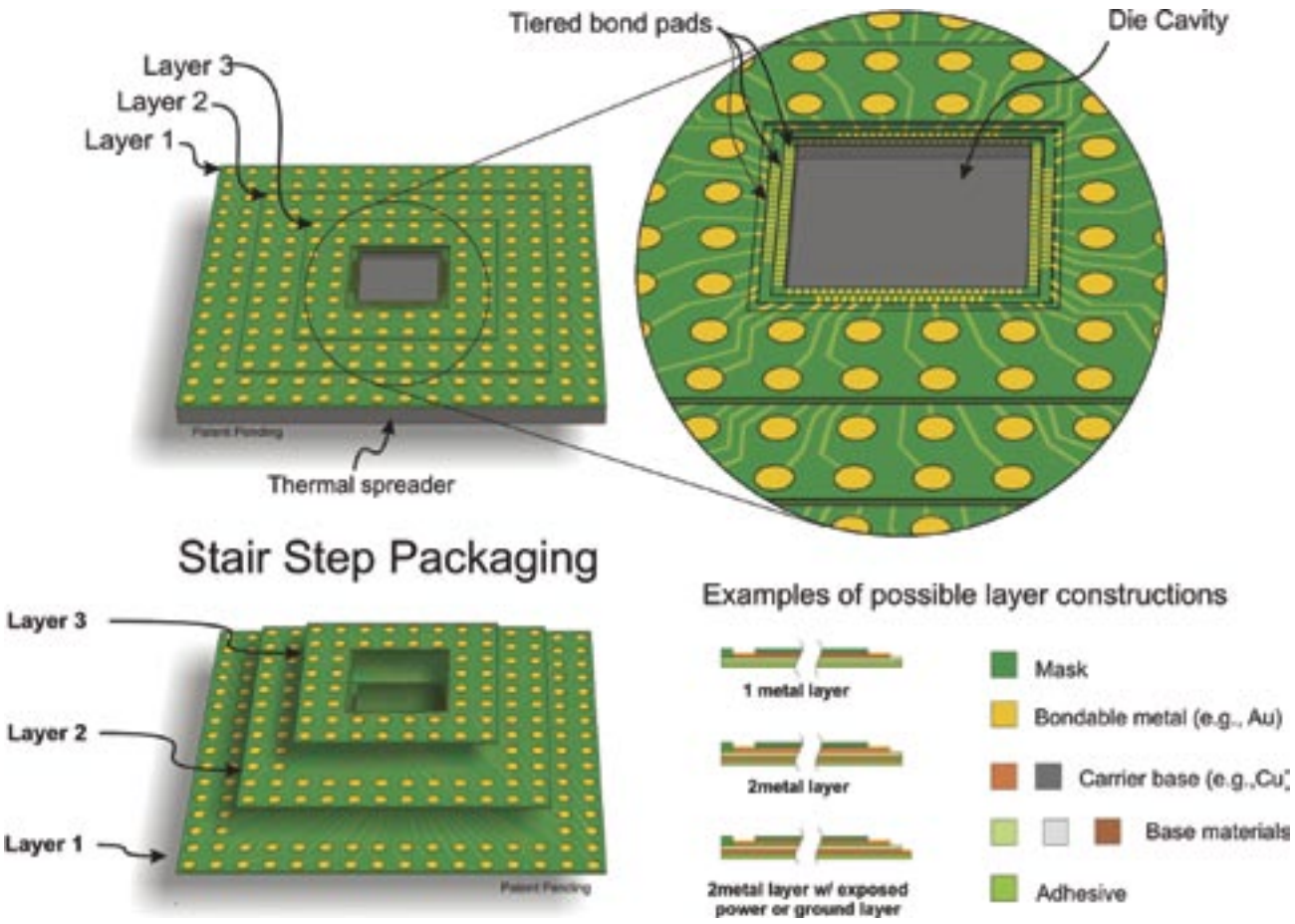


Figure 3. By reconsidering design and assembly the IC package structure is considerably simpler and can be constructed using inventoried layers if desired.

reach when making connections to the board will elongate, creating column-like terminations. Solder joints elongation has been identified as a condition that appears to provide improved solder joint reliability in some studies.[v],[vi]. If concerns remain about assembly, because of the differing ball heights, ball height can be made uniform by simple using course pitches on outer (periphery) I/O rings. (see again Figure 4)

In summary, in all important aspects of package design, cost, performance and reliability, the benefits flow from simplicity. As the 13th century philosopher monk, William of Occam observed, "It is vanity to do with more that which can be done with less". Simplicity is inevitably the key. It is believed that, when simplicity is properly applied, the features of high performance, low cost and high reliability, which are often viewed a mutually exclusive set of conditions in IC packaging design, can instead be intrinsically linked. By reconsidering the design and manufacture of IC packaging, all potential benefits can be reaped simultaneously. ◆

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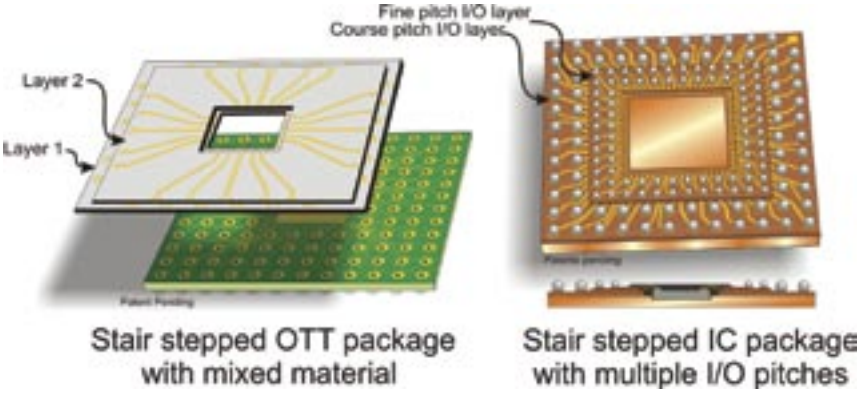

Figure 4. Stair stepped IC packaging provides options that are not common to most traditional approaches to package design including "off the top" (OTT)[iii] and use of dissimilar materials (left) as well as mixed I/O pitches on the same package (right). Moreover, the structures themselves are highly amenable to stacking of die within the package.

Navigating E142: SEMI's Specification for Substrate Mapping

Jim Davis, Sales Manager, Kinesys Software, Inc. and Jerry Secrest, President, Secrest Research

Figure 1. A Stacked Die package requires 3D placement information for all components.

SEMI has recently published a new standard, E142 - Specification For Substrate Mapping. This standard was spearheaded by Kinesys Software, a supplier of Substrate Map data management and utilization and Device tracking software. Other contributors include Intel, Freescale Semiconductor, Infineon Technologies, Philips Semiconductors, ST Microelectronics and TSMC. The push came for E142, because the industry was moving towards more complex packaging and there were separate maps for metrology, sort, strips, trays and PC boards with conflicting or incomplete Standards, and In-House developed solutions.

E142 provides or enables:

1) A solid Inkless Assembly standard: Unifies G81, G84, G85. Based on an XML Schema… well defined structure and content, but extensible.
2) A method to address complex advanced Assembly requirements: Multi-Product Wafers, Stacked Die Packages, Multi-Die Packages. Has multiple Substrate types: Wafers, Frames, Strips, and Trays. Has multiple Data types: Bin Codes, Device ID's, and Transfers.
3) Device traceability. The data structure supports actual Forwards / Backwards Device traceability.

E142 helps the semiconductor industry with manufacturing stacked die packages, placement of passive components on packages, mapping assembly strips, probing multi-product wafers, and probing WLP. In addition, E142 can be used as a general map in semiconductor Fab, Assembly, and Test. For example, a die in a stacked package in a tray can be related to its position in a reticle shot on a wafer by implementing E142 at specific manufacturing steps. Another use can be PC board assembly.

This article will describe some applications that utilize Mapping and the associated data structure defined in E142, the contents of the standard, and how one can get started using this new standard.

SOME E142 APPLICATIONS

Assembling Stacked Die Packages

The map structure in E142 can contain all the information needed to place die and passive components into a stacked die package. (See Figure 1.) This means that once the map in E142 is set up for a stacked or multi-die package, the same map can be used on all the equipment placing components into the package.

The stacked die can have different placement coordinates. For example, the first die down can be on a 10 mm pitch of the assembly strip. Next, two dies can be placed side by side on top the first die.

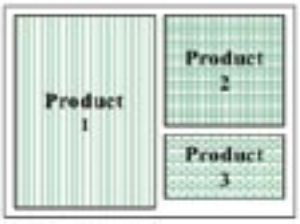

Figure 2. Three-product reticle field.

Die Sorting Multi-product Wafers

Multi-product wafers are used to significantly reduce the initial cost and time of fabricating a new or low-volume product. A few products with different die size may be placed in one reticle field, and this is done for the entire reticle mask set. (See Figure 2.) E142 has the capability of mapping these different products such that when the wafers get to die sort the Prober/Tester knows how to test each Product.

Temporary Wafer ID

Most wafers are thinned after test prior to going into dicing. One of the problems in this procedure is the loss of the wafer ID mark on the back of the wafer. E142 has the capability of containing an alias to a substrate (wafer) ID and then tracking that wafer via its position in the cassette until a new ID can be hard coded into the wafer. Also, the alias can stay with the wafer through die attach.

Improving WLP Probing

Bumping wafers is used to make Wafer-Level-Packages. The bumped wafer needs to be probed at wafer sort. There will be some variation in bump height across the wafer due to process shift. Without bump height information the prober will typically have different amounts of over drive in the Z dimension across the wafer. Too much overdrive damages the probes. Too little overdrive results in poor contact, reducing test yield. A solution to this problem is to use E142 as the mapping software at bump inspection. The inspection data containing bump variation height in a bin code format, Z coordinate, can be transferred to the prober using E142 to adjust the Z direction overdrive in different areas of the wafer. The plus: Avoid unplanned Prober/Tester downtime due to a probe crash.

E142 Factory Overview

A typical E142 factory hook-up is shown in Figure 3. A map server is commercially available. It is used to download maps to equipment and accept new or revised maps uploaded from the equipment. The server

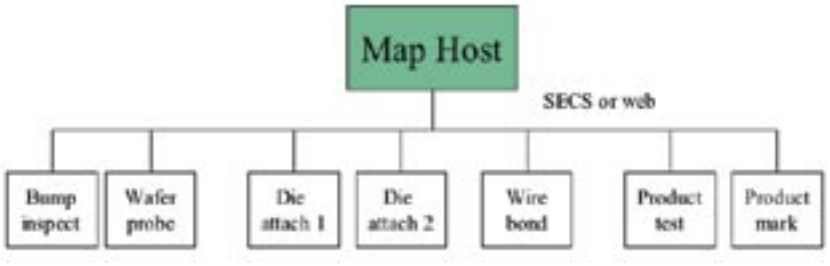

Figure 3. One possible factory map system configuration for stacked die packaging.

also keeps an archive of maps for diagnostic and device traceability purposes.

E142 and Equipment

The equipment manufacturer can download and upload E142 maps over a SECS/GEM interface using existing messages. This is defined in the E142.2 (4067) proposal expected to be approved in July 2005. Parsing the maps into and out of E142 format is relatively straight forward as most software development tools today contain extensive support for XML Schemas.

The more difficult task that equipment manufacturers will face is upgrading their control systems to handle the newer features made possible by E142, e.g. multi-product wafers, reporting the transfer maps, etc.

A map cycle for a process step will look like the following:

1. The equipment will read the substrate ID and request a map from the host.
2. The host will send the map to the equipment.
3. The equipment will process the substrate and update the map.
4. The equipment will send the updated map to the host.

E 142 OUTLINE

The E142 document layout follows typical SEMI Standards. It starts out with Purpose, Scope and Terminology. The main portion of the standard is used to describe the required data in a map file. Object convention using UML notation, with an XML Schema to define structure and content. In order, the following information is provided by the standard:

1. Layout information
   a. XY dimensions
2. Substrate information
   a. Substrate Alias
3. Substrate map
   a. Type
   b. Orientation
   c. Side
4. Overlay Data
   a. Bin Codes
      i. Cell Status
      ii. Defect codes
   b. Device ID
   c. Transfer Data
5. Graphics for:
   a. Wafer Maps
   b. Strip Maps
   c. Tray Maps
6. Example files for the three map types above.

RELATED STANDARDS

SEMI Standards

E142 was approved in October 2004 and E142.1, the XML Schema, in March 2005. E142.2, SECS II Protocol and E142.3, Web Services, are expected to be approved in July 2005. E142.2 is needed for transfer of a substrate map between a Host system and the equipment via a SECS II formatted message, E142.3 Web services is needed to transfer substrate maps between factories.

SEMI and RosettaNet are working on enabling E142 map transfers via RosettaNet. In July 2005, they are officially meeting to implement this capability. This will be useful for Company-to-Company map data transfers, which will be integrated into their B2B processes.

Figure 4 shows the relationship between these standards.

(continued at right)

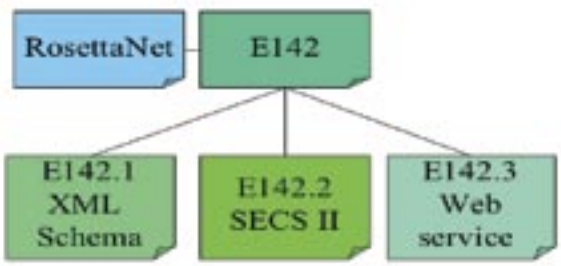

Figure 4. E142 Substrate Mapping and related standards.

HOW TO GET STARTED USING E142

Here are some possible initial steps:

1. Purchase a copy of the standard from SEMI through their website and study it. You may choose to implement it on your own.
2. Attend the SEMI E142 educational program at SEMICON West. Then figure out your approach.
3. Contact Kinesys Software, and ask for a presentation of their Substrate Map data management and utilization and Device Tracking software Solution, ALPS 3, which is E142 compliant.
4. Contact Jerry Secrest who can assist with an implementation plan.

For more information contact Jim Davis at jim.davis@kinesyssoftware.com or Jerry Secrest at secrest@ix.netcom.com. ◆

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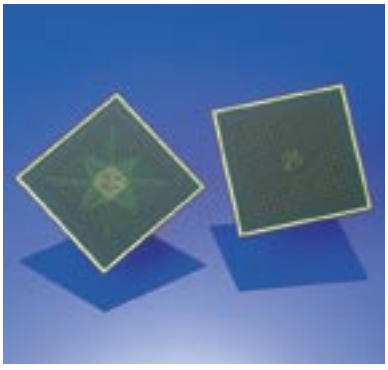

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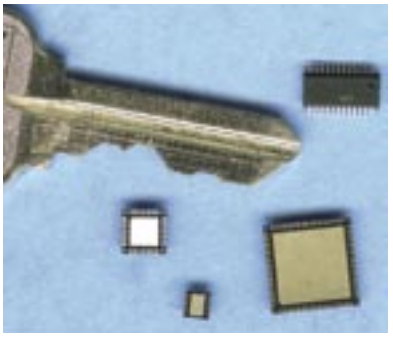

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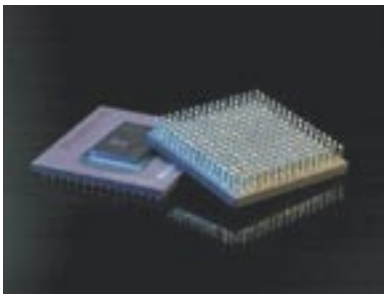

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The MEMS Packaging Problem; the MEMS Packaging Opportunity

Joseph Mallon
memvent

The "MEMS packaging problem" is a phrase that has been used repeatedly over a period of many years at conferences, in presentations and on panels offered to the MEMS community. Why does such a problem persist in the face of the extensive efforts of so many individuals to advance this technology?

MEMS Packaging Inherent Challenges

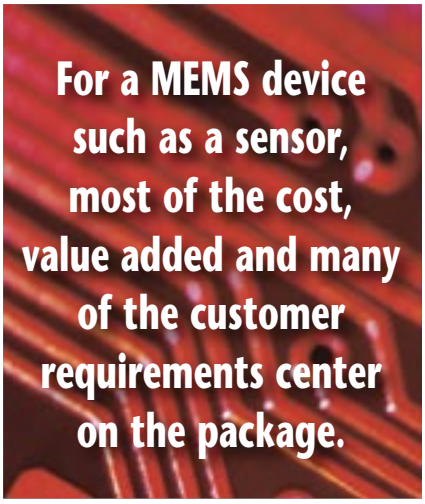
The MEMS designer must couple a selected mechanical input to the small silicon die while excluding the unwanted or destructive effects of all other mechanical variables. The designer cannot follow the conventional strategy of isolating the device by means of the primary and secondary packages. Immersed in the environment, MEMS devices often see levels of vibration, strain, humidity temperature, force and pressure only rarely encountered by mainstream semiconductor chips.

In a modern semiconductor industry practice, wafer manufacturing and the packaging have become increasingly standardized. Most of the value added is in the intellectual property embodied in the mask design, which is tailored for existing wafer process flows and designed to fit in industry standard packages. This model has been attempted in MEMS with limited success despite significant effort and government funding. The diversity of MEMS seems to resist such standardization.

Moreover, for a MEMS device such as a sensor, most of the cost, value added and many of the customer requirements center on the package. The fundament enabling technology is the MEMS die, it can provide significant user benefit and product differentiation, but only if packaged in a way that meets customer needs.

The focus of the effort in MEMS research and product development is at the die level. Each year sees satisfying advances in new and refined structures in everything from sensors, to cell sorters to atomic clocks. But many of these are demonstration devices. Their limitations are often limitations of the packages in which they are tested.

Much of this work is done in universities with government funding. In this setting, the researcher, typically a PhD candidate is far removed from the customer for whom the device is ultimately intended. Access to detailed customer needs, many of which are packaging-related, is limited and filtered. Packaging has not traditionally been viewed as good thesis material. While universities operate wafer fabs with professional staff, they typically do not sustain packaging facilities with a sufficient flow of devices processed to achieve critical mass, or continuity of processes and skills.



Such facilities and skills are available in industry, but packaging advances are seldom published, and the efforts are most often focused on the project at hand. So, MEMS packaging is not undertaken in a coordinated way to advance it as a field in the way that such attention has been given to MEMS chip level devices.

In other words, the "problem" is only in the smaller part fundamental; in the larger part, the issue is structural. The actions of funding sources and the structure of the university degree system favor wafer level development. The result has been an imbalance with a surfeit of technology available at device the level that cannot be commercialized without further development, especially packaging development.

But, there are tremendous opportunities here. Opportunity for those who fund such research to shift focus somewhat toward more support for MEMS packaging. Opportunities for researchers to have the pleasure of seeing their efforts result in commercial devices that are use in daily life. Opportunities for entrepreneurs to exploit the abundant wealth of technology that has been developed in the field waiting to be commercialized. Opportunities for those who work in semiconductor packaging to both apply their skills to a new field, and also to use elements of MEMS technology that can advance packaging technology for mainstream devices.

When imbalances exist, they eventually are resolved. The MEMS community should strive to make the resolution more packaging effort, not less device funding. The interest level and the skill sets certainly are there as attested to by the success and energy level at the recent one day MEPTEC conference on MEMS packaging. Let's hope that the next decade will see increased emphasis on packaging MEMS. This is needed if we are going to see the full benefits of the technology make its way into the market place. ◆

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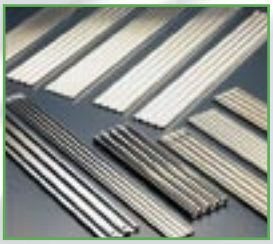
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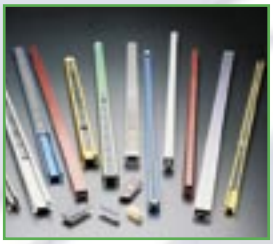
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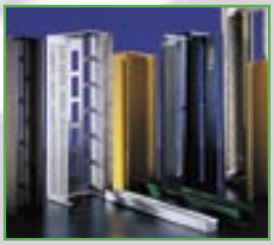
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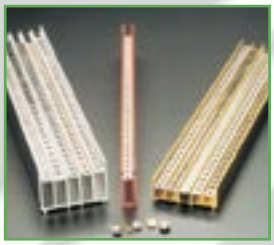
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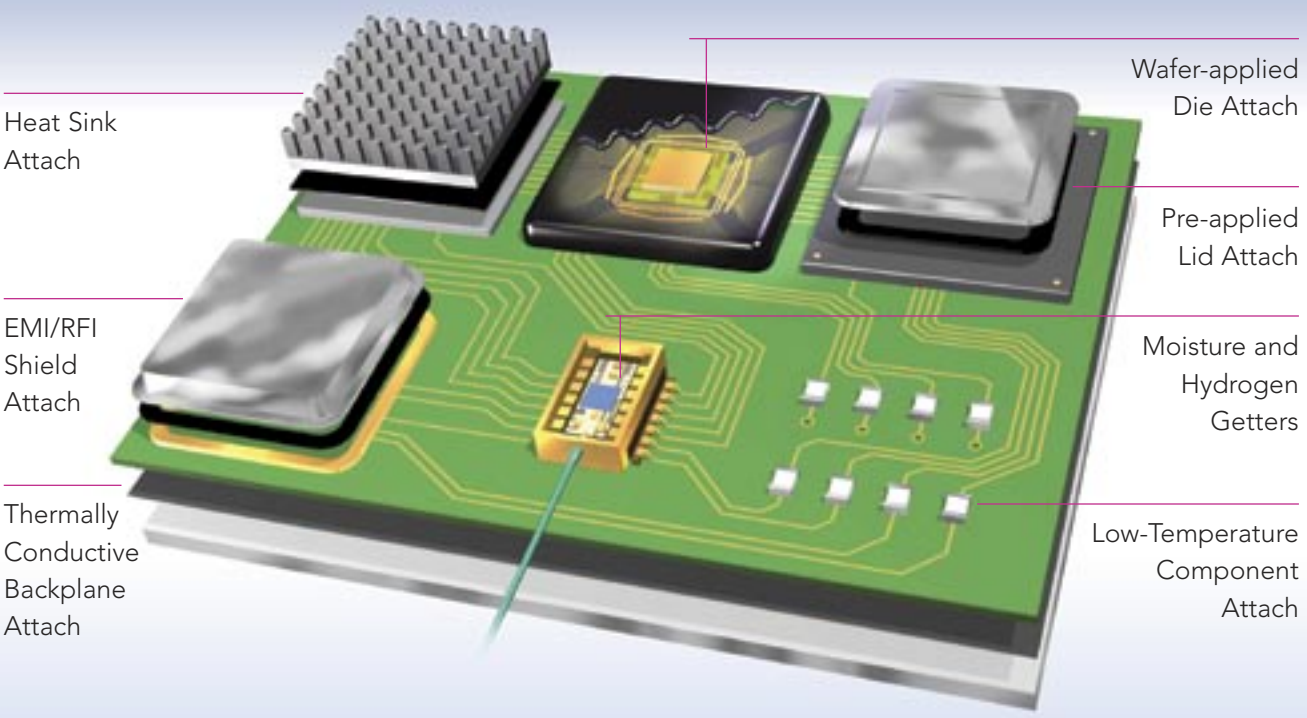

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