

# MEPTEC Report

SPRING 2014



A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 18, Number 1

TWELFTH ANNUAL MEPTEC

## MEMS TECHNOLOGY SYMPOSIUM

**ADVANCES IN MEMS -**

Foundations of Design, Process, Packaging, and Test

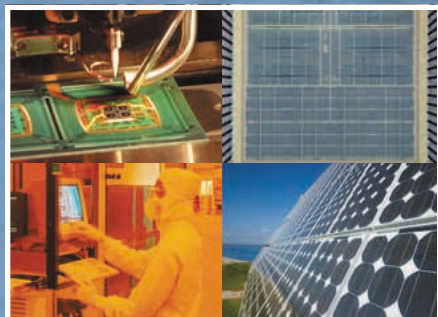
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**SPECIAL PREVIEW:**

**ALL THIS FUN, AND A PAYCHECK, TOO?**

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**MEPTEC MEMBER COMPANY PROFILE**

Founded in early 1996 in Bangkok, Thailand, and incorporated in the state of Texas, N-Able Group International serves a client base that spans North and South America, Asia and Europe.

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Industry Analysis: Substrate and Interconnect Material Trends in Packaging

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Is it Time to Reinforce In-Package Solder Joints Using CNFs?

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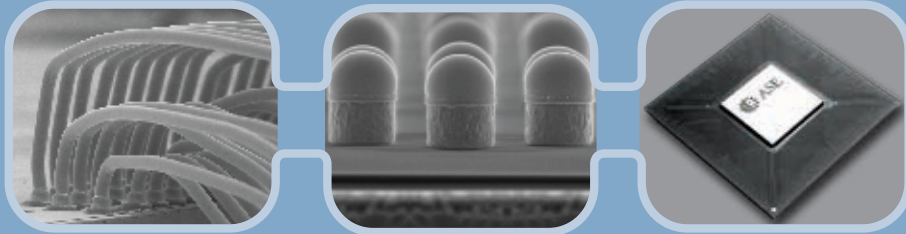
BCB is one of very few materials to have a significant impact on the microelectronics industry.

30

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# Silicon's Rapid Scaling and Packaging Technology Roadmap

*John Xie, Director, Packaging Technology R&D  
Altera Corporation*

PEOPLE HAVE BEEN TALKING ABOUT the slowdown of Moore's law. Yet in 2014 alone the industry can see wide range, multiple generation platforms of leading-edge silicon nodes in action at the same time. The 32nm/28nm/22nm is ramping to high volume demand; the 20nm is also starting customer shipment with strong momentum; 16nm and 14nm silicon tape out will occur; and 10nm product planning at the customer end is already getting started.

Along with continued silicon scaling, packaging's role has evolved from the off-shelf operation solution provider in the past to the technology solution enabler role today. Further, it is being granted a new status as a key business solution enablement component and market differentiator. The demand on packaging technology solutions to provide product solutions comes from all fronts: the rapid increase of system bandwidth and memory integration is driving density scaling of circuitry and interconnect, high speed IO and channel density, the memory solution, the power management and heat dissipation solution, the form factor reduction, etc. Meanwhile, the scaling of the silicon is also benefiting smart phones, pads and other gadgets, which is also demanding small form factor packaging and ultralow cost packaging solution development. All these activities have made the packaging industry a very hot and active field.

Scaling from 28nm to 10nm, the bump pitch of a flip chip device, even with very large die like FPGA, is pushed down to 100-130 $\mu$ m range. The tight bump pitch is also prompting Cu bump implementation for better scaling capability, which has made it a ROHS6 compliance solution by default. The horizontal interconnect scaling is also phenomenal: The 20 $\mu$ m pitch circuitry (with sub-10 $\mu$ m line resolution) is rapidly moving to the main stream. Leading worldwide R&D teams are starting to target 5 $\mu$ m line resolution as the next technology development milestone. Another challenge is how to make smaller via, and there are techniques being

developed using nontraditional processes.

3DIC packaging technology is also making good progress, thanks to the increased bandwidth and density needs. 2.5D integration started limited production experience and multiple flow have been developed by both leading foundries and OSATs. Multiple foundries' entry into the interposer market has prices showing a strong downward trend. The native stacked die architecture concept and design approach could potentially reduce interconnect complexity, metal stack parasitic, and timing and power budgets. It could, in the meantime, achieve both cost reduction and manufacturing process yield improvement; it could also result in wider implementation of 2.5D in certain product portfolio. Lastly, high bandwidth memory development and heterogeneous integration are among the highest in future potential and has been the focus of both memory suppliers and semiconductor ODMs.

Low cost stacked die packaging is also a hot topic in the advanced die staking domain. The Face-Face stacking offers unique 3D style stacking with a very low cost premium, which can be applied to both flipchip and wire bond style packages. TSV-less 2.5D integration is also under development. Meanwhile, the ultra-high density organic interconnect and interface development (2.1D) is propelled by rapid advances of interconnect density by leading substrate and material players. The ultra-high density organic interconnect technology has started to point to a sub 2 $\mu$ m future. People have demonstrated an organic interposer enabled ASIC and multiple high density memory stacking with UIB2 interface (55 $\mu$ m  $\mu$ -bump pitch density). There are also demo units built using 2.1D integration concept using FPGA and memory.

On the ultralow cost packaging front, single layer, embedded trace substrate technology entered high volume production; UBM-free WLCSP are also being developed; improved lead-frames with higher IO efficiency have been in the market with

different formats. If Fan-Out WLCSP is considered not as cheap, applying it to multi-die stacking applications with high density silicon grade interconnects can be considered an ultra-low cost stacked die packaging solution with huge market potential, which is not too far from production phase.

For small form factor (SFF) packaging, in addition to various format of WLCSP and Fan-Out WLP, panel embedding and substrate-less FCCSP have created a new series of SFF packaging. Cu pillar BOT (bump-on-trace) has replaced some WB BGA application space down to 50 $\mu$ m pitch range. BGA ball pitch has been reduced to 400 $\mu$ m or even 350 $\mu$ m. High density lead-frames, hybrid lead-frames, paper thin packages, ultra short WB loop technology development, etc., have given customers a very wide range of cost effective small form factor package options meeting different application requirements. The challenges are how to apply effective strategies and innovation on Si-PKG co-design/co-development to drive down the total product cost while facing the increased transistor cost, interconnect density and product performance requirements.

As for ROHS compliance, while people are still waiting for news from the EU, the aggressive scaling of silicon technology has put Cu bump into emerging or even the main stream product application, which will achieve the new generation product ROHS compliance at initial release. For exiting product lines, we need to be prepared well and early for any EU potential decision in 2014. People are still trying to make choices between Cu bump and lead-free solder bump for existing product lines and we need to see clearer differentiations between each soon.

In conclusion, simply stated, with continued silicon scaling at a rapid pace, we will see the continued increase of transistor cost, with the R&D cost supporting each generation silicon development and each silicon design. Innovation on packaging and integration technology will be the future business enabler and market differentiator. ♦

# MEPTECReport

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## ON THE COVER



MEPTEC presents its Twelfth Annual MEMS Technology Symposium titled "Advances in MEMS - Foundations of Design, Process, Packaging, and Test" on Wednesday, May 22, 2014 at the Holiday Inn - San Jose Airport in San Jose, California. Invited speakers will focus on the technologies that form the basis for advancements in MEMS products, to achieve future capabilities, enabled by innovations unthinkable a decade ago.

**12 ANALYSIS** – The electronics industry trend towards smaller and thinner form factors, coupled with green initiatives and cost reduction efforts, has resulted in many changes in packaging materials. As these trends continue, innovative material solutions will be needed to address emerging requirements.

BY JAN VARDAMAN, TECHSEARCH INTERNATIONAL AND DAN TRACY, SEMI

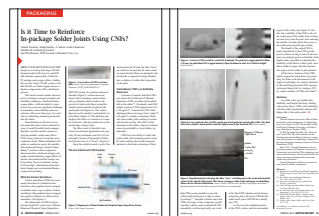


**17 PROFILE** – N-Able Group International (NGI) is a semiconductor focused consulting and executive search firm with a particular emphasis in the fabless and outsourced manufacturing space. N-Able Group serves a client base that spans North and South America, Asia and Europe.

N-ABLE GROUP INTERNATIONAL  
MEMBER COMPANY PROFILE

**20 PACKAGING** – The trend towards smaller interconnects is starting to present assembly and reliability challenges. Smaller diameter copper pillars present an even more significant challenge to assemblers and reliability issues for end-users. However, there may be a solution by embedding reinforcing materials into the solder.

BY VINCENT DESMARIS, SMOLTEK AB AND PHIL MARCOUX, PPM ASSOCIATES



**22 MATERIALS** – There are very few polymeric materials that have made significant impact on the microelectronics industry. It's been a little over 20 years since one of them, BCB, began its commercial path at Dow Chemical. Take a look back at some of that early BCB history.

BY DR. PHILIP GARROU  
MICROELECTRONIC CONSULTANTS OF NC

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## Brocade Integrates Altera's 120G and 150G Interlaken IP into its Multi-Terabit Core Routers

*Stratix V FPGA Featuring Interlaken IP Provides Brocade Line Modules the Flexibility to Scale Cloud-optimized Networks*

ALTERA CORPORATION has announced its Interlaken intellectual property (IP) core has been qualified and selected for production shipments in Brocade® MLX® Series multi-terabit core routers for use in datacenters. The Interlaken IP is implemented on a Stratix® V FPGA and helps enable Brocade routers to rapidly and efficiently scale cloud-optimized networks. Using Altera FPGAs and IP to scale cloud-optimized networks allows businesses to manage high volumes of network data and make real-time decisions based on the results.

“Altera provides us a single Interlaken IP design that is extremely configurable and robust, which enables the high-bandwidth efficiencies



required on our various line module configurations. This unique, single configurable design, coupled with our service cost model infrastructure, benefits our enterprise and service provider customers who have tight budgets and require a specific set of services,” said Majid Afshar, VP, ASIC and hardware engi-

neering, Brocade.

Altera's Stratix V FPGA-based Interlaken solution enables chip-to-chip packet transfers at rates over 100 Gbps, which helps OEMs move the nearly 2.5 exabytes of data that are created each day. The Interlaken IP is a fully integrated solution that includes the MAC, PCS, and PMA layers.

Altera's Interlaken IP core scales as the demand for more bandwidth and higher performance grows. The IP has been through extensive simulation and verification and is proven to work on multiple internal and customer platforms.

To learn more about Altera's Interlaken IP solutions visit [www.altera.com/interlaken](http://www.altera.com/interlaken). ♦

## STATS ChipPAC's fcCuBE® Technology Achieves Significant Growth in 2013

*Performance and Cost Advantages Drive Customer Adoption and Key Design Wins in Mobile, Consumer and Cloud Computing*

STATS CHIPPAC LTD. HAS ANNOUNCED that unit shipments of semiconductor packages utilizing the Company's patented fcCuBE® technology more than quadrupled in 2013 compared to 2012. The performance and cost advantages of this advanced flip chip packaging technology has driven adoption by customers in the mobile, consumer and cloud computing markets.

The most significant area of growth and adoption of fcCuBE technology to date has been in application processors, baseband processors, power management and connectivity integrated circuits (ICs) for the low to high-end mobile market as well as global positioning systems (GPS) and set top box chipsets in the consumer market. Key building blocks of this innovative flip chip technology, namely copper (Cu) column bumps and Bond-on-Lead (BOL) design and interconnection, have delivered clear advantages to customers by providing a higher routing density at a lower cost.

The advantages of fcCuBE are driving

wider customer adoption from cost sensitive markets such as mobile and consumer to networking and cloud computing where increased routing density and performance are imperative. An important feature of fcCuBE technology is the inherent compatibility of the basic design with both mass reflow (MR) and Thermo-Compression Bonding (TCB) processes. STATS ChipPAC's uniquely developed MR process supports bump pitches down to 80µm and below, providing customers a lower cost alternative to TCB at these pitches.

Dr. Raj Pendse, STATS ChipPAC's VP and Chief Marketing Officer noted, “The attributes of fcCuBE® technology offer our customers a scalable path for first level interconnection of new Si nodes. Furthermore, fcCuBE® complements our other flagship technologies such as fan-out wafer level packaging, providing customers the optimum solution across the full spectrum of IC designs and end applications.”

Further information is available at [www.statschippac.com](http://www.statschippac.com). ♦

### ▶ VALTRONIC IS HONORED WITH GOLDEN MOUSE-TRAP AWARD

Valtronic has announced that their active implant advancement using the Glass Encapsulation Implant Technology of **mb-microtec ag** was selected a winner for the Golden Mousetrap Award in the Materials and Assembly Category. The Awards celebrate the companies, products, and people who are energizing North American design, engineering, and manufacturing. The Golden Mousetrap Awards were announced at the Golden Mousetraps Ceremony February 11, 2014 in Anaheim, California. [www.valtronic.com](http://www.valtronic.com)

### ▶ DELPHON APPOINTS RAJESH VARMA TO CTO

Delphon has appointed Rajesh Varma to Chief Technology Officer. Mr. Varma will support all four of Delphon's divisions, including Gel-Pak, Quik-Pak, UltraTape, and TouchMark. Mr. Varma joined Delphon in 2012 as Director of Technology and has played a significant role in developing new materials for Delphon's next generation of products. Prior to joining Delphon, Mr. Varma was instrumental in R&D of polymer-based products for companies including Neocork Technologies and PolyOne/GLS Corporation where he served as Director of Technology and Commercial Innovation Manager respectively. [www.gelpak.com](http://www.gelpak.com)



## ▶ FINETECH & MARTIN UNVEIL LATEST REWORK SOLUTIONS AT APEX

Finetech & Martin, global suppliers of advanced rework and high accuracy bonding equipment, demonstrated their latest rework capabilities at IPC/APEX March 25-27.

The rework Process Shuttle, introduced by Martin (a Finetech Company) last November, was on display for the first time in North America. This new transport slide for Martin's EXPERT 10.6 rework system streamlines flux and solder paste dipping, component printing, and pre-positions even the smallest surface mount devices for precise placement.

Also on display was SmartControl, a new "Touch Screen" user interface on Finetech's FINEPLACER® coreplus advanced rework system. SmartControl provides intuitive navigation of the popular Reflow Command rework software.

[www.finetechusa.com](http://www.finetechusa.com)

## ▶ CORWIL COMPLETES ASSET PURCHASE OF VIKO TEST LABS

CORWIL Technology Corporation has announced the asset purchase of VIKO Test Labs, a division of Infiniti Solutions. The addition of electrical, environmental, and mechanical test services enhances CORWIL's market position as a true OSAT (Outsourced Semiconductor Assembly & Test) leader, joining an



# Altera Joins IBM OpenPOWER Foundation to Enable the Development of Next-Generation Data Centers

*Collaboration with OpenPOWER Members Enables FPGA-based Compute Solutions Based on the IBM POWER Architecture*

ALTERA CORPORATION recently announced it joined the IBM OpenPOWER Foundation, an open development alliance based on IBM's POWER microprocessor architecture. Altera will collaborate with IBM and other OpenPOWER Foundation members to develop high-performance compute solutions that integrate IBM POWER CPUs with Altera's FPGA-based acceleration technologies for use in next-generation data centers.

FPGAs provide POWER users configurable hardware accelerators in the core compute complex that help system architects reduce operating expenses by achieving very high performance at lower power. IBM and Altera have already worked together to create a coherent interface between the POWER8 processor and Altera's Stratix® V FPGAs. This collaboration provides developers a roadmap to use the high-performance capabilities of Altera's Arria® 10 and Stratix 10 FPGAs and SoCs in next-generation POWER-based systems. Leveraging the Altera SDK for OpenCL, developers are able to integrate IBM Power CPUs with Altera FPGAs as a high-performance compute solution.

"The OpenPOWER Foundation will greatly increase the rate of innovation by giving developers an expanded and open set of technologies that will power the next generation of big data and cloud computing applications," said Jeff Waters, senior vice president of Altera's military, industrial and computing division. "Collaborating with IBM and other OpenPower Foundation members enables us to proliferate the use of

FPGAs in a wide range of high-performance computing applications."

The OpenPOWER Foundation includes a group of industry-leading companies working together to develop high-performance compute solutions based on the IBM POWER architecture. OpenPOWER Foundation members include Altera, IBM, Google, Mellanox, NVIDIA, Samsung Electronics, Suzhou PowerCore Technology and Tyan. Together, the companies are building advanced server, networking, storage and hardware-acceleration technologies aimed at delivering more choices, control and flexibility to developers of next-generation hyperscale and cloud data centers. For information on the Open-

POWER Foundation visit [www.ibm.com](http://www.ibm.com).

"We are excited Altera will be collaborating with us on the IBM POWER architecture by providing OpenCL and its powerful FPGAs to the OpenPOWER development community," said Bradley McCredie, IBM Fellow. "This foundation will benefit greatly from Altera's FPGAs enabling a wide set of customized server, networking and storage hardware for future data centers and cloud computing."

Altera® programmable solutions enable designers of electronic systems to rapidly and cost effectively innovate, differentiate and win in their markets.

Visit [www.altera.com](http://www.altera.com) for more information. ♦

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# Honeywell Introduces New High-Performance, Environmentally Preferable Solvent

*Solstice® PF helps manufacturers meet current and future environmental & safety standards*

HONEYWELL RECENTLY introduced a new high-performance, low-global-warming-potential solvent that offers excellent cleaning power for metal and plastic parts.

The new solvent, Solstice® Performance Fluid (PF), effectively cleans oils, greases and other substances commonly encountered in many cleaning applications, ranging from electronics manufacturing to military and aerospace equipment repair. Solstice PF has a global warming potential (GWP) of 1, which is more than 99 percent lower than the GWPs of today's most commonly used solvents. The new material provides solvent users with a cost-effective, energy-efficient and environmentally-preferable alternative to high-GWP solvents.

The widespread adoption of Solstice PF could save about 18 million metric tons of carbon dioxide emissions each year, which is comparable to eliminating carbon dioxide emissions from more than 3 million cars every year.\*

"Solstice Performance Fluid meets all of the needs of today's solvent users, blending superior cleaning power with an excellent health, safety and environmental profile," said David Cooper, global business director for Honeywell Fluorine Products. "Solvent users no longer have to sacrifice performance to achieve environmental benefits."

Solstice PF is suitable for use in vapor degreasing equipment and line flushing, and can be dispensed from an aerosol can. It is available

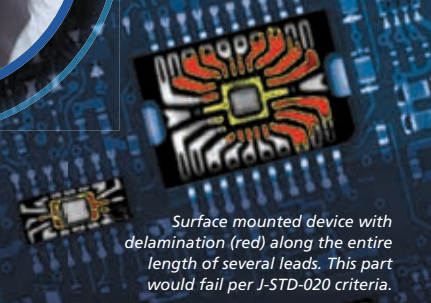
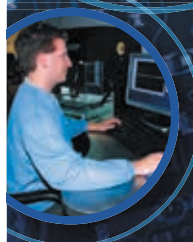
in two alcohol blends for electronics applications, with one of the blends specifically designed to meet California environmental regulations.

Solstice PF is an environmentally-preferable alternative to high-GWP HFC and HFE solvents used today, including HFC-4310mee and HFE-7100. It is also a suitable replacement for HCFC-225ca, which will be prohibited in the U.S. for most uses beginning January 1, 2015. Solstice PF is nonflammable, per ASTM E681 testing, and is not a volatile organic compound (VOC) as determined by the U.S. Environmental Protection Agency (EPA). Solstice PF also has an occupational exposure limit (OEL) of 800 parts per million (ppm), compared with 10 ppm for n-propyl bromide (nPB).

Solstice PF is the latest addition to Honeywell's family of Solstice-branded products, which includes stationary and mobile refrigerants, liquid and gaseous blowing agents, and propellants. The Solstice product line is based on Honeywell's new hydro-fluoro-olefin technology, which is designed to help customers lower their carbon footprint without sacrificing end-product performance.

For more information about Solstice PF, visit [www.honeywell-solvents.com](http://www.honeywell-solvents.com). ♦

*\*Based on broad customer conversions from HCFC-225ca, HFC-4310mee, and HFE-7100 to Solstice PF, and calculated using the EPA's greenhouse gas equivalencies calculator ([www.epa.gov/cleanenergy/energy-resources/calculator.html](http://www.epa.gov/cleanenergy/energy-resources/calculator.html)).*



Surface mounted device with delamination (red) along the entire length of several leads. This part would fail per J-STD-020 criteria.

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### ► MICROSS TO CONSOLIDATE MANUFACTURING SERVICE FACILITIES

**Micross Components** will expand its Hatfield, PA and Clearwater, FL facilities with operations from its Tempe, AZ plant (formerly Premier Semiconductor Services). After extensive analysis, Micross concluded that it can provide more effective service and value to its customers through consolidating its primary back-end semiconductor processing services into one centralized location, which will be in Hatfield, PA. Concurrently, Tempe's Counterfeit Testing and DNA Marking services will be relocated to Micross Clearwater.

[www.micross.com](http://www.micross.com)

### ► 3D INCITES, SEMI AND TECHSEARCH PARTNER FOR AWARDS PROGRAM

**3D InCites**, the premier online content source for reliable 3D technology information, announced that it has partnered with **SEMI** and **TechSearch International** to host the second annual 3D InCites Awards. Proceeds of the 2014 awards program will fund a newly formed 3D InCites STEM Scholarships program, which this year will award a scholarship to a graduate of the SEMI High Tech U Program.

[www.3dincites.com](http://www.3dincites.com) ♦

## Promex Industries of Silicon Valley Completes Key Personnel Hiring Spree

PROMEX INDUSTRIES OF Silicon Valley has announced the hiring of key operations, engineering, project management and sales personnel to support the company's strategic growth forecast for 2014 and beyond.

Richard Otte, President and CEO of Promex stated "Our customers recognize the value of a single entity providing microelectronics process development, new product introduction and volume manufacturing from one centralized location. We are delighted to add these highly talented people to Promex's customer-centric culture. Our rapidly growing customer base is bound to approve of the even greater competitive advantage Promex provides".



### Ed McBain, Vice President of Operations

Ed McBain joined Promex Industries in May, 2013. Prior to this, Ed has applied his 30 plus years of operations experience in the Semiconductor industry in engineering and management. His experience spans wafer fab, sort, domestic assembly operations, high reliability manufacturing for Military and Aerospace applications, as well as component assembly for MCM's, high speed optoelectronic devices and 3D integration. Ed has worked at Harris Corporation, Zilog and has startup experience in MCM technologies with Micro Module Systems as well as Lightlogic. Ed holds a BS (Metallurgical Engineering) from Purdue University and a MBA from Florida Institute of Technology.



### Dr. Suzette Keefe Pangrle, Senior Scientist/Technical Project Manager

Dr. Pangrle joined Promex Industries in November, 2013. Prior to this, she applied her 10 plus years of experience in technology and product development, technology integration and reliability, and project/program management. Dr. Pangrle has worked with reputable Bay Area companies including Vertical Circuits, Spansion and AMD. Suzette received her Project Management Professional (PMP) Certification from PMI and her PPM from the University of California, Santa Cruz, Extension. She received her B.S. (Chemical Engineering) along with a M.S. (Metallurgy) from the University of Illinois and her Ph.D., Ceramic Science, from Pennsylvania State University.



### Dr. Annette C. Teng, Senior Process Engineer

Dr. Teng recently joined Promex after spending the past three years working in Australia. Prior to Australia, she held IC packaging engineering positions in the Bay Area including CORWIL Technology, Linear Technology Corp and Philips Semiconductor (now NXP). Annette received her BS in Chemistry from Sweet Briar College and PhD in Materials Engineering from University of Virginia.



### Serafin Pedron, Technical Program Manager

Serafin joined Promex in October, 2013. He has over 30 years of experience in packaging, assembly technology, specialized processes, technical marketing, quality control, and industry standardization. Prior to joining Promex, Serafin has worked for companies that include UTAC, Advanced Interconnect Technologies, Nchip, Inc., and Indy Electronics. Serafin's early career in engineering and manufacturing management was in the Philippines. Serafin received his BS in Electrical Engineering from the University of the Philippines.



### Paul Gagliano, Business Development Manager

Paul joined Promex in November, 2013. Paul's background includes over 20 years of sales experience focusing on technology companies. Paul has applied his knowledge of account management, sales engineering, product development support and program management at reputable Bay Area companies that include Cooler Master, Solectron/Flextronics, SCI/Sanmina and Vishay. Paul received his BA in Business Administration from Northeastern University.

For further information about Promex Industries Inc. visit [www.promex-ind.com](http://www.promex-ind.com) or call 1.408.496.0222. ♦



## INDUSTRY INSIGHTS

By Ron Jones



# Implications of the Semiconductor Supply Chain on Conflict Mineral Management

▶ EVERY MANUFACTURING industry has a supply chain. Some are simple, say toothpick (start with tree, make toothpick in one factory). Some are not so simple, say 747, with 6,000,000 parts from 33 countries. OK, so we're somewhere in the middle.

If you step back and look, we have built IC's the same way for the past 50 years. The supply chain consists of sand (sort of), purified silicon, silicon starting wafers, processed wafers, probed wafers, assembled die and tested final devices. In the early days, all operations took place in a single factory and now the processes may be done in factories all over the world . . . but it's the same basic processes. We start with a wafer then go through multiple processes where we oxidize, spin resist, bake, expose, develop, etch, strip resist, put something in the hole via furnace, implanter or vapor dep, oxidize . . . apply, rinse, repeat. The assembly side is basically the same also. Separate die from wafer, attach die to some substrate and wire bond or flip a bumped die onto a substrate. Protect the die with some plastic, mark and ship. We have certainly made huge advances in speed, device geometry, wafer size, reliability et al. but we still string a bond wire the same way . . . just a lot faster.

As I've been focusing on Conflict Minerals Compliance over the past several months, several things have struck me about our now worldwide semiconductor supply chain.

First, it is very shallow. What I mean by that is we start with a very short list of high purity materials, e.g. silicon, a few metals (Au, Cu, Al, W, Sn, Fe, Ni . . . a few organics and some gasses and dopants. We combine those first in a wafer fab, then in an assembly operation. Voilà, we have an integrated circuit.

Second, the supply chain is serial and quite predictable. We do fab first, then probe or not, then assemble and then test.

Third, we know where all the factories are. You don't find a wafer fab in the back corner of a warehouse. We have a list of every wafer fab that has been built and a list of virtually all assembly factories. There are approximately 150 foundry factories (plus IDM captive fabs) and approximately 150 OSAT factories (plus IDM captive assembly factories). Fabless and IDM semiconductor companies use some subset of those known fab and assembly factories. We know exactly what direct materials go into every IC. Ignoring contamination, some unintended element doesn't just jump on a wafer or into a package. We pride ourselves on control, control, control.

Not only do we know what materials go in, we know exactly when and where they go in. You introduce TiW barrier metal at a TiW sputtering operation. You introduce gold wire at a wire bonding operation.

There are a fairly limited number of suppliers of direct and indirect materials we use. You just don't have dozens of vendors making TiW sputtering targets, for instance.

So why have I drug you through the last 50 years of semiconductor manufacturing and the unique structure of the semiconductor supply chain.

The reason is that public companies are expected to supply information to the SEC about the source of the Tin, Tantalum, Tungsten and Gold in their products. We don't have to get rid of them, just say where they come from. We can even use materials from then Democratic Republic of the Congo as long as it is not from operations that fund groups that oppress the people.

Semiconductors make up approximately 25% of the content of electronic products. If the semiconductor industry could become totally conflict free, it would go a long ways toward helping customers of semiconductor companies prove they are conflict free. Even private companies get involved as they must supply information about their supply chain to their customer that must use it in their reporting.

The various attributes of the semiconductor supply chain enumerated above provide a real opportunity to leverage our compliance efforts across out entire industry. There is no need for every fabless company using TSMC or ASE to

talk directly to them. The opportunity exists to gather and share the data saving money and time for all parties involved.

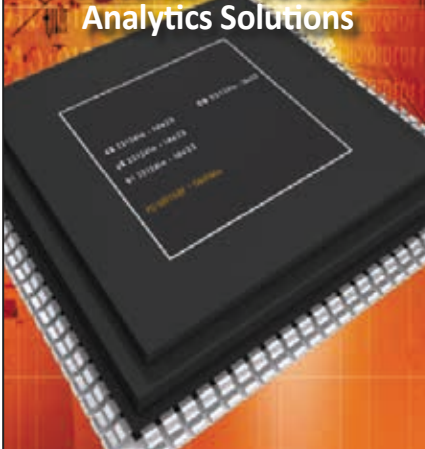
Right now, everybody is scrambling to get their info together for the SEC filing on May 31, 2014. When that date passes, I hope we step back and decide to work together to achieve much better results with much less effort. Time will tell. ♦

*RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Visit [www.n-ablegroup.com](http://www.n-ablegroup.com) or email [ron.jones@n-ablegroup.com](mailto:ron.jones@n-ablegroup.com) for more information.*

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## COUPLING & CROSSTALK

By Ira Feldman



*Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and “couples” with your thinking. Most of the time I will stick to technology but occasional cross-talk diversions like this one may deliver a message closer to home.*

## Disposable Chips?

▶ I'M NOT A FAN OF DISPOSABLE cups and other tableware. Yes, they are convenient and in some cases even economical. However, they are not great substitutes for the “real thing”. Splinters from your chopstick? A broken plastic knife from attempting to cut something? Spork? Need I say more?

Seeking to lessen our family's environmental impact and set a good example for our children, **we practice the green philosophy of reduce-reuse-recycle**. Recycle paper, containers, and packaging? Rechargeable batteries? Cloth napkins? Hand-me-downs of children's clothing to/from friends? All yes plus plenty more. Note the word “practice” which means we are not perfect and can always do better. Do I always leave the house with a reusable water bottle or coffee/tea mug instead of using disposable cups and bottles? No. Should I? Probably.

Last year on the way to the *International Technology Roadmap for Semiconductors* (ITRS) meeting in Lyon, France I had a revelation on the Rhônexpress light-rail between the airport and downtown. No, it wasn't my typical jetlagged “where am I?” or “where am I headed?” ... What I had noticed was my paper transit ticket purchased from the kiosk had no magnetic strip or printing indicating validity. One side had the basic information about the system. The other side was blank other than a very small dot matrix printed serial or control number. Did the vending machine malfunction and neglect to print my purchased fare on the card?

Being very tired and figuring I could be just another non-French speaking tourist if need be, I boarded the train. While waiting for the conductor, I discovered a telltale lump approximately 1 mm in diameter. Watching the conductor tap the cards to his handheld terminal and holding the card up to the light confirmed my suspicions. These tickets have embedded radio-frequency identification (RFID) circuits consisting of an antenna and an integrated circuit (IC).

The use of RFID “tags” was not exactly a revelation since I've seen them for a number of years in everything from credit cards to library books. I've had RFID chips in my credit cards since American Express introduced Express Pay in 2005. Our local library installed RFID checkout system several years ago. And I'm no stranger to using “reloadable” RFID cards for transit systems. I've got Suica, Oyster, Clipper, Octopus, and Shanghai Public Transit cards sitting in my travel box. (Bonus points if you can name the matching cities. Shanghai Metro marketing gets no points for naming creativity.)

The revelation is that the **RFID tags especially the silicon IC have become sufficiently inexpensive to use them for one-time disposable applications**. In the other cases the useful life is far longer – one or two years for credit cards, several years for transit passes, and years if not a decade or more for library books. And these are definitely higher value and multi-use applications.

Until the recent Target credit card data theft fiasco, US banks and merchants have resisted the costs to implement the Europay Mastercard Visa (EMV) “smart card” system. The EMV chip card has been proven to reduce fraud across Europe and around the globe. In light of the recent fraudulent transaction and lost business costs, those smart cards with encryption chips have since become “essential”. Previously the inconvenience of transitioning the United States (US) was greater than the perceived value. Target has pledged to spend \$100 M to accelerate their deployment in their nearly 1,800 stores and all of their proprietary charge & debit cards within the next year.

Beyond RFID ICs it is clear that more of **our electronics have or will shortly become disposable**. There are electronic greeting cards that play pre-recorded tunes or allow the giver to personalize their message. Hopefully the batteries

last long enough to play the message more than a handful of times. Do you too have a collection of USB “memory sticks” from conferences and suppliers in your desk? Certainly the older ones with as little as 128 MB capacity are basically disposable.

Mobile phones exceeded 100% penetration at the end of 2012 –marketing speak for having more active mobile phone accounts than the world's population (~7 B). And many mobile carriers are shortening phone replacement cycles from two years. Clearly some mobile phones are becoming disposable. I've been lucky enough to resell (reuse) some of my prior generation high-end smartphones when I've upgraded. But what happens to feature phones costing less than \$25? I have a few of those in my travel box too...

**Proteus Digital Health even has an ingestible semiconductor based sensor**. The sensor is encapsulated in individual pills and powered by stomach acid. Their system can then report the time of ingestion and specific serial number for each dose of medicine. It is not clear how much of chip is broken down and absorbed versus what remains to be “passed”. Proteus simply says the sensor moves “through the body in the normal process of digestion”. I'm not certain I want to try to recycle what remains. Clearly a single-use application that is disposable.

Sometimes we can **reuse** our electronics by moving them to new users or uses. With current trends of increasing number of “must have” electronics and the market pressure of Moore's Law continuing to decrease the price of semiconductors, is it very unlikely that the world will **reduce** its consumption. What about **recycling**? Even though some in-process scrapped materials (such as full silicon wafers) can be recycled or reclaimed, significant recycling of finished semiconductors is difficult and inefficient. Yes, miniscule amounts of gold can be extracted. However gold use is declining rapidly with the transition to lower cost copper wire bonds and flip-chip packaging. At the same time an even greater set of exotic materials from all across the periodic table including several new III-V materials are being used to build semiconductors. When is the last time you purchased hafnium, let alone recycled it?

The **Internet of Things** (IoT) and sensor applications being described by

the **TSensors Roadmap** ([www.tsen-sorssumit.org](http://www.tsen-sorssumit.org)) require a few fundamental technologies. In order to enable applications with massive numbers of sensors (millions and above), **sensor units will require both wireless connectivity and internal power** – either long lasting batteries and/or self-generation. Wireless communication is needed since with these quantities of sensors it will be neither practical nor economical to “hard wire” them. By using the appropriate sensors and low power electronics, the devices will last the needed five to ten years or more without maintenance to replace the batteries.

It is clear to many in the TSensors community that **ultimately the price per microelectromechanical system (MEMS) sensing element needs to be on the order of \$1 to enable the economics of these applications. TSensors applications are the ultimate high volume application for disposable electronics.** We will need to determine what to do with a million, let alone a trillion or more, sensor units when they are no longer useful. **Recycling needs to be added alongside cost, power, and wireless requirements to enable this exciting new technology!**

*For more of my thoughts, please see my blog <http://hightechbizdev.com>.*

*As always, I look forward to hearing your comments directly. Please don't hesitate to contact me to discuss your thoughts. ♦*

*IRA FELDMAN ([ira@feldmanengineering.com](mailto:ira@feldmanengineering.com)) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.*

*Ira follows many “small technologies” from semiconductors to MEMS to nano-technology. He volunteers for numerous industry committees and events including the organizing committee of the MEPTec MEMS Technology Symposium, organizing committee and editor of the “Environmental Sensing” chapter of the TSensors Roadmap & Summits, general chair of the Burn-in & Test Strategy (BiTS) Workshop, and the Test Working Group of the International Technology Roadmap for Semiconductors (ITRS).*

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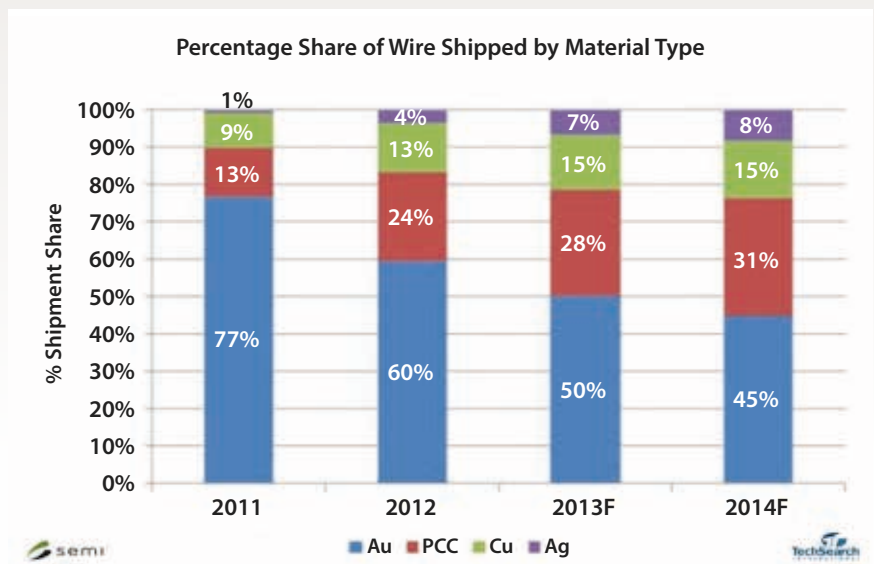
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# Substrate and Interconnect Materials Trends in Packaging

Jan Vardaman, TechSearch International and Dan Tracy, SEMI

THE ELECTRONICS INDUSTRY TREND towards smaller and thinner form factors, coupled with green initiatives and cost reduction efforts, has resulted in many changes in packaging materials. As these trends continue, innovative material solutions will be needed to address emerging requirements related to product integration, mobility, reliability, and performance. Key semiconductor packaging growth areas include flip chip, ball grid array (BGA), wafer-level packages (WLP), leadframe-based chip scale packages (CSP), stacked-die packages, and system-in-package (SiP)/multichip packages. For the latter, package-on-package (PoP) designs continue to experience strong growth, and Through Silicon Vias (TSV) are being developed to further address requirements for increased integration in 3-D packaging form factors. The drivers for flip chip packaging continue to be electrical performance, on-chip power distribution, and pad limited designs as these factors, as well as form factor, shift interconnect technology from wire bond to flip chip for processors and devices used in wireless applications.

For packaging substrates, many high-end devices have migrated from wire bond to flip chip the high-density interconnections on the chip are at a minimum bump array pitch on the substrate of 140 to 150 $\mu\text{m}$  for solder bumps in many applications and 40 to 130 $\mu\text{m}$  for copper pillar. Bump pitch reductions to 50 to 60 $\mu\text{m}$  pitch can be found on company roadmaps corresponding with the introduction of 14nm node silicon. To support these circuit densities the substrates have to be fabricated by the more expensive build-up process, which consists of thermosetting organic films with vias that are laser drilled and circuit patterns formed by a semi-additive process.



Source: Global Semiconductor Packaging Materials Outlook - 2013/2014 Edition

According to SEMI, today's leading-edge CSP substrates have 15 $\mu\text{m}$  lines and spaces and are moving toward finer line and spaces, to handle fine bump pitch of  $\leq 110\ \mu\text{m}$ . Substrate vendors are targeting 5 $\mu\text{m}$  lines and spaces and 40 $\mu\text{m}$  via diameters in the build-up layers in 2015. Core layers are fabricated with 12 $\mu\text{m}$  lines and spaces with vias as small as 50 $\mu\text{m}$  and capture pads as small as 110 $\mu\text{m}$ .

Solder balls are an important interconnect material in substrate-based packaging. Most of the solder balls shipping today are lead (Pb)-free, but a few companies still offer tin lead (SnPb) solder balls. High-Pb balls are used to provide improved standoff for packages such as ceramic BGAs, but these packages have small unit volumes. The most popular Pb-free solder ball composition is the SAC alloy (tin-silver-copper) but a variety of compositions are used in production today. Increasingly, companies have adopted variations of these alloys with

small amounts of other elements in the alloy to modify mechanical and physical properties. The solder ball market is forecasted to experience a compound annual growth rate (CAGR) of 9.4 percent in revenues and 11.2 percent in volumes from 2012 through 2017. Approximately 85 percent of solder balls are used for BGAs and CSPs, and 15 percent for WLPs. WLPs typically use  $\leq 300\ \mu\text{m}$  diameter solder balls. More information is available on the SEMI website ([www.semi.org/en/MarketInfo/PackagingMarket](http://www.semi.org/en/MarketInfo/PackagingMarket)).

While flip chip interconnect continues to see strong growth, wire bonding remains the interconnect choice for many of today's semiconductor packages. However, there are many changes underway bonding wire materials. As a result of much development by companies along the bonding wire supply chain, copper wire, including palladium-coated copper (PCC), usage soared as gold metal pricing rose. In 2013, it is

estimated that total copper wire will represent 43 percent of wire shipments, up from less than 2 percent shipped in 2007. Even with the recent drop in gold metal pricing, the industry transition to copper wire is well established and, over the last couple of years, interest in using silver bonding wire has grown as well.

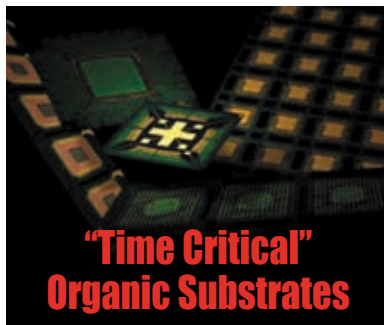
Silver bonding wire usage emerged as a low cost alternative to gold wire without, necessarily, the need for investments in high-end bonding equipment that are required for copper wire. Interest in silver wire developed initially for use in LED packaging and for some memory devices, though usage has ramped in production for other IC devices, such as mobile baseband chips. While advanced packaging has the strongest unit growth rates, it is estimated the wire bonded packages represent 80% or more of the total packaged IC shipments and these packages are estimated to grow at a CAGR of 6 percent through 2017. ♦

*All of the information in this article was derived from a recently completed market research study, **Global Semiconductor Packaging Materials Outlook—2013-2014 Edition**, produced by SEMI and TechSearch International. In developing this report, over 150 in-depth interviews were conducted with semiconductor manufacturers, packaging subcontractors and packaging materials suppliers throughout the world.*

*TO ORDER YOUR COPY of **Global Semiconductor Packaging Materials Outlook—2013-2014 Edition**, please contact Dr. Dan P. Tracy, research development director, Industry Research and Statistics, SEMI, via email at [dtracy@semi.org](mailto:dtracy@semi.org), or telephone 408-943-7987.*



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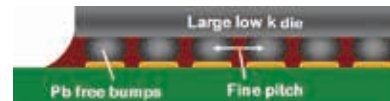
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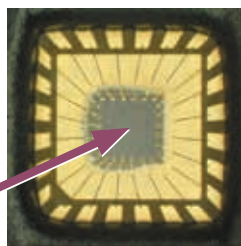


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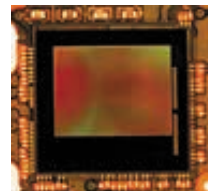
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# “All This Fun, and a Paycheck, too?”

*A collection of stories from a long and satisfying engineering career; showing how much fun, worthy, and enriching a technical life can be.*

by Tom Clifford

THIS BOOK IS A COLLECTION OF stories: assignments from a long and enjoyable engineering career as well as anecdotes and experiences from summer jobs, vacations, and consulting. The focus is technical; each little story pivots on some scientific principle. The intent is three-fold: a) genealogical: to capture descriptions of a lifetime of fun times and accomplishments for descendents who might be curious about old great-grandpa Tom; b) to inspire a next generation of youngsters to consider pursuit of engineering, science, and critical thought, as a door to a fruitful life; and c) to try to bridge that pervasive “boring and/or over-my-head” gap by showing that “engineering” concepts are essentially common-sense and intuitive (you learned them in kindergarten playground), and the jargon should not be off-putting. The book’s message: Engineering/science can be fun; it happens every day and everywhere; a degree is not a prerequisite.

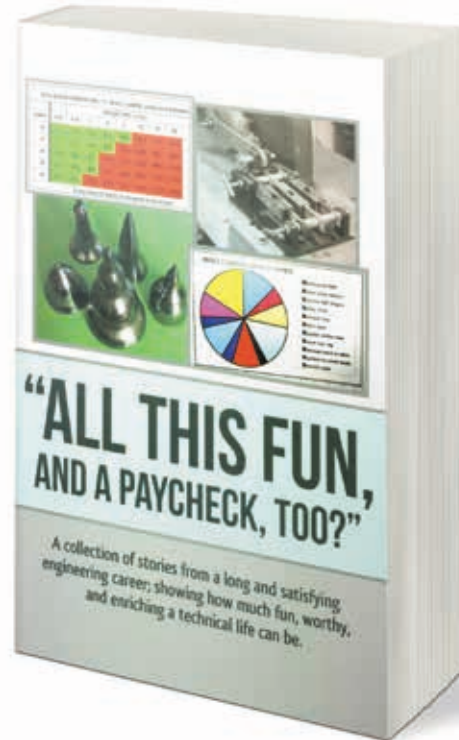
Following are six items randomly selected from the 160 items described in the book, now available on Amazon.

At **Raychem**, we had developed an ablatative material for a hypervelocity missile nose cone. The qual test involved ogive samples on the nose of a Mach6 3-stage rocket sled at White Sands. First trial, midnite, on grandstand a mile away. ...sled lights up; 1st, 2nd, 3rd stages burn, sled leaves the track (est Mach 5) and powders into a trackside concrete camera blockhouse, massive fireworks fill the desert sky, only fragments of sled and samples remain. Couple days later we fashioned another set of samples, and staff set up another sled for another test

run. Midnite, from a viewstation farther back. Sled lights up, 1st, 2nd, 3rd stages burn, and the sled again leaves the track, this time arcing high slow-motion flaming trail overhead, we see it will miss us, so we all pile into jeeps to recover it. Smoking wreckage reveals our nosecones had survived Mach5 plus impact with New Mexico desert. Successful trial and lots of fun.

At **Siltec** in the 70s, we made silicon wafers, for the emerging semicon industry. Safety for workers handling fuming nitric and hydrofluoric acids appeared irrelevant.... pre-OSHA sweat-shop conditions! I took acid-burned operators to the Emergency Room. I designed and implemented a rotary acid-etch station, which uniformly etched the wafers, so operators did not need to reach into the orange acid fumes, to mike the wafers to check the process. Load the wafers, drain the acid a few minutes later, check dry wafers to confirm, and don’t dissolve the flesh off your hands. Nice to make a difference!!!

**Summer Job 1959, Engineering Aide**, south of Laredo Texas. The only way to determine the storage capacity of the big Falcon Dam was to measure the bottom depth. The dam retained precious water for the survival of crops and people in the desert delta when needed, and also contained flood waters that could drown all of Brownsville, Matamoros and points south. After a big muddy flood was contained, by design, and dropped zillions of cubic yards of silt on the bottom; they needed to know the new depth and therefore the storage capacity of Falcon Lake. My job, perched high on a mid-lake tower with plane-table, maps, timers and visual triangulation protocols, was to help locate the depth reading from the boat with the fathometer, as it crossed the lake on prescribed traverse paths. Between runs: fishing, swimming, diving from the tower. Simple geometry, fundamental engineering concepts, plus 12-hour days, 7 days per week, overtime, double time, with no place to spend the money! Never had so much money, before or since. Lots of fun.



At the **Sinclair** refinery in Texas in the 60s, I helped a paradigm-shift in oil analysis. Crude oil needed to be characterized ... tar, heavy/light oils, gasoline constituents (heptane octane, nonane) light ends, ethylene, methane etc. Even back then millions of dollars in sales price and optimum set-up of refinery operation pivoted on this analysis. The method then employed a small-scale, but fully representative crude distillation column system, a Poddelniak Fractioneer, with pumps, pipes, valves, boilers and condensers, kettles, etc. occupying big lab rooms, several operators and many hours/days to run several barrels of crude, laboriously obtained and transported, to measure what you got. The new method required only a thimble-ful of crude, couriered or mailed from the tanker or well-head, and the new mass-spec, GPC system. One lab tech in 30 minutes got the answer. I schleped and weighed samples, and helped confirm that this new quick and fundamentally sound micro-lab method gave exactly the same results as the nasty, expensive old way. I was aware even then that something important was being created.

At **McDonnell**, on project Gemini, I (starry-eyed rocketeer-worshipping rookie) was on a Propulsion Dept. team to create/demonstrate EVA (Extra-Vehicular-Activity). Astronauts needed to move controllably around in space. Any thruster not vectoring thru their CG would send them spinning into deep space, doomed. Three thruster approaches were considered ... hand-held single, double handlebar, and multi-axis backpack style. As the best group cartoonist, I provided the necessary sketches along with our RFQ (Request for Quote) to Rocketdyne, Bendix, Aerojet, and others. The task progressed, detailed engineering designs were finalized, Gemini EVA was a proven success. EVA is now a routine Space-Station, Hubble activity; and I was a part of all that. Cool!!!

At **Lockheed Martin**, Group Lead, Advanced Electronics Packaging, I got to introduce new technologies (SMT, MEMS, nano-) to the local designers. My group identified and demonstrated specific components and assembly configurations that were reliable enough to survive harsh long-term mission environments, where failure wasn't an option.

We tested BGAs, mBGAs, Column Grid Arrays, QFNs, plastic and ceramic, assembly variants, embedded passives, etc. on a variety of PWBs. We contributed to important aerospace technology.

And, a few more excerpts...

### Accelerated-Aging Bleach, Pumped Thru Metal Plumbing

Another lesson learned: apply your book-learning or ask around, before you make dramatic changes to your "standard" test procedures.

At Lockheed Martin, Group Lead, Advanced Electronics Packaging, I got to introduce new technologies (SMT, MEMS, nano-) to the local designers. My group identified and demonstrated specific components and assembly configurations that were reliable enough to survive harsh long-term mission environments, where failure wasn't an option.

We were testing HDPE formulations targeted for the bleach bottle market. That required molding and testing big plastic bleach-bottles of candidate plastic formulations. We would mold the bleach-bottles, fill these with standard off-the-shelf, well-controlled Clorox bleach, seal the lids, and put them in an oven according to standard methods, check them every couple days to see when the bottles started to crack. That required buying, and ultimately discarding many, many gallons of expensive household bleach.

Our group-leader suggested we consider buying industrial bleach in 55-gallon drums, to save a few pennies. Sure. No problem. To dispense it efficiently, we rigged up some stainless steel piping, valves and hoses, to fill our test bottles. The first test series to use this resource took the usual several expensive weeks to make the resin formulations, another week to mold the test specimen bottles, a few days to set up and initiate the oven-aging test. A week into the testing it became clear that the bottles were bulging under unexpected high internal pressure, and a few had already failed (way too soon!!!!), spraying bleach all over the

inside of the test chamber. "What the...?"

Turns out that bleach in contact with steel will start corroding everything it touches, and start itself along the road to very rapid thermal decomposition. So the test was a waste. It cost K\$\$\$ and months of plant runs, formulating, test sample prep, and testing. We were not real proud of that one!! We should have used plastic plumbing, or go back to off-the-shelf Clorox. We did the latter, later.

### Mentoring New-Hires

The new hires were scary bright, the cream of the graduating engineering classes of some of the best schools across the country. I managed to capture several for critical assignments, in R&D type projects.

One created the software for an analytical model for failure predictions, based on a joint project with Sandia. Another co-authored a paper with me on test-plan optimization; her contribution was the cost-reduction aspect of optimized testing: time costs money, test technicians cost money, liquid nitrogen to chill the chamber costs money. She wanted our readers to know that statistical optimization is not a dry academic exercise, but a real-world resource. Last I heard, Vanessa was back East somewhere carving out her niche.

Another spearheaded the advanced packaging materials effort for a big reliability test series; another combined testing and data-reduction, correlations, and reportage of a major study on the reliability of embedded passives (which did get published!). Another did preliminary feasibility work on possible applications of MEMS (micro-electro-mechanical systems), who later got a good gig in a space-probe program in our Palo Alto research lab. Another tackled, and successfully handled the automated failure detection and instrumentation in our Phase1 and Phase2 test series. He wrote a paper on his own time on stress-distribution and impact vulnerability/correction of mountain bike design, and then left to start his own business.

Another worked out the "ppm" quality statistics that served to guide the mil-aero industry's test specs. We co-authored a paper at the China Lake conference, back in the day. Another became project lead ("principal scien-

continued on page 29 ▶





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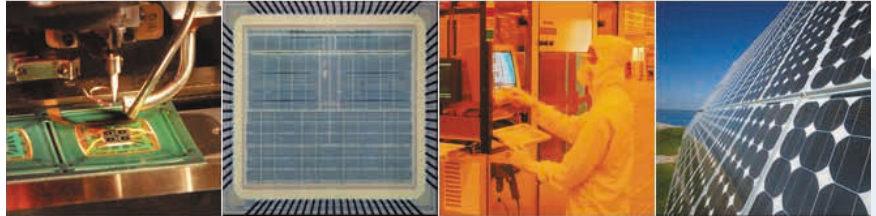
N-Able Group International (NGI) is a semiconductor focused consulting and executive search firm with a particular emphasis in the fab-less and outsourced manufacturing space. Founded in early 1996, N-Able Group serves a client base that spans North and South America, Asia and Europe. The company was founded in Bangkok, Thailand, and incorporated in the state of Texas. Within a few months, NGI opened a second office in Hsin-chu Science Park, Taiwan, to serve IDM, foundry and OSAT customers. In late 1997, N-Able Group moved its headquarters to Silicon Valley, while maintaining its offices in Bangkok and Hsin-chu. The company completed its 18th year in business in February, 2014. The N-Able resource model utilizes a combination of employees and outside subject matter experts to deliver value in the most efficient and cost effective manner possible.

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industry, N-Able recruiters understand the nuances of semiconductor specific requirements. The process starts with a clearly defined job description. Potential candidates are identified in accordance with job parameters and fully vetted before presentation to the client. N-Able stays fully engaged through the interview, offer presentation and negotiation phase and the final resignation to reporting process.

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  - N-Able Group has performed a wide variety of projects including: supply chain formation and optimization; yield, cost, quality, cycle time and on-time delivery improvement; organizational structure analysis and improvement; and executive mentoring.
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  - N-Able Group has provided support to numerous companies for the identification, evaluation and selection of software including ERP, MES, Advanced Planning Scheduling, Supply Chain and Yield Management systems. NGI has also advised a wide range of software companies and installers on the unique features of the semiconductor industry.
- **Investment and Acquisition Due Diligence**
  - N-Able Group has provided industry specific analysis and recommendations for a variety of investments, acquisitions and divestitures.
- **Expert Witness**
  - N-Able Group has provided expert witness support for a variety of commercial and government agencies and services.
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  - N-Able Group initiated and architected the Semiconductor Manufacturing Data eXchange standard. Although never formally adopted by the industry, the struc-

ture is still used today for data collection, mapping, manipulation and storage.

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■ **THE CHANGING LANDSCAPE OF MEMS MANUFACTURING AND PROCESS TECHNOLOGIES** will provide a look at MEMS product development involving the creation of new fabrication processes, fabrication sequences, and the use of new materials in the context of the “manufacturing renaissance” happening worldwide.

■ **MEMS PACKAGING – IMPACT ON DEVICES AND VOLUMES** will include speakers with insights into packaging of MEMS and the impact of MEMS on devices and their packaging at volume.

■ **MEMS DEVICE TESTING CHALLENGES** speakers will address some of the issues and solutions that have been used in testing devices and which could be used in creating standardized testing of MEMS devices for high volume low cost applications in the future.

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## The Current Entrepreneurial Environment for MEMS

Kurt Petersen, Ph.D.

Several converging trends are transforming the entrepreneurial process for starting MEMS companies and getting MEMS devices into production and into the market. First, recent market set-backs have caused traditional VC funds to view any hardware start-ups with renewed scrutiny and skepticism. The large investment in money and time is on top of the already risky prospects for a start-up being commercially successful. Secondly, MEMS is recognized by investors, foundries, and large consumer electronics companies, as a very successful new product area due to the huge up-take of MEMS components in mobile devices in recent years. Third, key strategic issues in huge upcoming new consumer markets, such as wearables, are sensors and contextual awareness; areas which are uniquely solved by MEMS devices. And fourth, the sheer number of successful, high volume MEMS devices currently on the market, has created a huge pool of skilled MEMS developers and manufacturers which can be drawn upon for new devices and new start-up companies. All these factors dramatically influence how companies get funding and operate. All these issues will be discussed as they relate to new MEMS companies.

*Dr. Petersen has published over 100 papers, and has been granted over 35 patents in the field of MEMS. In 2011, Dr. Petersen joined the Band of Angels in Silicon Valley. The Band is an angel investment group which mentors and invests in early stage, high-tech, start-up companies. Today, he spends most of his time helping and mentoring such companies. ♦*

# Is it Time to Reinforce In-package Solder Joints Using CNFs?

Vincent Desmaris, Shafiq Shafiee, A. Saleem, Anders Johansson  
Smoltek AB (Gothenberg Sweden)  
and Phil Marcoux, PPM Associates (Mountain View, CA)

DIRECT PCB MOUNTED FLIP CHIP bumps are evolving from large 350  $\mu\text{M}$  diameter solder balls down to small 50  $\mu\text{M}$  diameter copper pillars. Inside the IC package most copper pillars, whether they are the “large” 50  $\mu\text{M}$  version or the thin 20  $\mu\text{M}$ , are solder capped and use a thermo-compression reflow attachment process.

This trend towards smaller interconnects is starting to present assembly and reliability challenges. Smaller diameter copper pillars, while desirable by users, present an even more significant challenge to assemblers and reliability issues for end-users. However, there may be a solution by embedding reinforcing materials into the solder.

Nanostructures in the form of carbon nano-tubes have been evaluated for years. A small Swedish based company, Smoltek, recently created a means of growing metallic carbon nano-fibers, CNF's using catalysts of common semiconductor metals. When embedded with solder or conductive epoxy the metallic fiber reinforced bumps, named Carbon-Bump™ produce robust component interconnections which are stronger and enable smaller diameter copper pillars. If desired, the reinforced fiber bumps can be less than 10  $\mu\text{m}$  in diameter and up to 20  $\mu\text{m}$  high. Attachment of the fiber micro bumps uses conventional thermo-compression bonding.

## What Are Carbon Nanofibers

Carbon nanofibers (CNFs) are commonly described as cylindrical nano-structures with graphene layers arranged as stacked cones, cups or plates. Carbon nanofibers with graphene layers wrapped into perfect cylinders are called carbon nanotubes. (See Figure 1)<sup>[1]</sup>

The fabrication of CNFs involves placing finished IC wafers into a Plasma Enhanced Chemical Vapor Deposition



**Figure 1. Cross-section of CNFs in a Nano-tube.** (Source: [http://www.springerimages.com/Images/Chemistry/1-10.1007\\_s10853-006-0676-5-3](http://www.springerimages.com/Images/Chemistry/1-10.1007_s10853-006-0676-5-3))

(PECVD) system. In a plasma enhanced chamber, Figure 2, carbon atoms are mixed with a transition metal catalyst, such as platinum which results in the growth of carbon rich fibers around the catalytic metal particles located on the metal pads (See Figure 4). The carbon deposits on the catalytic metal particles to form fibers (Figure 3). The diameter and length of the fibers is a function of a number of factors, with the particle size of the metal being a major factor.

The fibers used by Smoltek's processes for electronic applications are typically 30 nm in diameter and 10 to 30  $\mu\text{m}$  in length. Clusters of thousands of fibers result in the form of a “forest”. (Figure 3)

Since the catalytic metal is part of the

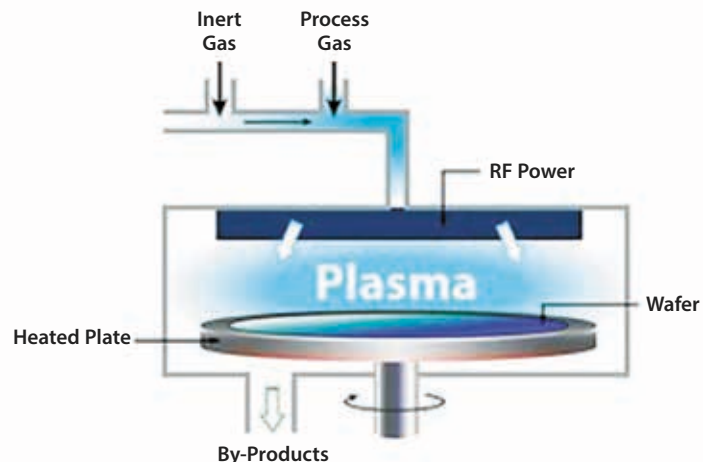
metal pad on the IC then the fiber “trees” are rooted to the pad. By the term rooted we mean that the fibers are attached to the metal pads as opposed to being blended into a solution of solder that's deposited on the pads.

## CarbonBump™ CNF's as Reliability Enhancers

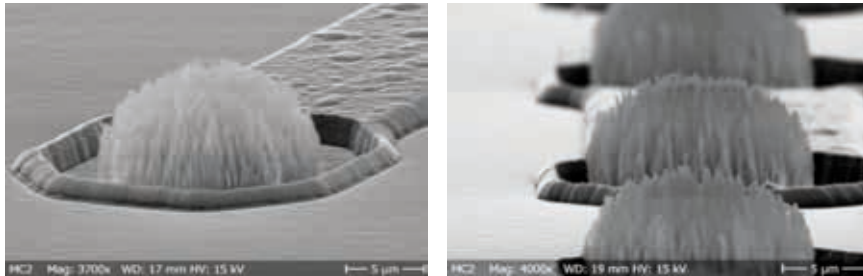
A number of studies find that CNF's can reduce the Coefficient of Thermal Expansion (CTE) of solder when embedded in the solder<sup>[2,5,6,7]</sup>. Commonly used SAC solders can have CTEs ranging from 16.7 to 26 ppm/°C<sup>[3]</sup> whereas the CTE of the adjoining silicon can range from 3 ppm/°C to 8 ppm/°C creating a mismatch which can cause solder joint cracking over time and thermal cycling. The effect of this mismatch as the solder volume is reduced raises the probability of joint failure significantly.

CNFs have the ability to bond with solder while still remaining rooted on the IC pads enabling them build composite materials, which take advantage of their

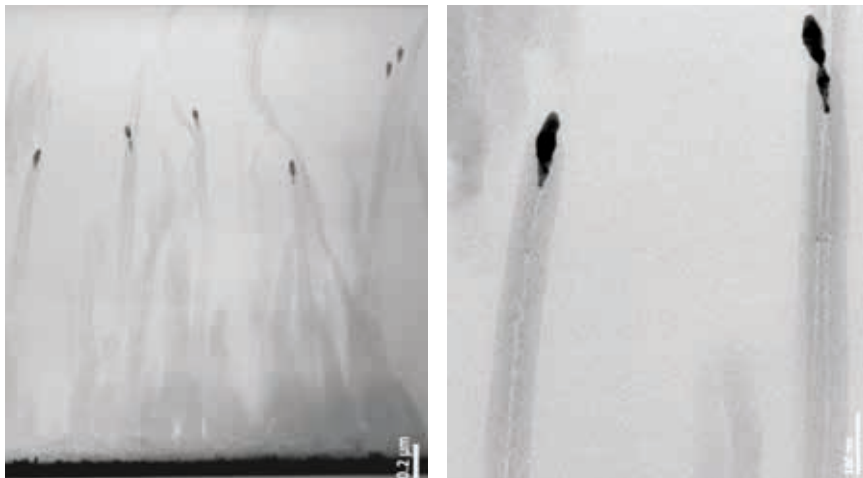
## Plasma Enhanced CVD System



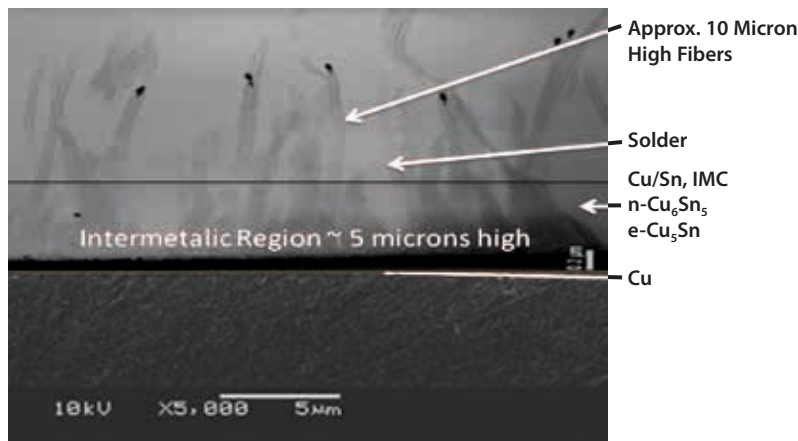
**Figure 2. Diagram of a Plasma Enhanced Chemical Vapor Deposition System.** (Source: Dow Corning Corporation)



**Figure 3. A forest of CNFs rooted to a metal IC bond pad. The pad size is approximately 20 $\mu\text{m}$  x 20  $\mu\text{m}$ . An individual CNF is approximately 30 $\mu\text{m}$  in diameter and 10 to 15 $\mu\text{m}$  in height (Source: Smoltek)**



**Figure 4. Cross sectional view of CNFs rooted in a metal pad and wetted with solder. The dark area is the catalytic metal particle and the lighter area is the attached CNF. (Source: Smoltek)**



**Figure 5. Simulated picture showing the fiber “trees” extending above the weak intermetallic region of the typical solder joint. This forms a stronger solder joint analogous to embedding rebar rods in concrete fabrication. (Sources: Smoltek, PPM Associates, and [http://wings.buffalo.edu/academic/department/eng/mae/cmrll/Carbon\\_fiber\\_reinforced\\_tin-lead\\_alloy\\_as\\_a\\_low\\_thermal.pdf](http://wings.buffalo.edu/academic/department/eng/mae/cmrll/Carbon_fiber_reinforced_tin-lead_alloy_as_a_low_thermal.pdf))**

high (TPa) young modulus to provide robust joints between two chips or chips to package<sup>[4,5]</sup>. Smoltek’s studies show that CNFs wet many of the commonly used IC assembly solders, such as Indium IN 290, remarkably well leaving hardly

any voids at the fiber/CNF interface and forming a composite joint with lower CTE than the solder itself, since VACNF have hardly any CTE.

As shown in the simulated picture of the CNFs, solder, and the intermetallic

region of the solder (see Figure 5). Further, the wettability of the CNF to the solder could prevent the solder from wicking out and away from the pads, thus reducing the number of solder shorts that occur as the solder pad-pad pitch gets smaller.

The length of the rooted CNF is solely determined by the CVD growth process. Fibers as long as tens of micrometers are routinely grown at Smoltek. Such length make it possible to enhanced the reliability of the fiber to solder joint, since fibers could be longer than the intermetallic region on the solder to pad interface.

All the above features of the CNF/solder composites make them very promising for Nano-scale interconnects with improved reliability. In a study conducted by Ho and Chung found an 87% increase in thermal fatigue life by creating a 29% by volume mixture of CNFs and solder<sup>[2]</sup>.

## Summary

As solder joints get smaller their reliability and fatigue life drops. Adding carbon nano fibers, CNFs, and combining with the solder significantly enhances the fatigue life of the solder joints. ♦

## First Author

Vincent Desmaris received a MSc in Material Science from the Institute of Applied Science, Lyon France (1999). He received a PhD in EE from Chalmers University of Technology, Gothenburg, Sweden (2006).

In 2007 he joined Smoltek AB, where he now is the CTO. His main interests are the development and modeling of devices, components and prospective technologic solutions for the microelectronics industry, based on Carbon Nanofibers (CNF).

Since 2013, Vincent Desmaris is also an associate professor at Chalmers University of Technology in the field of THz technology and microwave electronics. His research deals with radio-astronomy instrumentation and superconducting electronics.

Vincent Desmaris is author or inventor of more than 60 articles and patents.

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*CarbonBump™ is a Trademark of Smoltek AB Gothenburg, Sweden.*

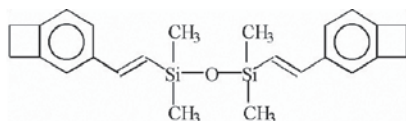
# Benzocyclobutene (BCB)... the Early Years

Dr. Philip Garrou  
Microelectronic Consultants of NC

*THERE ARE VERY FEW POLYMERIC materials that have made significant impact on the microelectronics industry. It's been a little over 20 years since one of them, BCB, began its commercial path at Dow Chemical. Lets take a look back at some of that early BCB history.*

## BCB the Early Days...

The earliest Dow Chemical R&D on BCB chemistry was conducted in 1980 by Dr. Bob Kirchoff. In the early 1980's Dow studied various derivatives of the BCB molecule under a Wright Patterson Air Force contract focused on advanced thermoset resins for use as aerospace composites. Alan Schrock was the first to synthesize divinylsiloxanebisBCB monomer, 1, precursor to the commercial BCB resin.



1

Dow Chemical has over 100 US patents assigned to it concerning various compositions of and applications for benzocyclobutenes, BCB's. There have been more than 1000 BCB publications in the microelectronics literature since our initial publication in 1990<sup>[1]</sup>.

In 1986, Don Dix, with the support of R&D Director Robert Nowak, moved the materials development program into his newly created "Electronics Business Unit". Enough customer interest was generated by 1992 to commercialize the dry etch resin (Cyclotene™ 3000 series) followed by the photosensitive version (Cyclotene™ 4000 series) in 1994.

In order to develop processes and applications, joint development programs

were initiated with Iwona Turlik at the Microelectronics Center of NC (MCNC) in RTP NC (1993), Herbert Reichl at the Fraunhofer, Berlin (1993) and Eric Beyne at IMEC in Belgium (1994). From 1993–1996 Dow field engineers trained with Boyd Rogers and myself at MCNC and developed the photo BCB thin film process<sup>[2-3]</sup>.

Young graduate student Michael Toepper, joined the BCB process development team at Fraunhofer IZM Berlin in 1994 and initiated the first work on photo BCB/Cu WLCSP and redistribution.

## BCB Applications

### MCM's

Early application development in the 1990's concentrated on MCM technology<sup>[4]</sup> which today are known as "System in Package" (SiP).

In 1995-1997 a joint development program with MicroModule Systems (MMS) developed a qualified copper / BCB process which was commercialized by Intel as the Twinstar™, (Figure 1), a dual Pentium module used in commercial servers<sup>[5]</sup>.

During this period Dow and MMS also led a DARPA consortium for "Intelligent Large Area Processing", CILAP. Flat panel display equipment was modified and used to generate thin film modules on

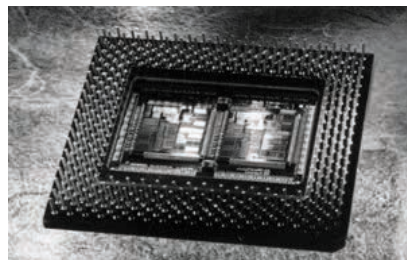


Figure 1. MMS Twinstar™ MCM.

350 mm format as shown in Figure 2<sup>[6]</sup>. This can be considered the forefather of today's attempts to build 2.5D interposers on large area glass panels.



Figure 2. Large Area Processing.

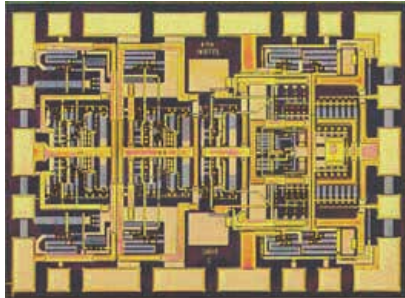
In 2000 Strand in Sweden, developed a BCB process to fabricate a two chip module for Infineon. Several million of these parts were fabricated and used in Infineon TV's<sup>[7]</sup>.



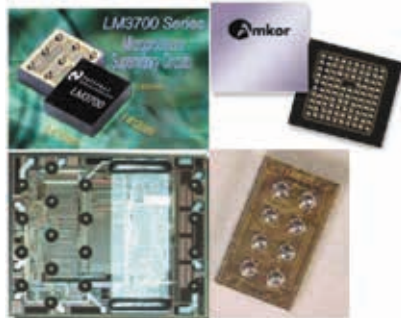
Figure 3. Infineon / Strand MCM.

## GaAs Applications

BCB has also been used extensively as a dielectric in compound semiconductor fabrication<sup>[8]</sup>. TriQuint first detailed the commercial use of BCB to fabricate GaAs chips with multilevel interconnect in 1994<sup>[9]</sup>. Nortel used this technology commercially in the 10 GHz OC-192 optical switch chips such as the Amplifier chip shown in Figure 4.



**Figure 4. Nortel 10 GHz OC-192HBT ACG Amplifier chip.**



**Figure 5. BCB bump/WLP (clockwise) National Semi Supervisory Circuit, Amkor WLP, Atmel EEPROM, Dallas Semi Battery Controller.**

## Bumping and Wafer level Packaging

The most active application for BCB has been bumping and wafer level packaging (WLP) assembly<sup>[10,11]</sup>. In the mid 1990's the industry was determining whether bumping technology, could become a more widespread packaging / assembly technology. At a meeting sponsored by MCNC in late 1994, MCNC described their BCB based redistribution and passivation technology and convinced Delco's Mike Varneau and others that BCB was the dielectric of choice for this application.

MCNC soon after spun out Unitive Corp and Delco entered into a JV with K&S to form Flip Chip Technologies (today known as FCI). Although the Uni-

versity and FCT technologies developed down different paths (i.e. FCT screen printed solder vs Unitive plated solder) their common choice of BCB as the dielectric for bumping and later wafer level packaging influenced the merchant industry at global accounts such as Amkor, ASE, Siliconware, STATChip-PAC, National Semiconductor and many others. At one point it was estimated that BCB controlled ~ 75% of this expanding bumping and WLP market space.

## High Density Interposers

From 1995 to 2001 Dow, MCNC, Cray, IDT and the Len Schaper group at the University of Arkansas participated in a DARPA program entitled "Seamless High Off Chip Connectivity" (SHOCC). This was an early system-in-a-package approach to fabricate complex chips from simpler, smaller pieces using a high density interconnect substrate and high density flip chip bumping technology. BCB was used in top level routing of the HD substrate and in the 100  $\mu\text{m}$  bump

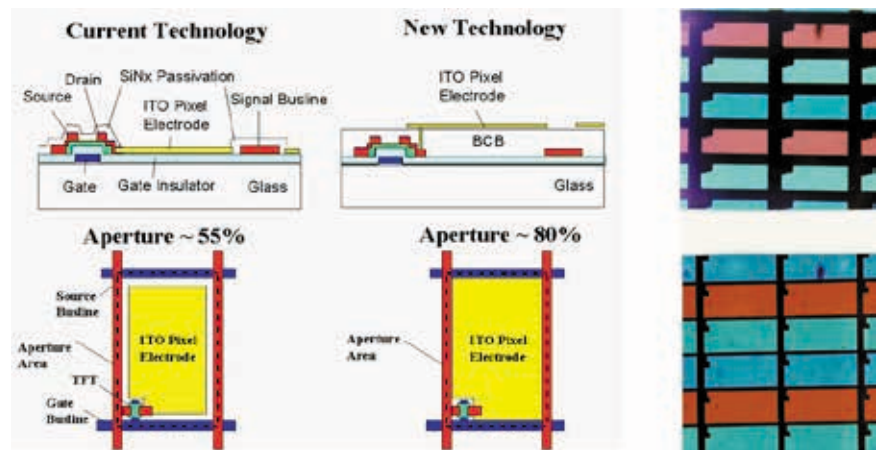
pitch process as the passivation layer<sup>[12]</sup>.

## Active Matrix Flat Panel Displays

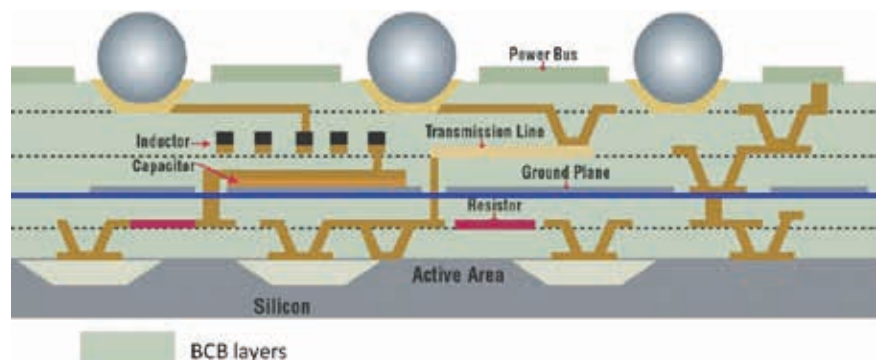
LG Phillips developed and commercialized "high aperture" technology based on BCB planarization properties in the late 1990's<sup>[13]</sup>. This technology imparts higher brightness and lower power consumption to lap top displays by planarizing the transistor and bus structures and allowing the ITO conductive layer to overlap as shown in figure 6.

## Rf Devices and Passive Integration

Low-K, compatibility with copper and low moisture uptake made BCB a natural choice for high frequency Rf devices. Beyne and co-workers at IMEC<sup>[14]</sup> have detailed the processes and designs used to fabricate thin film BCB based passive devices as sand alone components or on top of chips, i.e. post passivation processing, shown in figure 7 below. Such technology has been commercialized by ST Micro, Freescale and many others.



**Figure 6. LG/Phillips "High Aperture" AMLCD Technology.**



**Figure 7. "Post Passivation Processing" - fabrication of R, C and L on top of IC.**

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## Conclusions

Following the commercialization of BCB in 1992 -1994 rapid expansion of commercial applications occurred. 20 years later BCB has become one of the standard materials used in a variety of microelectronic applications. ♦

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## Cost-Competitive Conductive Die Attach Film Breakthrough Material Enables Cost-Effective Laminate Packages

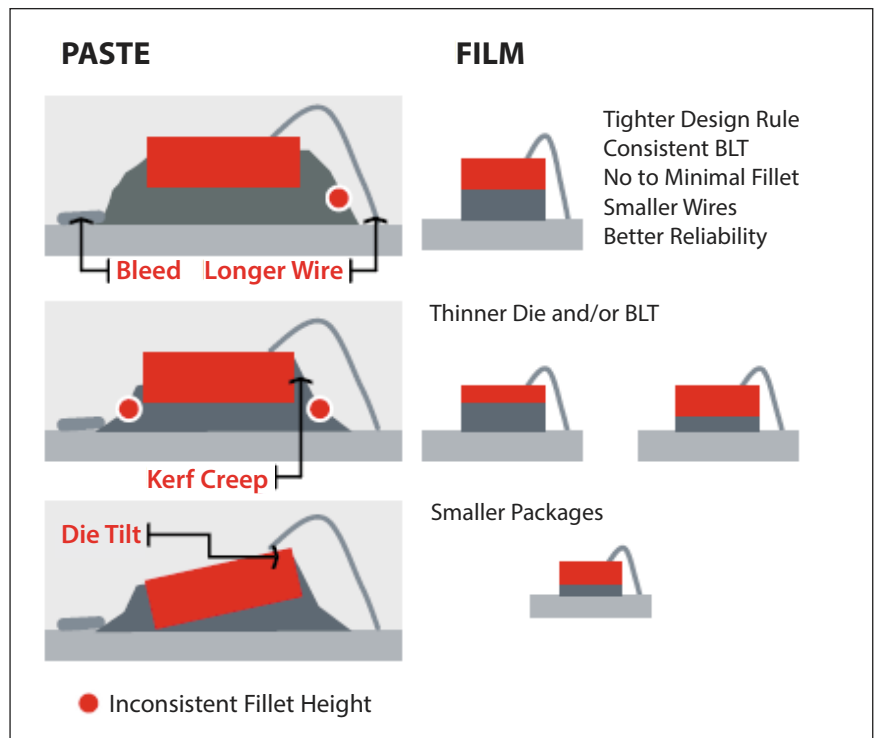
Shashi Gupta  
Henkel Electronic Materials, LLC

SINCE ITS INTRODUCTION IN 2010, when Henkel developed the market's first-ever conductive die attach film (cDAF), the semiconductor packaging industry has readily embraced the technology as a cost-effective and, in many cases, superior performance alternative to traditional paste-based die attach materials. With the formulation of LOCTITE ABLESTIK CDF 200, Henkel broke new ground in the packaging sector and has steadily innovated new cDAF materials, expanding on the initial development with the addition of LOCTITE ABLESTIK CDF 500P and LOCTITE CDF 800P to the portfolio.

Each material was designed with specific performance and manufacturing needs in mind, but all of them offer the undisputed advantages of film over paste, including:

- Design flexibility and ability to integrate more die per package due to tight clearance between the die and die pad
- Enables thinner packages with higher densities
- Facilitates thin wafer handling
- Provides for a clean process with no bleed, uniform bondlines and no kerf creep

To date, Henkel's cDAF material development has centered on solutions for leadframe packages – and to overwhelming market acceptance. Now, Henkel brings the unmatched benefits of cDAF to manufacturers of laminate-based devices and does so cost-competitively. LOCTITE ABLESTIK CDF 600P is the industry's first cDAF material designed for use with many of

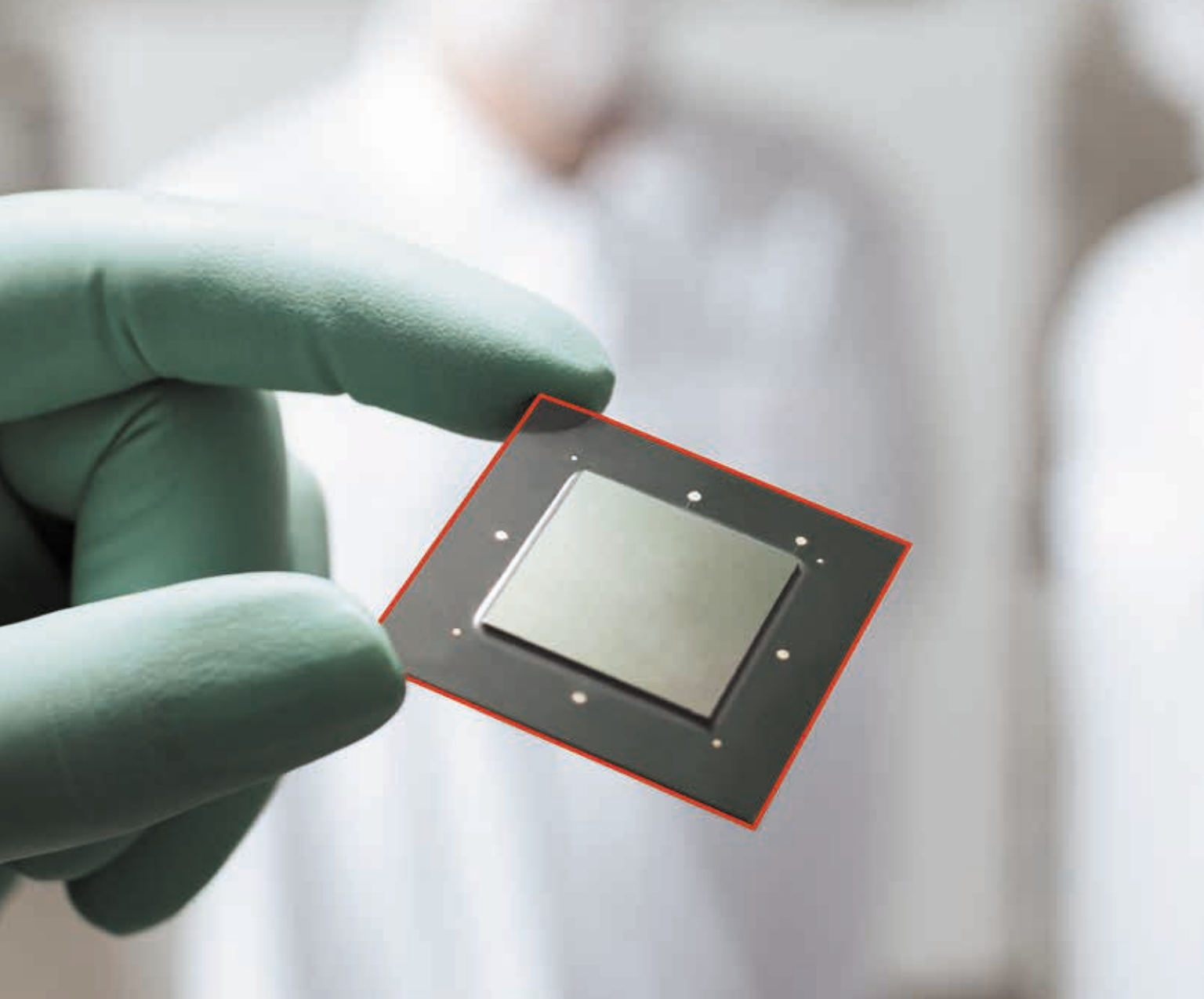


today's laminate packages. In addition to the above-mentioned advantages, cDAF can also offer overall cost reduction benefits for laminate device manufacturers. Because many of these packages are more expensive to produce, incorporating gold wire interconnects, cDAF's ability to streamline design rules and tighten the die to pad ratio means packaging specialist can achieve results as good as or better than that of paste and at lower cost.

LOCTITE ABLESTIK CDF 600P has been formulated for use on large die, laminate-based LGA and PBGA applications. The material – which is priced competitively – has shown excellent

performance and MSL 2 capability on die sizes that range from 1 mm x 1 mm up to 10 mm x 10 mm. This wide range of die sizes offers package manufacturers extreme flexibility, allowing the sourcing of a single material for multiple package configurations. With electrical and thermal conductivity that is comparable to commercialized paste materials used in similar applications, LOCTITE ABLESTIK CDF 600P now affords laminate-based package designers and manufacturers a cost-effective, high-performance and design-rich alternative to die attach

continued on page 28 ▶



## The smaller the device - the more solutions

No matter where you are or what your process requires, you can count on Henkel's expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel's world-class global team ensures your success and guarantees a low-risk partnership proposition.

▶ continued from page 30

bond product was developed for room temperature mechanical debonding that addresses industry issues and is now available. It features tunable film thickness, low total thickness variation (TTV) for surfaces ranging from low topography to Cu Pillars to C4 bumps, and is extendable to fine pitch TSV applications. Additionally, short cycle time for depositing and curing coupled with rapid, simple, and clean mechanical debonding results in a lower COO.

Lastly, to address the fine-pitch, tight-space, thermal processing issues for underfill steps in Cu pillar and TSV applications, non-conductive films (also known as pre-applied underfill) are in development. They are showing promise for void-free bonding, good joint forma-

tion, and no filler entrapment for high reliability and yield.

**Conclusion**

While suppliers clearly stand ready to handle the material challenges of MCI, we do believe the packaging world would benefit overall from more industry consensus on technology, logistics and supply chain solutions to packaging problems with input from the entire industry. It would also benefit from more clearly defined roles for the foundries and OSATs. Unlike semiconductor processes, there are a vast number of packaging technologies with very few standards defining them. It's a delicate balance between commoditizing packaging and allowing for a broader coordinated effort to solve issues while still leaving room for differentiation for packagers,

materials and equipment manufacturers. Fortunately, ongoing collaboration with industry partners is resulting in better materials and better solutions for MCI challenges that are available on the market today. ♦

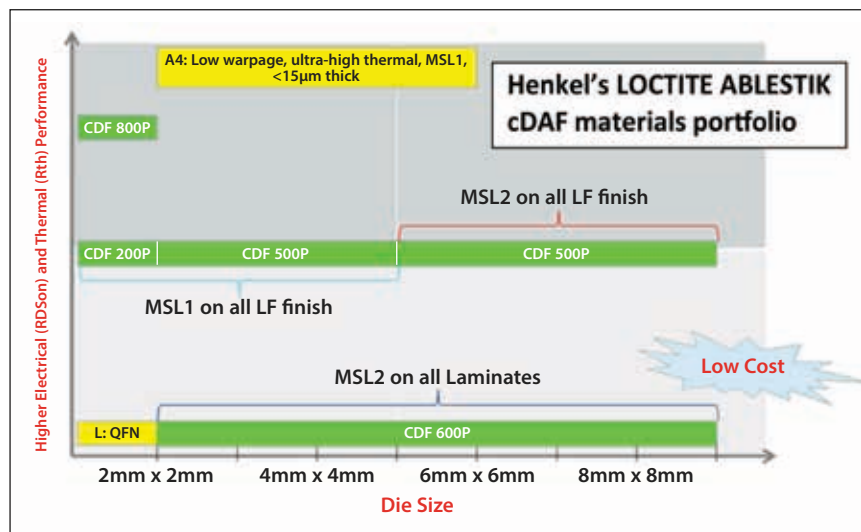
*BHAVESH MUNI is currently Global Business Director for Advanced Packaging Polymers for Dow Electronic Materials, where he is focused on sales and business development of lithography, dielectric and assembly materials for advanced semiconductor packaging. Bhavesh can be reached at [bmuni@dow.com](mailto:bmuni@dow.com). For more information about Dow Electronic Materials, visit their website at [www.dowelectronicmaterials.com](http://www.dowelectronicmaterials.com).*



▶ continued from page 26

paste. Lower stress and high adhesion are also critical characteristics of the new cDAF and facilitate production of larger die sizes that are particularly susceptible to stress and warpage.

Like the other Henkel cDAF materials, LOCTITE ABLESTIK CDF 600P is a two-in-one, pre-cut dicing die attach conductive film that combines dicing tape and die attach material into single 8" or 12" wafer-sized film formats. The material is compatible with most lamination equipment used in the field and has shown good results with lamination temperatures as low as 65°C. The two-in-one construction also helps reduce cost by enabling an in-line process for thinner wafers and a single lamination process in one, combined step. Compatible with various substrates including Cu, Ag spot and NiPdAu, LOCTITE ABLESTIK CDF 600P can be used with wafers thinner than 75µm and has an architecture that has been designed to provide excellent wetting for the unique topology of laminate substrates.



The undisputed performance and processing advantages of cDAF are now available for laminate package manufacturers in an exceptionally cost-effective formula. Henkel's complete portfolio of cDAF materials capability now spans a broad spectrum of package type, die sizes and cost/performance ratios.

For more information on Henkel's

complete portfolio of cDAF materials or to find out more about the company's new laminate-compatible film, LOCTITE ABLESTIK CDF 600P, log onto [www.henkel.com/electronics](http://www.henkel.com/electronics), send an e-mail to [electronics@henkel.com](mailto:electronics@henkel.com) or call 1-888-943-6535 in the Americas, +44 1442 278 000 in Europe and +86 21 3898 4800 in Asia. ♦

▶ continued from page 16

tist”) for a materials science exploration. Last I heard these youngsters were busily fast-tracking into powerful R&D, project engineering and Management positions. I cannot take any credit for their technical capabilities and success, but I did help a bit, and might have shown them that mil/aero engineering is not just a hive of grey-cube dwellers, but an opportunity for excitement!

### Workshops, QC Workmanship

Another task, actually not unpleasant, was to review quality management in a series of site-wide workshops. These were targeted to folks involved in design, procurement, manufacturing, and quality control of electronics components, especially the newest technologies in the Programs as well as in the support divisions.

Most electronics being deployed in the early 2000s were designed in the late 80s, with robust military-approved proven technologies. These were therefore bulky, heavy, and relatively stupid, compared to the smart electronics spawned by newer consumer communication/recording devices. My task was to offer new component styles and new circuit board designs to our designers, to help enable next-generation, smart, mil/aero electronics.

I reviewed the important attributes, identified the consequences (performance and reliability) of deviations from nominal conditions, offered accept/reject thresholds, and suggested referee protocols for borderline cases. Many of these specifics were tentative and arbitrary; revisions and fine-tuning were ongoing, as we got into these now technologies. Many presentations covered revisions, case histories, customer feedback, etc. Some sessions were in auditoriums; others were out on the shop floor, pro-

viding hands-on engagement and even participation in samplings, inspections, and decision-making. Communication within Lockheed as well as with our suppliers and sub-contractors was crucial. I enjoyed being part of that.

### Lead-Free Soldering

Elimination of lead became a powerful driving force in the 1990s, because of environmental/health concerns. The European Union in 2003 formalized these concerns by enacting the ROHS (Restriction of Hazardous Substances) directive. The outside commercial/industrial electronics world (using 95% of all solders) began a scramble to replace conventional tin-lead solders with some sort of soldering alloy that was “lead-free”.

Early tests of various lead-free solders demonstrated profoundly disadvantageous processing requirements and wretched long-term reliability. Another more cynical trigger for the commercial world’s lead-free activity was to gain market advantage by offering a “green” product, which would sell better into a consumer marketplace. The mil-aero industry violently resisted the trend and the legislation. The reason: the standard solder (Sn63) is a eutectic blend of 63% tin and 37% lead. This solder melts nicely at 218C, wets properly, is widely available and specified rigidly within the industry, functions at the heart of all microelectronics computing devices, has all the printing, hand-soldering, board-fab, and processing equipment built around it; and most importantly has decades of reliability data and qualification documentation backing up ALL military/space and high-reliability industrial systems on earth. The mil/aero community was comfortable with this situation.

Further, mil-aero represents only a tiny fraction of solder supply world wide; so maintaining a supply-chain of a tiny

obsolete solder formulation (Sn63 becoming problematic. The outside world recognized the severe environmental health danger of lead and was going ahead in directions that would make Sn63 obsolete. My role, from the vantage point of real-world exposure (going to electronics trade shows and hearing presentations by electronics visionaries), was to try to warn L-M designers that lead-free solder was coming (despite certain exemptions), throughout the supply chain and would severely impact mil/aero reliability considerations. I made local presentations and offered defensive development plans. I believe I stirred up some appropriate discussion and action. ♦

*Tom Clifford, one of nine kids, was born in Texas in 1940 into a heritage of academics and engineering. The family followed Daddy across New Mexico as he helped create wartime infrastructure with the Corps of Engineers. With his BS in ChE in 1963, Tom helped the birth of space travel (Gemini at McDonnell; Space Shuttle at UTC; satellites at Lockheed); the development of microelectronics (stints in Silicon Valley), and “green” initiatives (eliminating of asbestos, lead and ODC solvents), as well as developing OSHA-safe manufacturing processes. He was a research, design, process and manufacturing engineer, and later an R&D and operations manager and consultant, enjoying every minute. He has accumulated many patents and publications, and particularly treasures his mentoring of young engineers, helping them on to successful careers. Retired, he now enjoys kayaking, fishing, hiking, photography (often from his wife’s aerobatic airplane), world travel and family. ♦*

## MEPTEC Symposium Proceedings on CD





# Material Supplier Challenges for Multi-Die Integration

*Bhavesh Muni, Global Business Director  
Dow Electronic Materials  
Advanced Packaging Technologies*

FOR MANY YEARS, CMOS SCALING has been the name of the game as shrinking line geometries and increased wafer sizes have enabled the semiconductor industry to drive down the cost per transistor. But, these two variables are running out of steam. Industry idealists consider that the ultimate solution for any application is the single chip. But sometimes, the single chip solution is not the lowest cost or even the most reliable or best quality solution. Going forward, there are other capabilities that can be used to allow the industry to continue lowering the cost per transistor. One trend that is emerging today is multi-die integration (MDI), which enables us to pack more and more transistors in a package as opposed to on the chip.

Packaging experts say that advanced packaging technologies are the next frontier for innovation, as chips find their way into multitudes of unconventional applications including those that touch everyday lives like medical, consumer, automotive etc. The electronics market sector is increasingly driven by consumer spending, where electronic products require more than just performance and speed. Product look-and-feel, functionality, time-to-market, and cost are critical factors, and packaging plays a major role in delivering solutions to meet these needs.

In particular, the explosion of smartphones and tablet computers, automotive electronics, and the emerging Internet of Things (IoT) market is strongly driving the need for further high-volume, high-speed, low-power-consumption large-scale integrated circuits (LSIs), and smaller/thinner semiconductor packages. Meanwhile, the technical challenge involved in furthering fine-pitch-design is shifting the focus to assembly technology, which is becoming the core technol-

ogy required to achieve high-volume, high-integration semiconductor packages.

“Multi-die integration” is a catch-all term that encompasses advanced packaging technologies from 2D heterogeneous system-in-package (SiP) integration, to package-on-package (PoP) stacks, 2.5D and 3D interposers, and 3D stacked ICs (3D ICs) enabled by through silicon via (TSV) interconnects. Which technology gets designed into a given device depends on the I/O density requirements for the target application, and the performance gain weighed against the cost-of-ownership of legacy technologies already in place. Due to the needs of the aforementioned consumer electronics growth, I/O density requirements are expected to grow rapidly in the next few years.

While package stacking is expected to plateau, parallel opportunities are emerging in wafer-level thick-film based technologies like fan-in and fan-out (FOWLP), reconstituted wafers, and organic interposers, with the highest available density options at Si-level TSV. In particular, we’ve seen great success in FOWLP as an alternative package that, unlike 3D TSV technologies, can deliver the required performance without increasing the cost or adding complexities to the supply chain.

The value proposition all these technologies have over system-on-chip (SoC) integration is not only the ability to pack in more transistors, but the ability to cost-effectively integrate disparate technologies into one package, thereby satisfying performance, form factor, and power requirements. As such, it is expected that all of these will continue to coexist. The primary challenge this poses to the material supplier is supporting such a wide range of process requirements.

MDI involves six or seven key

materials that fall into three categories: metallization, photodielectrics/resists and bonding/assembly materials. Specifically, key challenges for MDI include thin wafer stress management, void-free filling of high-aspect ratio (HAR) TSVs, temporary bond/debond processes for thin wafer handling, metallization and underfill process steps for fine-pitch bumps and thermal management. Additionally, cost-of-ownership has been a major issue. The good news is that industry leaders have recognized these challenges, and partnerships between foundries, OSATS, research institutes, materials suppliers and equipment suppliers have been formed to take on the challenges. In this collaborative environment, many companies have successfully developed enabling new products that are tailored for these applications.

For example, to address challenges facing Cu TSV interposer and via middle applications, the ideal material must feature fast filling times and low Cu overburden, which translates to lower cost of ownership (COO). Additionally, it must achieve a void-free deposit with low defects and high purity for improved reliability and yield.

One of the single most significant bottlenecks in 3D IC manufacturing is the temporary bond/debond (TB/DB) process for thin wafer handling, due to the inability of adhesive materials to meet all of the requirements set forth by manufacturers. Up until a year ago, there were multiple approaches for TB/DB, but today the industry is settling on room temperature mechanical or laser debonding to achieve the preeminent yield at the lowest COO. Again, through collaboration, tremendous progress has been made in this area, and now a temporary wafer

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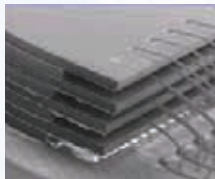
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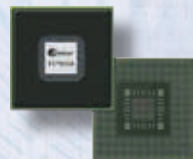


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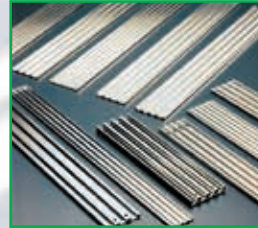
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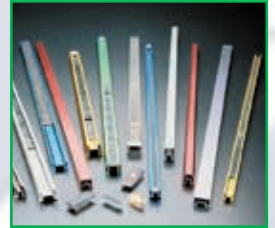
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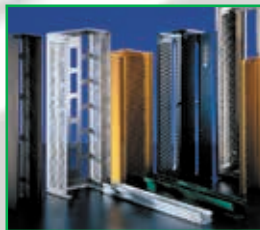
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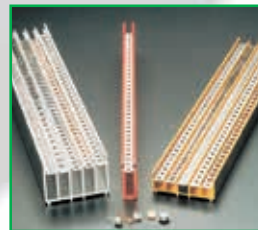
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