MEPTEC Report

WINTER 2014

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 18, Number 4

2015

LOOKING AHEAD...

- 13th Annual MEPTEC MEMS Technology Symposium
- First Annual IOT Online/MEPTEC Internet of Things Symposium
- iNEMI/MEPTEC/SMTA Medical Electronics Symposium 2015
- 2015 MEPTEC Packaging, Assembly & Test Symposium
- and More...

+

SPECIAL REPORT:

CHINA'S IMPACT ON THE SEMICONDUCTOR INDUSTRY 2014 UPDATE

page 19

MEPTEC MEMBER COMPANY PROFILE

Founded in 1972, Carsem is a leading provider of turnkey packaging and test services to the semiconductor industry, offering one of the largest package and test portfolios in the world.

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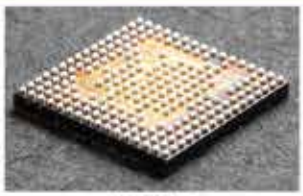
INSIDE THIS ISSUE

ASE GROUP

IC Packaging & Test for the next big thing in electronics.


Copper Pillar


MEMS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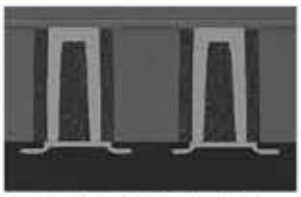
2.5D/3D/TSV


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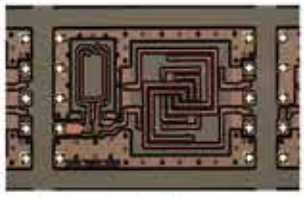
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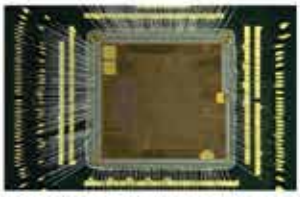
Copper Wire Bond

With a proven track record spanning three decades, ASE continues its tradition of dedication and commitment through close collaboration with customers, suppliers and partners, alike. Alongside a broad portfolio of established technologies, ASE is delivering advanced packaging and SiP solutions to meet growth momentum across a broad range of emerging applications and end markets.

For more: www.aseglobal.com

Pushing the Limits of Packaging Design and Manufacturing in a Post Moore's Law World

Ivor Barber
Xilinx, Inc.

ON THURSDAY OCTOBER 23RD MEPTEC held its annual Packaging Symposium at the Biltmore Hotel in Santa Clara. In the Post Moore's Law World, packaging Engineers around the globe are stepping up to take on the challenge of delivering more functionality per unit area at lower cost. Appropriately the Symposium was titled *Pushing the Limits in Packaging Design and Manufacturing*.

The first session, *Wafer Fab, Packaging, and Test – Supply Chain Coordination as a Critical Capability,* was led by Phil Marcoux. Jim Walker of Gartner's talk, *Morphing the Semiconductor Outsourcing's Business Model: Wafer Level Packaging,* set the scene suggesting that current business models are outdated and there is a need for vertically integrated outsourced models. The increasing capital investment required for new packaging technologies will drive a greater reliance on R&D partnerships, consolidation of fabless and IDM companies and drive foundry manufacturing to be more cost-competitive. Wafer Level Packaging is a disruptive force and a driver for the vertically integrated outsourced model. The following sessions underlined these changes in thinking as James G. Gandenberger, Vice President of Worldwide Operations & Foundry Business Unit, Micrel, Inc. gave an extraordinarily detailed account of his daily visibility into his many outsourced manufacturing partners, while Ariel Meyuhas, COO, The MAX Group proposed bringing foundry Supply Chain Benchmarking techniques into the Packaging world.

John Xie's session titled *Design Considerations for Advanced Package Development* brought the attendees back into the packaging world but continued the theme of integration. James Church, a solutions architect at Zuken's R&D center demonstrated with exciting animation Zuken's tools for Optimizing Product Cost and Performance with System-level 3D Chip, Package, Board Co-design. Jenny Jiang, Principal Engineer of SIPI, Altera Corporation continued this theme of integration from a pure SI perspective while Herb Reiter, Founder, eda2asic Consulting, Inc. addressed the question: Will IoT (Internet of Things) Drive 2.5/3D IC Revenue Growth and Change our Lives? With more than a simple "Yes". Herb's sumptuously illustrated presentation also featured multiple resources for IOT research and development, backing his assertion that the technologies and the partnerships are in place to launch IOT.

Tim Olsen, Founder & CTO, Deca Technologies gave a Keynote titled *Transforming Electronic Interconnect* which tied together some of the themes of the conference – the blurring of lines in supply chain as SATS have extend themselves into the domain of wafer fab processing while foundries extend their reach into the classic domain of SATs. Tim cited fan-out wafer level packaging (FO-WLP) as a key building block for 2.5D and 3D architectures of the future while challenging traditional supply chain boundaries. These techniques can merge disparate silicon nodes and technologies in a format that combines wafer processing with assembly techniques.

Joel Camarda's session, *Pushing the Envelope on IC Package Manufacturing*, provided insights into activities of packaging engineers at distant points in the packaging spectrum from Jenny England's introduction of Henkel's silver sintering for power device cooling to Ivy Qin of Kulicke & Soffa's highlighting of continued advancement and innovation in wire bonding technologies. Jay Hayes, Director of Business Development – Bumping & Flip Chip at Unisem provided a historical perspective of flip chip bumping before detailing advances in die interconnect including Cu RDL, plated solders and copper pillar bump. Ed Binkley, CTO of Promex Industries summarized the characteristics of Medical Device manufacturing including tight regulatory oversight, lifetime BoM and process documentation, demanding layout size control, mixed assembly processes and a longer time to market, all of which is typically rewarded with a long, stable product life.

The Final Session co-chaired by Jeff Demmin of STATSChipPAC and myself was titled *Enabling Multi-Die Packaging as a Mainstream Solution* and featured speakers with diverse multi die applications. Frank Juskey, Senior Member of the Technical Staff, Advanced Technology Development Group, TriQuint Semiconductor presented the challenges of building RF multi-chip modules. Frank showed how developments in low cost flip chip, low cost Cu Pillar bumping and the development of the 01005 passive SMT components drove corresponding developments in precision and throughput of SMT chip placement equipment resulting in lower manufacturing cost. Terry Kang, Sr. Packaging Development Manager, NVIDIA addressed the package design, material and assembly process development challenges NVIDIA faced in developing MCM's to meet the performance and reliability test conditions for automotive applications. The final speaker of the day, Tom Gregorich, VP of Package Technology at Micron, modeled the integration of memory and logic in high-performance systems. Five different levels of integration of logic/memory systems were modeled. Tom's presentation showed that system power reduction through integration were not enough to offset increased thermal challenges with die stacking and proximity of memory to high-powered logic. Clearly higher Tj memory and innovative cooling techniques are required.

Once again the MEPTEC organization delivered a roster of speakers and topics which reflected the dynamic developments and challenges relevant to semiconductor packaging and test professionals in Silicon Valley. The conference themes of changing outsourcing models and continued development of strategies for device integration will continue to shape our profession as we push the limits of Packaging Design and Manufacturing in the post Moore's Law, IOT world. ◆

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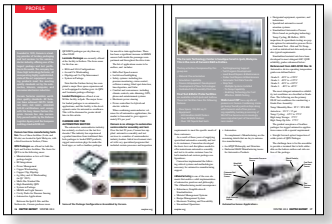
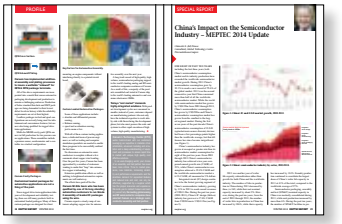
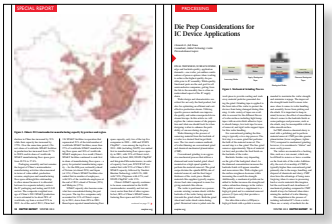
ON THE COVER

In 2015 MEPTEC brings back its popular annual events and adds another. In May our MEMS Technology symposium is in its 13th year, and a new alliance with IoT Magazine will present the First Annual Internet of Things Technology Symposium, to be co-located with the MEMS event in San Jose. Our successful Medical Electronics event will again be held in Portland in September. As always we will end the year with our annual Packaging, Assembly and Test symposium, to be held in November.







MEPTEC

THE NEXT GENERATION

The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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Editor Bette Cooper
Art Director/Designer Gary Brown
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STATS ChipPAC Announces Plan to Relocate China Manufacturing Operation

STATS CHIPPAC LTD., a leading provider of advanced semiconductor packaging and test services, has announced its plan to relocate the Company's wholly-owned subsidiary, STATS ChipPAC Shanghai, Co., Ltd. ("SCC") to a new manufacturing site in China.

SCC is a 983,000 square foot packaging and test operation located at No. 188 Huaxugong Road, Xujing Town, Shanghai, People's Republic of China (PRC). Recent changes in the long term zoning, development and construction plans for the West Hongqiao area of China have resulted in the need to relocate SCC by the end of 2017. STATS ChipPAC will be working with the Qingpu Land Planning Bureau, the Qingpu District Land Reserve Center and the Shanghai Qingpu District Xujing Town House and Land Expropriation Compensation Office to transfer the land currently occupied by SCC to the relevant PRC local authorities and identifying a new location for the manufacturing operation.

"As we work with the local PRC authorities to develop a timeline to relocate SCC, our top priority will be to minimize any potential disruptions for our customers and employees. The relocation of SCC to a new site is expected to take place in late 2017," said Tan Lay Koon, President and Chief Executive Officer, STATS ChipPAC. "Our goal is to select a new location that will be in close proximity to our current site. Once a new site has been identified, we will prepare a carefully phased transition plan with each of our customers to ensure a successful move."

Established in 1994, SCC provides high volume, low cost turnkey solutions encompassing wafer bump, wafer probe, packaging, final test and distribution services. SCC offers a broad portfolio of leaded, laminate, stacked die, memory card and flip chip packages to support multiple customers in the communications, consumer and computing markets.

With global headquarters in Singapore, STATS ChipPAC has design, research and development, manufacturing or customer support offices throughout Asia, the United States and Europe. STATS ChipPAC is listed on the SGX-ST. Further information is available at www.statschippac.com. ◆

Finetech to Strengthen Its Presence in Japan

FINETECH, A GLOBAL SUPPLIER OF high accuracy bonding and advanced rework equipment, has announced the opening of a new Sales and Support Center in Japan. With the creation of Finetech Nippon Co., Ltd, Finetech seeks to strengthen the company's local presence and responsiveness in Japan. This Tokyo location is Finetech's third facility in Asia, adding to the Penang, Malaysia and Shanghai, China locations.

Finetech Nippon will be directed by General Manager Mr. Kotaro Iida who is looking forward to the task: "I am convinced that - with the long years of experience - Finetech is in the position to achieve great things in Japan. Many companies, mainly from the communications sector, are facing demanding laser, VCSEL/PD or FlipChip application challenges during their product development. Supporting them in finding tailor-made and competitive application solutions is an exciting challenge. Other promising markets with lots of potential include the widely developed Japanese education and research landscape, medical technologies, automation and robotics."

Gunter Kürbis, CEO of the Finetech group, also thinks starting a base in Tokyo is the logical next step for this market: "With this new branch we are able to respond immediately to inquiries from Japan - a market which is growing more and more important to us. Also, we can provide better advice to new and existing customers and broaden our service offerings. This complies with our principles of establishing a close and long-term partnership with our customers; an approach which encompasses the joint evaluation of their application, finding a corresponding optimal machine solution and providing continual support."

Finetech develops and manufactures innovative equipment solutions for a variety of micro assembly and SMD rework applications. Due to their modular architecture, the manual, semi-automated and full-automatic systems offer maximum process flexibility. Typical fields of use range from R&D and prototyping to fully-automated production environments with high yield. Corporate headquarters and main production are in Berlin, Germany. Sales and Technical support centers are located in Gilbert, AZ; Manchester, NH; Shanghai, China; Kuala Lumpur, Malaysia and Tokyo, Japan. To learn more about Finetech visit www.finetechusa.com. ◆

AEHR TEST ANNOUNCES CHANGE TO BOARD

Aehr Test Systems has announced that John M. Schneider has joined the Company's Board of Directors, effective December 3, 2014. Mr. Schneider is founder, President and CEO of Private Wealth Advisors. He replaces Mukesh Patel, who has served on the Aehr Test Systems board since 1999 and has resigned for personal reasons. The number of Aehr Test board members remains at seven. *www.aehr.com*

AMKOR LICENSES COPPER PILLAR WAFER BUMP TECHNOLOGY

Amkor Technology, Inc. announced that it has granted GLOBALFOUNDRIES a non-exclusive license to its proprietary copper pillar wafer bump technology. The agreement provides for the transfer of Amkor's copper pillar wafer bump technology to GLOBALFOUNDRIES and a license under Amkor's intellectual property to enable GLOBALFOUNDRIES to bump wafers based on this technology. *www.amkor.com*

ASE RECEIVES 2014 BSI GRC EXEMPLARY AWARD

Advanced Semiconductor Engineering, Inc. has announced that it has received an Exemplary Award at the annual GRC (Governance, Risk and Compliance) management strategy awards event organized by the BSI Group Taiwan. The annual 2014 awards event was held on Dec 11, 2014 in Taipei covering views

and strategies from global leaders in diverse industry segments on the topics of 'Technology Risks' and 'Managing Sustainability'.

The BSI Group, also known as the British Standards Institution, is a business standards company that develops standards and provides its services to companies to improve performance, reduce risk and achieve sustainability.
www.bsigroup.com.tw

CORWIL COMBINES TEST AND ASSEMBLY IN ONE LOCATION

CORWIL Technology now offers assembly and test services to their customers all under one roof. CORWIL has announced the completion of the CORWIL Test Division (CTD) move from their Santa Clara location to the newly remodeled facility located at 1635 McCarthy Boulevard, Milpitas, CA. The building redesign includes the addition of 21,500 sq ft to house the CTD equipment which includes ATE such as Teradyne UltraFlex and Advantest 93K, Seiko Epson Handlers, Accretech & TEL Wafer Probers, Burn-in testing equipment and End-of-Line equipment such as scan, laser mark, tape and reel.
www.corwil.com

EXAR PROMOTES DANIEL WARK TO VP OF WORLDWIDE OPERATIONS

Exar Corporation has announced the promotion of Daniel Wark to the position of Vice President, Worldwide Operations. Mr. Wark succeeds Robert Todd Smathers, who is retiring after three years of

SPIL Orders ACS300 Coater/ Developer-System for Advanced Packaging Applications

SUSS MICROTEC HAS recently received an order for its ACS300 coater/developer tool from SPIL. The ACS300 is a modular cluster system designed to meet manufacturers' needs for clean, reliable and high throughput photolithography applications. The tool will be equipped with new features especially developed for advanced packaging applications.

Established in May 1984, Siliconware Precision Industries Co., Ltd. has become one of the leading providers of comprehensive semiconductor assembly and test services.

For more information visit www.suss.com. ◆

KYOCERA Holds Inauguration Ceremony for New Manufacturing Plant in Vietnam

KYOCERA CORPORATION has announced that it held an inauguration ceremony on December 16 to mark the launch of the company's manufacturing plant in Vietnam. The plant consists of two factory buildings, managed by Kyocera Vietnam Company Limited (herein "KVC") and Kyocera Connector Products Vietnam Company Limited (herein "KCPV").

The Kyocera Group obtained the plant site in 2011 to expand its business and respond to an increasing global demand for components. KVC began production for surface mount ceramic packages in August last year, and KCPV launched production for connectors in November last year. The plant will play a central role in the future development of the Kyocera Group.

For more about Kyocera and its products please visit global.kyocera.com. ◆

Palomar Technologies Announces the Latest in Wedge Bonding Technology: The 9000 Wedge Bonder

PALOMAR TECHNOLOGIES HAS announced the launch of the 9000 Wedge Bonder. The 9000 Wedge Bonder is a high-speed fine wire wedge and ribbon bonder, offering control and flexibility. The 9000 features a large 12"x6" work area and the ability to easily change from a 45-60° wire feed range to 90° deep access. The quality control enabled by the 9000 is unparalleled, with real-time bond monitoring and process control software as well as a robust, low maintenance bond head. With the 9000 there is no need for an expensive bond head change, as the wire clamps are easily replaceable and adjustable.

There are seven strategic components to the 9000 Wedge Bonder that help customers achieve modern wedge bond requirements: large work area, inline factory automation, advanced user control, bond data miner, high-speed wire bonding, wire feed clamp versatility, and high-precision. Palomar Technologies pioneered the first automated fine wire wedge bonders in the 1980s and today carries the technological legacy into the industry's most advanced fine wire wedge bonder on the market.

Palomar Technologies, a former subsidiary of Hughes Aircraft, is the global leader of automated high-accuracy, large work area die attach and wire bond equipment and precision contract assembly services. For more information, visit www.palomartechnologies.com. ◆

Nordson Advanced Technology K.K. Japan Moves to Larger, Customer-Focused Facility

Supports Nordson ASYMTEK, Nordson DAGE, Nordson MARCH, Nordson YESTECH for applications in semiconductor packaging and electronics assembly

NORDSON CORPORATION has announced that Nordson Advanced Technology K.K. Japan has relocated to new, larger facilities in Tokyo to deliver superior sales, service, technical training, and support to its customers in Japan. With an expanded demonstration room, applications lab, and office space, Nordson Advanced Technology K.K. is able to integrate its dispensing and coating, test and inspection, and plasma treatment equipment and expertise to improve the processes and products of electronics manufacturing companies. The move was effective November 25, 2014.

The Advanced Technology group sells and supports the products from several Nordson divisions (Nordson ASYMTEK, Nordson DAGE, Nordson MARCH and Nordson YESTECH) under a unified, in-country management and physical infrastructure to regionalize their products and services to benefit customers, suppliers, and employees. Customers have the flexibility to purchase in Japanese Yen or US dollars.

"We want to deliver high quality services that exceed our customers' expectations," stated Nobuo (Neal) Okuda, general manager, Japan Nordson Advanced Technology K.K. "Bringing together the experts from the different Nordson Advanced Technologies companies will lead to new discoveries for customer solutions."

The address for the new office is: Nordson Advanced Technology K.K., West Tower 17th Floor, TOC Ariake Building, 3-5-7 Ariake Koto-ku, Tokyo 135-0063. For more information contact the office at Tel: +81.3.5762.2801 or email info-jp@nordsonasymtek.com. ◆

Qualcomm Commits to Invest $40 Million into Several Promising Chinese Companies

QUALCOMM INCORPORATED HAS ANNOUNCED THAT IT AND its subsidiaries have committed to invest an aggregate of $40M into four Chinese companies and the China Walden Venture Investments, L.P. fund, which is primarily focused on investing in semiconductor or semiconductor-related companies with business in China. Qualcomm is pleased to announce that 7Invensun, an eye-tracking solution provider; Chukong Technologies, a mobile entertainment platform provider; inPlug, a smart home device/platform solution provider; Unisound, a voice recognition and processing technology provider; and the China Walden Ventures Investment are all expected to be funded through the Company's $150 Million strategic China venture fund that was announced earlier this year.

For more information visit www.qualcommventures.com. ◆

service with Exar and over 35 years of service in the semiconductor industry.
www.exar.com

MOBILE CHIP-MAKER ROCKCHIP SELECTS FORM-FACTOR MEMS PROBE CARD FOR WAFER TESTING OF 28NM APPLICATION PROCESSORS

FormFactor, Inc. has announced that Rockchip, based in Fuzhou, China, has chosen FormFactor's Apollo™ MF100 MEMS probe card for wafer testing of its 28nm generation of application processors. Rockchip is China's leading fabless semiconductor company for mobile internet terminal devices, digital multimedia solutions and wireless communications, as well as application processors used in tablets, mobile phones, and IOT ecosystem products.
www.formfactor.com.
www.rock-chips.com.

SEMI LAUNCHES NEW EUROPEAN MEMS SUMMIT

SEMI has announced the launch of the European MEMS Summit, to be held on 17-18 September 2015 in Milan, Italy. The Summit will address MEMS technologies, manufacturing, applications and time-to-growth. Over the course of the two-day event, more than 20 keynote and invited speakers from the entire supply chain will share their perspectives and latest updates. In addition, a focused industry exhibition will complement the conferences offering with additional networking opportunities.
www.semi.org/european-MEMSSummit

Master Bond's Thermally Conductive, Electrically Insulative One Part Epoxy for Die Attach Applications

FORMULATED FOR DIE attach applications, Master Bond Supreme 3HTND-2DA is a fast curing, high performance one component epoxy system. It cures in 5-10 minutes at 150°C and has unlimited working life at room temperature. It is available in syringes and has a shelf life of 6 months when stored at 40-50°F.

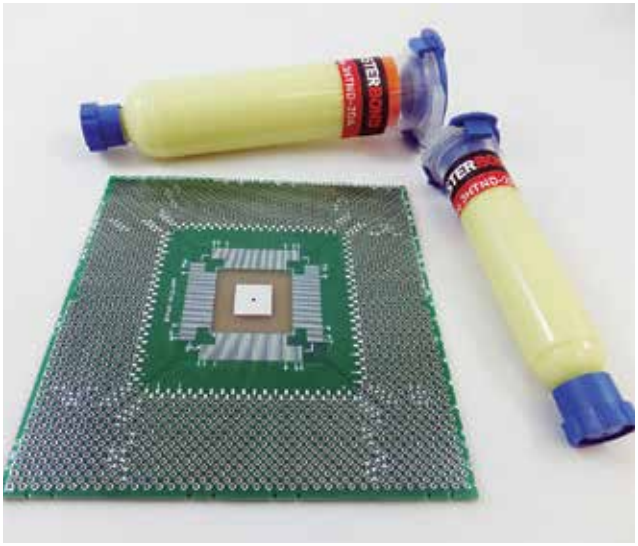
Supreme 3HTND-2DA has a die shear strength of 19-21 kg-f and performed very well in 85/85 testing. This epoxy has excellent adhesion to metals, ceramics and silicon dies. It is serviceable over the wide temperature range of -100°F to+400°F. As a toughened system, it offers the ability to withstand rigorous thermal cycling and shock.

In accordance with die attach application requirements, this product passes NASA low outgassing test specifications. Supreme 3HTND-2DA has low ionics, particularly chlorine (<15 ppm). It also features dimensional stability, superior thermal conductivity, electrical insulation properties and a glass transition temperature of 100-105°C.

Unlike many other die attach systems, Supreme 3HTND-2DA is not premixed and frozen, but it requires refrigeration for storage. This system dispenses smoothly or without any tailing. It well suited for automatic dispensing equipment. With a viscosity of over 300,000 cps (thixotropic), it can be applied to a defined area without running.

Master Bond Toughened Epoxy Compounds

Master Bond Supreme 3HTND-2DA is a NASA low outgassing system for die attach applications featuring thermal conductivity, high temperature resistance and toughness. Read more at http://www.masterbond.com/properties/flexibilized-and-toughened-adhesive-systems or contact Tech Support.
Phone: +1-201-343-8983
Fax: +1-201-343-2132
Email: technical@masterbond.com.



INDUSTRY INSIGHTS

By Ron Jones

Control and Compliance in the Semiconductor World

I'VE SAID THIS IN PREVIOUS columns: to me, one of the words that best typifies the semiconductor industry is *control*.

During the design phase, we go through myriad phases and checks to ensure we have the highest probability of generating good die on the first spin before we commit to what might be tens of millions of dollars on a photomask set.

During the fab process, we gather enormous quantities of in-process data during the hundreds of process steps required to build a 40 mask level device and then use highly sophisticated software tools to manage the process in order to achieve the highest wafer and probe yields.

During the probe operation, we perform hundreds of tests to optimize total cost. We want to pass every die that has a reasonable chance of becoming a good finished unit, without passing die that will waste the money spent on packaging by failing at final test.

During the assembly process, we use statistical process control to manage all operations so that we catch potential issues before they cause us to scrap a die and package.

During the final test operation, we test and retest to ensure the highest yields, while guaranteeing the product we ship meets our product specifications and committed quality levels.

This isn't like baseball where a player that bats .400 is a hero. We can't be successful by doing well in one part and mediocre at another. One error in a fab masking step can cause a production lot worth $50,000 to be scrapped. On misplaced wire at bond setup can cause the scrapping of thousands of units that have all their manufacturing cost already invested.

The controls I discuss above are self-inflicted. No outside forces tell us that we have to maintain these levels of control. We do it of our own free will to generate IC's that meet the specification we created at the lowest cost.

There are, however, requirements put on us by outside forces:

- These may come from customers, governments or groups like investors.
- They may range from absolute requirements to gentle nudges.
- Some have been around since the early days of our industry, while others are just beginning to show on the horizon.
- Their overall impact may range from minor to major.
- Some may have no impact on product design and sourcing, while others directly impinge on the design and supply chain.

Some examples are listed in the table below.

The overall direction is pretty clear. There will continue to be more requirements over time . . . with none of the current requirements going away.

Details of future requirement are not very clear, however. Something like Conflict Minerals can come straight out of left field, in this case as a rider tacked on to the Wall Street Reform and Consumer Protection Bill . . . who saw that one coming? ISO 62626 is just appearing on the scene, but will have major implications on the design and manufacture of devices that are parts that relate to the automotive industry.

Whatever requirement come, we have a long history of doing what it takes to rise to the occasion. ◆

REQUIREMENT	YEAR	FOCUS
MIL-STD	1940's	Military Quality and Reliability
Int'l Traffic in Arms Regulation	1976	National Security
ISO 9001	1987	Operations Control
ISO 14001	1996	Environmental Responsibility
OHSAS 18001	1999	Occupational Safety
ISO/TS 16949	2002	Automotive Quality
RoHS	2006	Hazardous Substance Control
REACH	2007	Hazardous Substance Control
Conflict Minerals	2013	Social Responsibility
ISO 62626	2015	Automotive Safety
Future ??		Who knows?

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions like this one may deliver a message closer to home.

First World Problems

RETURNING HOME WITH A CARload of food for our Thanksgiving feast, we discovered **our garage refrigerator had died**. The only appropriate response other than panic was to laugh at **this truly epic "First World Problem"** (FWP). Most of the people in the world would wish they had such luxuries. (They may aspire to having a car and large quantities of perishable food; having a second refrigerator in a garage is beyond their dreams.)

A feast with friends and family to celebrate the harvest season is a worldwide tradition – even in poverty stricken and primitive societies. (Among other social factors it demonstrates the "fruits of labor".) But the scale of the bounty for our celebrations with friends and family may be hard for others to comprehend. However, if you are a middle class American, it was probably easy to grasp the entire frustrating scene described. It is probably far harder for many of us, myself included from time to time, to realize how privileged we are. I am working on a new habit to look at things through the lens of **FWP** in an attempt to put things into perspective and remember how fortunate we are.

Speaking of abundance and **FWP**s, Peter Diamandis and Steve Kotler in *Abundance; The Future Is Better Than You Think* (2012) describe solving global problems using technology to achieve balance between supply and demand. One part of this technology is a vast array of trillions (perhaps as many as 45 T) networked sensors to monitor our resources, increase efficiency, and reduce per-capita consumption. Sensors such as these and the corresponding actuators are many of the "things" envisioned by the Internet of Things (IoT).

I am thankful to be a member of the TSensor Summit (www.tsensorsummit.org) organizing committee. Our mission is to identify the specific applications and technology required to build the trillions ("T") of sensors for the IoT and achieve "Abundance".

When one looks closely at credible data on the many global challenges including:

• World population growing to over 9 billion in 2040. (US Census Bureau)

• Significant levels of air and water pollution in the developing and third world and the corresponding decrease in years of life. (World Health Organization)

• Primary and secondary education enrollment of 82% which implies approximately 267 million children worldwide are not in school. (United Nations Educational, Scientific and Cultural Organization – UNESCO)

The **size of these global challenges in terms of the numbers of people or the changes required** to achieve "Abundance" is mindboggling. More disconcerting, is that the **5 to 10 year data shows only minor incremental change**. The trend lines do not show responses that are sufficient to avoid crises. The only abrupt change seen in the data was Japan's sharp reduction of alternative (renewable) and nuclear energy sources from ~17% to ~2% of its total energy supply over two years. This was due to Japan's immediate curtailment of nuclear power production after the 2011 Fukushima Daiichi disaster. It also revealed minimal use of alternative energy in Japan.

Governments and global organizations have developed programs to make progress on these global challenges. However, the improvements have been incremental and gradual - typically a percent or less per year. It is clear that **disruptive change is required to make significant improvements**. Disruptive change can be from new technology and/or significant "willpower" through massive shifts in government priorities and policy. As repeatedly shown, technology adoption is far quicker than government action absent a crisis and accompanying public outcry on the scale of Fukushima.

A number of recent technologies have shown exponential improvements in terms of increased capabilities and decreased cost over time. Semiconductors are the most prominent example and have tracked Moore's Law, which predicts the minimum cost of an integrated circuit is achieved by doubling of the number of transistors every two years. **This exponential growth in capabilities and lower costs typical drives very rapid user adoption.** These user growth rates often exceed exponential growth and resemble a hockey stick when graphed versus time.

Only these **"exponential technologies" have the ability to quickly and economically bring about the disruptive change required**. At the end of 2012, the number of active mobile phone numbers exceeded the global population. This is the only technology that has achieved 100% market penetration – 1 per person on average. No other technology including running water in the home (57%), improved sanitation e.g. toilets (61%), or FM radio (58%) has yet achieved 100% penetration. Mobile phone technology took thirty years to develop with the most significant growth in the last ten years displaying the typical hockey stick adoption pattern.

As we develop new disruptive technologies, care must be taken since one size does not necessarily fit all. Even though it is desirable to have the greatest economies of scale to make these trillion of sensors economical. **The end applications and requirements may differ vastly**. The potential groundwater contamination here in Silicon Valley may be significantly different (possibly industrial chemicals) versus those found in sub-Saharan Africa (fertilizer run off). And those areas requiring air pollution monitoring (such as regions of China and India) may not necessarily be those in the greatest need for water monitoring. Therefore, solution "platforms" that can be economically targeted to the specific end application are preferred. The ultimate goal of the TSensors Roadmap is to identify the end applications and sensing technology with the greatest applicability.

One other area of concern for the development of exponential technologies, including the IoT with trillions of sensors, is avoiding "shifting" the problem. **Many previous technologies have shifted the problem in time and/or place.** Nuclear power generates radioactive waste that has no reasonable

treatment options and requires storage for thousands of years. Many obsolete electronic devices contain "e-waste" with toxic materials that are sometimes "processed" in third-world countries with inadequate personal and environmental protection. The FWP of disposable and obsolete electronics quickly has become a third-world problem.

As we develop trillions of sensors that will last ten or more years to solve these global challenges, we need to be sure we don't cause pollution or other environmental harm in the process. **A total product life cycle (TPLC) from concept to end-of-life that encompasses the entire supply chain is necessary.** Industry standards should be established to ensure these problems are not shifted.

Having traveled the world extensively for work and pleasure, I have seen a wide range of living standards from extreme poverty to lavish opulence. At the same time, I have witnessed all manner of labor. Professionally, I have reviewed all aspects of the electronics supply chain in the US, Europe, and Asia from grungy manual assembly lines to gleaming new semiconductor wafer fabs. **The good news is that I have found many people who take pride in their work producing quality products and services even in the most trying of situations.**

My family and I are blessed with good health and well being that comes with the privilege of living in Silicon Valley. For this **I am extremely thankful!** I will "just deal" with my FWPs with a minimum of complaining. And I will continue to work diligently with my clients to solve our global challenges without creating new problems or shifting them elsewhere.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.

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Is Mass Customization Coming to Semiconductors?

Adrienne Downey, Semico Research

3D PRINTING HAS TAKEN THE world by storm. It offers the ultimate in customization, from prototypes to earbud-style headphones that are made to fit precisely in your ear (OwnPhones) to medical implants designed with information from scans taken of a person's organs. As the wearable technology market develops, there will be a need for electronic devices that can be customized for the individual wearer. In a sea of fitness bands and smart watches on the market, the way to differentiate a product will be to allow the consumer to have input into the color scheme, pattern, and material used to create the device. This is called "mass customization" and, combined with the burgeoning wearable market, could be the next killer app for the electronics industry. Semico forecasts the wearable electronics market to grow from 54.3 million in 2014 to over 400 million units by 2018.

OwnPhones is an example of the response that customized wearable electronics can generate. The company raised more than 300% of its original goal on Kickstarter in August 2014. They had to add extra pledge levels to accommodate the demand. Key to the success of OwnPhones is that they solve a problem: ill-fitting earbuds that hurt and/or fall out of your ears, particularly when exercising.

But OwnPhones are only partially 3D printed. The casing that touches your ear will be printed, but the board and electronics inside are not. What if one day the entire earbud, chips and all, could be 3D printed? Now the consumer could customize not only the outer appearance and feel of the earbud, but also the functionality of the device. Do you want to maximize battery life? Or is sound quality more important to you? What about noise cancellation?

Semico believes the future of the electronics industry lies in this concept of mass customization. Already we are seeing efforts from research groups such as PARC (Xerox's Palo Alto Research Center) to revolutionize semiconductor manufacturing. With financing from DARPA (Defense Advanced Research Projects), PARC has developed a method of programmable electrostatic assembly, inspired by xerography. Tiny chiplets are produced and mixed into a solution-based "ink." The chiplets, which have an electrical charge pattern on them, are subjected to dynamic electric fields which are used to orient and position them with micron-level accuracy. Once assembled, the chips are put onto a final substrate with interconnects. The technology used is similar to laser printer technology, which is essentially the assembly of large numbers of micron-sized toner particles, a Xerox development from the 1970s. The resulting circuits can be microprocessors, memory or any other desired semiconductor chip. Although production quantities will not be feasible for several years, this could lead to desktop printing of almost any semiconductor.

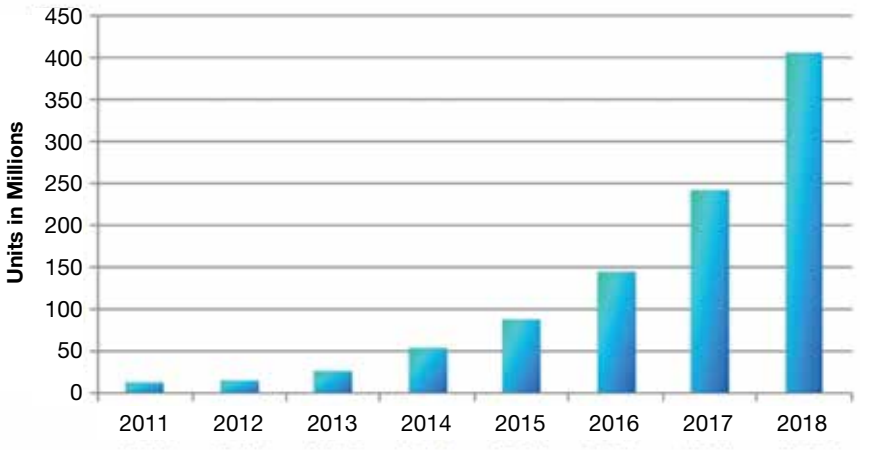


Figure 1. Wearable Electronics Forecast. *(Source: Semico Research)*

The advantages for the semiconductor industry are clear. The depreciation costs for today's leading edge fabs are so high that the only way to cover them is to manufacture millions of identical ICs. But, there are only a few kinds of advanced ICs needed in those kinds of quantities, primarily processors, DRAM, and NAND flash. The demand for other semiconductors is for smaller volumes, or for ICs that do not need to be manufactured on leading edge technology. Many could be manufactured using four or five generations' old technology.

The semiconductor industry has addressed this problem in several creative ways. Multi-project wafer services combine different ICs on one wafer. Multi-wafer lots combine different wafers in one processing lot. But, each of these solutions imposes constraints. A process optimized for memory chip production is not well suited for logic chip production. Even a logic chip process cannot be optimized for a particular IC. Every IC must be designed to perform satisfactorily on one given set of process parameters.

However, if wafers could be processed in a desk-sized volume instead of in a massive clean room, there would be multiple advantages. Clean room and process equipment costs would be much lower. Smaller, less expensive wafers could be used, and it would be easier to manufacture ICs in volumes that match the demand. The PARC technology promises IC production in the volume occupied by a laser printer. In that small volume, the PARC device might be able to manufacture ICs economically in small quantities.

While PARC's technology lies well in the future, we already have the capability of printing a substrate and then printing metal lines on that substrate to duplicate

the function of a PC board or hybrid substrate. Soon, it may be possible to print transistors. How long after that will it be before a 3-D printer becomes a desk-sized semiconductor fab?

Printed Electronics

A complementary technology to 3D printing is Direct-Write printed electronics, such as aerosol jet printing and inkjet printing. Combining the two could have a distinct impact on the way electronics are manufactured in the future. Inkjet printing with conductive and dielectric inks can be used to print interconnects directly in electronics packaging.

Neotech AMT is a company in the 3D printed electronics space. Neotech's printers have enabled the mass production of 3D printed antennas for cell phones at Lite-On Mobile. Google and 3D Systems are exploring a similar technology for the antennas in the Project Ara phones, due out in 2015. Neotech uses an aerosol jet print process developed by Optomec. The process can be used to create electronic structures with a line width as small as 10 microns, and as large as 10mm. The printed antennas can be used with standard injection-molded plastics.

Figure 2. 3D Printed Antenna.
(Source: Lite-On Mobile)

So far, Optomec's technology has been used to create LTE, NFC, GPS, Wi-Fi, WLAN and Bluetooth antennas; their performance is comparable with antennas made with other production methods. Optomec's Aerosol Jet printer is also used to print 3D interconnects, dispense micro beads, die and component attach, and bond pad layout.

At Swansea Universities Welsh Centre for Printing and Coating, they are developing an electrically conductive material based on a mixture of polymer and carbon powder, or "carbomorph" material. Custom circuit boards can be printed using a dual-extrusion method

Figure 3. 3D MID Demonstrator Circuit – Ag on PA6 with added SMDs.
(Source: Neotech AMT)

that can detect changes in temperature, moisture, pressure, or whether the device is being flexed. The idea is to eventually 3D print fully integrated circuit boards, which would enable embedding sensors and electronics inside 3D printed objects in a single build.

Multi-Material 3D Printing

3D printing is a fascinating new technology with lots of promise, but right now one of the things holding it back is the inability to print disparate materials at the same time. Few items in the average home or office are made of only one material. However, as with so many other aspects of this market, this is changing. Some 3D printers already are labeled "multi-material", which means they can print different types of plastic in the same print job. This is certainly a welcome addition, as you can print flexible materials alongside more rigid ones. Printing different colors together is also an option.

Figure 4. Dual-Material 3D Printed Items.
(Source: Airwolf3D.com)

Perhaps the most intriguing area of research is in the area of using conductive materials (like metal) together in the same print with nonconductive ones, like any of the many plastic polymers in use today. Rabbit Proto is a company that has developed a solution to achieve this with a syringe extruder that enables the inclusion of conductive ink into a

Figure 5. Structur3D's Discov3ry, Filled Syringes, and Final Printed Products. *(Source: Structur3D)*

print job. It is available as an add-on for an existing plastic extrusion printer. Bare Conductive's ink enables the printing of capacitive touch sensors with Rabbit's system, which allows for printing circuits on 3D surfaces in complex patterns. Rabbit Proto's solution allows you to print with other materials besides conductive ink, basically anything that will fit into a syringe. In fact, they offer a video on their website showing peanut butter as it is 3D printed.

Structur3D has announced the Discov3ry paste extruder add-on; it is a peripheral device that attaches to extrusion-type printers, like Rabbit Proto's device. This one allows the printing of any paste; examples include latex, silicone, playdough, cake frosting, ceramics, polyurethane, peanut butter, and Nutella. Neither Rabbit Proto nor Structur3D have begun shipping their devices, although they are accepting preorders. However, the proof of concept is there, which opens up the 3D printing market to so much more than is available today.

Unfortunately, neither of these achieves printing metal and non-metal in the same print job. Currently the process for printing metal is vastly different from that of plastic. Some metals are processed using a process like Direct Metal Laser Sintering (DMLS), where a laser sinters metal powder together layer by layer to form an object. For precious metals, a wax mold is 3D printed, and then the wax mold is used to cast the final object. Plastics are usually extruded, much like a hot-melt glue gun works, but some are created with lasers and powder or resins.

The future of electronics manufacturing will certainly include at least some of the technologies mentioned above. Whether it will be PARC's technology, direct-write printed electronics, multi-material 3D printing, or some combination thereof, it's clear that new technologies are on the horizon.

For a complete look at the 3D printing market, Semico Research recently published a report titled 3D Printing: The Next Industrial Revolution. Contact Rick Vogelei at ricky@semico.com for more information. ◆

Carsem

A Member of the Hong Leong Group

Founded in 1972, Carsem is a leading provider of turnkey packaging and test services to the semiconductor industry, offering one of the largest package and test portfolios in the world. The company has three high technology factories, all incorporating highly sophisticated, state-of-the-art equipment; ensuring products meet the exacting quality standards set by the automotive, telecom, computer, and consumer electronics industries.

Carsem factories maintain world-class quality standards. All factories have achieved ISO/TS 16949, ISO 9001, ISO 14001, ANSI/ESD S20.20 certifications and comply with the Sony Green Partner Program. Carsem has also successfully passed audits by the Defense Logistics Agency and the European auditing standard VDA 6.3.

Carsem has three manufacturing facilities. Two of these facilities (S-site and M-site) are located in Ipoh Malaysia, with a third location in Suzhou, China.

QFN Packages are offered in both the Ipoh and Suzhou facilities. The focus for QFN is in the following areas:

- Miniaturization as low as 0.3mm package height
- RF Integrations
- Portable Power Management
- Industrial Power Management
- Copper Wirebonding
- Copper Clip, Flipchip
- Ag Alloy and Al Wirebonding (in Q1' 2015)
- Multi-Die /Stacked Die
- High Routability QFN
- System in Package
- MEMS and Light Sensors
- Cavity Packs for Pressure Sensing
- Automotive Applications

Between the Ipoh S-Site and the Suzhou site, Carsem produces more QFN/DFN packages per day than any other OSAT.

Laminate Packages are currently offered at the facility in Suzhou. The focus areas for this line are:

- BGA and LGA Configurations
- Au and Cu Wirebonding
- Flipchip and Cu Clip Interconnect
- System in Package

Note that the Suzhou factory has completed a major floor space expansion and is well-equipped to further grow its QFN and Laminate package offerings.

Leaded Packages are offered at our M-Site facility in Ipoh. The major focus for leaded packages is on automotive applications, and this facility is the development center for automotive excellence. This will be discussed in greater detail later in this article.

CARSEM AND THE AUTOMOTIVE SECTOR

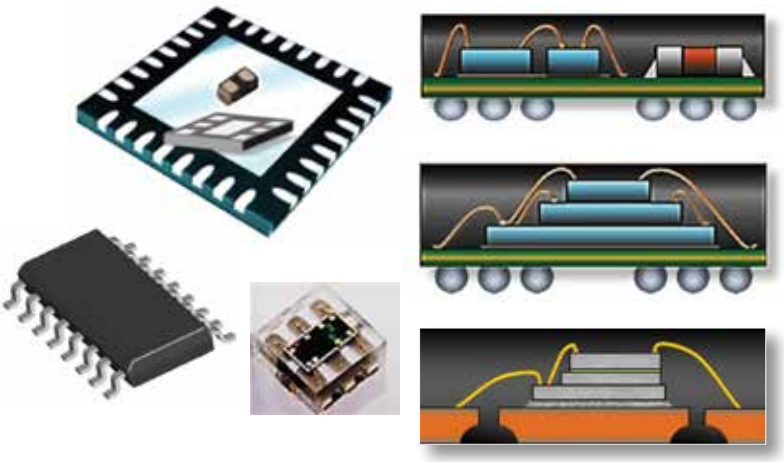
The automotive semiconductor industry has certainly evolved over the last few decades! The industry has experienced a gradual transition from traditional thru hole packages to leaded SMT products, rugged semi-custom pkgs for under the hood apps, as well as leadless packages for non-drive train applications. There has been a significant increase in MEMS sensors both inside the passenger compartment and throughout the drive train.

The list of applications seems to be endless, and includes:

- Hall effect Speed sensors
- Led drivers/backlighting
- Safety systems: including tire pressure monitoring, cruise control, collision warning, blind spot detection, lane departure, and Lidar
- Comfort and convenience: including climate controls, auto-dimming, GPS, phone and entertainment systems
- Electronic power steering
- Power controllers for hybrid and electric vehicles

When combining semiconductor volumes for all automotive applications, the market is forecasted to grow approximately 8% per year!

Carsem is no stranger to automotive semiconductor assembly and test. Over the last 20 years, Carsem has supplied automotive assembly and test services to a number of semiconductor industry leaders. Initial involvement started with very specialized programs that



Some of the Package Configurations Assembled by Carsem.

The Carsem Technology Center is headquartered in Ipoh, Malaysia. This is the core of Carsem's R&D activities.

The key activities championed by this group are:

- Material Characterization
- Simulation Capability
- Process & Equipment Development
- Development of New Technologies
- Dedicated 24x7 Assembly Pilot Line

Final Test & Wafer Probe Facilities are available in both Ipoh and Suzhou. These test facilities have the following features:

- Floor Space: 105,000 sq. ft.
- Equipment:
  - 600 Handlers & 600 Testers
  - Over 80 Wafer Probers
  - Over 100 Tape & Reel tools
- Test Engineering Support
- Test Program Development
- Load Board Repairs & Maintenance
- Probe Card Repairs & Maintenance
- Automatic Test Data Transfer
- Strip Test:
  - Multiple Systems Installed
  - Tri-Temp Capability
  - Enabling Technology for Cost Effective MEMS Testing

Wafer Level CSP has a significant presence in Carsem. Combining strategic bump foundry partnerships along with Carsem's end of line processing capability, turnkey processing of WLCSP has become an increasingly more important part of Carsem's business model.

included custom processes and inspection requirements to meet the specific needs of these customers.

As a result of these years of supplying specialized automotive assembly and test to its customers, Carsem has developed the know-how and disciplines needed to offer mainstream automotive assembly and test to its entire customer base for both standard and custom package configurations.

Carsem has implemented the following critical systems and methodologies necessary for automotive manufacturing support.

i-Manufacturing is one of the core elements that enable a solid implementation of automotive practices and philosophy. The i-Manufacturing model encompasses:

- Robustness, Simplification & Standardization
- Material Management Systems
- Recipe Management System
- Electronic Tracking and Traceability
- Streamlined Operations
- Automation

To complement i-Manufacturing are the remaining details that are key to automotive manufacturing:

- An APQP Philosophy and Structure
- Dedicated R&D/ Manufacturing teams for Automotive Products
- Designated equipment, operators, and technicians
- Specialized automotive record retention systems
- Standardized Automotive Process Flows based on packaging technology

Temp Cycling, IR-Reflow, 100% inspection, & open/shorts testing are popular options for automotive process flows.

Functional Test – Hot and Tri-Temp, as well as statistical test data analysis are also typical requirements.

Standardized material sets have been developed to meet stringent AEC-Q100 reliability grades referenced below:

Referenced from AEC-Q100 Rev G: Automotive device operating temperature grades are defined below:

Grade 0: -40˚C to +150˚C
Grade 1: -40˚C to +125˚C
Grade 2: -40˚C to +105˚C
Grade 3: -40˚C to +85˚C

The most stringent automotive reliability test conditions are classified as Grade Zero. The following are the primary OSAT test conditions for constructing a Grade Zero Assembly:

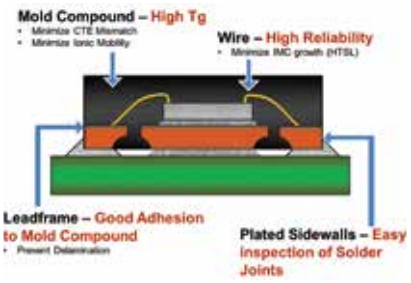
Temp/ Humidity Bias: 85˚C / 85% RH
Autoclave: 121˚C / 15 psi
Temp Cycling: -65˚C to 175˚C
High temp Storage: 175˚C
High Temp Op Life: 175˚C

The gradual acceptance of leadless packages for rugged automotive applications comes with a special requirement:

- Straight forward optical inspection of solder joints of QFN Packages

The challenge here is for the assembler to provide a terminal that is both solderable on the bottom surface and side surface of the package.

Automotive Sensor Applications.



QFN Cross Section.

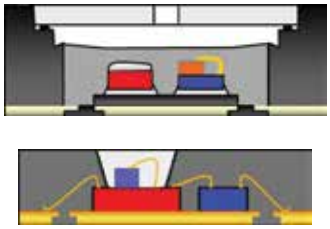
QFN Sidewall Plating.

Carsem has implemented additional assembly and plating processes to insure a wettable "sidewall" for QFN & DFN package terminals.

All of the above requirements are incorporated into a model that causes automotive packaging development and production to remain a challenging endeavor. Production of Jedec standard thru-hole and SMT packages are being demanded to their lowest defect levels in history while the reliability requirements are set at their highest.

Leadless packages in dual and quad configurations are not only being used for infotainment and convenience features, but are now also being qualified for rugged drive train applications.

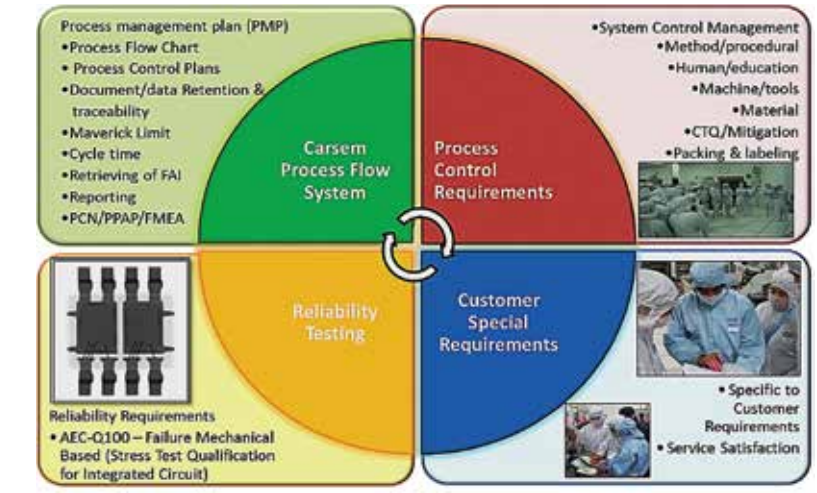
Multi-die MEMS cavity pack QFNs are now in full production for tire pressure sensor applications. These assemblies include a pressure sensor, accelerometer and a controller in a stacked configuration.



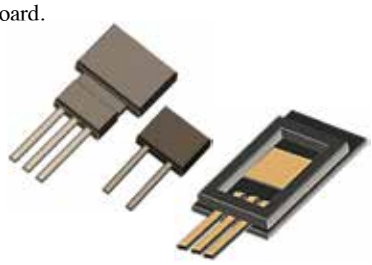
Carsem Cavity Packages.

Customized leaded packages for automotive applications are not a thing of the past.

Since rugged drive train applications take years of development and reliability testing, there are still many products built in customized leaded packages. Many of these custom packages are designed for direct mounting on engine components without interfacing directly to a printed circuit board.



Key Factors for Automotive Assembly.



Custom Leaded Automotive Packages.

Some of these applications include:

- absolute and differential pressure sensing,
- Balance sensing,
- speed and acceleration sensing, just to name a few.

With all of these custom tooling applications, a dedicated team of process engineers, as well as tooling and computer simulation specialists are needed to enable these programs to be successfully realized the first time.

No discussion on automotive semiconductors is complete without a few comments about copper wire bonding. Over the past few years, Carsem has been approached by a number of customers wanting to make that "leap" into automotive copper wirebonding.

Extensive qualification efforts as well as auditing to heightened automotive requirements are well underway.

The efforts have paid off. The Carsem M-Site team has now been qualified by one of its long standing automotive customers to run Grade 0 assembly of leaded IC packages using Cu wire.

Carsem expects a steady ramp of customers adopting copper wire for automotive assembly over the next year.

A long track record of high quality, high volume, semiconductor packaging support to the world's leading analog and RF semiconductor companies continues at Carsem. As a result of this, a majority of the products assembled and tested at Carsem ship to the world's leading automotive and consumer electronics OEMs.

Todays "end market" demands highly-integrated solutions. With product development cycles now measured in months, instead of years, customers depend on manufacturing partners who not only have the technical expertise to work side-by-side with them during the development phase, but also must possess the scale and systems to allow rapid execution of high volume, high quality manufacturing. ◆

Carsem's Technology Center (CTC) works hand-in-hand with our customers leveraging our expertise in materials characterization, advanced modeling and simulation and a deep understanding of equipment and processes to ensure rapid time to market with unique, high quality, cost effective solutions.

In an ever-changing world, your choice of an assembly and test partner has never been more critical. Time to market pressures, new materials, increasing reliability and performance requirements and the relentless demand for expanded features and reduced size and cost, can only be effectively supported by a supplier which has the proper resources and experience. We invite you to contact Carsem and learn for yourself why **the leading global analog and RF semiconductor companies have selected Carsem as a strategic semiconductor assembly and test partner.**

China's Impact on the Semiconductor Industry – MEPTEC 2014 Update

Clements E. (Ed) Pausa
Consultant, Global Technology Centre
PricewaterhouseCoopers

FOR EIGHT OF THE PAST TEN YEARS including the last three years, both China's semiconductor consumption market and its industry production have exceeded the worldwide semiconductor market growth. During 2013 China's semiconductor consumption grew by 10.1% to reach a new record of 55.6% of the global market. 2013 was the second consecutive year that China consumed more than half of all the worldwide semiconductor market. While the worldwide semiconductor market has grown by US$139bn from 2003 through 2013, China's semiconductor consumption has grown by US$150bn and China's semiconductor consumption market has grown from the smallest to the largest regional market. During the first seven years of the past decade China's semiconductor consumption of O-S-D (optoelectronic-sensor-discrete) devices had been a few percentage points higher than the worldwide average, but that difference has since become insignificant (see Figure 1).

China's semiconductor industry has grown at an equal or greater rate than its semiconductor market consumption for eight of the past ten years. From 2003 through 2013 China's semiconductor industry has achieved a ten-year compound annual growth rate (CAGR) of 23%, while China's semiconductor consumption achieved a 19.4% CAGR and the worldwide semiconductor market a 6.3% CAGR, all measured in US dollars.

Integrated circuit (IC) design continues to be the fastest growing segment of China's semiconductor industry, growing by 33% in 2013 to reach record revenues of US$13.2bn. During the past ten years (2003-2013), China's IC design (fabless) industry has grown at a 37.6% CAGR from US$541mn to US$13.2bn (see Figure 2).

Figure 1. China's IC and O-S-D market growth, 2000-2012.

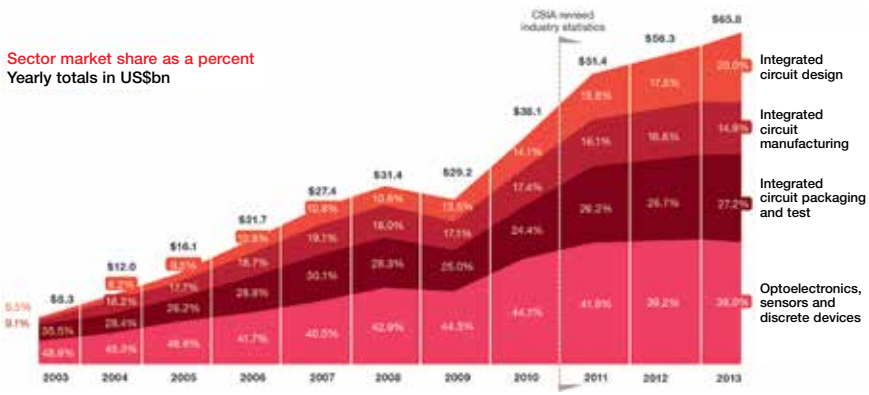


Figure 2. China's semiconductor industry by sector, 2003-2013.

2013 was another year of wafer fab capacity rationalization rather than growth for both China and the worldwide industry. The number of fabs in production in China during 2013 decreased by three, to 160, while their net nominal capacity increased by about 2%. However, during the past ten years, from the end of 2003 through 2013, the number of wafer fabs in production in China has increased by 186%, while their capacity has increased by 314%. Foundry production continued to constitute the largest share of China's wafer fab capacity in 2013 at 43% of the total, compared to the worldwide average of 27%.

Semiconductor packaging, assembly and test (SPA&T) nominal capacity in China was modestly consolidated during 2013, while unit production increased by more than 6%. During the past ten years, the number of SPA&T facilities in pro-

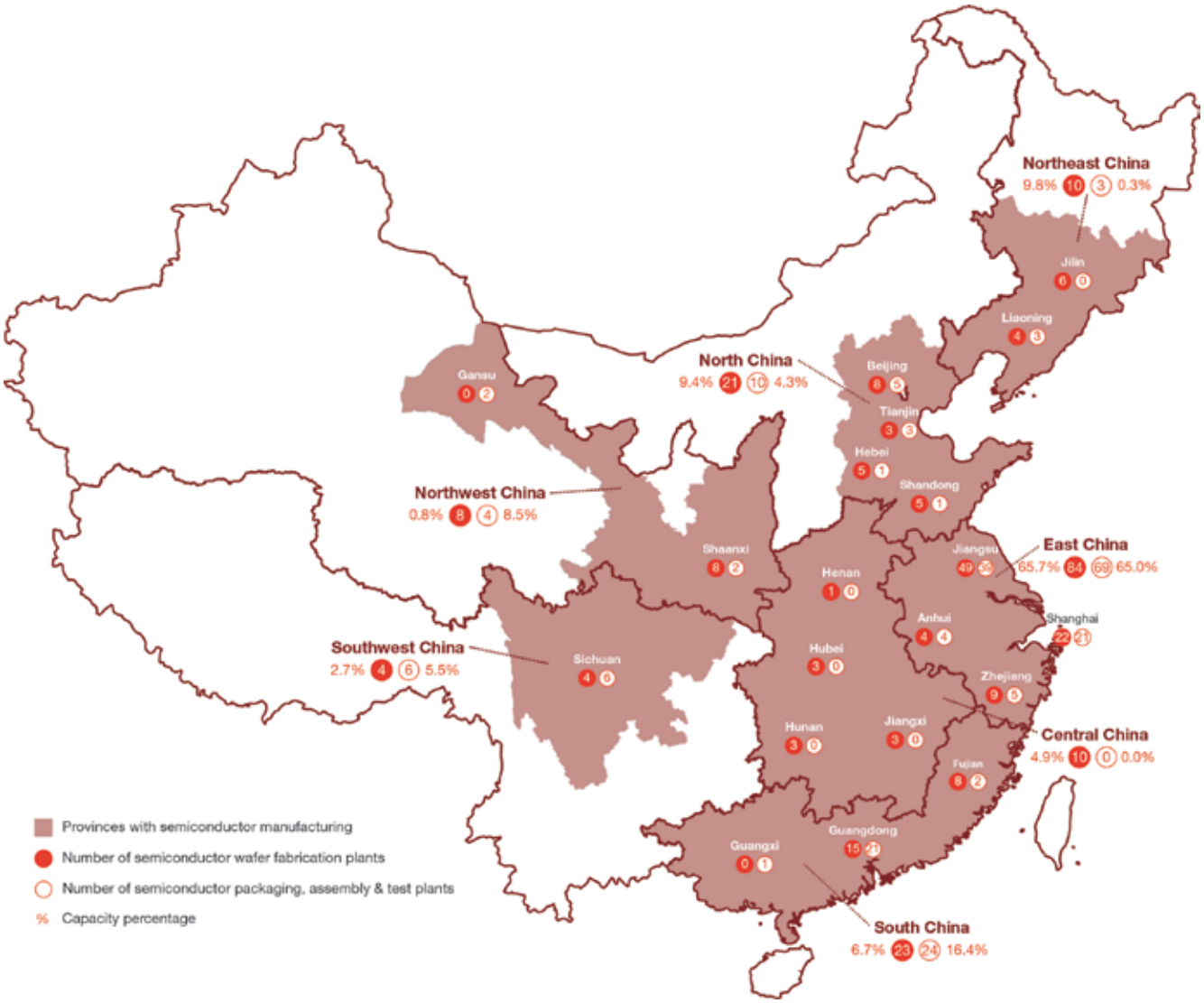


Figure 3. China's 2013 semiconductor manufacturing capacity by province and region.

duction in China has increased by 51% while their capacity has increased by 175%. Over the same time period, China's share of worldwide SPA&T facilities in production has increased from 17.7% to 20.8% and its share of worldwide SPA&T manufacturing floor space grew from 10.5% to 27.4%.

Packaging assembly and test remains the largest of China's semiconductor manufacturing activities when measured in terms of value added, production revenue, employees and manufacturing floor space although this relationship is often missed because it is allocated between two separate industry sectors: the IC packaging and testing and O-S-D sectors. The composite weighted average of China's 2013 SPA&T production is now estimated to be about 58% of worldwide, up from a revised 52% in 2012. As of the end of 2013, China had 116 SPA&T facilities in operation that represented 21% of the total number of worldwide SPA&T facilities, more than 27% of worldwide SPA&T manufacturing floor space and 24% of worldwide SPA&T employees. As a result, China's SPA&T facilities continued to rank first in share of manufacturing floor space – a proxy for potential manufacturing capacity – for the fifth year, noticeably ahead of Taiwan (at almost 20%) and Japan (at 11%). China's SPA&T facilities also ranked first in number of employees, with 24% of the worldwide employees at the end of 2013, ahead of Taiwan (19%) and Malaysia (17%).

SPA&T capacity also became somewhat less concentrated during the past ten years. The top five companies only accounted for 33% of China's capacity in 2013, down from 48% in 2003. Based upon reported manufacturing floor space capacity, only two of the top five companies in 2003 – ASE and STATS ChipPAC – were among the top five in 2013. ASE (including GAPT) was ranked first in manufacturing floor space capacity in 2003, with 22% of China's total, followed by Intel, SDI, STATS ChipPAC and Integrated Microelectronics, in order of capacity. Last year, JCET/JCAP was ranked first with 9.5% of China's 2013 SPA&T capacity, followed by Tanshui Huatian Technology with 8.3%; ASE with 7.0%; Chipmore with 4.7%; and STATS ChipPAC with 3.5%.

China's SPA&T capacity continues to be more concentrated in the SATS (semiconductor assembly and test services) sector than that of other regions. In fact, 80% of China's SPA&T manufacturing floor space and 64% of China's

continued on page 23

Die Prep Considerations for IC Device Applications

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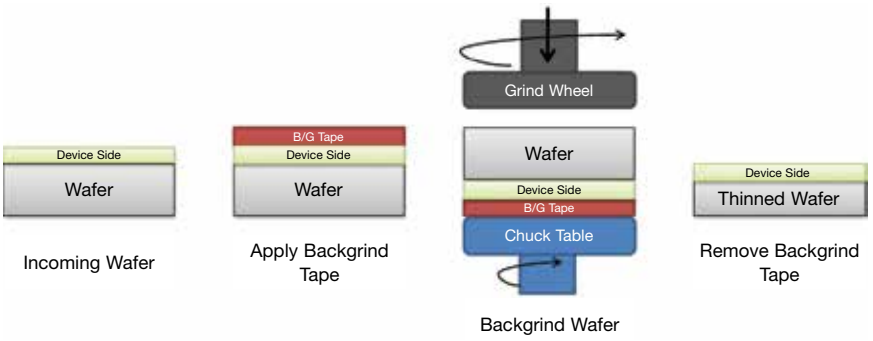

Figure 1. Mechanical Grinding Process.

FINAL THICKNESS, SURFACE FINISH, edge and backside quality, application demands... one wafer, yet endless combinations of process options when working to achieve the highest quality die possible prior to IC assembly. While quality, functional parts are the end goal for all semiconductor companies, getting from the fab to the assembly line is often an undervalued aspect of the IC supply chain.

Wafer design and characteristics are critical for not only the final product, but also for optimizing an efficient and cost-effective production stream. Utilizing specific process methods can improve die quality and reduce unexpected downstream hiccups. In this article we will explore the various means of die preparation and what one should look for when designing wafers to enhance the probability of success during die prep.

Wafer thinning is the process of removing material from the backside of a wafer to a desired final target thickness. The two most common methods of wafer thinning are conventional grind and chemical-mechanical planarization (CMP).

Conventional grinding is an aggressive mechanical process that utilizes a diamond and resin bonded grind wheel mounted on a high speed spindle to perform the material removal. The grind recipe dictates the spindle RPM, rate of material removal, and the final target thickness of the work piece. Harder materials like sapphire typically require slower feed rates compared to more forgiving materials like silicon.

The wafer is positioned on a porous ceramic rotating vacuum chuck with the backside of the wafer facing upwards (towards the grind wheel). Both the grind wheel and wafer chuck rotate during grind. Deionized water is jetted onto the work piece to provide cooling and wash away material particles generated during the grind. Grinding tape is applied to the front side of the wafer to protect the devices from being damaged during thinning. A wide variety of tapes are available to account for the different flavors of wafer surfaces including high-bump tapes with an extra thick adhesive layer to absorb bumps, low tack tape for ease of removal, and rigid wafer support tapes for thin wafer handling.

For conventional grinding the thinning is typically a two-step process. The first step is a coarse grind that performs the bulk of the material removal. The second step is a fine grind. The fine grind removes approximately 50μm of material (or less) and provides the final finish on the backside of the wafer.

Backside finishes vary depending on the grit of the backgrind wheel. As the diamond concentration increases the backside finish will appear smoother and more mirror-like. With a higher grit the surface roughness decreases while increasing the overall die strength. Additionally, a mechanical polish can be added to further increase die strength and reduce subsurface damage in the wafers. The polish is used as a supplement to a high grit grind and is a minimal removal process (2-3μm only) that provides a mirror finish.

For ultra-thin wafers (<200μm) a high grit finish with a polish is recommended to maximize the wafer strength and minimize warpage. The improved die strength lends itself to more tolerance when it comes to wafer handling and assembly forces from picking and die attach. It is important to keep in mind, however, the effect of smoothness when it comes to the backside finish as some packages and processes, such as die attach, may be incompatible with an ultra-smooth surface.

In CMP, abrasive chemical slurry is used with a polishing pad to perform material removal. CMP provides greater planarization (lower roughness, tighter TTV) compared to mechanical grinding, however, it is considered a "dirtier" and more costly process.

The wafers are mounted to a backing film, such as a wax mount, which can be difficult to remove or leave a residue on the front side of the wafer. Additionally, the cost of ownership of CMP is typically higher than conventional grind primarily due to the usage, handling, and disposal of chemicals and slurry. CMP does have the advantage of being more forgiving when it comes to processing hard or exotic materials like tungsten, but the cost-benefit and cleanliness of mechanical grinding compared to CMP should always be factored when determining the method of wafer thinning.

Die singulation is the process of isolating individual IC's from a wafer. There are a variety of methods for die

singulation with the most common being conventional dicing, laser dicing, scribe and break, and dice before grind (DBG).

Conventional dicing is the current industry standard for die singulation. Conventional dicing typically utilizes diamond enriched resin-bonded blades on high precision saws to cut through materials like silicon, alumina nitride, sapphire, gallium nitride, and mold compound.

Conventional dicers are equipped with a porous ceramic chuck to hold the work piece during dicing. A blade mounted on a high speed spindle cuts the material while high pressure water nozzles flood the work piece and blade to provide cooling. Standard dicing feed rates range from 0.5 to 3.0 inches per second depending on the material, material thickness, and quality requirements.

In addition to providing cooling, the chilled deionized water used during dicing provides lubrication to remove particles generated during saw. Re-ionized water can be used instead of deionized water to lower resistivity and minimize ESD effects on ESD sensitive products. Surfactant can also be added to the process water for ESD purposes and to provide additional lubrication and cleanliness. Furthermore, specific surfactants are enriched with corrosion inhibitors to minimize the effects of galvanic corrosion in copper embedded bond pads.

The blades used in conventional dicing vary in size depending on the material thickness and saw street width. The saw street is the distance between the outer edges of adjacent die on a wafer. As the blade cuts through the material a saw kerf is generated. The kerf includes the extra material removed in addition to the blade width. While more robust and flexible than other methods, mechanical dicing produces a larger kerf and chipping is inherent. Therefore, blade selection, as it relates to street width and wafer thickness, is critical in defining a quality process with mechanical dicing.

Dicing blades are limited in terms of its width to exposure (height) ratio, thus, the narrower the blade the smaller the blade exposure. A tall, skinny blade would be unstable and prone to blade wobble and breakage. With thick materials, wide blades are a necessity in order to provide adequate blade strength to cut through more material while keeping

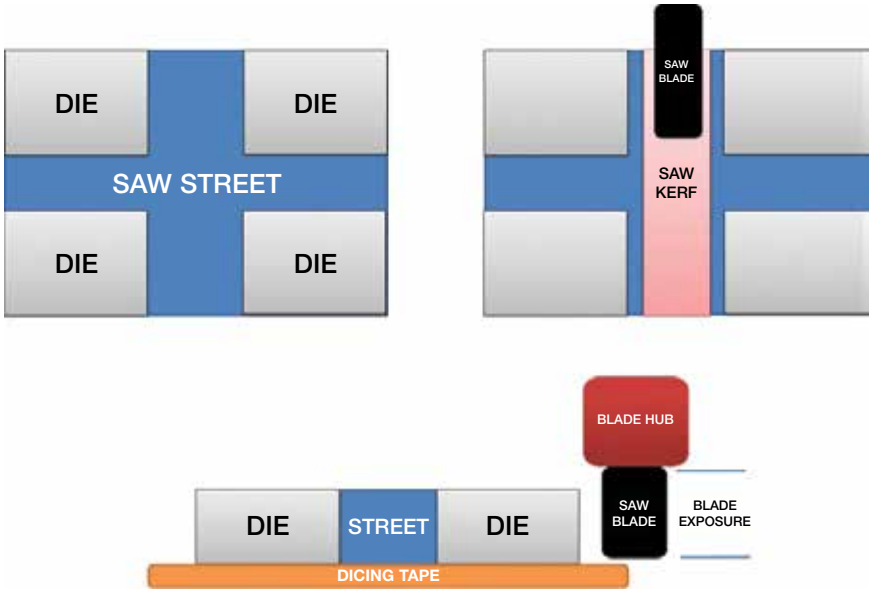

Figure 2. Conventional Dicing Process - Blade Selection.

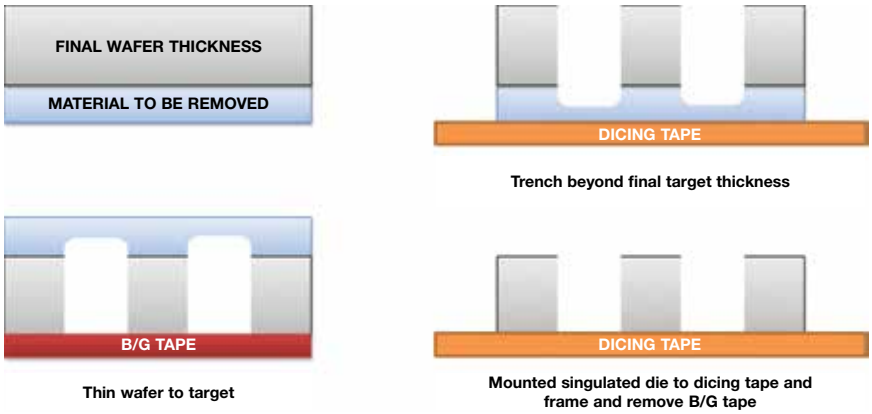

Figure 3. Dice Before Grind Process (DBG).

the blade intact. Because a wide blade is required to dice a full thickness wafer, the street width must be designed for a wide kerf; otherwise the wafer must be thinned to the appropriate thickness to accommodate the blade. A wafer with a narrow 40μm street, for example, must be 400μm or thinner for conventional dicing.

Finally, with conventional dicing chipping is the main quality concern. Chipping quality is governed by feed rate, cut mode, blade width, blade concentration, and blade grit. Typically, the higher the feed rate the larger the chipping. Two different cut modes are typically used, step cut and single pass. Single pass uses one blade to cut all the way through the material. Step cut uses two blades to cut at different depths in the wafer. Single pass provides greater throughput, but larger chipping compared to step cut. Blade grit and concentration are selected based on whether topside or backside chipping is critical and whether metal peeling or chipping is of concern.

Dice Before Grind (DBG) is a process in which the wafers are trenched prior to backgrind and then thinned to singulate the die. The DBG process utilizes the same equipment and consumables as mechanical thinning and dicing with the only change being the order in which the operations are performed.

In DBG the wafer is trenched beyond the final target thickness and then thinned to the final target resulting in the die separating and leaving clean backside cor-

ners and edges. Because the trench goes beyond the final target thickness, the dicing "foot", inherent from the rounded dicing blade edge, is removed when the die is thinned. This results in the DBG process virtually eliminating backside chipping.

DBG does have its limitation in that all wafers that are processed through DBG must be thinned. Additionally, die size, street width, and final thickness can also be inhibitors for the process, but for applications with strict backside requirements DBG is an effective process method.

Another viable singulation method is Scribe and Break. Scribe and break is the process of depressing material into the saw street to create stress in the wafer and then fracturing the wafer along that stress line. Scribe and break is a completely dry process involving no liquids or chemicals and there is no material loss during the process. Scribe and break is ideal for fragile materials like GaAs or InP or ultra-thin silicon.

Scribe and break is limited by wafer thickness, die size, and crystalline orientation. Thick wafers will have difficulty breaking as the distance the fracture must travel can be too great causing the break line to go off in angles resulting in poor quality. Additionally, if the crystalline orientation goes against the fracture direction then the die will be incapable of breaking. As a result, scribe and break is considered more of niche process specific to certain materials with the wafer being designed specifically for scribe and break.

Stealth dicing is essentially a scribe and break process where the scribe tool is a laser rather than a diamond. The laser generates a melt zone in the middle of the saw creating a stress line in the wafer. The stress line is then broken and the die are separated. Stealth dicing is ideal for wafers that have extremely narrow streets or non-contact products such as MEMS devices.

The stealth process can accommodate ultra-narrow streets (~20μm); however, the heat generated from the laser can have adverse effects on die performance. While the throughput of stealth dicing can far exceed that of conventional dicing, stealth is limited by die thickness and cost of ownership, which is exorbitant.

An alternative laser process is that of laser ablation. Ablation is the process of removing material in the wafer street with a laser to singulate the die. Laser ablation is ideal for thin wafers with narrow streets, however, ablation generates molten debris, or slag, that can get on the die surface and is difficult to remove. Protective coatings can be applied to the wafer surface to shield the die from the slag, but this will add time and cost to the process.

Like stealth, laser ablation can have a very high throughput and can process wafers with extremely narrow streets. Ablation also has the advantage of being able to process specialty materials like GaAs and InP, but cleanliness, power effects, and cost of ownership are all prohibitive for the laser ablation process.

With the variety of process methods available to satisfy an assortment of needs, die preparation should always be considered when creating new products. By understanding the means of preparing die for assembly the wafer design can be tailored to accommodate the most effective and efficient processes directly resulting in an improvement in overall quality and yield.

For more information about CORWIL and its services visit their website at www.corwil.com. ◆

SPECIAL REPORT

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SPA&T facilities were dedicated to the SATS sector in 2013 versus 58% and 54% for all other countries. Eight of the ten largest worldwide SATS companies had one or more facilities in China for a total of 19 out of the 83 top ten SATS facilities worldwide. These 19 facilities accounted for 32% of the top ten SATS manufacturing floor space worldwide. One of the ten largest worldwide SATS companies is a Chinese company, Jingsu Changjiang Electronics Technology (JCET), ranked sixth in 2013, and there is a second Chinese SATS company, Natong Fujitsu Microelectronics (NFME), ranked 18th in 2013, within the top twenty. In total, there were 28 Chinese SATS companies with 36 existing facilities that accounted for 18% of worldwide SATS manufacturing floor space in 2013.

From a regional perspective, the Yangtze River Delta, or East China region, continues to have the heaviest concentration of China's semiconductor industry, accounting for 55% of China's IC industry revenues in 2013. Of the 160 semiconductor wafer fabrication facilities in operation in China at the end of 2013, 84 are located in the East China region, representing 66% of China's total wafer fabrication capacity. Similarly, East China had 69 of China's 116 semiconductor packaging, assembly and test (SPAT) facilities in operation during 2013, representing 65% of China's total SPAT capacity. The majority of these plants are located in Shanghai, Suzhou and Wuxi.

During the past five years, however, there has been a noticeable shift in the regional location of China's IC industry, with South China and the other four regions (Central, Southwest, Northeast and Northwest) gaining share and the East and North China regions decreasing share.

Readers can learn much more about all of these developments and others from the PwC report *China's Impact on the Semiconductor Industry – 2014 Update*, which is now available at the PricewaterhouseCoopers website at www.pwc.com/chinasemicon. ◆

New Materials Solutions Deliver Miniaturization-Friendly, In-Package EMI Shielding Options

Simon Turvey
The Electronics Group of Henkel

THE ISSUE OF ELECTRO-MAGNETIC interference (EMI) has been well understood by electronics specialists for decades. If not controlled, EMI – which is a disturbance to an electrical circuit due to electromagnetic coupling from external sources – can compromise or inhibit the function of a circuit and can lead to data degradation or loss. Traditionally, the most common way to protect against EMI is through EMI shielding caps – metal lids attached to grounding pads – to prevent outside interference, minimize interference between components within a design and to prevent crosstalk of components on printed circuit boards (PCBs). This solution is effective, but market dynamics are forcing non-conventional approaches to EMI shielding.

The drive toward highly miniaturized designs, increased integration and greater functionality is driving package designers and materials specialists to innovate new approaches to EMI package shielding. Not only are device dimensions dictating smaller package profiles, which limit the use of traditional cans, but multiple parts that have higher and lower operating frequencies are now within the same package and can experience EMI. So now, not only is there package interference concern with other adjacent packages on the same board, but with parts within the same package. This is the case with today's System-in-Package (SiP) designs and, in the longer-term, EMI will also have to be addressed for system-on-chip (SoC) devices.

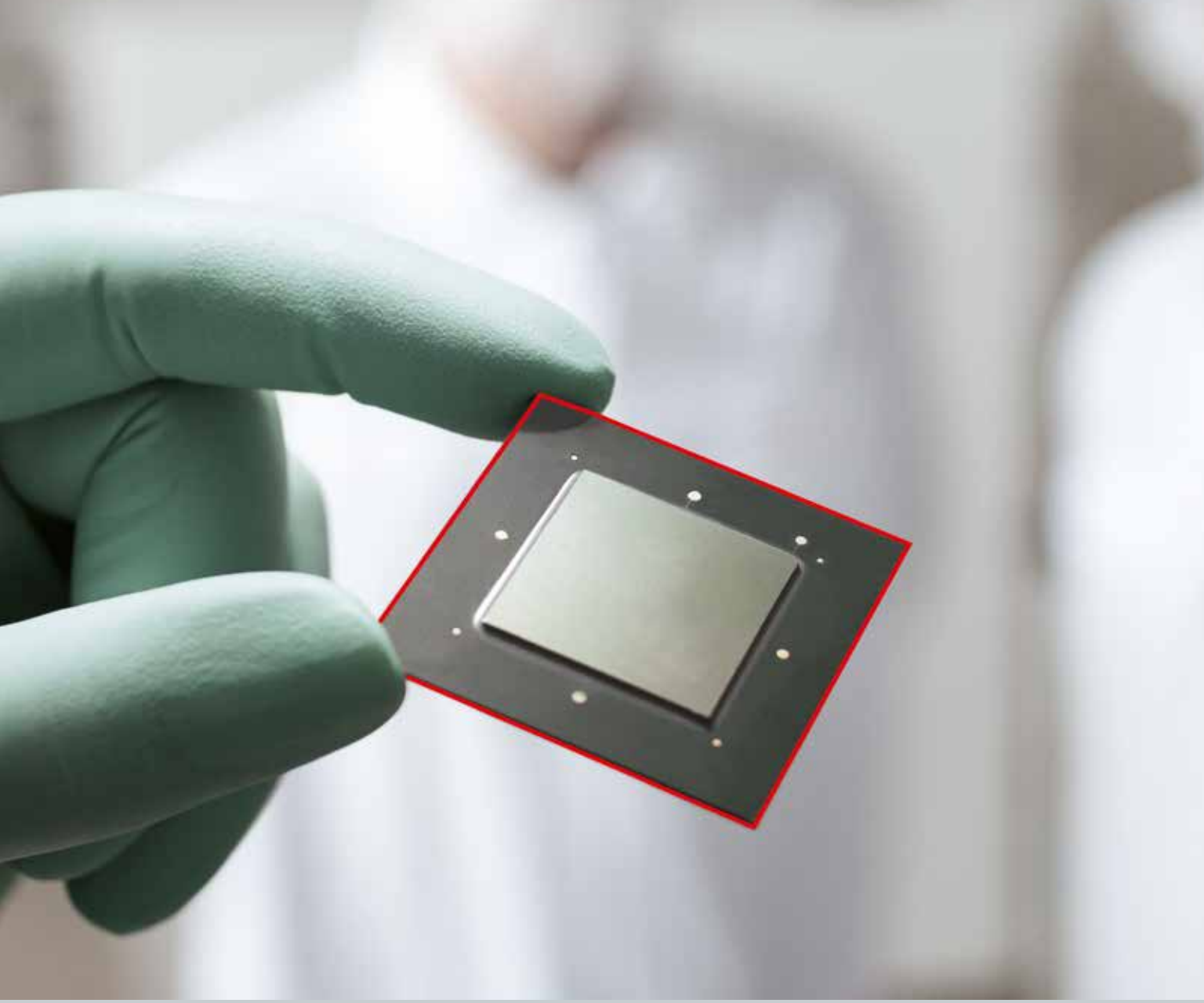
Understanding material formulation complexities and in-field performance requirements, the materials specialists at Henkel have begun developing some novel solutions for EMI shielding. The three Henkel approaches address solutions for traditional package shielding, SiP compartment shielding and shielding in package and are promising strategies to manage current and future challenges.

First, Henkel is actively working on two different methods for cap shielding. While conventional metal cans provide good board level package shielding at comparatively low cost, the cans are not practical as designs become thinner and smaller. Some industry alternatives have already emerged and include plating and sputtering shielding material directly onto the package so as to lower the profile and deliver a thinner conformal shielding solution. While both of these methods are being used in production, they do have some drawbacks. Primarily, the challenge with plating and sputtering is the ability to cover the sides of the package at the strip level prior to singulation. Sputtering requires the individual parts to be singulated first, placed on a dicing tape, marked before coating and then coated: it's a time-intensive and expensive process. The two alternatives Henkel is investing resource in are techniques that enable coating and part marking prior to singulation. The first method leverages the speed of stencil printing and has been successfully carried out at a well-known package subcontractor. The second approach is a unique spraying deposition method that can apply a very thin coating on the top of the package and in the narrow pre-singulated molding lanes, delivering a streamlined and high UPH solution. Both conformal shielding methods are being developed in tandem, with early results very promising.

For SiP devices, where targeted die need to be separated from each other to avoid signal interference, Henkel has commercialized two gap filling materials that create two Faraday cages to separate the die from each other within the package. Once the part is molded, a groove is laser cut through the mold compound down to the package substrate and runs in conjunction with a series of ground pads that are in the printed circuit board (PCB). That gap then has to be filled, which is challenging. Filling the gap aspect ratio, which can be anywhere from 5:1 up to 10:1, involves not just depositing the material, but also displacing the air so that the gap is completely filled. Henkel's LOCTITE® ABLESTIK® ABP 2820 and LOCTITE® ABLESTIK® ABP 2821 are currently the market's only viable materials for this application. Both materials are high solids loading conductive epoxy/acrylate systems that are jetted into the gap to effectively fill them while providing low shrinkage, good adhesion and low voiding. The materials create the fourth wall of the Faraday cage and deliver robust compartment shielding in a high UPH process. Following this process, the package is then coated with a conformal shield as described above.

Finally, Henkel's innovative technologists have moved from the package to the chip and have applied for a patent for materials that provide shielding directly on the die in the package. Put simply, instead of the Faraday cage being formed on the outside of the package as in the SiP process, this takes the idea to the chip level. Using novel encapsulants, shielding materials and then final molding compound, a package within a package that already contains shielding functionality is formed. Indeed, it is a novel concept and one for which Henkel has already applied for patents on the enabling materials. Beta testing will soon be underway, moving the industry closer to a viable, user-friendly in-package shielding solution.

Package- and chip-level functionality will only continue to increase, driving the need for creative solutions for EMI shielding to protect device and product performance. With a forward-looking approach, Henkel has already developed innovative materials and processes for on-package and in-package shielding, offering manufacturers high UPH, cost-effective ways to achieve design and performance objectives. For more information on any of Henkel's package shielding solutions, visit www.henkel.com/electronics or call +1-888-943-6535 in the Americas, +32 1457 5611 in Europe or +86 21 3898 4800 in Asia. ◆



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2015 Internet of Things Symposium – Another IoT event? Really?

Ramesh Ramadoss, Ph.D.
IoT Online

THE INTERNET OF THINGS (IOT) will connect everything with everyone to form a global integrated network. IoT will be driven by the need for connectivity of devices, systems and services for a wide variety of applications. IoT is anticipated to create the next technological revolution. With 10 billion devices connected today and 50 billion projected by 2020 according to Cisco Systems, the global IoT market will see an explosive growth. IDC predicts that the global IoT market would grow at a rate of 17.5% from $1.9 trillion in 2013 to $7.1 trillion in 2020.

In August 2014, Garnter published the latest report on Hype Cycle for Emerging Technologies. According to this report, IoT is at the "Peak of inflated expectations." After going through the stages of "Trough of disillusionment" and "Slope of Enlightenment", IoT is expected to reach the "Plateau of productivity" in about 5 to 10 years. This was evident from the flurry of IoT conferences and expos organized all over the world in 2014 (http://www.iotevents.org/).

In the San Francisco Bay Area alone, there were about a dozen IoT conferences in 2014. This does not include plethora of evening meetings organized by several IoT meetup groups in the Bay Area. I attended 4 conferences and found that only about 25-30% of the presentations were interesting (i.e., worth your time and money!). It dawned to me that there is a need for an IoT event with a strong focus on the core technology, emerging applications and new market opportunities. Bette Cooper with MEPTEC supported my proposal and decided to team up to put together our *First Annual Internet of Things Symposium* (See meptec.org) on May 21st, 2015 at the Holiday Inn – San Jose Airport, San Jose, CA. This IoT event will be held right after the long running *13th Annual MEPTEC MEMS Technology Symposium* to be held on May 20, 2015 at the same location.

The IoT symposium committee has prudently assembled a team of leading experts to discuss the state-of-the-art architecture, hardware, software, connectivity, data analytics and cloud platforms that will fuel the growth of IoT applications. The attendees will get to an opportunity to hear from a broad spectrum of players in this rapidly growing field. The symposium will feature presentations from big players (Intel, GE, Microsoft, Oracle, etc.) and small players. Attendees of this Symposium will go home with some perspectives on the recent developments and insights on future trends in the IoT field.

We would like to cordially invite everyone to attend this exciting event and get ready to ride the next technological wave with us. ◆

Source: Gartner, August 2014.

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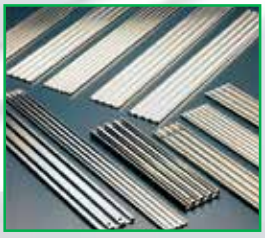
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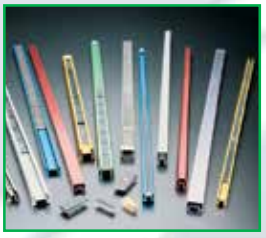
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