MEPTEC report
Volume 14, Number 2
SUMMER 2010
A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

National Semiconductor and **Green Energy Solar** have developed GESOLAR brand modules with embedded SolarMagic™ power optimization technology from National. *page 14*

STATS ChipPAC Ltd. has announced that its low cost flip chip (LCFC) technology now utilizes copper column bump to deliver a powerful packaging solution at a dramatically reduced cost for its customers. *page 14*

Unisem has announced the introduction of a new high density leadframe packaging technology, the Leadframe Grid Array (LFGA). *page 14*

Sonoscan has recently demonstrated acoustic imaging of defects in the seal that surrounds and protects the cavities in MEMS devices. *page 16*

SUSS MicroTec has introduced the next generation of its MA100e mask aligner, a dedicated lithography solution for manufacturing high-brightness light emitting diodes (HB-LEDs). *page 17*

SEMICON West2010

SEMICON West returns to Moscone Center in San Francisco July 13 through 15.

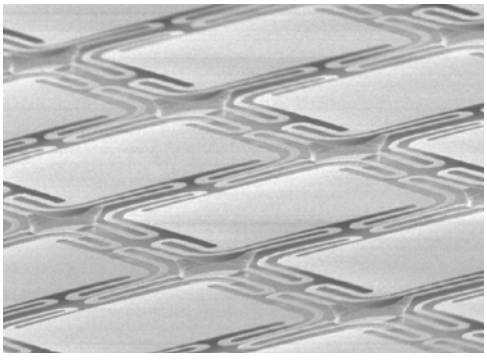
2010 MEPTEC and SMTA

Medical Electronics Symposium

Successful Strategies for the Medical Electronics Sector

A Special Two Day Symposium at Arizona State University
Tempe, AZ September 22nd and 23rd

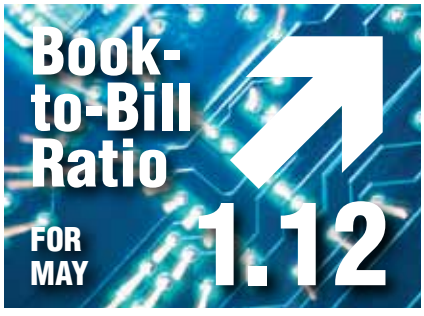
MEMBER COMPANY PROFILE



To date, A.M. Fitzgerald & Associates has served over 70 customers of all sizes and has developed new MEMS products for applications as diverse as long wavelength infrared imaging, tissue scaffolds, microphones, biological and chemical sensors, pressure sensors and optical waveguide switches.

A.M. Fitzgerald & Associates, a MEMS product development firm located in Burlingame, CA, bridges the gap between new product concept and foundry production. The company offers fully integrated engineering services to get a client from the proverbial cocktail napkin sketch all the way to the foundry's doorstep. Founded in 2003 by Dr. Alissa M. Fitzgerald, AMFitzgerald is now recognized as the leading MEMS product development firm in the emerging area of MEMS design and prototyping services. *page 8*

Semiconductor equipment billings increase 236.0% over May 2009 level. *page 16*



MEPTEC & SMTA PRESENT

Microelectronics Packaging & Test Engineering Council

Surface Mount Technology Association

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Ira A. Fulton Schools of Engineering

ARIZONA STATE UNIVERSITY

2010 Medical Electronics Symposium

Successful Strategies for the Medical Electronics Sector

Wednesday & Thursday • September 22nd & 23rd
Arizona State University • Tempe Campus
Tempe, Arizona

Day One Sessions Include:

- Market Trends and Forecasts in Medical Electronics
- Emerging Materials and Miniaturization Technology
- Component Manufacturing at Chip and Package Level
- Implantables and Wearables in New Diagnostics and Therapies

Day Two Sessions Include:

- Materials and Design at the Board and System Levels
- Systems Assembly and Trends on Captive vs. Outsource
- Product Reliability, Safety and Regulatory Requirements
- Equipment and System Level End Product Applications

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MEPTEC report

Council Update

Volume 14, Number 2
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Welcome to our Summer issue! Of course in our industry summer means *SEMICON West* where this issue is being distributed. This important conference hit a major milestone this year: its 40 years old. Started in 1971, SEMICON West has over the years come to be considered the flagship annual event for the global microelectronics industry.

MEPTEC's next event will be a two-day technical program titled *"Successful Strategies for the Medical Electronics Sector: Steady Growth Keeps the Momentum Moving Forward"* and again will be held jointly with **SMTA** at **Arizona State University**. Scheduled for September 22-23, the symposium will focus on medical electronics and medical device applications and will include the most up to date information about company electronics expertise, practices, technology and applications as it relates to medical electronics. **Dr. Ben Costello** of **Proteus Biomedical** is the keynote speaker, and will be discussing *"Improving Health Care with Intelligent Medicine"*. ASU's **School of Biological and Health Systems Engineering** will co-sponsor this event.

Our Industry Analysis is from **Yole Développement** on *"WLCSP Quietly Edges into #1 Position"*. Written by **Jean-Marc Yannou**, the article explains how WLCSPs became the semiconductor industry's most popular package type of 2009, despite the fact that they comprise only about 6% of all ICs (see page 6). Yole plans to release at a later date dedicated reports on embedded and fan-out WLP.

Our Company Profile this issue is from MEPTEC Corporate member **AMFitzgerald**. Founded in 2003 by **Dr. Alissa M. Fitzgerald**, they are now recognized as the leading provider of engineering services to develop novel MEMS-enabled products. See their story on page 8.

Our feature article is from long-time MEPTEC member **CAD Design Software**, a division of **CAD Design Services, Inc.** In *"Advances in 3D Package Design for Electrical and Thermal Modeling"*, CTO **John Sovinsky** states that the purpose of the article is not to analyze 3D capabilities of every CAD and analysis software, but instead to show cases of 3D CAD design and analysis where it has never been done before. See page 10 for this detailed and informative article.

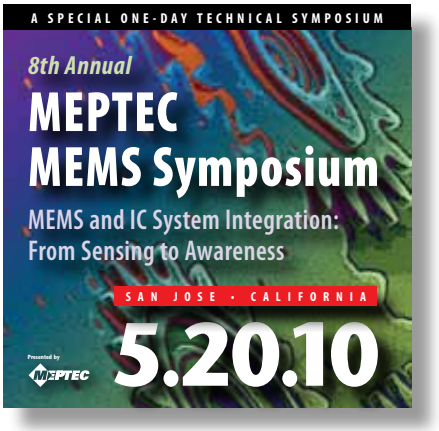
Paul Werbaneth of **Tegal Corporation** opines on our *8th Annual MEMS Technology Symposium, "MEMS and IC System Integration: From Sensing to Awareness"* in *"On the Scene at the MEPTEC MEMS Symposium"* (see page 4). He presents a great follow up of the event in a fun and edifying way. We'd like to thank Paul for the informative yet witty look at this popular annual event.

Our Editorial this issue is especially exciting and interesting (page 22). For those of you keeping track, 2010 marks the 25th anniversary of the founding of **NovaSensor**, one of the first MEMS start-ups, and the only early company to commercialize MEMS in a big way. With the founding of NovaSensor 25 years ago, 1985 is considered now to be the inception year of the MEMS industry. **Dr. Kurt Petersen**, one of the founders of NovaSensor along with **Janusz Bryzek** and **Joe Mallon**, explains in his editorial *"25 Years of MEMS Technology"* that the acronym "MEMS" was not even in the vernacular yet in 1985; it was known then as "micromachining". He tells an amazing story, starting with him waiting at the baggage carousel at San Jose Airport to pick up a box that contained their first funding check of $1.29M. Perhaps Federal Express was not being widely used yet! Beyond doubt, NovaSensor put the MEMS industry on the map. To mark this auspicious anniversary, the three NovaSensor founders, along with **Roger Grace**, key figure in the MEMS industry, are organizing a conference called the ***MEMS Technology Summit***, to be held at and sponsored by **Stanford University** on November 15-16, 2010. The event will be both a technical conference as well as a celebration to honor key contributors to MEMS technology and market development, and hear their views on the future of MEMS. We at MEPTEC are pleased to announce that the founders have asked us to help them coordinate this important event. For information please visit www.meptec.org or contact Bette Cooper at bcooper@meptec.org.

We'd like to thank all of our contributors for making this another great issue. If you're reading the MEPTEC Report for the first time at the Semicon West show, or at another of the many events where we distribute, we hope you enjoy it.

Thanks for reading! ◆

On the Scene at the MEPTEC MEMS Symposium



Paul Werbaneth
VP Marketing and Application
Tegal Corp.

On May 20th MEPTEC held its 8th Annual MEMS Symposium – MEMS and IC System Integration: From Sensing to Awareness. The conference had a little something for everyone notes guest blogger for 3DIncites, Paul Werbaneth, VP marketing and applications, Tegal Corp. Read on for Werbaneth's musings and perceptions of this event, as well as a few others that took place concurrently.

Four compelling events, three disparate locations, two willing travelers, one solid week.

Something had to give for me. And it did. Sorry ***CS MANTECH 2010***. My heart was with you in Portland this week, even while my head was in San Jose. I hope the conference was as wonderful as ever, and that the scruffy Pearl District dude picking out a quiet, wistful tune on his guitar was playing one for Elliott Smith, playing one for me.

So, with my colleague, **Yannick Pilloux**, back east picking up purchase orders, I'm in San Jose at the Wyndham Hotel for the ***MEMS Industry Group METRIC 2010*** meeting, the monthly Bay Area MEMS Social Hour, and the ***MEPTEC MEMS Symposium***.

I'm not a groupie or anything like that, but I seem to be following the Tour of California this week, quite literally, as the tour winds from Sacramento, CA, to Sonoma to San Jose. Note to self: inflate bike tires, dust-off helmet, hit the road!

What of this MEMS – IC integration symposium, put on by the **Microelectronics Packaging and Test Engineer Council**? (Kudos to **Bette Cooper**, by the way, for another well-promoted, smoothly run event.) Well here's one thought: "We finally have a conference on MEMS – IC integration, and the picture has never been less clear," (**John Heck, Intel**). Thank you, John.

But whether you are a MEMS enthusiast, or from the IC-side of the house; whether you like your IC in 3D with a healthy side of TSV (and that's why you're reading this, isn't it?), or if you are just a dog person: there's a little something for everyone coming from the wise perspectives of the "rifle shooting" array of speakers the conference co-chairs brought to the podium.

Opening the symposium, and setting the tone for much of what was to come, **Jeff Perkins** (**Yole Développement**) thinks MEMS component manufacturing is now a "Make-or-Buy" proposition, not "Make-or-Don't-Have". It's the era of the Fab-optional option, to be added to the other standard options of "Real men have fabs" (thank you T.J. Rodgers), Fab-Lite and Fabless. And, with advanced packaging suppliers now offering 3D wafer-level packaging services or otherwise working on 3D WLP w/ TSVs, size reductions in MEMS products can be achieved by leveraging these new OSAT capabilities to push low-cost, two-chip (MEMS and IC) products like microbolometers on Read-Out-ICs, packaged using 3D WLP w/TSV.

Roger Grace, **Roger Grace Associates**, is clearly of the opinion that monolithic integration of MEMS and CMOS system components is on its way down, and that 3D chip stacking is ascending. The commercial drivers here are things like gesture recognition systems (just how am I meant to interact with my Google-Intel-Sony Web TV?), analytical instruments that are hand-held portable, and mesh-network autonomous sensing seismic detection platforms, all of which benefit from the building block (Lego blocks? Erector sets? Lincoln logs?) approach 3D chip stacking begets.

But it's not all rosy in 3D WLP land.

I heard along the way: "Everything we make is a strain gauge, and there is lots of interaction with the package." (**Rob O'Reilly**, **ADI**.)

Meaning, says **John Bloomsburgh**, **Jyve, Inc.**, that "MEMS is subsuming the package, and the package can screw-up the MEMS." Imagine if you will the thermal expansion-related problems arising from a cap – MEMS w/ TSV – ASIC stack combined in the same package. It's a CTE "Chain of Pain" that does no one any good. Fortunately, there are new design tools now available from **Intellisense**, and others, to model WLP MEMS-ASIC integration, break the chain, relieve the pain, and lead us into third-wave industrial MEMS.

Some of the Tour of California support crews (not the riders) stayed in the Wyndham Hotel during their San Jose overnight. I'm looking at these support crew guys today: tanned, lean, fit, sunglassed, sandal-wearing ….. smokers! I guess the pressure gets to you during the tour. It reminds me of a famous photo from an early Tour de France, smoking in the Peleton, back in the pre-helmet era. Too bad it's a lot more complicated than just nicotine these days, eh?

Speaking of bicycling, **Rob O'Reilly** shows us a pretty nifty implementation of how **ADI**'s MEMS sensing technology helps Cannondale mountain bikes read the trail. Trail readers take note: this ADI product (the ADXL78) is a "Complete acceleration measurement system on a single monolithic IC." Rob says the merits of monolithic integration shouldn't be completely discounted; predictability (in areas like start-to-finish in-fab time, and design spin time) has its advantages. Complete integration isn't always the optimum solution, but people do seem to be cycling (ha!) back to monolithic integration, because thinning a MEMS wafer in order to squeeze one more flapjack into a short packaged stack isn't trivial, and maybe you can't afford the line-yield hit you take during MEMS wafer thinning.

Emmanuel Quevy, **Silicon Clocks**, offers the idea that maybe MEMS resonators for timing applications can be functionally integrated in simple integrated components just like passive devices for ESD and EMI protection are today. Imagine a TiPAD – Timing integrated Passive Active Device. More functionality goes from the board to the chip, leaving room for something else on the circuit board, or, making for smaller PCBs. **STMicro** seems to have done well with their iPAD product, and iPDIA are pushing integrated silicon passive components, so why not bring resonators and timing to the party too?

I'm enthusiastic, so I ask someone in the passive device sector their opinion about monolithically incorporating resonators with passives. Like maybe in a silicon interposer, with TSVs?

Shot down! We won't be seeing that product coming anytime soon, I hear. Quartz is still king in the resonator realm - long live Quartz!

Somehow I get to thinking after lunch that my Apple iPhone is great, but what I really want is to train my cellphone to recognize me like my dog recognizes me. Is that too much to imagine? So I ask **Philippe Kahn**, **Fullpower Technologies**, our keynote speaker, about the cellphone and the dog. I didn't know Philippe was the dog lover he is, and that he has ideas on the subject of training smarter phones, having trained his household dog pack to hunt for and find his hidden wallet. "Advanced software is the next frontier for complex sensing solutions," is the gist of Philippe's talk, and if you were to tackle a dog-level pattern recognition software product for sensor-laden cellphones you would probably employ a statistical predictive technique approach to the problem.

I like thinking "It's feasible to think about anything." (**Kenneth Wojciechowski**, **Sandia National Labs**.) And anything could be TSV at **Amkor**. Or stealth dicing for MEMS applications at **Fraunhofer**, who are generally thinking TSV technology to be expensive and risky. Or anything could be cognitive radio (**UC Berkeley**, **Clark Nguyen**), employing massive banks of tuned MEMS filters to implement the cheap, low-power spectrum analyzers cognitive radios need in order to identify which part of the available spectrum is clear of competing traffic and therefore free to use, briefly. Anything could be having MEMS on the inside from a non-MEMS MEMS company (**Jeffrey Hillbert**, **WiSpry**).

Anything could be, to circle back around to **Jeff Perkins**' talk, thinking there's still space for monolithic integration of ICs and MEMS in the product world of today, there's still space for the hybrid approach, and that 3D WLP w/ TSV MEMS – IC system integration has a shot too, commercially speaking. The integration technologies are all there, ready to deliver, and it's mostly a matter of negotiating the integration costs in order to make the business economics work in your favor (besides, of course, doing the engineering).

And that's not such a bad place to be, is it?

From the *8th Annual MEPTEC MEMS Symposium*, thanks for reading. - P.W. ◆

We'd like to thank our media sponsor 3DInCites for covering this event. Paul's blog first appeared on the 3D InCites website on May 25.

INDUSTRY EVENTS CALENDAR

July 13-15, 2010	**Semicon West** San Francisco, California	USA
July 25-30, 2010	**IEEE EMC Symposium** Fort Lauderdale, Florida	USA
Aug 16-19, 2010	**ICEPT - Electronic Packaging Technology** Xi an	China
Aug 24-26, 2010	**VLSI Packaging Workshop** Kyoto	Japan
Aug 25-26, 2010	**MedTec China** Shanghai	China
Aug 31 - Sept 2, 2010	**Nepcon China - Shenzhen** Shenzhen	China
Sept 7-10, 2010	**electronica India** Bangalore	India
Sept 8-10, 2010	**Semicon Taiwan** Taipei	Taiwan
Sept 16, 2010	**GSA Expo** Santa Clara, California	USA
Sept 21-22, 2010	**RF and Microwave Packaging - IMAPS** San Diego, California	USA
Sept 28-30, 2010	PCB West Santa Clara, California	USA
Sept 22-23, 2010	**MEPTEC/SMTA Medical Electronics Symposium** Arizona State University, Tempe, AZ	USA
Sept 28-30, 2010	**Assembly Tech Expo** Rosemont, Illinois	USA
Sept 28-30, 2010	**PCB West** Santa Clara, California	USA
Sept 28-30, 2010	**IMAPS Thermal Management** Palo Alto, California	USA
Oct 3-8, 2010	**EOS / ESD Symposium** Sparks, Nevada	USA
Oct 11 - 14, 2010	**IWLPC - International Wafer Level Packaging** Santa Clara Marriott Hotel, California	USA
Oct 11-14, 2010	**Taitronics** Taipei	Taiwan
Oct 12-15, 2010	**Korea Electronics Show** Seoul, KINTEX	Korea
Oct 13 -14, 2010	**MD&M Medical Design & Manufacturing** Minneapolis, Minnesota	USA
Oct 19-20, 2010	**Thermal Management & Technology** Dallas, Texas	USA
Oct 19-21, 2010	**Semicon Europe** Dresden	Germany
Oct 21-23, 2010	**China Intl IC Industry Exhibition** Shenzhen, China	China
Oct 24-28, 2010	**SMTA International** Orlando, Florida	USA
Oct 31-Nov 4, 2010	**IMAPS Symposium** Raleigh, North Carolina	USA
Nov 8-9, 2010	**SVTC - Test Conference & Exhibition** San Jose, California	USA

Calendar Listings Courtesy Topline. Visit **www.topline.tv/tradeshows.cfm** for more details.

WLCSP Quietly Edges into #1 Position

Yole Provides a 'Primer' on Wafer-Level Packaging Trends

Jean-Marc Yannou
Project Manager, Advanced Packaging & IPDs
Yole Devéloppement

Wafer-level chip-scale packages (WLCSPs) comprise only about 6% of all ICs, yet quietly became the IC industry's most popular type of package in 2009. This just goes to show how many packaging options are out there, Yannou says, but also proves that WLCSP has finally established itself within the industry. WLCSPs are now the fastest-growing package on the market, on target to claim 8.3% of the entire market by 2013.

Background

Wafer-level packages (WLPs) are created through a set of techniques of wafer-level-based assembly operations. This can apply to a variety of process flows for different purposes. The most common form of these process flows is the WLCSP. There are several emerging WLCSP technologies, which encompasses 3D ICs, MEMS devices, and fan-out WLPs. Silicon interposers are also emerging as an enabler for 3D stacking.

Difference Between 'Fan-in' and 'Fan-out'

The well-established WLCSPs, commonly known as "fan-in," are on a R&D track of their own. There are still innovations being made, such as trying to extend the maximum array size of WLCSPs with reliability. "WLCSP is limited to small-sized devices because of reliability; the thermal mismatch between the device and PCB is a serious problem, since the PCB contracts and expands 5x faster with temperature than silicon," explains Yannou. "When you have a direct silicon bonding on the PCB, such as with WLCSP, you want to keep the device as small as possible so the outer bumps won't move too much. The greater the maximum distance between two bumps, the more difficult it is to ensure reliability, because thermal cycling deforms the bumps. This is known as 'solder fatigue.' New dielectric materials and solder alloys and increasingly innovative structures are helping to solve it, though."

Fan-out WLCSPs are relatively new, and based on the principles of wafer reconstitution with known good die, and then wafer molding and redistribution. No package substrate and, consequently, no so-called first-interconnect bumping are required because the package is essentially built on top of a reconstituted wafer. There's a lot of industry interest in this type of package, Yannou notes.

Chip Embedding in Laminate Substrates

Due to observed packaging yield issues, Yannou believes chip embedding or embedded ICs in laminated substrates won't target integration of ICs in motherboards or in complex modules or system-in-packages (SiPs), although it's now considered an alternative to provide "near CSP fan-out packages" with a wafer-level type of balling for single packaged IC-while waiting for assembly yields to stabilize.

Many substrate manufacturers are pursuing this new market opportunity to gain even a small portion of the $30B semiconductor packaging industry. This move isn't an obvious one to make, Yannou says, because it completely shifts their business models.

"Trust must be built for foundries and fabless semiconductor players to rely on PCB players to package their valuable ICs," he notes. "A bridging infrastructure is also needed between the wafers and PCBs to provide for redistribution and interconnect between both. Also, a few high-volume lead applications are needed to prove the capabilities of this technology with good yields and acceptable reliability."

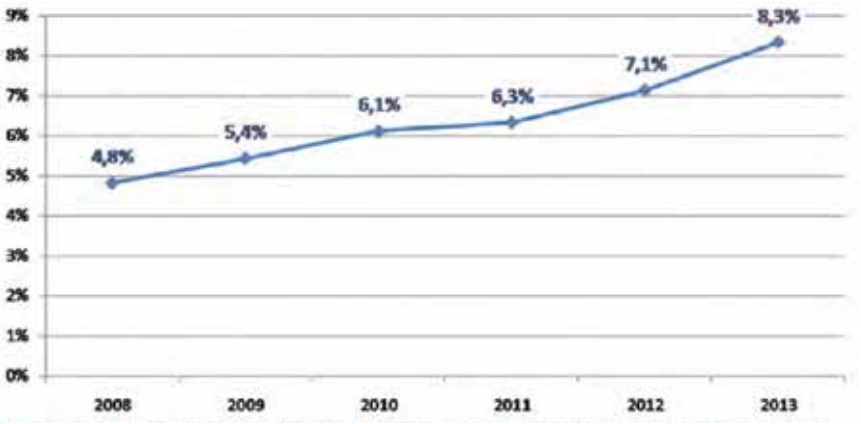
Silicon Interposers

Many industry players are considering using silicon interposers, which are substrates made of silicon with fine-pitch geometries obtained with the usual silicon processing techniques. And now, thanks to TSVs, these substrates can be made in 3D like any other PCB. But Yannou says that the cost is 5 to 10x per surface area more than a regular organic PCB.

History/Timeline

Back in 2000, when WLCSP began production, it was almost exclusively used in integrated passive devices (IPDs) for EDS/EMI interface conditioning on 6-in. wafers, and most of its production

'Fan-In' WLP penetration rate into overall IC Packaging (In Units)



'Fan-In' WLP is undoubtedly the current fastest growing package type in the whole IC packaging industry!

Source: Yole Développement, WLP report, 2009

has remained on 6-in. wafers. "This is captive production," notes Yannou.

By around 2005, WLCSP spread to other analog functions such as DC/DC converters, driver ICs for displays, LEDs, audio codecs, amplifier, etc., mainly on 6-in. and 8-in. wafers. While some of it is packaged internally by IDMs, according to Yannou, most of it is outsourced.

More recently, CMOS production started using WLCSP. This is primarily for digital+RF system-on-chips (SoCs) used in connectivity in the form of Bluetooth, WiFi, GPS, etc. "These are 8-in. and 12-in. wafers," Yannou points out. "This trend was driven by fabless companies like CSR, which weren't bound to any production lines and the need to amortize them as a way to differentiate themselves from the competition. Integrated companies such as STMicroelectronics kept lagging behind because they had broad TFBGA capacity." Due to the growing demand, Yannou is already seeing what appears to be a capacity shortage on 12-in. WLCSP service production in 2010.

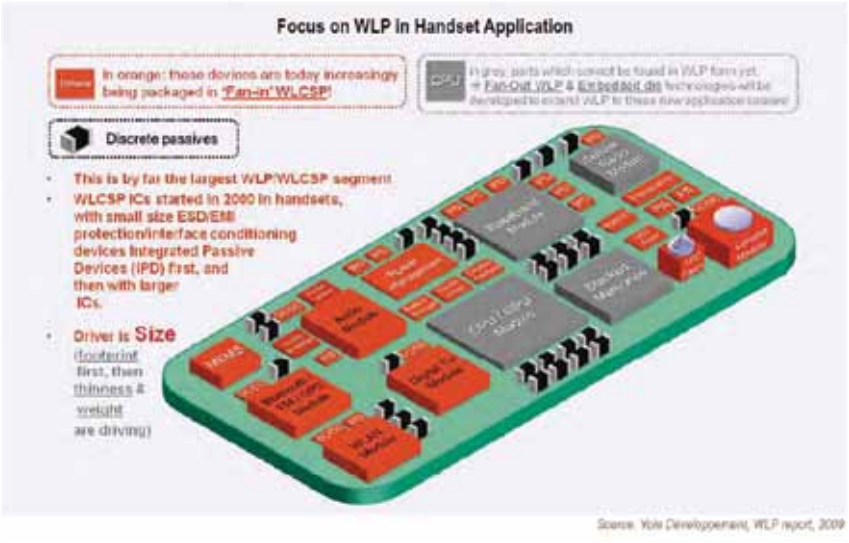
Cost No Longer a 'Roadblock'

Size and miniaturization, as well as performance, are the historic market drivers for WLCSP, Yannou notes. But the cost of fan-in WLCSP is no longer a roadblock to high-volume applications. Nokia paved the way, but Tier 2 handset manufacturers recently started to buy and mount WLCSP solutions on their boards.

Decreasing costs are helping make this a mainstream platform now, he says. "It took about 10 years to amortize the equipment," he explains. "The first factories to get into WLP have amortized their loans and are now seeing more competition than ever. Many companies are proposing WL services they weren't previously offering. This competition is such that the margins are lower for OSATs. On the other hand, however, it benefits the IDMs and other customers, so it makes WLCSP truly competitive with respect to other packages like QFNs, SOTs, and smaller BGAs like TFBGA."

Yannou believes cost is coming down for 6-in. and 8-in. wafers, but not much yet for 12-in. wafers, which still have rather high margins.

"... The cost of fan-in WLCSP is no longer a roadblock to high-volume applications..." says Jean-Marc Yannou, Project Manager at Yole Développement.



"The cost of a simple WLCSP (or fan-in package) is in the range of 15 to 40¢ per pin. This is the cost for high-volume manufacturing of more than 100,000 units per month," he says. "And that price doesn't include final test. The reason why this range is quite wide is based on several factors. One is that you can have different I/O densities. The most common one is 0.5mm, but it now goes down to 0.4mm, or even 0.3mm pitch, which means you can place more I/Os per surface area. And because this is a wafer batch type of operation, the price per pin will be lower with higher I/O density. On the other hand, the total cost of the package solution isn't necessarily lower-that's an important point. It's not necessarily lower just because you shift to a smaller pitch, because this means a higher-cost PCB for the customer. So the cost per pin has been proposed by the OSAT because the range I mentioned is what an IDM will pay to get ICs packaged by the OSAT. It's a cost margin, a price basically. For an IDM with a smaller pitch, for example, it'll be cheaper, but for the customer of the IDM (the OEM), going to smaller pitches isn't cheaper because they have to pay more for higher-density PCBs, which are expensive."

Another parameter Yannou sees as very important in the cost structure of WLCSP is the number of layers in the redistribution. It's usually one or two; in more than 90% of cases it's one. That's why most packages are in the lower end of that cost range. The actual cost of fan-in WLP is more in the range of 15 to 25¢ per pin, he says. There are other options that add to the cost structure, such as depositing a backside protection on the wafer so that after singulation it's protected with an epoxy-type of resin.

"And of course yields are very important too, because one of the biggest drawbacks of this package is that the work is done at wafer-level, so nothing is tested before packaging," he explains. "For all other package platforms, the units are singulated prior to packaging. With WLPs, you pay at the wafer-level whether the unit is good or scrap. So you need to get good yields on your device wafer to get a lower price per pin in the end."

Emerging Applications

WLP can address essentially all ICs within handsets, except basebands, CPU/GPU module, and memories. Two key new applications are laptops and netbooks. "These use TSVs for CMOS image sensors, which is another form of WLP that's becoming very popular as well. And MEMS packaging is encompassing WLP more and more, and we're seeing a more than 40% compound annual growth rate (CAGR) for MEMS packaging, so that's another good growth area. New WLP devices in automotive and industrial applications for ICs are another strong growth area, as well as MEMS and sensors, and we'll likely see others," Yannou predicts.

Yole plans to release dedicated reports on embedded WLP and fan-out WLP at a later date. ◆

Jean-Marc Yannou is a technology and market expert in the fields of advanced packaging and IPDs at Yole Devéloppement. He has 15 years experience in the semiconductor industry, and has worked at TI and Philips (then NXP). Jean-Marc Yannou may be contacted at yannou@yole.fr.

AMFITZGERALD & ASSOCIATES

The leading provider of engineering services to clients developing novel MEMS-enabled products

If a company wants to design a new MEMS product, to whom should it turn for assistance? The answer that first leaps to mind is a MEMS foundry. After all, MEMS foundries advertise and market prototyping and product development services.

But the reality is that foundries only support late stage development efforts, in the ramp up to volume production. Foundry engineers are focused on supporting production customers and solving the technical problems of volume manufacturing, such as yield improvement and process recipe characterization and monitoring. These are a foundry's true strengths, and it is quite a different skill set from that needed for new device development. Furthermore, the foundry's business model hinges on wafer production, not non-recurring engineering (NRE) charges. A customer with an early stage development project, who is working from either a concept or a university prototype, and who has an uncertain timeline to production, will find that the foundries are uninterested in their business or simply unable to support them.

AMFitzgerald & Associates, a MEMS product development firm located in Burlingame, CA, bridges this gap between new product concept and foundry production. The company offers fully integrated engineering services to get a client from the proverbial cocktail napkin sketch all the way to the foundry's doorstep. Founded in 2003 by Dr. Alissa M. Fitzgerald, AMFitzgerald is now recognized as the leading MEMS product development firm in the emerging area of MEMS design and prototyping services. To date, the firm has served over 70 customers of all sizes and has developed new MEMS products for applications as diverse as: long wavelength infrared imaging, tissue scaffolds, microphones, biological and chemical sensors, pressure sensors and optical waveguide switches.

Successful MEMS Development Requires Skilled Engineers

The MEMS industry, despite its semiconductor heritage, is still quite young, and as such, is missing many of the sophisticated capabilities enjoyed by the semiconductor industry. Thanks to powerful (and verified) electronic design automation (EDA) tools, foundry-specific design rules and kits, and standardized fabrication processes, an ASIC designer can sit at his computer, design and completely verify a new chip layout, tape out to a foundry, and receive high-yielding, functioning silicon chips in less than 12 weeks.

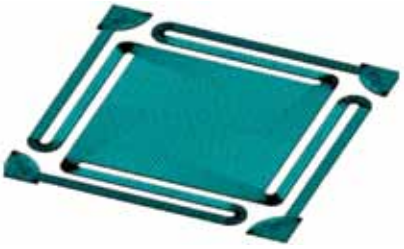
This fast and high fidelity design process is not yet possible in MEMS. One of the missing links is EDA; although several MEMS-specific EDA tools exist on the market, they do not yet provide the end-to-end simulation capability available to the IC industry.

It is hardly the fault of EDA software suppliers – the problem is the nature of MEMS themselves. MEMS are mechanical devices, whose vertical (Z-axis) architecture dictates process flow, and for which process details such as sidewall angle, roughness or etch undercut can have a profound impact on device performance. Furthermore, MEMS processes are not standardized and the material properties of thin films vary widely by foundry, tool and recipe. Process and layout design rules are difficult to quantify because so many key MEMS processes (deep reactive ion etch, in particular) are extremely sensitive to multiple variables such as pattern load factor, linewidth and location on the wafer.

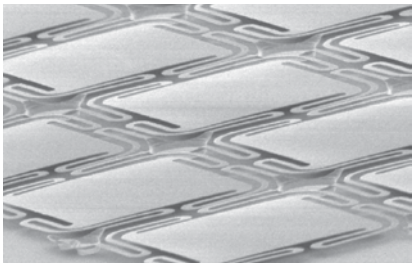
The net result is that successful MEMS design requires highly skilled engineers who are cognizant of the complex interactions between coupled-physics behavior (e.g. structural-thermal-electrostatic interactions) and process limitations, who can fill in the gaps left by MEMS EDA tools. New MEMS development takes months to years, not weeks, since multiple design-fabricate-test cycles are mandatory to converge and finalize a new product design.

Unique Design and Simulation Capabilities

AMFitzgerald's unique capabilities for MEMS design are rooted in the deep process experience of its staff. All engineers have a minimum of two years of hands-on MEMS processing experience, and the senior staff members have over six years. The unwritten design rules of MEMS have been learned through years of process experience, looking through microscopes, making measurements, and learning first-hand what works and what doesn't. AMFitzgerald staff engineers can quickly take a client's concept sketch and develop it into a full mask layout, process flow and fabrication runsheet.



ANSYS model of a pixel from an infrared imaging array.



Fabricated infrared imager pixel array.

As needed, designs are optimized and validated using ANSYS Multiphysics, an industry standard finite element (FE) simulation tool. Modeling MEMS devices requires understanding of micro-scale phenomena that are not commonly known to general FE practitioners. Simulation may be used to examine sensitivity to design variables, explore the effects of process variation, evaluate design rules, and to develop more focused Design of Experiment fab runs. AMFitzgerald's FE analysis techniques, when applied concurrently with prototype development efforts, can reduce the number of process runs required to converge and verify a new MEMS design.

Reliability Prediction and Materials Testing

The company has also developed a proprietary methodology and software tool to predict the reliability and fracture load limits of MEMS and other microstructures such as through-silicon vias (TSV), 3D stacked chips, optoelectronics and photovoltaic cells. The tool can predict where a brittle structure is most likely to break and under what conditions, significantly shortening design cycle time and saving money.

The reliability prediction method is a two step process: first, the physical effect that a

manufacturing process has on the silicon surface (and therefore its strength) is quantified using test structures. This provides information that is specific to a particular process on a particular tool. By design, the customer's proprietary process details do not need to be revealed.

Next, the stresses in devices under load are modeled. Using ANSYS Multiphysics, we can model any type of load input, such as thermal, electrostatic, shock, or sinusoidal. Load limits and failure points are then predicted by combining stress simulations with knowledge of surface strength obtained from test structures.

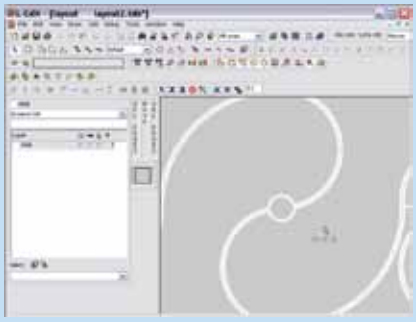
AMFitzgerald's test equipment is also available for basic material properties measurements, such as stress-strain curves, shear tests, tensile strength, etc. on both brittle and ductile materials.

Prototype Fabrication by Expert Process Engineers

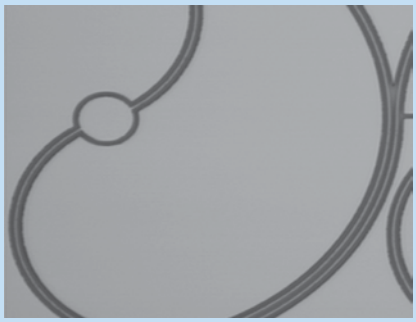
One of AMFitzgerald's main values and strategic advantages to customers is its ability to quickly fabricate small quantities of prototypes. The first prototypes are often the most challenging, but they are also where the most learning and insight can be gained.

The company's own expert process engineers perform the fabrication work. Because AMFitzgerald's engineers are doing the fabrication work, they can apply their experience and judgment to make design and process adjustments on the fly, enabling a faster and cheaper path to a successful prototype.

Prototyping work is performed at the UC Berkeley Microlab, where AMFitzgerald is an industrial member company. Prototypes may be fabricated on 100 mm or 150 mm wafers, with most customers preferring the latter in order to access more modern tools and to ease the future transition to foundry (most MEMS foundries operate on 150 mm wafers).



From Mask Layout



To Prototype

AMFitzgerald's staff control all wafer and mask movement within the fab in order to protect its customers' intellectual property. The university has no access to nor claim over any work product developed in the facility.

Using this world-class research facility enables cost-effective small batch production and process versatility. While quality control and tool performance can not match that of a production MEMS foundry, at the prototyping phase, it does not need to. The focus of a prototyping effort is to establish a baseline robust process and a functional design. Perfection of a process is best performed by a foundry during late stage development.

Foundry Selection and Transfer

When a prototype is ready for volume manufacturing, AMFitzgerald works with its customers to select the right foundry partner and to transfer the new MEMS technology. Choosing a foundry is a critical business decision; a bad choice can cost millions of dollars and years of delay because processes are not easily ported from one foundry to another. Each MEMS foundry has its process strengths and weaknesses, so engineering due diligence of each candidate foundry is a must.

Customers from outside of the MEMS industry are typically not well-equipped to conduct this level of diligence simply because they are unfamiliar with the process technology. AMFitzgerald can serve as the customer's liaison and will determine which foundry is the best fit for a specific process flow, product, and manufacturing volumes. Although the company enjoys good relations with all of the major MEMS foundries, it does not have any sales or commission relationships, in order to maintain its independence and impartiality. AMFitzgerald represents only its customer's best interests in the interaction and transaction with a foundry.

At the end of a MEMS development project, AMFitzgerald's final task is to transfer the knowledge base to the selected foundry's engineers. All mask data files, runsheets, lessons learned and in-process metrology requirements are transferred and if needed, engineering support is provided to the foundry during pilot batch fabrication.

The transfer to and interaction with the foundry's engineers provides excellent value to both parties: the customer enjoys a lower NRE charge for bringing a developed design and process and a faster transition; the foundry benefits from the wealth of process information provided, which minimizes their cost and technical risks and enables faster and more efficient production ramp-up.

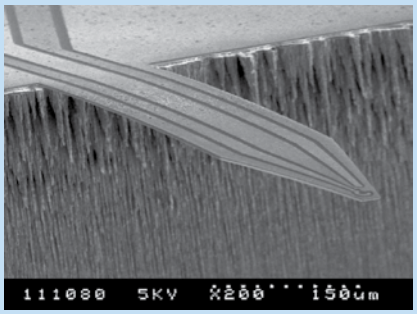
MEMS Product Development

In summary, the firm's integrated engineering services enable it to provide unique and comprehensive product development support to customers developing novel MEMS products.

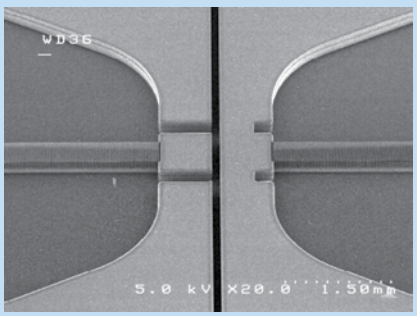
To learn more about AMFitzgerald & Associates and how they can help with your MEMS product development effort, please visit the company website: www.amfitzgerald.com. ◆

Gallery of prototypes designed and fabricated by AM Fitzgerald.

A dense array of 10 micron diameter pillars for a tissue engineering application.



A micro-cantilever customized for materials science measurements.



A microfluidic chip for a blood analysis product.

Advances in 3D Package Design for Electrical and Thermal Modeling

John Sovinsky
CTO, CAD Design Software
A division of CAD Design Services, Inc.

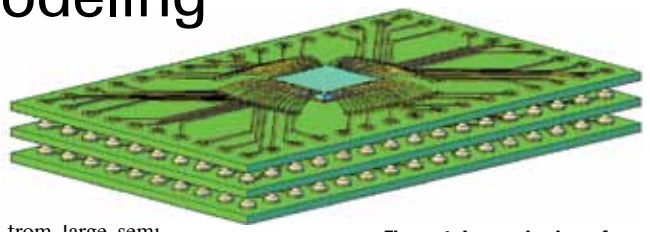


Figure 1. Isometric view of 3 stacked substrates in the CAD software.

Until now most BGA and Lead Frame package designs were done in 2D and modeled in 2-1/2 D. This is partly due to the limitations inherent in most currently available package design software. It is impossible to export the 2-1/2D final data that is typical of most package design tools as suitable 3D models in 3D analysis tools, especially in the case of lead frames.

With lead frame packaging, for instance, a large gap exists between the three dimensional reality of Lead Frames and the way most simulation software portrays them. This limitation is in some cases, a shortcoming with the linkage between the CAD software and the Analysis software.

It is not the purpose of this article to analyze the 3D capabilities of every CAD and Analysis software, but to show some cases of 3D CAD design and analysis where the ideal full 3D model has been fully accomplished, where it has never been done before. These cases represent significant advances in 3D package design for Electrical and Thermal modeling.

About EPD

EPD is a complete Semiconductor Packaging design system that runs on top of AutoCAD and is capable of doing Wire Bonded BGAs, FlipChip BGAs, Wire Bonded Lead Frames, Stacked Dies, Stacked Packages and all types of printed circuit boards on any substrate including all types of ceramic technologies. EPD is capable of unlimited geometries and can be adapted to integrate new technologies quickly.

The Electronics Packaging Designer (EPD) software suites available from CAD Design Software addresses and overcomes the limitations caused by the lack of 3D design software. EPD runs on top of the well known AutoCAD graphics engine which has advanced 3D capabilities. Examples in this document show some of the capabilities of this versatile tool.

Stacked Substrates

Stacked packaging is an emerging technology that is growing, but not yet widely used partly due to the lack of accurate analysis models. Figure 1 shows an isometric view of a typical Package on Package (POP) design. Design managers from large semiconductor OEMs claim that they would not try to manufacture a device they could not simulate before fabricating. For high-speed and power devices simulating the substrates separately and merging the results together cannot achieve the accuracy of modeling and simulation of the entire physical structure, which is only available with intelligent design. EPD enables seamless interface of design, modeling and simulation platforms for short development schedules as well as cost savings through automated optimization routines and software integration.

The ideal way to simulate a stacked substrate package is as one continuous 3D model. This is accomplished, for instance, in EPD using the Package on Package (POP) module. This software will stack any combination of multiple substrates using interposers such as balls or micro-pillars, to create a single composite substrate. Example: four stacked four-layer substrates now appear as a single sixteen-layer substrate which can be modified and optimized simultaneously in the CAD tool. Optimizations and simulations are accomplished as if the stacked substrates were a single substrate. When the POP layout is fully designed each substrate can be extracted into a separate fabrication job. Figure 2 shows a typical three-layer 3D model in EPD.

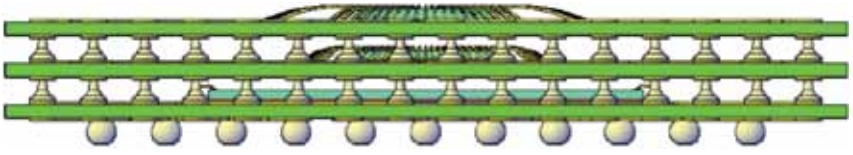


Figure 2. Side view of 3 stacked substrates in the EPD software. The physical parameters of all structures including wirebonds, PoP vertical interconnects, planes, traces and vias can be exported directly into many popular modeling and analysis software.

A thermal or electrical simulation will be accurate only if the CAD tool is able to produce all geometries accurately. Workarounds are typically used to get a design to fabrication, yet do not create an accurate image for 3D purposes and will produce inaccurate simulation results. Therefore, the CAD tool must be fully capable of accurately capturing all 3D geometries.

Imbedded actives and passives can be placed on any level facing up or down. Cavities may be used on any substrate level to any depth with shelves for internal wire bonding and discrete component mounting. A complete 3D image with slopes and arcs may be automatically generated within the EPD environment. This data can be exported as an ACIS or Step file for use by thermal/mechanical analysis software such as Ansys, Cosmos, FloTHERM® and others.

The ACIS file may also be imported into electrical analysis software but EPD provides a more efficient and accurate method. EPD can automatically generate a file that can be extracted in your analysis tool which creates a full 3D electrical model. Ports may

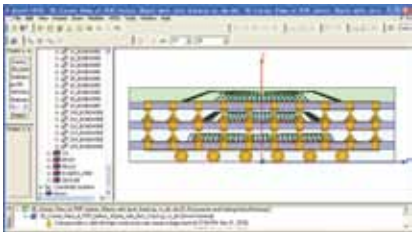


Figure 3. 3D model of 3 stacked substrates in Ansoft HFSS electromagnetic modeling and simulation program. The 3D information was imported from EPD design output.

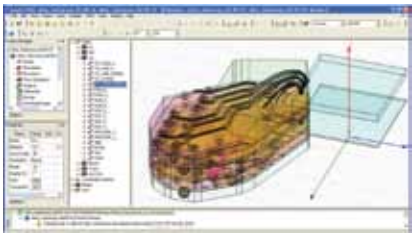


Figure 4. Isometric view of a cookie cut of a 2 stacked substrates in the HFSS Full Wave Solver.

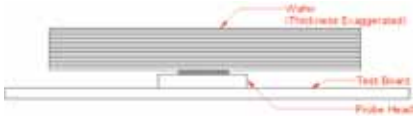


Figure 5. A model to simultaneously simulate the Die, Probe Head and Probe PCB.

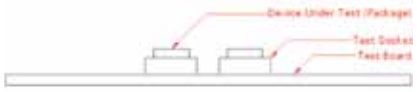


Figure 6. A model to simultaneously simulate the Die, Package, Test Socket and Test (Load) PCB.

be automatically generated and exported into the file along with their parameters. Currently, full 3D models may be exported to Ansoft's HFSS and Q3D and CST's Microwave Studio via a Visual Basic Script (.vbs). CAD Design Software is continually adding more modeling, simulation and analysis programs to our export list. Figures 3 and 4 show models imported into Ansoft HFSS directly from the EPD design environment.

Stacking the Device Under Test (DUT) with Its Test Structures

To be certain that a die will perform to specification it must be tested twice, once before dicing from the wafer, see Figure 5, and again after packaging, see Figure 6. If the both test structures can't play together with the die then the die will have to be changed and new tooling made. To avoid this huge expense and delay in the schedule both test systems can be simulated after using the POP software to make a complete 3D model.

In the case of Probe testing the POP software is used to stack the die (while still part of the wafer), the Probe head and the Probe PCB. This will then be seen as one substrate and can be simultaneously sent to simulation.

In the case of Final (Load) testing the POP software is used to stack the Packaged Chip (DUT), the Test Socket and the Test (Load) Board. This will then be seen as one substrate and can be simultaneously sent to simulation.

Lead Frame Packaging - *The Only Fully Intelligent Lead Frame Design Tool*

CDS's Lead Frame designer handles all types of lead frame designs with full electrical and parametric mechanical intelligence. An advanced optimizing editor automatically selects the best combination of many parameters to reduce gold bond wire usage for lowest cost, a task that would take a designer literally 100's of hours to complete.

EPD can create new designs using parametric QFN and QFP lead frame programs with automatic die placement and wiring bonding functions or automatically intelligize existing designs. After intelligization the design can be edited using our advanced optimizing editor which is over 100 times faster than manual editing. EPD can mount single die, MCM, and single or multiple side by side die stacks with stack-to-stack bond

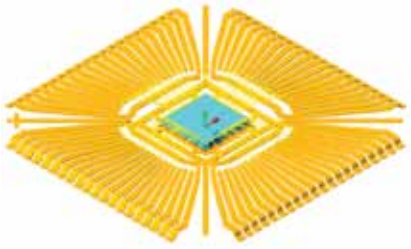


Figure 7. Isometric view of a Lead Frame in the CAD System.

Figure 8. Side view of a Lead Frame Design in the CAD System.

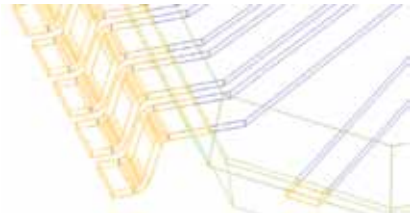


Figure 9. Isometric wireframe model.

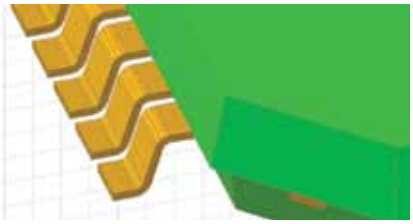


Figure 10. Isometric filled model.

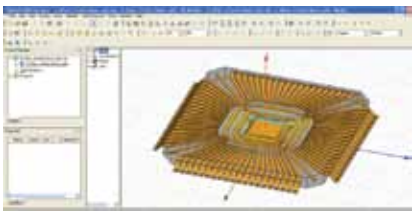


Figure 11. Isometric view of a 3D model in Ansoft's Q3D.

wires and/or flip-chip interconnects.

EPD can generate full 3D models of any lead frame design including bond wires and export the 3D electrical model to Ansoft HFSS or Microwave Office CST for full wave analysis or to Ansoft Q3D for parasitic extraction. Exporting ACIS or STEP models to thermal analysis tools is easy and 3D bond wires can be modeled using a dynamic profile system or using the JEDEC standard. Figures 7 through 11 show examples of 3D models generated by EPD.

The CAM-Links System

A need exists in the electronics industry for a way to transfer designs between any design software and any modeling, analysis and simulation software in 3D. If such tool existed it would save immeasurable time in product development.

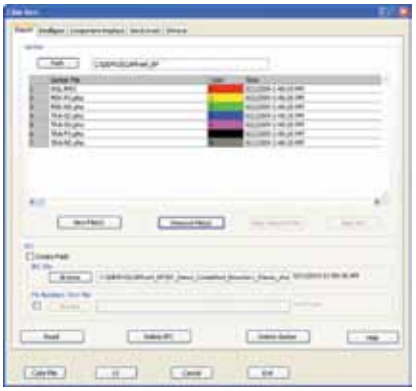


Figure 12. The Import folder is used to select the RS274X Gerber and IPC net list files.

Until now specialized software providing a link between design and analysis tools has not been commonly available. When translating data files from design to analysis tools you may be looking forward to one of the following unpleasant tasks:

1. Reading the design's DXF data into the analysis tool and using the capabilities of the analysis tool to extrude or otherwise convert it into a crude 2-1/2D model.

2. Redrawing the parts of the model you need to analyze directly inside the analysis tool and creating the ports

EPD CAM-Links can read CAM data (RS274X Gerber files and IPC-D-256A Net List) from any PCB or package layout software into EPD for use in advanced DRC and 3D functions. After reading in and intelligizing the CAM data the full suite of advanced editing features available in EPD can be used. If die and wire bonding are present in the design, integrated tools convert the entities to EPD format for further edit or optimization. The optimized design data can be exported as a 3D design directly to many electrical and thermal analysis tools. Figure 12 shows the import folder control panel.

New Development: Creating an Analysis model of stacked TSV Die

A new module is being developed that enables CAD data import from various sources such that each element becomes a substrate compatible with the POP stacking software. This allows the generation of a model of a TSV die stack with optional interposers including the package substrate and evaluation PCB. This function enables modification on individual substrates while maintaining location and connectivity with the entire stackup. Figure 13 shows the design flow for TSV stacked die using EPD.

Chip data may be imported from open access data. After the die are stacked using a POP approach, the net list (automatically generated from the system schematic) is read in. Silicon interposers are routed by turning the guides (rats, unroutes) into routes using manual and automatic routing commands.

The entire stack is now ready to generate a full 3D simulation model. Figure 14 shows a contiguous equivalent circuit path through a TSV stack including silicon and interposer routes, package substrate and PCB routes achievable with EPD.

Summary

High levels of integration and miniaturization require advanced tools to assure performance, cost and efficiency in manufacturing. The integration of software tools that best fit the company needs may require various suppliers and incompatible software. Interfacing design, modeling, and analysis and simulation tools from one program to another is not straightforward and iterating design modifications can take time and effort creating unexpected costs and delayed schedules for product development. CAD Design Software's EPD suite capabilities have been reviewed and applied to practical problems facing design organizations across a wide range of high-technology industries. EPD provides an integrated design platform with the capability to interface with CAD/CAM/CAE, thermo-mechanical and electrical tools, layout and manufacturing systems. EPD is bridging the gap for next generation product design integration and optimization. ◆

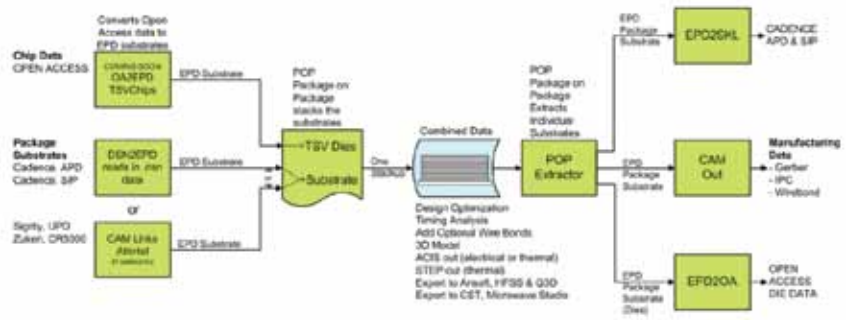


Figure 13. EPD flow diagram for combining die and substrates into one analysis model followed by extraction for further processing, and manufacturing.

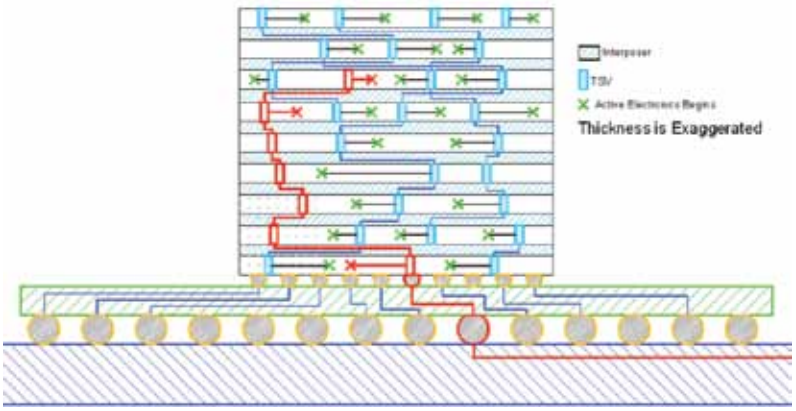


Figure 14. Diagram showing model of TSV Stacked Dies on a Package Substrate and PCB.

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National Semi and GESOLAR Develop Smart Solar Panels

MUNICH - National Semiconductor and Green Energy Solar, a leading provider of solar energy products and services, have developed GESOLAR brand modules with embedded SolarMagic™ power optimization technology from National.

The award-winning SolarMagic product line combines National's unique expertise in power electronics with advanced monitoring and management capabilities to maximize energy capture across a solar installation. GESOLAR's high-efficiency polycrystalline photovoltaic modules incorporate SolarMagic power optimization to offer an affordable "smart panel" solution to the underperformance issues common with solar energy installations.

National's SolarMagic SM3320 is the first analog-intensive power management chipset in a new category of in-panel electronics that improves power output, reliability and cost-effectiveness of solar systems. SolarMagic enables each solar panel to produce the maximum energy regardless of whether other panels in the array are under-performing due to mismatch. In worldwide tests, SolarMagic can recoup up to 71 percent of power lost to mismatch – regardless of cell technology – giving installation owners more predictable power output and increased return on investment.

Additional information is available at www.gesolar-power.com and www.national.com.

STATS ChipPAC Drives Innovation in Low Cost Flip Chip Technology with Copper Column Bump

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced that its low cost flip chip (LCFC) technology now utilizes copper column bump to deliver a powerful packaging solution at a dramatically reduced cost for its customers.

STATS ChipPAC's LCFC technology, introduced in 2009, has offered semiconductor companies the opportunity to have flip chip packages at price points below wire bond packaging due to its innovative routing efficient interconnection structure, simplified substrate design and cost effective mold underfill process. The unique structure of LCFC when combined with copper column bump achieves an even lower cost solution with higher routing densities and is scalable to finer bump pitches.

As technology continues to move toward finer silicon nodes to achieve increased functionality, input/output (I/O) densities are steadily increasing. The use of conventional solder bump makes the chip attach and underfill processes become more challenging and there is potentially an increased risk of electromigration due to the higher current density induced by the scaling of features. Copper column bumps enable a higher I/O density with a much finer pitch between the columns than standard solder bumps along with a higher resistance to electromigration. Although copper column is a hard bump material that can typically cause damage to low K (ELK) layers in finer silicon nodes, the LCFC interconnect structure dramatically reduces the mechanical stress on silicon sub-surface layers resulting in the elimination of the low K damage phenomenon commonly observed in sub-45 nm silicon modes.

Further information is available at www.statschippac.com.

Unisem Introduces New High Density Leadframe Based Packaging Using TL Li Technology

KUALA LUMPUR, MALAYSIA – Unisem has announced the introduction of a new high density leadframe packaging technology, the Leadframe Grid Array (LFGA). This latest offering, developed by TL Li, the founder and major shareholder of QPL International Holdings Limited, and pending for patent, is a solution that offers I/O densities traditionally only found in ball grid array packages, yet it uses a much more cost effective material set.

As consumer electronics continue to become more and more complex, semiconductor manufacturers also continue to push the demand for a reduced cost packaging solution. The LFGA package provides the best of both worlds with a high density, fully populated array of I/O's attached to a leadframe based on their patented leadframe design and etched leadframe process. In fact the routing density of the LFGA makes it a great replacement for a 2 layer FBGA package.

Other key benefits of the LFGA package are its shorter bond wire lengths compared to standard QFN packaging which not only helps improve the electrical performance, but also helps to reduce material costs. Package footprint reduction is also benefit with the LFGA package's ability to take a 10x10, 72 lead QFN package down to 5.5 squared body size. Finally, the LFGA offers a higher MSL level due to the absence of organic materials in the interface of mold compound and leadframe.

The LFGA package is available now in small quantities for

customer evaluation.

For more information visit www.unisemgroup.com.

Gartner Says Worldwide Semiconductor Revenue to Grow 27 Percent in 2010

STAMFORD, CT – Worldwide semiconductor revenue in 2010 is forecast to reach $290 billion in 2010, a 27.1 percent increase from 2009 revenue of $228 billion, according to the latest outlook by Gartner, Inc.

The outlook for the semiconductor industry has improved from Gartner's first quarter 2010 forecast, when it projected worldwide semiconductor sales to grow 19.9 percent. Analysts said this improvement in market conditions is in part due to an accelerated broad-based recovery in all regions and most product categories.

"Sequential semiconductor growth has been very strong over the last five quarters, well above seasonal norms, and manufacturing capacity is tight" said Bryan Lewis, research vice president at Gartner. "Chip revenue growth is clearly outpacing system revenue growth and that is a concern. Gartner's new semiconductor forecast has below-average growth in the second half of 2010 as we are anticipating a minor correction to realign semiconductor sales with electronic system sales. Even with this minor correction, we are still expecting very strong growth and record semiconductor sales in 2010."

In this quarter's update, Gartner raised production forecasts for PCs, mobile phones, automotive and select consumer products. The PC and mobile phone markets will account for about 40 percent of the semiconductor market's growth in 2010. In the PC market, processor average selling prices (ASPs) are firming, and 2010 PC processor revenue is now expected to grow 15.5 percent, up from 10.0 percent in the previous update.

Strong PC growth coupled with rising DRAM prices is causing the 2010 DRAM market to surge 78 percent, making it the strongest-performing semiconductor device market. Analysts believe that the demand for media tablets, such as Apple's iPad, will noticeably impact the PC market by 2013, further fueling growth in this category. However, in the near-term, these devices will have a minimal impact on PC and smartphone markets.

Gartner analysts expect the semiconductor industry to show continued growth through its forecast period in 2014. The market is on track to surpass the $300 billion mark in 2011, when the market is forecast to total $307 billion.

For more information, visit gartner.com.

Sonoscan Acoustic Imaging Inspects MEMS Cavity Seal Integrity

ELK GROVE VILLAGE, IL – As part of its bonded wafer inspection technology, Sonoscan has recently demonstrated acoustic imaging of defects in the seal that surrounds and protects the cavities in MEMS devices.

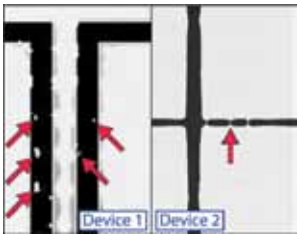
The defects most frequently take the form of voids (Device 1 shown at right) within the seal, which may be direct Si, metallic, glass or polymer, depending on the reliability level of hermetic seal required as per SEMI MS8-0309. In some locations on a wafer the seal may be breached (Device 2 shown at right). Another frequent defect is delamination of the seal from one or both substrates, the result of poor wetting or contamination during fabrication.

The defects are risky because thermal and mechanical stresses can cause them to grow until they cause a leak in the seal and the subsequent loss of the desired atmosphere within the cavity. The seal prevents outside particles, gases and humidity from reaching the cavity. Humidity, for example, can result in freezing up of moving parts within the cavity.

Defects in the seal may be only a few tens of microns in diameter and of sub-micron thickness, but can be imaged by Sonoscan's C-SAM® systems because they represent a gap that reflects >99.99% of the VHF/UHF ultrasonic pulse.

In production, a percentage of MEMS devices may be imaged with C-SAM acoustic micro imaging systems in order to verify that process parameters are preventing the formation of voids. Where high reliability is essential, as in mil/aero or medical MEMS, 100% of devices may be inspected.

For information on inspection services contact SonoLab manager Ray Thomas at 847-437-6400 x 245. For more information on inspection systems contact technical marketing manager Steve Martell at 847-437-6400 x 240.



Sonoscan acoustic images of voids (left) and a breached seal (right) in MEMS devices before wafer dicing.

North American Semiconductor Equipment Industry Posts May 2010 Book-To-Bill Ratio of 1.12

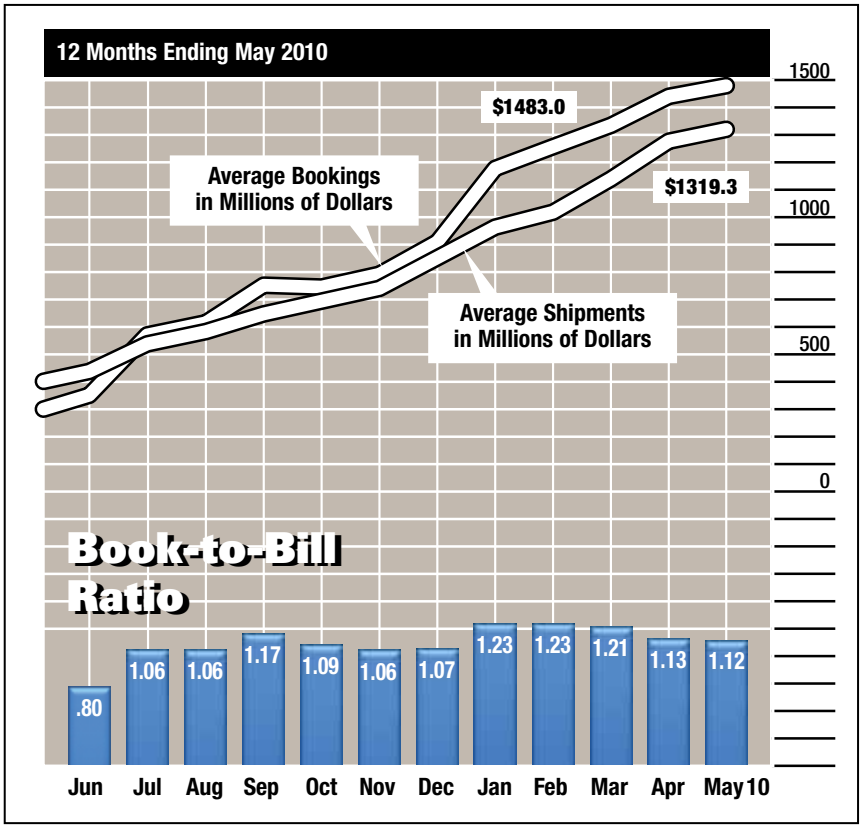
SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted $1.48 billion in orders in May 2010 (three-month average basis) and a book-to-bill ratio of 1.12, according to the May 2010 Book-to-Bill Report published by SEMI. A book-to-bill of 1.12 means that $112 worth of orders was received for every $100 of product billed for the month.

The three-month average of worldwide bookings in May 2010 was $1.48 billion. The bookings figure is up 2.8 percent from the final April 2010 level of $1.44 billion, and is 415.3 percent above the $287.8 million in orders posted in May 2009.

The three-month average of worldwide billings in May 2010 was $1.32 billion. The billings figure is up 3.1 % from the final April 2010 level of $1.28 billion, and is 236.0 % above the May 2009 billings level of $392.6 million.

"Orders have increased for 14 consecutive months, commensurate with the turnaround in the market and the increase in announced capital spending plans," said Stanley T. Myers, president and CEO of SEMI. "SEMI members throughout the supply chain are working hard to fulfill customer orders and meet this rising demand."

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average shipments. Shipments and bookings figures are in millions of U.S. dollars. ◆



SUSS Tackles the LED Market with Dedicated Lithography System

GARCHING, GERMANY – SUSS MicroTec has introduced the next generation of its MA100e mask aligner, a dedicated lithography solution for manufacturing high-brightness light emitting diodes (HB-LEDs). Based on SUSS MicroTec's production proven mask aligner design the automatic MA100e Gen2 processes wafers up to 4 inches and enables an industry leading throughput of 145 wafers per hour with reduced cycle times. LED equipment manufacturers will need to support the significant growth of LED production that is driven by the exploding demand for LED backlighting for televisions, monitors and other systems. With the MA100e Gen2 SUSS MicroTec has designed a highly competitive automatic mask aligner solution that meets the cost-sensitive technology requirements of the LED industry. High-intensity exposure optics and pre-alignment options shorten precious process time while functionalities like proximity exposure for high resolution down to 2.5 μm maximize yield and cost-efficiency. The MA100e Gen2 provides exceptional process scalability and fast time-to-market for new device designs.

For more information visit www.suss.com.

Rudolph Adds Direct-Dock Probe Card Capability to PrecisionWoRx VX4

FLANDERS, NJ – Rudolph Technologies, Inc. has announced the availability of direct-dock probe card capability for its PrecisionWoRx® VX4 probe card test and analysis tool. The VX4 inspects and repairs the delicate probe tips that contact the electrical device during testing.

Direct docking probe cards increase testing speeds and signal bandwidth by reducing the number of electrical connections and shortening the trace lengths from the tester and the device, however, they are larger and heavier than conventional probe cards. The new capability allows users to accommodate direct-dock cards while retaining all the features and functionality that have made the VX platform the unchallenged market leader. Shipments to a device manufacturer in Thailand for a VX4 System, and a California probe card manufacturer, MicroProbe, for a VX4 with direct dock, are scheduled for Q2 2010.

With hundreds of systems installed worldwide, the VX platform has become the industry standard for testing, analyzing and reworking probe cards. Its advanced capabilities allow semiconductor manufacturers to evaluate and correct the planarity, alignment, contact resistance, leakage current, probe force, tip wear, scrub characteristics and numerous other critical probe card parameters that impact probing process performance. Information provided by the new PrecisionWoRx VX4 tool can help test floor managers and test engineers reduce yield losses in the probing process and extend the lifetime of probe cards.

Rudolph Technologies, Inc. is a worldwide leader in the design, development, manufacture and support of defect inspection, process control metrology, and data analysis systems used by semiconductor device manufacturers worldwide. Rudolph provides a full-fab solution through its families of proprietary products that provide critical yield-enhancing information. Rudolph offers yield management solutions used in wafer processing and final manufacturing through a family of systems for macro-defect inspection (detection and classification), as well as transparent and opaque thin film measurements.

For more information visit www.rudolphtech.com. ◆

Henkel News
Hysol® LOCTITE Multicore
July 2010
Henkel

Enabling Next-Generation Copper Pillar IC Technology

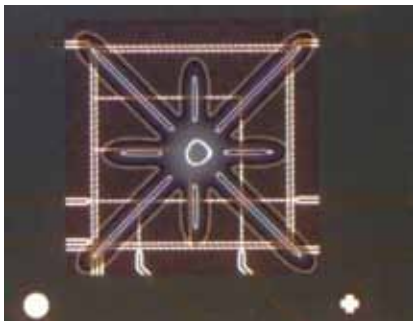
New NCP from Henkel also Compatible with Overmolding

Donald Frye and Shashi Gupta
Henkel Corporation

Well-known for their use with traditional Gold – Gold flip-chip processes, non-conductive paste (NCP) materials are now also enabling next-generation, high I/O fine-pitch technologies. In fact, the most recent advance of these materials, Henkel's Hysol FP5201, has been the key enabler for a new copper pillar (Cu Pillar) interconnect technology.

Copper Pillar technology has been driven by the need to increase functionality while maintaining or decreasing the device footprint. The structure, as compared to traditional solder bumps or solder balls, allows for much finer pitches and, therefore, higher I/O counts per die. For example, with Cu Pillar technology, a die can now accommodate 40 micron pitch, whereas traditional soldered flip chips would see pitches in the range of 150 microns to 200 microns.

Like traditional flip chips, the Cu Pillar technique can follow many of the same process steps, but an advanced process using Thermo-compression bonding has been developed. NCP materials are dispensed onto the substrate; the Cu Pillar die is heated and then pressed onto the substrate where heat and pressure form the electrical interconnections. The NCP's primary function is to act as an underfill and mitigate the stresses between the substrate and the die. Particularly with Cu Pillars and their finer pitches, traditional capillary underfill technologies are problematic: flow time required to surround the tight pitches of the copper pillars is a drain on throughput and UPH, while also introducing an element of uncertainty as to the completeness of the flow and coverage due to the tight dimensions. Because NCP materials are applied to the substrate prior to die placement and thermal compression, coverage is more robust and device protection is improved.



Hysol FP5201 has excellent rheological properties with no bleeding after dispense.

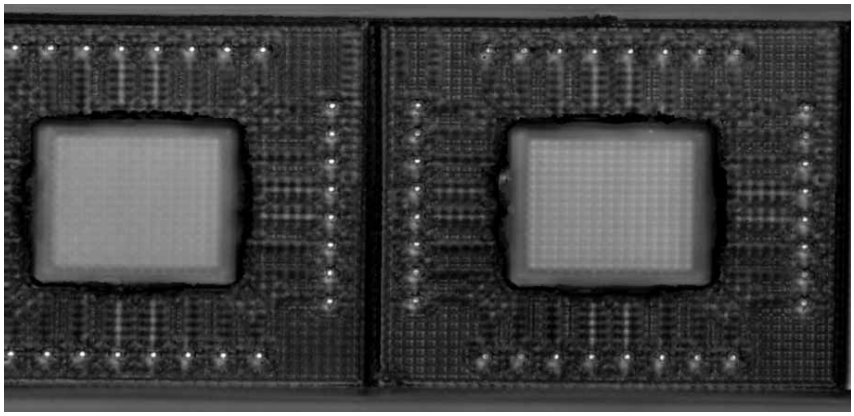
The latest generation of Cu Pillar technology also demands an NCP that is compatible with overmolding. So aside from the NCP material providing a physically reliable and stable bonded package, it also has to maintain its integrity and reliability following the molding process. Older generation NCP products were unable to deliver this post-molding performance, which led Henkel to develop Hysol FP5201.

In partnership with a beta-site customer, Henkel scientists undertook a year-long development process to formulate a material that met very stringent requirements: the new NCP had to cure very quickly to accommodate a very fast bonding process, provide a high level of reliability and work well with the overmolding process – all in a high volume production environment. Henkel was able to deliver with Hysol FP5201, currently the only commercially available NCP of its kind.

Hysol FP5201 cures between one and four seconds at a bonding temperature range of 220°C - 300°C, offering a wide process window and lower temperature bonding capability. The material exhibits little to no voiding and provides outstanding reliability performance of MSL3, TCT1000 and HAST168.

The significance of this material innovation cannot be underestimated as Hysol FP5201 now effectively enables robust, high-volume Cu Pillar processes for microelectronics advance. The material improves throughput through lower cure times, enhances package reliability and allows for exponentially greater I/O counts and finer pitches without sacrificing performance.

For more information on Henkel's Hysol FP5201 NCP material, log onto www.henkel.com/electronics or call the company's headquarters at 949-789-2500. ◆



CSAM Images of Hysol FP5201 shows no voids or delamination after cure.

25 Years of MEMS Technology

Kurt Petersen
KP-MEMS

Nearly 25 years ago, in October of 1985, I was waiting in front of the baggage carousel at the San Jose airport. Out popped a cardboard box sent from Joe Mallon addressed to Janusz Bryzek and myself. I grabbed the box and took it out to my car. Inside was a check from Solartron (a division of oil exploration giant Schlumberger) for $1.29M dollars written to NeoSensor Technology. This was the start of NovaSensor.

Ultimately, Schlumberger invested $2.5M in research programs and $2.5M in equity in NovaSensor. The company was sold in 1991 to Lucas Industries in the UK, then was variously owned by Varity and TRW. In 2002 NovaSensor was acquired by General Electric and is now a part of the GE sensor group of companies. By the way, our original name, NeoSensor, was changed shortly after visiting a number of Schlumberger locations in Europe. People asked us "oh, does your name come from neo-lithic, or neo-nazi?" Based on a suggestion from Roger Grace, we quickly changed the Neo- to Nova-.

Yes, there were other small companies making micromechanical devices at the time: Kulite, IC Sensors, Sensym, Transensory Devices, Microsensor Technologies, etc. Yes, there were also big companies manufacturing or doing research on micromechanical devices: Motorola, IBM, Texas Instruments, Honeywell, etc. However, no other company during that early timeframe in the history of MEMS uniquely captured and promoted the innovation, the push to commercialization, the excitement, and the promise of MEMS. The NovaSensor business plan was variously described by investors and lawyers as an enthusiastic "bible" for micromachining (the term "MEMS" had not yet been invented) The three NovaSensor founders, Janusz Bryzek, Joe Mallon, and myself shared a common vision of these devices proliferating into every conceivable application. We embraced new semiconductor processes, such as electrochemical etching, ion implantation, silicon fusion bonding, and DRIE, and rapidly applied these to new high volume products. We worked on silicon nozzles for fuel injection, resonant beam pressure sensors, capacitive pressure sensors, accelerometers, catheter-tip pressure sensors, very low-pressure sensors, electrostatically-actuated switches, micro-valves, and thermally-isolated high-bandwidth voltage sensors. At the same time as we were doing all this development work, the company was also manufacturing large volumes of pressure sensors; over 1 million/month packaged, laser-trimmed pressure sensors for disposable blood pressure sensing, oil-filled pressure sensors for scuba diving equipment and other harsh environments, very low pressure industrial pressure sensors for HVAC systems, and others. Over the past 25 years, NovaSensor has shipped a total of over 500M sensors.

As a start-up company, NovaSensor understood the significance and the critical importance of getting into production as soon as possible, even though the first product was a simple second source chip. Our first product shipped for sale to a customer a mere 7 months after receiving the first check from Schlumberger.

NovaSensor had a "style". We unabashedly promoted ourselves and our exciting, new technology. We held a lavish opening party for our facility in Fremont, attended by Schlumberger executives and by the mayor of Fremont. We sang songs at Sensor Tradeshows (and, for the executive board at Schlumberger). We published a book on MEMS. We filmed a video on MEMS. We added a style and an energy and a credibility and an entrepreneurial vision to the up and coming technology of micromechanics and MEMS.

In 1988, when Richard Muller, Long-Sheng Fan, and Yu-Chong Tai demonstrated the first micro-motor at UC Berkeley, one of the local TV stations was on-hold, waiting to receive a video of the very first operation of this break-through device. During this holding period, the TV reporter asked Professor Muller "what companies are doing research and building products based on this technology?" He said "NovaSensor". As a result, the reporter visited NovaSensor, did some interviews and filmed our facility. NovaSensor was prominently featured in the same TV news segment about the first micro-motor.

Despite its small size and youth, NovaSensor had an amazing balance between high volume production, a large portfolio of successful products, development, and research. NovaSensor introduced the first products ever made with silicon fusion bonding. NovaSensor was also the first to present a paper on DRIE at the Transducers '95 conference in Stockholm. Farzad Pourahmadi of NovaSensor was one of the first to do Finite Element Modeling on microstructures and produced a break-through paper on the strength of silicon at the Transducers '89 conference in Montreux, Switzerland.

Many NovaSensor founders and employees have since founded at least a dozen other MEMS companies.

When I began work on micromechanics at IBM in 1975, there were 3 MEMS-type products on the market, pressure sensors, etched silicon strain gages, and the TI thermal print-head. Total market value of these products was probably less than $100M/year. Today, there are dozens of different MEMS product areas, amounting to nearly $10B in shipments in 2010. Today, MEMS are literally everywhere. Every automobile contains up to 20 MEMS devices, including key safety-critical sensors for air-bags and for electronic stability control. In a few years, every cell phone will contain a dozen MEMS devices. The MEMS industry has grown from a small group of small cottage businesses to a multi-billion dollar behemoth, with a large pipeline of new high volume products (oscillators, switches, new direct view display technologies, bio-MEMS, etc.), with a huge impact on the daily lives of a majority of the people on the planet.

NovaSensor was a pioneer in this larger vision of MEMS. NovaSensor was the first company to expressly embrace and promote and proliferate this broad vision. NovaSensor played a unique role in the history of MEMS and was a catalyst for the commercialization and entrepreneurial spirit of the field. I am so happy and grateful that I was able to be a part of this history.

To mark the founding of NovaSensor, the company founders are organizing an event to be held at Stanford University on November 15-16, 2010. See page 3 for more information. ◆

COMPLIMENTARY REGISTRATION
through Friday, September 10, 2010!

GSA Emerging Opportunities eXpo & CONFERENCE

September 16, 2010

Santa Clara, California USA | Santa Clara Convention Center

The GSA Expo, now in its seventeenth year, is a key event bringing together leading companies throughout the supply-chain.

The 2010 conference program will focus on emerging opportunities in ***Global Mobile Data*** for the semiconductor industry. Hear from leading experts as they delve into the challenges and opportunities OEMs, operators and semiconductor companies face in managing consumer demand and connectivity trends in markets such as home networking, mobile Internet devices and communications networks.

In addition to providing insightful presentations, the event offers numerous opportunities for companies to network with partners across the ecosystem!

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Grip Ring Magazines

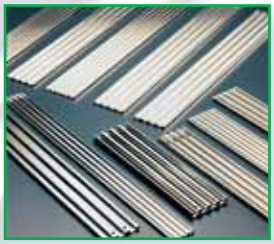
Grip Ring Shippers

Lead Frame Magazines - F.O.L./E.O.L.

Stack Magazines - E.O.L.

Process Carriers (Boats)

Boat Magazines



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