

WINTER 2010



A Publication of The MicroElectronics Packaging & Test Engineering Council

INDUSTRY NEWS

Trace Laboratories has expanded their customer service team with the addition of Nick Pawluk to the position of Account Manager-Technical. *page 16*



Stats ChipPAC and **Intersil** qualify and ramp copper wire interconnect for high-end analog and mixed-signal devices. *page 16*



SemiProbe has developed a new low-cost solar cell probe system for research applications. *page 16*



Semtech Corporation has announced that it is working with **IBM** and its innovative 3D through-silicon via (TSV) technology to develop a high-performance ADC/DSP platform. *page 17*



InvenSense, Inc. announces the world's first motion processing library with 9-axis sensor fusion for Android 2.3 Gingerbread. *page 20*



IPC APEX EXPO 2011 Conference and Exhibition will be held April 12th to 14th at the Mandalay Bay Resort & Convention Center in Las Vegas, Nevada. *page 27*

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THE HEAT IS ON

Beating the Heat:

Performance and Cost Improvements Through Thermal Management Design

*A Special One Day Symposium and Exhibits
Coming to San Jose, CA March 21st*

MEMBER COMPANY PROFILE



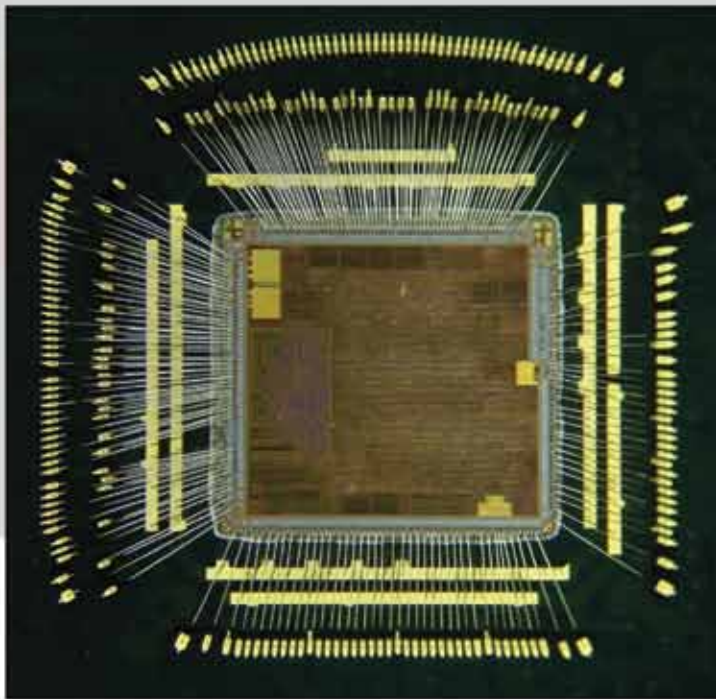
Founded in 1998, **GEM** specializes in small-outline surface-mount packages for power semiconductors, offering customers both industry standard packages and proprietary, leading-edge power management semiconductor packaging technologies from design and manufacturing centers in Greater China.

GEM Services, Inc. is a full-service outsourcing provider catering to both vertically integrated semiconductor product companies and fabless design houses located throughout the world focused in total or in part on power management semiconductors. Many customers in both groups are strategic partners with whom alliances have been formed in joint development projects. GEM's strategic decision to support both IDMs (Independent Device Manufacturers) and fabless design houses allows the company to better weather the semiconductor market's cyclicity. *page 8*

Semiconductor equipment bookings increase 90.6% over November 2009 level. *page 20*

Book-to-Bill Ratio
FOR NOVEMBER .96

Copper Wire



Copper Wire is a lower cost alternative to the traditional gold wire used in semiconductor packaging. Offering clear advantages, copper wire bonding is gaining popularity for products at 25 microns and below, where the majority of wire bond applications lie. ASE's copper wire bonding initiative is geared towards this group of applications. Bonding pad composition and wafer structure are major factors for copper wire evaluation, and ASE is customizing products based in specific customer needs.

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Welcome to our Winter 2010 issue! 2010 was quite a roller coaster ride...after all it was considered a "recession-free" year by definition: five quarters of GDP growth (albeit weak growth). Even if it is technically over, it doesn't feel like it to many companies and individuals. Unfortunately it has been a jobless "recovery", but the outlook for our industry is remaining positive. After a very strong 2010, most analysts believe that the 2011 semiconductor market will experience a modest, single digit growth, and depending on the analyst it will be anywhere from 2.5% to 10%.

Our Industry Analysis this issue continues this theme. **Morry Marshall**, Director of Strategic Technologies at **Semico Research Company** writes "Single Digit Growth for Total Semiconductor Sales in 2011". He explains the 2011 semiconductor sales forecast in detail, including some thoughts on the official end of the recession, and why we won't have a double-dip recession (see page 6). We'd like to thank Morry for this report.

Debra Vogler of **Solid State Technology & Advanced Packaging** reviews a couple of recent 2010 events. The **MEMS Technology Summit**, a **MEPTEC** produced event held at and hosted by **Stanford University** in October, was billed as a 25th "birthday" for MEMS technology, and provided a quarter century of perspective with lessons from the past and visions for the future. The speakers were a literal "who's who" of MEMS; see page 4 for this interesting review.

MEPTEC's most recent event was "Semiconductor Packaging Roadmaps: Applications Driving Requirements", and offered insights on advanced packaging roadmaps and the importance of collaboration between companies. Speakers from IDMs, subcontract assemblers, and end users gathered to discuss, as Debra states, "the challenges facing packaging technologists as they face the daunting task of fitting more functions into ever-smaller form factors". Go to page 5 for the review.

2011 will bring many changes for MEPTEC. Watch for a new look for the MEPTEC Report starting with our Spring issue. We also plan to beef up the content of the Report by putting in place some contributors who are experts in synergistic industries such as MEMS, medical electronics, etc. We will also be introducing some new events, so stay tuned. If you are not on our e-mail distribution list, please go to www.meptec.org and enter your e-mail address in the "Join our Email List" box.

We're pleased to be bringing back our popular "Heat is On" *Thermal Management symposium*. We have not held one since 2008,

but recently MEPTEC and the organizers of the long-running **SEMI-THERM Conference and Expo** joined forces to put together the "Electronics Thermal Week" (ETW). This week long event will bring together several different organizations in addition to SEMI-THERM including **JEDEC**, **ASME** and others. The event will offer a wide range of programs that will cover heat transfer cooling, thermal management, measurement and modeling markets, and much more. The "Heat is On" symposium, which will be held the first day of ETW, Monday, March 21, is titled "Performance and Cost Improvements through Thermal Management Design". All events will be held at the **DoubleTree Hotel** in San Jose, CA; see page 11 for details.

Our Company Profile comes from Corporate member **GEM Services, Inc.** They are a multinational power management semiconductor test and packaging service provider, and have facilities and customers throughout the world. See their story on page 8.

One of our feature articles this issue is from **QPL**, which is a global supplier of leadframes for the semiconductor industry. In their article "QFN Packaging Advances with Routable High Density Leadframe (HDL) Technology" they explain their innovative HDL technology which uses the entire package area unlike others which do not use the area under the die. We'd like to thank the authors for a look at this interesting technology (see page 12).

Our other feature article is from **Jan Vardaman** and **Linda Matthew** of **TechSearch International, Inc.** In "The Re-Birth of Silicon Interposers?", Jan and Linda give us a detailed look at the drivers for silicon interposers today, its uses for wireless applications, and other developments. See page 14 to see why they feel that "silicon interposers have finally found their niche".

Our editorial in this issue is from Advisory Board member **Ron Jones** with **N-Able Group International**. In "Can We Afford Moore's Law?", Ron introduces the idea of whether we will be able to maintain adherence to Moore's Law, given the fact that it applies only to the IC chip itself, but not to packaging or other IC performance factors. See page 26 for this interesting perspective on the Law that was written in 1965, and whether it can continue its amazing 45 year run.

We'd like to thank all of our contributors for making this a great issue. If you're reading our publication for the first time at one of the many events where we distribute, or if you're a new member, we hope you enjoy it.

Thanks for reading!



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MEPTEC Fall Events Tackled Packaging Challenges for ICs and MEMS Devices

Debra Vogler
Sr. Technical Editor
Solid State Technology/Advanced Packaging

Two MEPTEC events this Fall provided clear evidence of the challenges facing packaging technologists as they face the daunting task of fitting more functions into ever-smaller form factors.



MEMS Technology Summit:
a 25th Birthday Party (give or take a few years!)

The MEMS Technology Summit (Stanford University, 10/19-10/20/10) was billed as the 25th birthday party for MEMS technology and a recitation of the lessons learned by the industry. To listen to my podcast interviews with key presenters at this event, go to <http://tinyurl.com/3yfnvt> (from the 10/28/10 of the Daily Pulse).

While some of the speakers lightheartedly debated the actual birth date, the common theme echoed in the presentations was aptly summarized by Roger Grace of Roger Grace Associates, who was one of the organizers of the conference. He summed up what he thought was a key takeaway from the conference, which was brought out by a number of speakers: for MEMS to grow as an industry, it will have to figure out how to get from being component-centric to system-centric, noted Grace. That shift in focus will make the difference between an industry with relatively small ROI, and one that adds greater value – and thus can charge accordingly. He pointed to the recent example of Poly-

chromix' (now Thermo Fisher Scientific) Phazir – a MEMS-enabled, portable near-IR portable spectrometer. “We have to add value – we can’t be selling piece-parts at very, very small profit margins; we have to be selling solutions,” said Grace. “The higher amount of value you can add, the greater opportunity to make money.”

As if on cue for the “birthday party,” during the conference, Steve Senturia, Professor of Electrical Engineering, Emeritus MIT, and the former chairman and CTO at Polychromix (purchased by Thermo Fisher Scientific in June, 2010), received news from NASA concerning the Phazir. This MEMS-enabled near-IR portable spectrometer was used by NASA (LCROSS project) to detect water on the moon. NASA’s results from its 2009 findings were published in the 10/22/10 issue of Science, just as Senturia was preparing his conference presentation about it. (Go to the podcast link above to hear Senturia discuss the project in more detail.)

Other presenters echoed the same concerns: how to find R&D funds in an industry that is increasingly becoming commoditized. In his presentation at the conference, Peter Hartwell, Distinguished Technologist at HP Labs, did an interesting back-of-the-envelope calculation that illustrated just how challenging it is for MEMS component manufacturers to make a profit, given that the technology has become commoditized. Essentially, the revenues generated at the system integrator stage and up to the service provider are orders of magnitude larger than those seen by a MEMS device manufacturer. In his example, a MEMS device manufacturer might realize \$30M in revenues, while the systems integrator would see \$2.2B in revenue; but the service provider might see \$25B in revenue. Going forward, funding models will have to take this commoditization factor into account.

Hartwell also discussed HP’s sensor strategy – called CeNSE (central nervous system for the earth). In his podcast interview, Hartwell describes how HP has been leveraging its inkjet cartridge technology and high-volume manufacturing to tackle the need for distributed wireless sensing networks, in particular, sensing in harsh

environments. By harnessing the compute power in “the cloud,” the large amounts of data generated from wireless sensors provides the information required to monitor infrastructure.

In his podcast interview, Benedetto Vigna, Group VP, GM, MEMS, Sensors and High Performance Analog Division at STMicroelectronics, described what he calls MEMS “traps” – ways of thinking about MEMS that hold back the industry and slow its growth. He advises against “falling in love with the chip” or the technology; instead, the industry should fall in love with applications. Looking ahead, Vigna sees the industry metamorphosing from its current era of consumerization to what he calls “personalization,” i.e., sensors in/on/around the body.

Steven Walsh, the Albert Franklin Black Professor of Entrepreneurship at the University of New Mexico, provided attendees with lessons learned over the past 25 years of MEMS technology. In his podcast interview (go <http://tinyurl.com/27s8s51>), he summarizes the five major commercialization hurdles MEMS companies face whether they are in a disruptive, discontinuous-based product paradigm, or a sustaining, continuous-based product paradigm. In the first case, a company must have at least a 10% improvement in cost and at least a 2-3x improvement in some other parameter. For a sustaining technology, you can go with an ~2x improvement and you have to make it better, faster, cheaper. Another decision point: do you have the funds, can you develop the product yourself, and you have to decide whether to go fab-less. He also offers specific advice for the entrepreneurial team. He ends his podcast interview with a recitation of BioMEMS devices that are in exciting stages of development, including a MEMS needle that eliminates the need for a stabilization agent in vaccines, optical solutions that aid vision, and targeted cancer therapies.

In addition to looking back at the achievements in MEMS technology, some presenters challenged the audience to look ahead and address the next major issues. Thomas Kenny, Professor of Mechanical Engineering at Stanford University, told

attendees that nanotechnology promises have gone unfulfilled. "If we define a technology as the ability to make something exactly the way we want it, over and over, we do not have this capability at the nanoscale for many structures," said Kenny. In his podcast interview, Kenny discusses DARPA's Tip-Based Nanofabrication (TBN) Program, which is a response to the need for localized control over environments and position and all other characteristics of a nanostructure. The TBN program opens up the possibility for site-specific growth of nanotubes and nanowires.

Beth Pruitt, Assistant Professor of Mechanical Engineering at Stanford University, described how MEMS cantilevers have become a key enabler in science and consumer, aerospace, and automotive applications. Some applications include a novel scanning probe, cantilever-based chemical sensing, and mechano-transduction at the cell and organism level. In her podcast interview, Pruitt discusses the merits of cantilevers as well as funding opportunities that leverage these useful mechanisms.

Summing up key takeaways from the conference, co-organizer and industry pioneer, Janusz Bryzek of Jyve Inc., told ElectroIQ that, "Manufacturing MEMS is not a trivial job." But as the infrastructure is improving, "It's easier to get products to the market if you follow what the industry has developed, and not try to reinvent new manufacturing processes." While there are several companies today shipping over a billion MEMS-based devices a year, in the next 10 years, Bryzek observed that the industry has a roadmap to produce over a trillion devices.



The Semiconductor Packaging Roadmaps Conference:
Making the Pitch for Advancing Packaging Roadmaps and Collaboration

In his keynote address at the MEPTEC Semiconductor Packaging Roadmaps conference (11/10/10, Santa Clara, CA), Bill Bottoms, chairman of 3MTS (Third Millennium Test Solutions), gave attendees a dose of reality as he summarized the predicament facing the industry as it pursues 3D ICs. "Everything becomes more difficult at deep sub-micron," said Bottoms. "Deep sub-micron implies changes in every parameter and makes package functions of device protection, power delivery, and signaling into and out of the device more challenging." A few of the challenges facing the industry as it implements 3D ICs will be: 1) the need to control power and enhance performance, 2) dealing with transistors that wear out within an expected product's lifetime, 3) the introduction of new sources of stress, 4) thermal density increases, 5) operating voltage decreases, etc.

Another challenge with die stacking will be the need to establish KGD (known-good die), i.e., the testing challenges, will be tremendous. For example, Bottoms told attendees that no test equipment will handle the number of vectors (which can be close to a trillion) at a reasonable cost and no one has a probe solution for 17GHz. In a podcast interview (go to <http://tinyurl.com/27kdj8u> from the 11/18/10 Daily Pulse), Bottoms details some of the methods that will be needed to address the conundrum (e.g., redundancy, continuous testing, dynamic self-repair, graceful degradation). He also takes listeners on a kind of "back to the future" discussion as many of the solutions that will be needed for 3D ICs, he observes, were used years ago in mainframe computers 20-30 years ago. "It's not an issue of invention, but one of integration with what is already known," said Bottoms.

In his presentation, Lee Smith, VP, Business Development at Amkor, made a case for full supply chain collaboration as the industry moves to 3D ICs with TSVs. Among the drivers for collaboration in 3D packaging development are the rising R&D costs and capital intensity, shorter product and technology life cycles and the attendant margin "squeeze" along with the consolidation of demand to achieve ROI requirements.

One collaboration IDM/OSAT case study is Amkor's work with TI; in July of this year, the companies announced qualification and high-volume manufacturing of fine pitch copper pillar technology. Smith said that the new lead-free technology enables bump pitches of $\leq 50\mu\text{m}$ and is cost competitive with wire bonding.

In a podcast interview with ElectroIQ (<http://tinyurl.com/3xes2jy> from the 11/16/10 issue of the Daily Pulse), Smith

discusses the three generations in the transition to 3D packaging and how the OSATs shape the development roadmap. In the first generation of die stacking, it was the memory industry and their OSAT suppliers who collaborated; then logic plus memory integration led to further collaboration. In the second generation (package stacking), OEMs were the key drivers in initiating collaboration: the logic, memory, OSATs, plus EMS industry, all enabled package stack solution in high-volumes. And as the industry enters the third stage of 3D packaging – a complete 3D architecture with TSVs – Smith says that we need complete supply chain collaboration: EDA tool suppliers, equipment/materials suppliers, logic, memory, fabless, IDMs, and the SATs, to develop and deploy the technologies.

Jan Vardaman, President of TechSearch International, tackled the challenges in LED packaging and assembly, saying that there is room for improvement. She lamented the lack of packaging standards, "The footprints of LED packaging are not even the same," she said. The industry will also have to understand optical, thermal, and material science trade-offs to enable reliable, low-cost products.

She told attendees that OIDA predicts that by 2021, 32% of HB-LEDs will be on 4-inch wafers. Currently, 2- and 3-in. wafers are in high-volume production with volume production of 4-in. wafers having started in 2008. Four-inch wafers still cost more than 4x the cost of 2-in. wafers, observed Vardaman. R&D for 6-in. wafers started in 2008 and these are going into production volumes now, she said, while R&D on 8-in. wafers is currently underway.

In a podcast interview (<http://tinyurl.com/363rbhw> from the 11/17/10 Daily Pulse), Vardaman discussed sapphire and SiC substrates, as well as the various singulation methods currently in use by LED manufacturers (e.g., laser, stealth dicing, mechanical blade dicing, etc.). The key factor in which method is chosen is obtaining the maximum light output and Vardaman expects that there will continue to be a plethora of process, assembly, and packaging solutions for the next few years. ♦

Single Digit Growth for Total Semiconductor Sales in 2011

Morry Marshall
 Director, Strategic Technologies
 Semico Research Corporation

Total worldwide semiconductor sales will increase more than 30% in 2010, but the outlook for 2011 is much more subdued. Sales growth will be in single digits. Several factors are involved: the US economy, the world economy and the semiconductor sales cycle.

First, the US recession is over. It ended in June 2009. Regardless of what you read, hear or see in the media, the recession is over; and that isn't a technicality. As indicated in Figure 1, the US economy has been growing for the last five quarters. The proverbial person on Main Street doesn't believe that. To that person, it feels like the economy is still shrinking. That's because the media still reports that the US is in a "recession" and because jobs haven't returned. Even people who are employed know someone who doesn't have a job or are afraid that they will lose their own job.

Increased employment typically lags economic recovery, and that's happening now. As shown in Figure 1 the unemployment rate in the US increased steadily from 5.0% in January 2008 to a high of 10.1% in October 2009. It's been trending down since then but has been stalled at 9.6% for the last three reported months (August, September, and October 2010). Until the unemployment rate drops, the popular perception will be that the recession is not over.

Semico Research Corp. believes the US GDP will continue to grow at a rate of more than 2.0% per quarter through 2011. There will be no double-dip recession.

There are some reports of increased hiring. Semico believes these reports signal an inflection point. Unemployment rates will fall during 2011 and will be closer to 6.0% by early 2012.

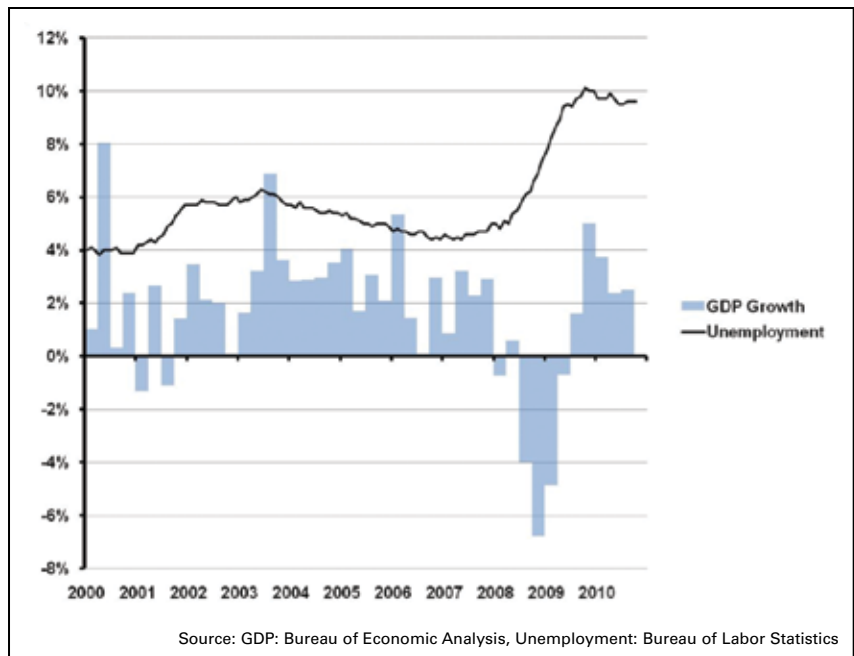


Figure 1. US GDP Growth by Quarter (\$US Constant), US Unemployment Rate by Month.

A stronger US economy is good news, but a new reality must be accepted. The US economy is no longer the primary economic driver for the semiconductor industry. China is Asia's largest economy, the second largest in the world behind the US. China's GDP will increase more than 10% annually in 2010 and 2011. India is Asia's third largest economy. India's GDP will increase more than 6% annually in 2010 and 2011. In addition, China and India are investing in manufacturing capacity, infrastructure and education. China and India are becoming the economic drivers for the semiconductor industry.

Economic conditions in the US, China, India and the rest of the world will support increased semiconductor sales; but the semiconductor industry can create its own downturn.

Figure 2 shows annual semicon-

ductor sales growth from 1980 through 2010. During that time, there has never been a year with annual growth of 30% or more that has not been followed by a downturn. This has also been true even in all the years prior to 1980. A growth rate exceeding 30% simply cannot be sustained. Semiconductor sales growth will dip in 2011 as it has in all previous years following a boom year.

Numbers can be deceiving. Figure 3 shows total worldwide semiconductor sales by quarter from 2006 through a forecasted 2011. The black line is a linear trend line. As illustrated, there is a mathematical reason that annual growth in 2010 was greater than 30%. That is because sales in 2009 were so far below the trend line. Normal quarterly sales growth in 2010 created abnormal annual sales growth. Similarly, there is a mathematical reason

why annual growth in 2011 will be in single digits. 2011 growth will be computed from a 2010 base close to the long term trend line. So don't despair, the quarterly growth rates in 2011 will actually be better than the annual growth rate implies. They will be very close to the long term trend line growth rates. 2011 will be a better year than the annual sales growth number seems to predict.

There are some real, non-mathematical reasons why semiconductor sales growth will be slower in 2011: decreasing memory ASPs, increasing inventories and overcapacity.

Total semiconductor sales are heavily influenced by swings in memory ASPs. A large part of total semiconductor sales growth in 2010 was due to dramatically increasing memory ASPs. But, memory ASPs already began to fall in the fourth quarter of 2010; and that trend is expected to continue into 2011.

Because NAND Flash is being used in new applications with rapidly increasing volumes (SSDs for example); demand will slow NAND ASP declines in 2011. With fewer new or growing applications, DRAM ASPs will fall faster and farther than NAND Flash ASPs. But, ASPs for DRAM and NAND will both decrease, creating a drag on total semiconductor sales growth.

At present, inventories are at a healthy level; but there is evidence that some companies, particularly distributors, are beginning to scale back on purchases to insure that inventory levels are kept in check. Purchasing cut-backs will continue into 2011, when pressure to control inventory levels will increase.

Capacity utilization will decrease in 2011. As usual, the semiconductor industry began planning for added capacity when growth was booming. That planned capacity is going to come on line in 2011, just as companies are beginning to cut back on sales to control inventories. The result will be overcapacity, which will decrease ASPs and hamper semiconductor sales growth. That's a normal part of the semiconductor sales cycle.

Total worldwide semiconductor sales are increasing at an unsustainable rate of growth in 2010. Worldwide, there will be sufficient economic growth to support increased semi-

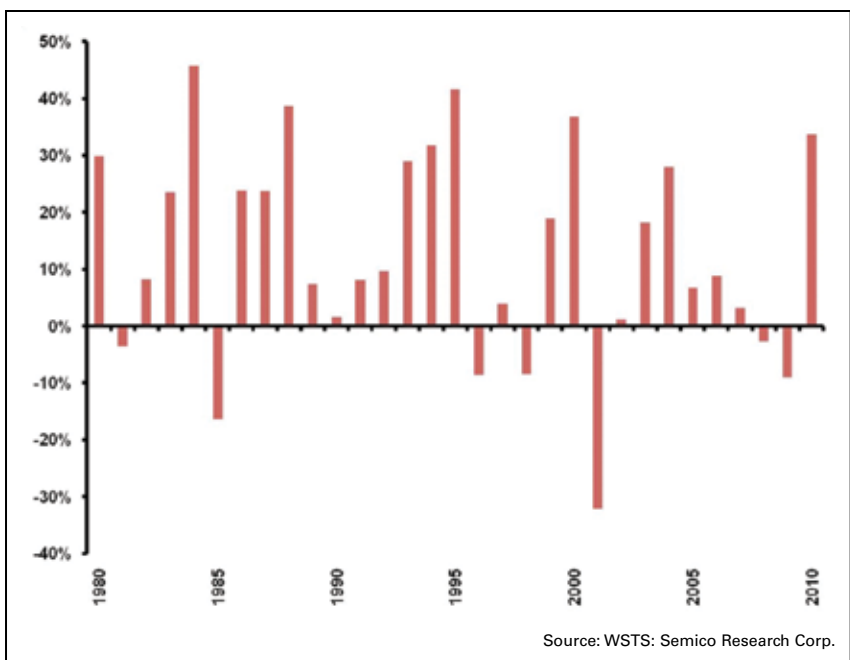


Figure 2. 2080 through 2010 Annual Increase in Total Worldwide Semiconductor Sales (%) .

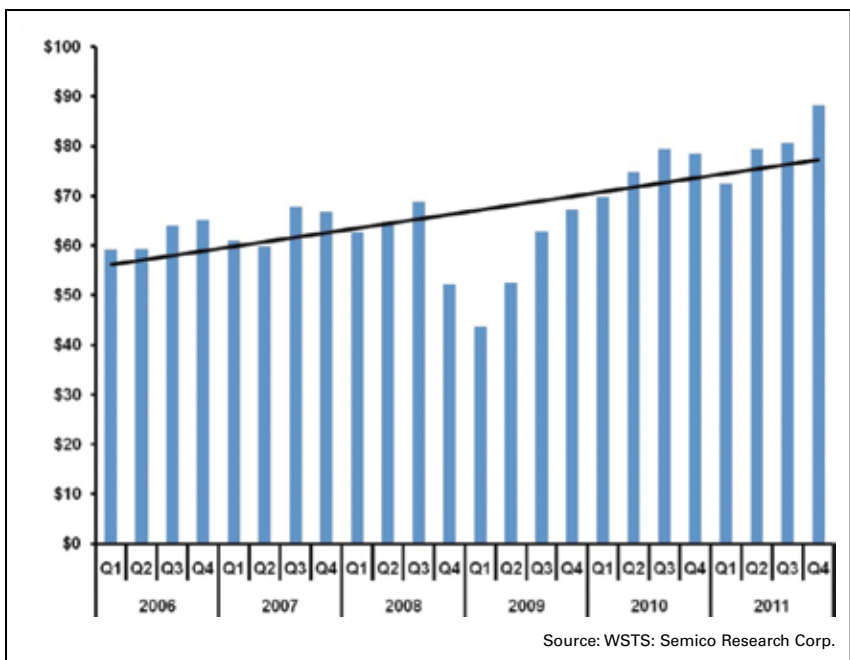


Figure 3. Total Worldwide Semiconductor Sales Quarterly Sales.

conductor sales in 2011, especially at a lower growth rate; but falling memory ASPs, increasing inventories and overcapacity will contribute to a downturn in semiconductor sales growth. Annual semiconductor sales growth in 2011 will be less than 10%. ♦

Morry Marshall heads up the Semico Research Corp. Strategic Technologies practice, which covers technologies and markets vital to the growth

of the semiconductor industry. At present, he is focused on the used semiconductor equipment market and has authored three studies identifying used equipment opportunities. Prior to those studies, he has provided custom studies evaluating the potential market for new products such as nanoprobing equipment and thermoelectric coolers. He has also authored studies about personal computers, automotive electronics, SiGe markets, semiconductor packaging and numerous semiconductor end-use products.



World Class Manufacturing Services for Power Management Semiconductors

GEM Services, Inc. (GEM) is a multinational power management semiconductor test and advanced packaging service provider of high quality, turnkey semiconductor packaging and testing services focused on the power management market. Founded in 1998, GEM specializes in small-outline surface-mount packages for power semiconductors, offering customers both industry standard packages and proprietary, leading-edge power management semiconductor packaging technologies from design and manufacturing centers in Greater China. Semiconductors packaged and tested by GEM go primarily into devices such as desktop and laptop computers, PC motherboards, mobile phones, PDAs, ultra-mobile PCs and LCD/plasma displays, as well as automotive and industrial applications.

GEM Services is a privately held company incorporated in the Cayman Islands with six wholly-owned subsidiaries:

- GEM Services USA, Inc. in Santa Clara, California;
- GEM Electronics, Inc. in Taipei, Taiwan;
- GEM Services Hong Kong, Ltd.;
- GEM Electronics Company Limited, which owns subsidiaries GEM Electronics (Shanghai) Co., Ltd. and GEM Electronics (Hefei) Co., Ltd.;
- GEM Electronics Trading, Inc.;
- Dino Electronics Manufacturing Inc., which owns subsidiary GEM Power Semiconductor Co., Ltd. in Kaohsiung, Taiwan.

GEM Services, Inc. is a full-service outsourcing provider catering to both vertically integrated semiconductor product companies and fabless design houses located throughout the world focused in total or in part on power management semiconductors. Many customers in both groups are strategic partners with whom alliances have been formed in joint development projects. GEM's strategic decision to support both IDMs (Independent Device Manufacturers) and fabless design houses allows the company to better weather the semiconductor market's cyclicity.

Through these strategic relationships, GEM has developed patented proprietary packages such as J-Lead GEM2021 and GEM2928 packages that offer customers improved performance over industry standard packages through the ability to place larger semiconductor die in relatively small packages with better heat dissipation and electrical conductive characteristics. GEM has also licensed technology from industry leaders for highly differentiated advanced semiconductor package types. In addition, GEM works closely with capital equipment suppliers to develop state-of-the-art machinery that improves manufacturing processes and product cost efficiencies.

Geographic presence in Greater China allows GEM's customers to take advan-

tage of the logistical and cost efficiencies related to close proximity to their semiconductor wafer suppliers and to their customer base, the electronic systems producers. It also provides us access to a highly-educated and cost effective labor force, low-cost raw materials, and manufacturing facilities supported by favorable government incentives. Geographic advantage, coupled with the experienced international management team, allows us to be cost efficient while maintaining high quality standards.

Operations are centered in Shanghai, with three manufacturing facilities in Greater China. The Shanghai facility, GEM's founding factory, was established in 2000, and focuses on advanced power discrete, power IC's and MCM packaging. The Shanghai site also houses GEM's corporate engineering and technology development center. GEM acquired the Kaohsiung, Taiwan facility in 2006, which primarily serves several Taiwan and Japan customers and provides quick-turn services for the Taiwan market and focuses on larger core packages. The Hefei, China facility began production in 2007, and is dedicated to high-volume turnkey packaging and testing, to accommodate growth and maintain cost advantage. The Hefei site is only 30% built up at this time and will provide available space for GEM's future expansion in the long term. In addition to the mentioned manufacturing facilities, sales and marketing offices are located in the United States, Taiwan and China and service the Japan market through a strategic distributor. There are a total of 2,230 employees worldwide.

Semiconductor Outsourcing Industry Background

Historically, power semiconductor companies designed and manufactured their semiconductor products in-house. However, over the past two decades, the power IDM's have increasingly outsourced some of the wafer fabrication, packaging and testing components of the semiconductor manufacturing process. As power semiconductor design complexity and manufacturing costs increase, com-





Founding Factory #1 - Jiading Industrial Development Park, Shanghai, China



Factory #2 - Hefei Economic & Technological Development Zone, Hefei, Anhui Province



Factory #3 - Kaohsiung, Taiwan

panies must invest more capital in the front-end of the design and manufacturing processes, leaving them with fewer resources to invest in the back-end of the manufacturing process. As a result, virtually all IDMs use some outsourced manufacturing services. Furthermore, fabless power semiconductor design houses typically outsource substantially all their semiconductor fabrication, packaging and testing needs. The emergence of fabless design houses has accelerated the outsourcing demand.

China Semiconductor Packaging and Testing Overview

Over the last three decades China has emerged as the leading manufacturing center for many industries. China's semiconductor packaging and assembly industry was slower to emerge as an industry leader. This delay may in part have been due to the significant capital, technical expertise and experience needed to package and assemble semiconductor devices. Many new Chinese vendors lack advanced packaging technologies, have questionable quality control, have limited production capacity and lack experienced international management and semiconductor production experience, making it difficult to attract quality customers.

Despite the challenges of operating in China, an increasing number of Chinese packaging and testing facilities have opened. China is an attractive semiconductor packaging and assembly location for several reasons, particularly:

- **Proximity to wafer manufacturers** -

Many manufacturers of wafers and die that are packaged into semiconductors are based in either Taiwan or China;

- **Proximity to component end-users and electronic equipment manufacturers** - Most devices that incorporate packaged semiconductors are manufactured and assembled in China; and
- **Beneficial cost base** - China has a manufacturing cost base anchored by lower labor, utilities, real estate and raw materials costs relative to most other countries.

Highly Experienced International Management Team Operating in China

- **Richard J. Kulle**, President and CEO, has over 40 years in the semiconductor industry, including leadership roles in Temic Semiconductor, Siliconix and General Electric.
- **Anthony Chia**, Chief Operations Officer, is a veteran of more than 35 years in the business, including Simconix and General Electric.
- **Dr. Anthony Tsui**, Executive VP, Quality & Technology, is also a seasoned veteran having experience in advanced device design, package development, and quality management.
- **Andrew Peng**, Vice President of China Business Development, has over 20 years of experience in business development, marketing and engineering.
- **Yu-Fu Lin**, Vice President of Finance, has many years of experience in cross-

border technology company financing, and recently joined GEM Services, Inc. from East West Bank.

This highly experienced international management team is strategically based in Greater China near GEM's packaging and assembly facilities. Managing locally allows management to personally gauge facility performance and obtain critical operational, personnel and market feedback which allows quick implementation and assessing effects first-hand. Several members of the management team have also worked through numerous semiconductor market cycles, providing them with valuable insight when making capacity and capital expenditure plans. Further, GEM's international board of directors have experience overseeing public companies in the United States with international business practices and implementing and maintaining corporate governance controls.

Proven Experience Improving Manufacturing Processes

GEM has a proven track record of improving manufacturing processes to improve package performance and increase production and cost efficiencies. Some of the process innovations include:

- **Three-dimensional molding**. Compared to industry standard two-dimensional molding, this technique allows GEM to use significantly less mold compound in the molding process;
- **Leadframe stamping**. GEM worked with equipment vendors to redesign lead-



Full line of discrete power packages



Improved thermal performance and current capability - GEMPAK5000



GEM's J-lead packages reduce PC-board footprints.



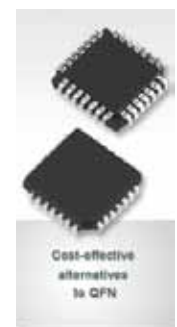
Direct electrical connection to the die and low thermal impedance.



GEM's 2021-5J and 2020-12J J-lead packages



Leadforms allow a variety of PC-Board mounting options.



Cost-effective alternatives to QFN

frame production process to quadruple output; and

- **Use of copper wire.** GEM was the first outsource vendor in the industry to use copper wire bonding in place of gold wire bonding in some packages.

Leading Turnkey Packaging and Testing Services Provider with Extensive and Specialized Power Management Expertise

GEM is a leading provider of high quality turnkey semiconductor packaging and testing services focused on the power management market. Power management packaging and testing requires specialized expertise and as a result there are few qualified vendors in this market. GEM exclusively offers many of their leading-edge semiconductor packages, which incorporate proprietary technology or technology licensed exclusively. GEM supplements their leading-edge packages with a range of industry standard semiconductor packages. End-market specialization allows them to maintain a technology leadership position in the power management segment.

GEM has in place many stringent internal operational management systems, including an extensive new hire qualification program as well as ongoing training programs. Locations in China afford access to a well-educated yet cost effective labor force. GEM maintains an advanced lab and a highly experienced team to analyze, diagnose and remedy production problems and through this, perfect the manufacturing process. GEM's manufacturing systems and processes have received ISO 9001, ISO TS16949 and ISO 14001 international quality and environmental certifications.

Develop Value-added Proprietary Packages and Manufacturing Processes

GEM has experienced package development teams in Silicon Valley and China that have designed and patented proprietary packages, such as J-leads, to meet customers' functionality, quality and cost requirements. Technical expertise will continue to be leveraged and we will continue to work closely with customers to develop innovative leading-edge packages that offer increased space saving, larger die sizes in smaller packages, thinner profiles, more integrated circuits per package, more leadframe options, and higher pin-counts.

Patents

The Company holds a total of 49 patents in United States, China and Japan.

Testing and Other Services

GEM provides a range of testing services for the power management semiconductor devices. These services include test programs, wafer probing, electrical testing and reliability testing. These test services are provided to customers as part of the semiconductor packaging solution.

Semiconductor device testing requires a technical understanding of how to use and optimize the test equipment and how semiconductors are built, how they work, and the specific applications and functions of the tested device.

Test Program Services

GEM offers customers value-added test software development, conversion and optimization services. Engineers work closely with customers on software programs to test their specific power management devices, including discrete devices, analog ICs and power ICs.

Wafer Probing

GEM performs wafer probing, which involves the automated inspection and electrical testing of the individual die on the wafers and then marking and discarding or mapping defective die that do not meet customers' criteria. Wafer probing is done after the semiconductor wafer manufacturing has been completed and immediately before die packaging. Die on an accepted wafer are then individually inspected under microscopes before packaging.

Final Testing

GEM conducts final post-packaging electrical testing which is designed to assess whether the packaged semiconductor complies with a variety of different operating specifications, including functionality, frequency, voltage, current, timing and temperature range. A semiconductor device is subjected to electrical tests using specialized test equipment and customized software applications.

Process Qualification and Reliability Testing

GEM's reliability testing assesses the long-term reliability of the semiconductor device and its suitability of use for intended applications. Testing can include burn-in services, which electrically stress a device, usually at high temperature and voltage, for a period of time long enough to cause the failure of marginal devices.

Drop Shipment

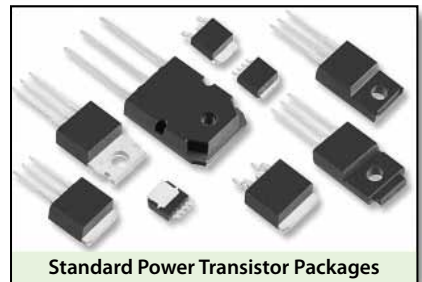
GEM Services, Inc. offers their customers direct drop shipment to their end-



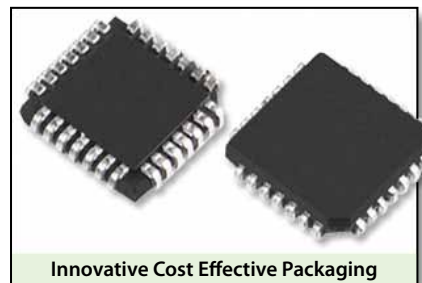
J-Lead Maximizes Board Area Utilization



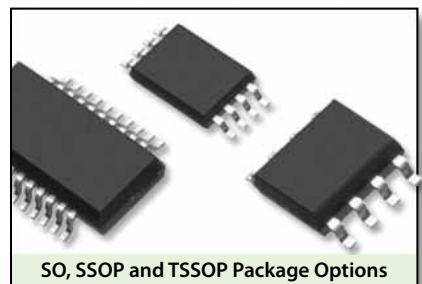
Value-added Packaging - Power BGA



Standard Power Transistor Packages



Innovative Cost Effective Packaging



SO, SSOP and TSSOP Package Options

user clients. Shipments are packaged in client's own branded boxes so delivery appears seamless, eliminating an additional step for customers.

For more information about GEM Services, Inc. visit www.gemservices.com. ♦

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THE HEAT IS ON

Performance and Cost Improvements Through Thermal Management Design

March 21, 2011 • Doubletree Hotel • San Jose, California

MEPTEC is pleased to bring back our popular "The Heat is On" series, which will be a part of the **Electronics Thermal Week**. This week long event will bring together several different organizations including IEEE's long running **SEMI-THERM** conference and exposition, **JEDEC**, **ASME** and others. The event will offer a wide range of programs that will cover heat transfer cooling, thermal management, measurement and modeling markets, and much more.

The electronics industry's top three buzz words - **integration, miniaturization and functionality** - are also the top three challenges for thermal management professionals. As devices continue their inexorable drive toward smaller and smaller footprints, the thermal load becomes bigger and bigger. But, effectively managing thermal output doesn't have to be an exercise in futility. In fact, new materials and design methodologies are proving that optimized thermal management design not only improves performance, but can also reduce cost.

At this symposium attendees will learn to identify potential problems with thermal management design, effectively heading off any issues before they arise. Sessions will provide in-depth discussions for applications and end markets including hybrid and electric vehicles, LED's, Photovoltaics and Displays and will present the thermal management challenges associated with each, along with possible solutions and the resultant impact on cost and performance. All professionals involved in or concerned about effective thermal management should attend, including managers and directors who wish to become educated on these important issues.

Keynote Speaker

Energy Reduction and Performance Maximization Through Improved Cooling

David Copeland

Thermal Engineering and Packaging Technology
Oracle Corporation

Leakage has become an increasing fraction of processor power with each technology node. As leakage is strongly temperature dependent, processor power dissipation can be reduced through improved cooling. Processor frequency is strongly dependent on temperature and voltage. The voltage dependence is approximately proportional, while temperature dependence has reduced with each technology node. In the near future, the temperature dependence may near zero and possibly even result in reduced frequency at reduced temperature.

Through improved cooling, temperature can be reduced while voltage and frequency are increased, resulting in higher system performance. For a given cooling configuration, a combination of voltage and temperature exists which maximizes system performance per watt. At higher powers, additional performance is achieved at the expense of energy. Such increases may be limited by electromigration and other failure mechanisms, which are functions of both temperature and voltage. Examples of recent systems with performance levels unachievable through conventional cooling are shown.

Sessions will include:

- Thermal Limitations in Hybrid and Electric Vehicles
- Enabling Higher LED Performance with Smart Thermal Management
- Beating the Sun – Thermal Challenges for Photovoltaic Systems
- TELCO & Server System Cooling Technology Update

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QFN Packaging Advances with Routable High Density Leadframe Technology

John McMillan (CTO) - QPL, China
Jack Chen (HDL Eng Mgr) - QPL, China
Willie Morrison - QPL (US)

One of the fastest growing segments in the market today is for hand held devices. This is placing new demands on current packaging technologies. These demands are for a smaller footprint and thinner devices with excellent electrical and thermal properties while still being cost competitive.

High Density Leadframe (HDL) is the latest innovation in the QFN (Quad Flat No-Lead) packaging evolution that delivers the greatest number of leads per body size while delivering the highest performance at a lower cost. While other recent advancements in QFN technology like Dual Row QFN¹, TAPP¹ and other etch back technologies have added additional leads per a body size they do not use the area under the die which result in long wire bonds. The HDL package Technology developed in 2009 by Mr. Li Tung Lok (TL Li) of QPL Limited uses all the package area. With his years of experience in leadframe etching and QFN assembly TL Li was able to develop the HDL routable LF based package and all the required assembly processes.

Figure 1 shows designs of the same 64 lead die in a QFP, a QFN and in an HDL package. The required PCB board area is reduced to 22.5 square mm for the HDL package versus 144 square mm for the QFP and 81 square mm for the QFN package. At the same time total the bond wire usage has been reduced from 172.7mm in the QFP and QFN packages to just 65mm in an HDL package. This gives a 62% Au wire savings.

The HDL process flow is shown in Figure 2. Steps identified as 1 through 3 are performed at the Leadframe manufacturer. **Step 1:** The LF starts in sheet form of the desired Cu alloy and thickness. **Step 2:** The top surface is patterned using a standard photolithography processes and then undergoes a topside partial etch. **Step 3:** The LF undergoes a selective Ag or NiPdAu plating process on either only the top for Ag or top and bottom for NiPdAu. The remaining steps shown in Figure 1 are performed at the IC Assembly site.

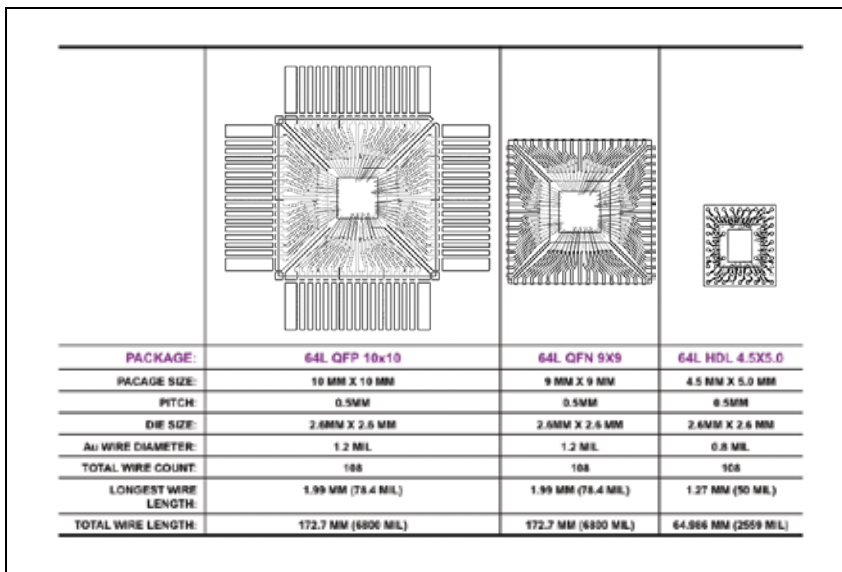


Figure 1. Package Size and Wire Consumption Comparison of QFP, QFN & HDL.

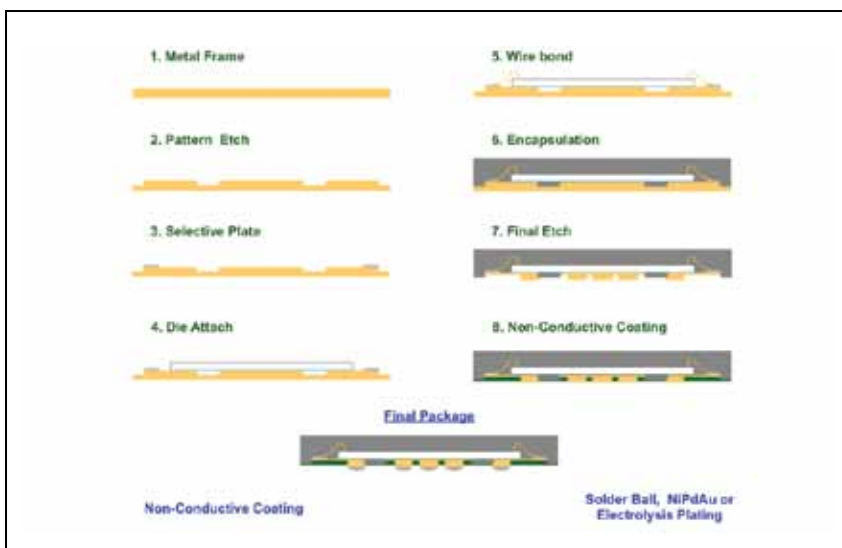


Figure 2. HDL Process Illustration.

Steps 4, 5 & 6: Die Attach, Wire Bond and Encapsulation are standard process steps used in the assembly of QFN devices. However, depending on the package configuration, the die attach epoxy can be either a conductive paste, a non conductive liquid or an

epoxy film. If traces are routed under the die, a non-conductive process will be required. HDL offers excellent wire bond characteristics as it has a solid platform and does not face the challenges of a taped QFN LF.

Step 7: The solid bottom Cu portion

¹ JEDEC Standard M0-247D

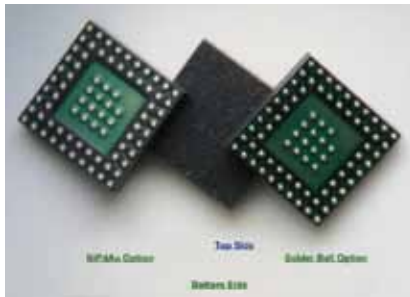


Figure 3. HDL 64L 5x5 Package with 0.5mm Pitch.

of the LF is configured and etched back isolating the traces and creating the IO's for connection to the Printed Circuit Board (PCB). Note that the traces are etched back to sit slightly below the plane of the mold compound. (See Figure 5)

Step 8: A solder resist is placed over the entire bottom surfaces but removed over the IO's and contact areas. This resist coating protects any exposed metal for being shorted during attaching the package to the PCB.

Final Package: If the contact areas are NiPdAu, the parts will proceed to saw singulation while unfinished parts with exposed copper will require a solder ball attach or an electroless plating process before singulation. (See Figure 3)

The HDL Technology allows total flexibility in designing an IC Package around a die and its application. By using the routing features contacts can be placed under the die so the final package looks similar to a Ball Grid Array (BGA) package (see Figure 3) with up to a full array of IO's on the bottom of the package.

The ability to route wire bond areas to IO's that are not directly beneath the IO gives the HDL Technology two meaningful cost reduction benefits: (1) a smaller package size per lead count & (2) the shortest wire lengths of any IC package technology with savings of between 15 and 85% of the wire used in any older packaging technology. Wire length reduction is achieved by being able to place the bonding point on the LF as close to the die as the wire bonding technology will allow. In many cases it is at .3mm or less. Figure 4 shows an HDL package compared to an 88Ld TAPP package where the body size is reduced from 7x7mm to 5x5mm and the total wire length from 112mm to 44mm, a 61% savings.

Figure 6 lists other advantages of the HDL technology over existing packaging technologies. A distinct and meaningful advantage that has been voiced by many IDM's and Subcons is that the HDL package is ready for electrical testing in strip form after the final etch process. A current subcon offering the HDL technology has proven that HDL strips can be attached to an 8-inch film frame and probe tested much like a wafer level CSP (WLCSP). This allows for easy integration of electrical testing into the HDL

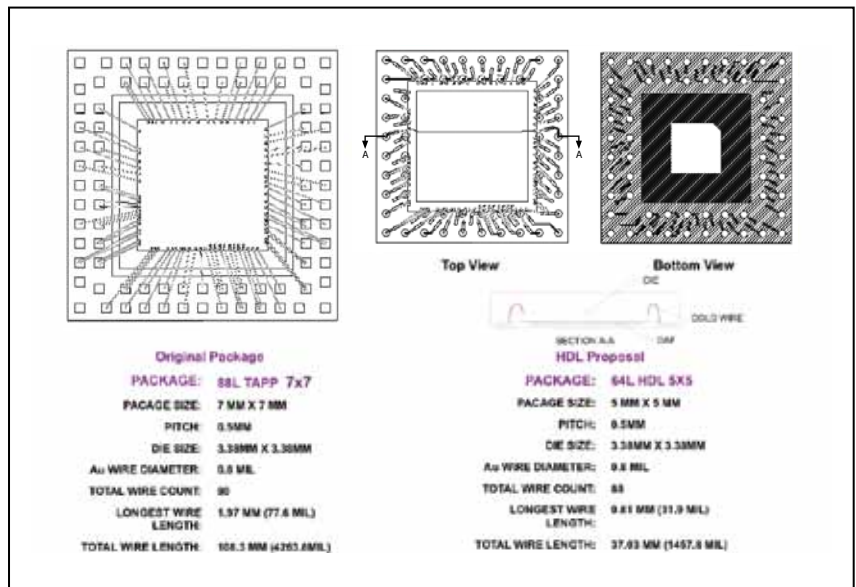


Figure 4. HDL Conversion for TAPP.

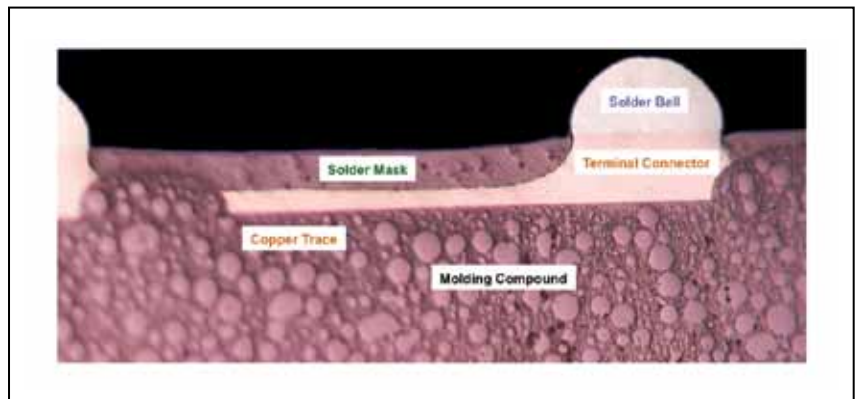


Figure 5. Cross-section of HDL Trace and Terminal Connector.

- A smaller body size per lead count that reduces PCB board area by up to 85% and increases units per strip by up to 50%.
- The shortest wire bonding lengths of any IC package technology.
- Lower cost electrical testing in its natural strip test format that allows testing like WLCSP.
- Ideal for combinations of stacked die, MCM & SIP with FC and/or WB.
- Excellent heat dissipation that is 20-30% better than BGA.
- Best wire bonded electrical performance with low inductance due to shortest electrical paths.
- Excellent reliability and MSL 1 performance - allows designs for optimum PCB routing and improves PCB mounting and rework yield.
- Thinnest package available in molded package.
- Short time to market.
- Just starting its Cost Reduction learning curve.
- No cost impact to go to finer terminal pitches i.e. .5mm to .4mm.

Figure 6. HDL IC Packaging Advantages.

assembly flow and eliminates the need for trays, tray to handler transfers and greatly reduces the total test cost. HDL technology is closing the cost gap between WLCSP and advanced QFN packages.

Conclusion

As a new packaging technology the potential for HDL technology is only just starting to be fully understood. HDL is currently in volume production and will continue to grow very rapidly going forward. More than seven IDMs are in package qualification and will soon be offering HDL packaged products. There are multiple subcons currently offering the HDL technology and more are in the final stages of evaluation. The HDL packaging revolution has started and will continue to expand and improve as it becomes the next standard in IC Packaging.

For more information on HDL Technology contact QPL sales at www.qpl.com or your subcontract assembly manufacturer. ♦

The Re-Birth of Silicon Interposers?

Jan Vardaman and Linda Matthew
TechSearch International, Inc.

Through most of the 1990s, silicon substrate technology was being developed at various companies as part of the multichip module (MCM) movement. Thin-film-on-silicon MCM-D, where D stood for “deposited”, was one substrate choice competing with laminate (MCM-L) and ceramic (MCM-C) substrates. Silicon substrates would have given a denser, higher-performance module than laminate substrates could, but ultimately the technology did not penetrate the high-volume commercial market and lost the battle to conventional laminate substrates. Essentially, the silicon substrates were excluded because of cost and logistics. The competing laminate substrates were less dense due to the rough topography of the FR-4, but had much lower cost. And from a logistics standpoint, the higher density of the silicon substrate could not be fully utilized because the large number of high lead count die that it could support created a package that was extremely difficult to test and had low yields. A technology that could not find a large market in 1995 may generate a different response today because packaging and integration have evolved substantially [1].

Drivers for Silicon Interposers Today

Silicon interposers are an option for partitioning large die, integrating single chips into a module, and reducing die size where substrate density is the constraint. One driver that has emerged more recently is the challenge of assembling die with extra-low-k (ELK) dielectrics. The problem is worst for large die, where thermal excursions are largest and stresses on the fragile dielectrics highest. Silicon substrates offer the following advantages:

- High wiring density due to the very flat substrate
- CTE matched to the silicon die
- Excellent electrical and thermal performance
- Lower laminate substrate cost due to reduced wiring density
- Lower cost of active devices due to partitioning large die with minimal effect on performance
- Higher yield (lower cost) of active devices due to smaller flip chip bump pitch

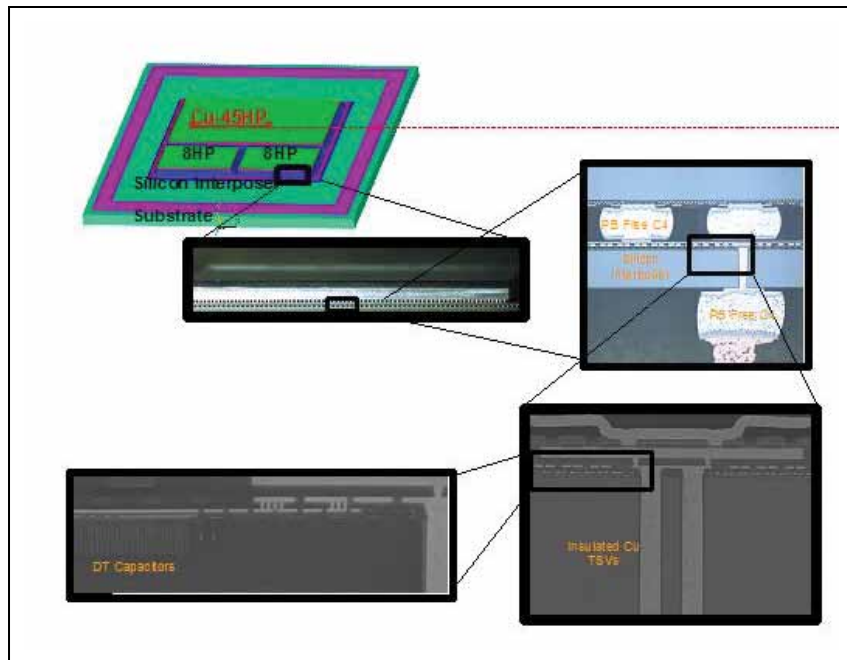


Figure 1. IBM 3D Packaging Technology.

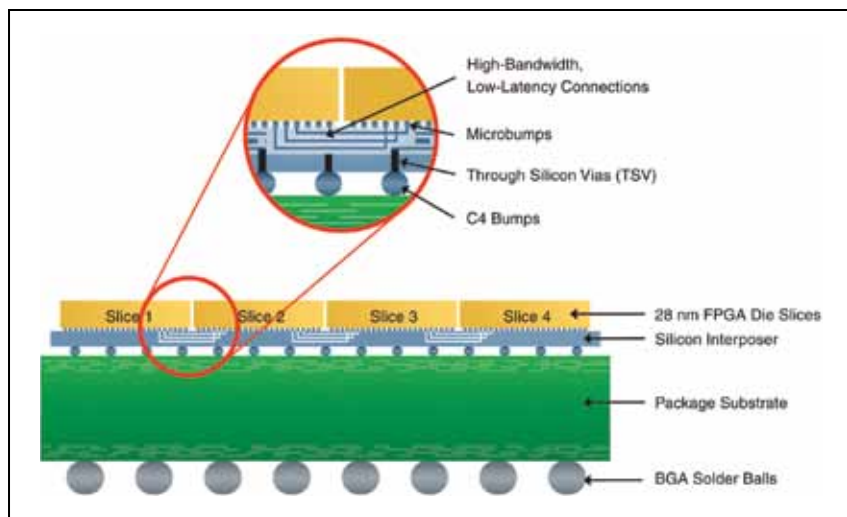


Figure 2. Package Substrate.

- Lower power requirements than equivalent single-chip packages due to multiple chips combined on one substrate
- Possibility of integrating passives into the substrate
- Cost-effectiveness if depreciated equipment is used

Silicon Interposers for Wireless Applications

Today silicon interposers are used for RF modules, where they offer the benefit of integrated passives. NXP’s spin-off, IPDiA, manufactures silicon interposers for RF modules and hundreds of millions of units have been produced. STMi-

croelectronics has internal production on thin-film-on-glass and thin-film-on-silicon and produces transceiver/receiver modules internally.

Silicon Interposer Developments

A number of companies, including IBM, have announced the development of silicon interposers as part of the flip chip package structure [2]. IBM has also described a silicon interposer in an optical transceiver module [3]. In its most recent announcement, IBM indicates that it will supply a silicon interposer to Semtech Corporation for a mixed signal application (see Figure 1). The module integrates a high-performance data converter with a DSP and includes deep trench capacitors in the interposer. The interposer enables mixed IC technologies and solves density, power, and bandwidth issues. Near-term applications include 100Gbps coherent receivers for fiber optic telecommunications, high performance RF sampling and filtering, test equipment and instrumentation, and sub-array processing for phased array radar systems. Prototypes will be available in 2011.

Xilinx announced its 28nm Virtex-7 LX2000T using a “Stacked Silicon Interposer,” a passive silicon interposer with through silicon vias produced by TSMC. The interposer, fabricated by TSMC uses 65nm silicon technology and has four conventional metal layers to connect each FPGA slice. The silicon interposer with through silicon via is mounted with flip chip interconnect on a conventional flip chip organic substrate supplied by Ibiden. Figure 2 shows the structure. It offers a 2X density improvement and provides a lower latency, and a high yield solution. Engineering samples are planned for mid-2011 and devices will be fabricated on 28nm node silicon technology. This technology development benefited from collaboration with leading industry organizations including IMEC, SEMATECH, and SEMI, as well as equipment manufacturers, fabs, and OSATs.

STATS ChipPAC described some of its developments in silicon interposers using Cu pillar and AgSn micro bumps for silicon interposer applications [4]. Test chips with a 5 mm x 5 mm outline were fabricated with 10,000 micro bumps on a 40 or 50µm pitch. The chips were flip chip bonded onto a 200mm wafer, using DOE to identify optimal process conditions. Parts were underfilled with nanoparticle underfill and subjected to JEDEC reliability testing. Samples passed MSL-3 with 3x reflow at 260°C peak temperature, unbiased HAST and HTS. No failures were reported after 500 or 1,000 thermal cycles from -55°C to +125°C.

Table 1. Specifications of Silicon Interposers under Evaluation.

Property	Value
Substrate length, width (mm)	5.5 - 55
Substrate thickness (µm)	100 - 250, 400
Via metal	Cu
RDL (number of layers)	1 - 5
Via diameter (µm)	10 - 75
Via pitch (µm)	35 - 200

Source: TechSearch International, Inc.

STATS ChipPAC has also demonstrated the ability to fabricate integrated passives on a silicon substrate [5]. A specially treated silicon substrate was used to grow three metal and two dielectric layers. M1 and M2 were 1µm and 3µm thick, respectively, and were used to form metal-insulator-metal (MIM) capacitors. Capacitance density was 330pF/mm². M3 was made of thick copper, and inductors were implemented in this layer. For RF inductors with a typical inductance <30nH, the Q factor was 25 to 35 depending on the inductance. The typical finished thickness of the wafer was approximately 250 µm. The company found that highly repeatable passive circuits such as filters and baluns could be made with this technology.

ASE sees silicon interposers as key differentiator for large die. The primary driver for silicon interposers is that they reduce the stress on die with extra-low-k dielectrics. They also provide a lower risk alternative to TSV and a high-performance multichip solution for processor-plus-memory applications where vertical stacking is not feasible due to thermal constraints. Interposers could be used for planar or stacked modules, depending on the application. According to ASE, silicon interposers could get a high-end package to market in nine months because they solve the chip-package integration issues. ASE plans for silicon interposers include using BEOL equipment for the cost advantage it provides. The timeframe for implementation will be customer-driven.

Supply Chain

The supply chain for silicon substrates has not been finalized, and there is no clear model of which companies will supply the substrates, finish the substrates (backgrind and pattern), and do the chip and package assembly. The substrate foundry could simply ship substrates, or it could manage the entire project to maintain clear hand-offs. Similarly, some package assemblers have plans to manufacture substrates in-house, while others will source interposers externally. An assembler whose customers use TSV-last technology would develop the capability to manufacture silicon sub-

strates as part of its TSV program. IDMs have some preferences in terms of materials and dimensions, but in many cases are waiting to see the offerings of the various suppliers.

Standard silicon interposers for package evaluation are beginning to be introduced, and will be helpful development tools. Dai Nippon Printing has recently introduced a standard interposer, but the specifications are larger than the interposer characteristics being considered by many companies in the industry, which may limit its usefulness. Other substrate suppliers also have plans to introduce standard evaluation parts.

A number of companies currently offer silicon interposers or have them under development. These companies include ALLVIA, ASE, Dai Nippon Printing, Ibiden, IBM, IPDiA, Nepes Corporation, Shinko Electric, Silix Microsystems, STATS ChipPAC, and TSMC. Table 1 shows specifications of silicon interposers under evaluation.

Conclusions

Silicon interposers have been investigated for more than 20 years. This time the infrastructure and the application needs seem to intersect. Facilitated by TSV development and serving as an intermediate step on the path to full 3D TSV, silicon interposers have finally found their niche.

- 1 TechSearch International, Inc., “Advanced Packaging Update: Market and Technology Trends,” June 2010.
- 2 K. Sakuma, et al., “IMC Bonding for 3D Interconnection,” Electronic Components and Technology Conference, June 2010, pp. 864-871.
- 3 F. Doany, et al., “Terabit/s-Class 24-Channel Bidirectional Optical Transceiver Module Based on TSV Si Carrier for Board-Level Interconnects,” Electronic Components and Technology Conference, June 2010, pp. 58-65.
- 4 S.W.Yoon, D. Shariff, J.H. Ku, P.C. Marimuthum and F. Carson, “3D TSV Interposer Technology with Cu/SnAg Microbump Interconnection,” 6th International IMAPS Conference & Exhibition on Device Packaging, March 2010.
- 5 K. Lu, Y.T. Lee, Y.T. Kim, G. Kim, Y. Lin, and B. Ahn, “Passive Device Integration from Silicon Technology,” 6th International IMAPS Conference & Exhibition on Device Packaging, March 2010.

Trace Laboratories Hires Nick Pawluk as Account Manager for Wisconsin and Northern Illinois



CHICAGO, IL – In order to better serve their customers, Trace Laboratories has expanded their customer service team with the addition of Nick Pawluk to the position of Account Manager-Technical. This new position will focus on the territory of Northern Illinois and Wisconsin in addition to providing increased sales support for Trace's entire customer base.

Nick has a Bachelor's degree in Mechanical Engineering and a Master's degree in Marketing Management. Prior to joining Trace-Chicago, he worked for more than 12 years as a Program Manager for an R&D (materials and mechanical engineering) testing laboratory in Milwaukee, Wisconsin. In that position he was responsible for sales, marketing, and project management. Prior to that, Nick spent most of his career in sales and marketing positions in the medical electronics industry. Nick has expertise in mechanical shock and vibration testing, durability testing, environmental testing, metallurgical and materials testing, and failure analysis.

Nick has authored several white papers on various testing modalities. He has a unique balance of both technical and sales/marketing skills, which enables him to offer quick, accurate responses aimed at providing customized solutions. With his extensive experience, Nick is a great asset to the organization.

Established over 30 years ago, Trace offers state-of-the-art testing, qualification, analysis, automation, and training in the areas of compliance, life cycle testing, printed circuit board design and best practices. Trace Laboratories has the ability to design and fabricate automation equipment for long-term reliability testing. Trace Laboratories, Inc. has facilities in Hunt Valley, MD, Palatine, IL, and Carthage, IL.

STATS ChipPAC and Intersil Qualify and Ramp Copper Wire Interconnect for High-End Analog and Mixed-Signal Devices

SINGAPORE and UNITED STATES – STATS ChipPAC and Intersil Corporation have announced that they have qualified copper wire interconnect on a number of high-end analog and mixed-signal devices that are in volume production.

Utilizing copper wire interconnect in semiconductor packages offers a number of advantages over gold wire. Copper wire is more electrically and thermally conductive, allowing it to readily replace gold wire without any decrease in electrical or thermal performance. Copper also possesses stronger mechanical properties and is capable of carrying higher currents than the same diameter gold wire, thereby allowing for longer wire lengths and increased manufacturability. These factors are important for enhanced device performance and yield.

“High-performance analog and mixed-signal markets are extremely competitive and require continuous innovation and enhancement of products and services. Using copper wire interconnect capability allows Intersil to provide its customers with performance and manufacturability advantages. Our business is dependent upon reliable fabrication, packaging and testing of our products and

we have worked closely with STATS ChipPAC to select and qualify copper wire interconnect for our package offerings. Copper may well be the new gold in semiconductor packaging,” said Sagar Pushpala, Senior Vice President of Worldwide Operations and Technology at Intersil.

Intersil and STATS ChipPAC completed a stringent qualification process with four major wafer foundries across multiple technology nodes. STATS ChipPAC established a Class 1000 cleanroom to ensure the integrity, yield and reliability of the copper material and a robust assembly and test process that has demonstrated best-in-class yields and reliability that is on par with gold wire bond interconnect.

“There are clear performance and cost benefits with the use of copper wire interconnect. Customer demand is steadily ramping up, particularly as customers see the technology mature and the proven range of package types and applications enabled with copper wire interconnect expand. STATS ChipPAC has shipped over 100 million units with copper wire interconnect in a wide range of leaded and laminate packages. We continue to expand our copper wire program to include more advanced packaging such as advanced wafer fab nodes with delicate bond pad structures, fine bond pad pitch, stacked die, die-to-die bonding and ultra low loop height applications,” said Wan Choong Hoe, Executive Vice President and Chief Operating Officer, STATS ChipPAC.

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed signal and power management semiconductors. Intersil's products address some of the fastest growing markets within the communications, computing, consumer and industrial industries.

For more information about Intersil or to find out how to become a member of their winning team, visit Intersil's web site and career page at www.intersil.com.

STATS ChipPAC Ltd. is a leading service provider of semiconductor packaging design, assembly, test and distribution solutions in diverse end market applications including communications, digital consumer and computing. With global headquarters in Singapore, STATS ChipPAC has design, research and development, manufacturing or customer support offices in 10 different countries.

Further information is available at www.statschippac.com.

SemiProbe Announces New Solar Research Probe System



WINOOSKI, VT – SemiProbe has developed a new low cost solar cell probe system for research applications. Built on the modular patented Probe System for Life™ (PS4L) platform, the system allows users the flexibility to configure their test instruments to best suit their experiments. The video microscope slides into position for probe placement and out of the way to bring in an overhead solar simulator.

SemiProbe provides manual and semiautomatic probe systems for solar cell research applications primarily focused on characterizing materials and finished solar cells.

The flexibility of the PS4L platform allows users to modify their system as their test structures and procedures change. According to Mostafa Daoudi, VP of Engineering, “This platform allows us to provide custom probing configurations in a few weeks and with unsurpassed flexibility. The PS4L system continues to gain widespread acceptance in meeting the flexibility requirements of

research and production disciplines from microelectronics, material science, biological and more.”

Modularity requirements, time to market pressures and limited research funding has all contributed to making the PS4L the ideal probing platform. The same system can be perpetually field upgraded as needs and budgets change.

SemiProbe is a global supplier of innovative probing and inspection equipment for microelectronics, photovoltaics, optoelectronics, MEMS, biotechnology, chemistry, microfluidics, and nanotechnology. SemiProbe works with leading R&D Centers globally to develop next generation equipment and then follows the product test requirements to produce full production solutions. SemiProbe offers a line of manual, semiautomatic and fully automatic systems and a complete line of accessories. The company is based in Winoski, VT USA.

More information about SemiProbe may be found at www.semiprobe.com or by calling (802) 860-7000.

Semtech & IBM Join Forces to Develop High-Performance Integrated ADC/DSP Platform Using 3D TSV Technology

CAMARILLO, CA – Semtech Corp., a leading supplier of analog and mixed-signal semiconductors, has announced it is working with IBM Corp. and its innovative 3D through-silicon via (TSV) technology to develop a high-performance ADC/DSP platform that has applications in fiber optic telecommunications, high performance RF sampling and filtering, test equipment and instrumentation, and sub-array processing for phased array radar systems.

Integration of high-performance data converters with advanced digital signal processing has traditionally been a

difficult problem due to mixed IC technology requirements, management of chip-to-chip interconnect with high density, high power and high bandwidth and limited options for high-reliability multi-chip packaging with excellent thermal man-

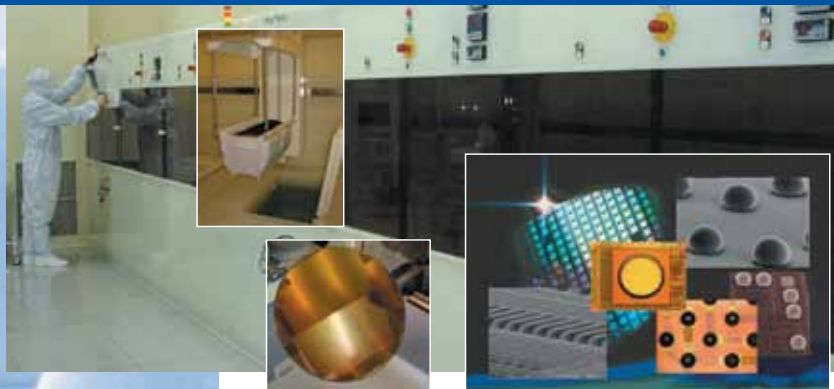
agement. Numerous emerging applications may be significantly cost-reduced, and other new applications enabled, if ultra high performance data converters and/or RF transceivers constructed in the most advanced RF-optimized technologies can

be efficiently married into a single package, along with highly-integrated application-specific digital processing constructed in the latest ultra-fine geometry CMOS technologies.

“Our strategic partnership with IBM is enabling Semtech

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<http://www.imaps.org/DevicePackaging>

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March 7-10, 2011

General Chair:

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Microelectronic Consultants of NC

3D Packaging Topical Workshop	Flip Chip Technologies Topical Workshop	Wafer Level Packaging Topical Workshop	MEMS & Microsystems Topical Workshop	Emerging Tech (LEDs & Passives) Topical Workshop
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The seventh Annual Device Packaging Conference (DPC2011) will be held in Scottsdale, Arizona, on March 7-10, 2011. It is an international event sponsored and organized by the International Microelectronics And Packaging Society (IMAPS).

The conference is a major forum for the exchange of knowledge and provides numerous technical, social and networking opportunities for meeting leading experts in these fields. The conference will attract a diverse group of people within industry and academia. It provides a chance for educational interactions across many different functional groups and experience levels. People who will benefit from this conference include: scientists, process engineers, product engineers, manufacturing engineers, professors, students, business managers, sales and marketing.

The 2011 conference will feature technical sessions, panel discussions, a poster session, professional development courses and a vendor exhibition and technology showcase. The conference provides a focused forum on the latest technological developments in 5 topical workshop areas related to microelectronic packaging.

For more information, please visit www.imaps.org/DevicePackaging

and our leading-edge customers to define and develop a unique and versatile integrated ADC/DSP platform, applicable to multiple highly demanding system applications,” said David Clark, Vice President of Microwave & Millimeter-wave Products at Semtech Corporation. “Further, this first-generation 3D multi-chip module will validate key building blocks that will enable the accelerated time-to-market of future products with unique DSP content for specialized applications.

Semtech is partnering with IBM to develop the end-to-end module solution utilizing IBM’s 3D interposer technology to interconnect ADC functions in IBM custom logic SOI-based Cu-45HP technology with interleaver ICs in IBM’s 8HP BiCMOS SiGe technology. These two different technologies are connected through a single wiring layer on an interposer, which supports a bandwidth of greater than 1.3 Tbps in this design.

IBM’s 3D technology combines cost effective 90nm BEOL wiring levels for high speed signaling between die as well as providing ultra high capacitance density by integrating deep-trench (DT) capacitors at the top surface of the interposer. As frequency increases, the use of integrated decoupling capacitors is more attractive to counteract power supply noise effects that typically may be second order issues for slower applications. The interposer also connects to a package using copper TSV technology.

“We are delighted to be working with Semtech to utilize IBM’s 300mm 3D technology for its advanced product applications,” said Dan Berger, IBM Manager of 3D Technology Development at its Semiconductor Research and Development Center (SRDC). “3D technology provides a path to integrate CMOS and SiGe technology at very high bandwidth and with low power to provide a seamless high-performance module solution. IBM’s semiconductor, wafer finishing and assembly facilities offer a one-stop module solution for Sem-

tech and its product partners. We also see significant benefits using 3D technology for other applications to address issues such as I/O power, power supply, interconnection bandwidth between components, modularity for re-use of IP or mixing technology nodes effectively, and form factor improvements that can be obtained by integrating components together in a smart cost effective manner.”

Clark added: “Once developed, the 3D TSV packaging platform can easily support future product upgrades by replacing any of the utilized IC technologies, either individually or in combination, to enhance the product performance as the next generation base technologies come on-line. For instance, future product versions could upgrade the 8HP ICs to 9HP, the custom logic Cu-45HP to 32-SOI, active circuitry could be incorporated into the interposer, etc. The modularity of the 3D TSV platform provides the utmost flexibility for product roadmap longevity.”

Semtech will have first ADC/DSP prototype modules available in 2011 and are working with partners to extend these product offerings utilizing these technology elements. Near-term applications include 100Gbps coherent receiver for fiber optic telecommunications, high performance RF sampling and filtering, test equipment and instrumentation, and sub-array processing for phased array radar systems. Semtech offers comprehensive design assistance, including field- and factory-based support. Data sheets, volume pricing, and delivery quotes, as well as evaluation kits and samples, are available at www.semtech.com/info.

Semtech Corporation is a leading supplier of analog and mixed-signal semiconductors for high-end consumer, computing, communications and industrial equipment. Products are designed to benefit the engineering community as well as the global community. The company is dedicated to reducing the impact it, and its products, have on the environment.

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For more information, visit www.semtech.com.

STATS ChipPAC's Copper Wire Bond Production Exceeds 100 Million Units with Rapid Volume Ramp

SINGAPORE and UNITED STATES – STATS ChipPAC Ltd. has announced it has shipped over 100 million semiconductor packages with copper wire bond interconnect and expects copper wire bond production volume to grow another 75% by the end of 2010 due to a rapidly growing customer base.

While copper has been used in the semiconductor industry

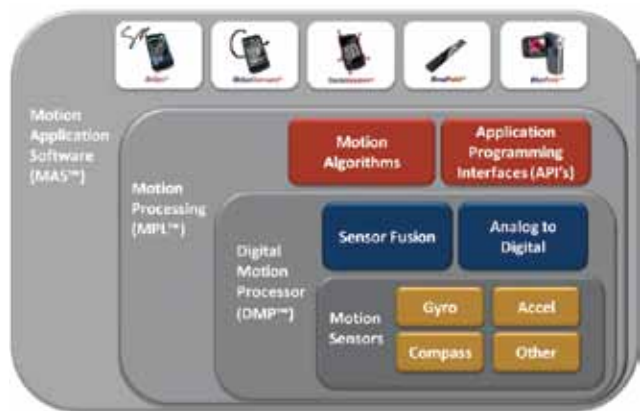
as an interconnect material for many years, there has been a recent surge in demand due to the fact that copper represents one of the most significant savings in material costs available today. The high price of gold has driven a rapid shift to copper as an attractive alternative to achieve cost savings in semiconductor packages. Originally used for low lead-count power devices, copper wire use has now expanded into mid- and high-end Input/Output (I/O) packaging, both lead-frame and laminate substrate based, and has been proven on advanced wafer fabrication nodes and fine pitch devices where it offers both a lower cost solution with improved performance. Copper wire provides better conductivity than gold or aluminum, improved electrical and thermal performance, and stronger mechanical properties.

For more information about STATS ChipPAC visit their website at www.statschippac.com.

InvenSense Announces the World's First Motion Processing Library with 9-Axis Sensor Fusion for Android 2.3 Gingerbread

SUNNYVALE, CA – InvenSense, Inc., the leading solution provider of MotionProcessors™ for consumer electronics, announced its MPL 3.2 motion processing library software support for Android 2.3 Gingerbread. InvenSense MPL 3.2 software and the companion

MotionProcessor product families provide a complete solution that delivers nine-axis sensor fusion data encompassing 3-axis gyroscopes, accelerometers and magnetometers to new Application Programming Interface (API) structures in Android Ginger bread. The new APIs (quaternion, rotation matrix, linear acceleration and gravity) for the first time allow application developers to fully leverage the benefits of the gyroscope together with the accelerometer and magnetometer. The MPL 3.2 software eliminates the challenges of integrating multiple motion sensors into Android by connecting directly to the Ginger-



bread sensor hardware abstraction layer (HAL) and delivering 9-axis sensor fusion data to the new APIs without the need for complex, processor-intensive

motion algorithm processing on the application processor. This is accomplished by pairing the MPL with a companion MotionProcessor device

North American Semiconductor Equipment Industry Posts November 2010 Book-To-Bill Ratio of .96

SAN JOSE, CA – North America-based manufacturers of semiconductor equipment posted \$1.51 billion in orders in November 2010 (three-month average basis) and a book-to-bill ratio of 0.96, according to the November 2010 Book-to-Bill Report published by SEMI. A book-to-bill of 0.96 means that \$96 worth of orders were received for every \$100 of product billed for the month.

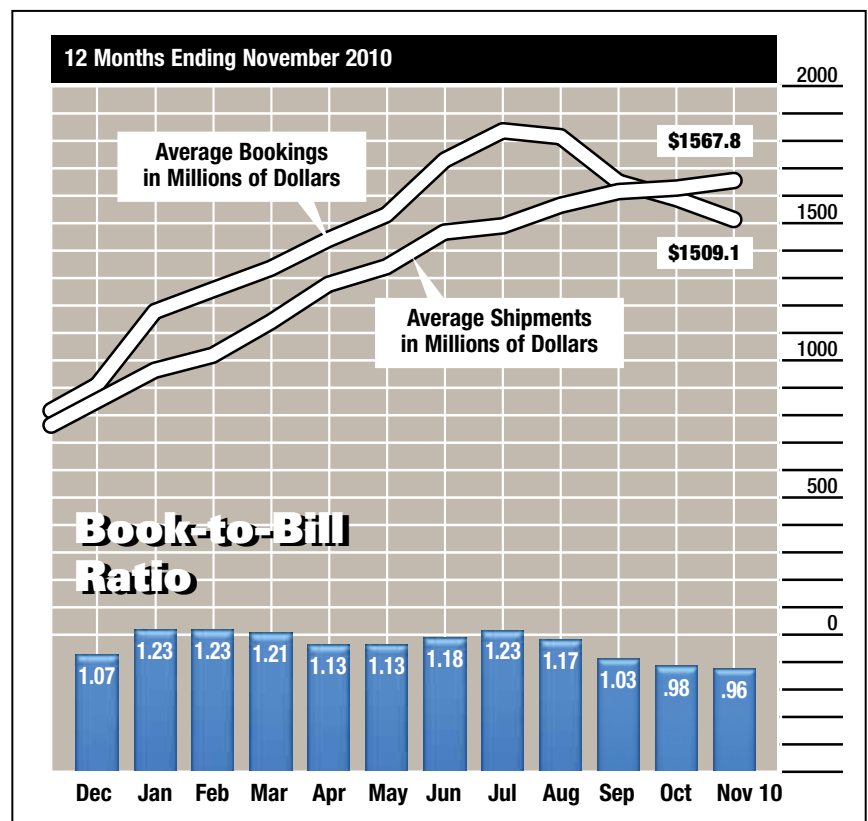
The three-month average of worldwide bookings in November 2010 was \$1.51 billion. The bookings figure is 5.3 percent lower than the final October 2010 level of \$1.59 billion, and is 90.6 percent above the \$791.8 million in orders posted in November 2009.

The three-month average of worldwide billings in November 2010 was \$1.57 billion. The billings figure is down 3.4 percent from the final October 2010 level of \$1.62 billion, and is 110.7 percent above the November 2009 billings level of \$744.2 million.

“Following a historic growth period and 18 months of sequential growth, and in accordance with seasonal trends, sales of semiconductor equipment eased in November,” said Stanley T. Myers, president and CEO of SEMI. “This tracks the bookings trend which peaked in July.”

The SEMI book-to-bill is a ratio of three-month moving average bookings to three-month moving average ship-

ments. Shipments and bookings figures are in millions of U.S. dollars. ◆



with its embedded DMP and integrated motion algorithms to offload 9-axis sensor fusion processing from the application processor. The InvenSense MPL software provides the fastest time-to-market Motion-Processing solution for Android platforms.

“The market for Android-enabled smartphones and tablets is growing exponentially due to its flexibility for UI design, hardware platforms, advanced OS features and expanding application store,” says Tina Teng, Senior Analyst, Wireless Communications, iSuppli. “The InvenSense MotionProcessing solution combined with new sensor fusion APIs in Gingerbread will allow Android devices to match or exceed the motion application capabilities of other leading OS platforms which will start a new wave of motion-based application development in the Android marketplace.”

The MotionProcessing solution from InvenSense for Android removes the complexities of multi-motion sensor integration and advanced motion algorithm development for OEMs allowing for rapid deployment of smartphone and tablet platforms incorporating 9-axis motion sensing components. The MPL software controls critical motion processing tasks including sensor device management, sensor bias calibration, sensor fusion, and gesture detection and removes the need for sensor driver and library coding by linking the sensor hardware with the Android sensor HAL and APIs and allows developers to immediately focus on unique and differentiating application development. The DMP reduces processor loading on the application processor by up to 10X and removes any real time constraints for accessing and processing the data which allows for 9-axis motion processing to be deployed on smart feature phone platforms using sub-1GHz application processors. The MotionProcessing Library is available for other popular mobile operating systems as well as for previous versions of

Android such as Éclair (2.1) and Froyo (2.2).

More information can be found at www.invensense.com.

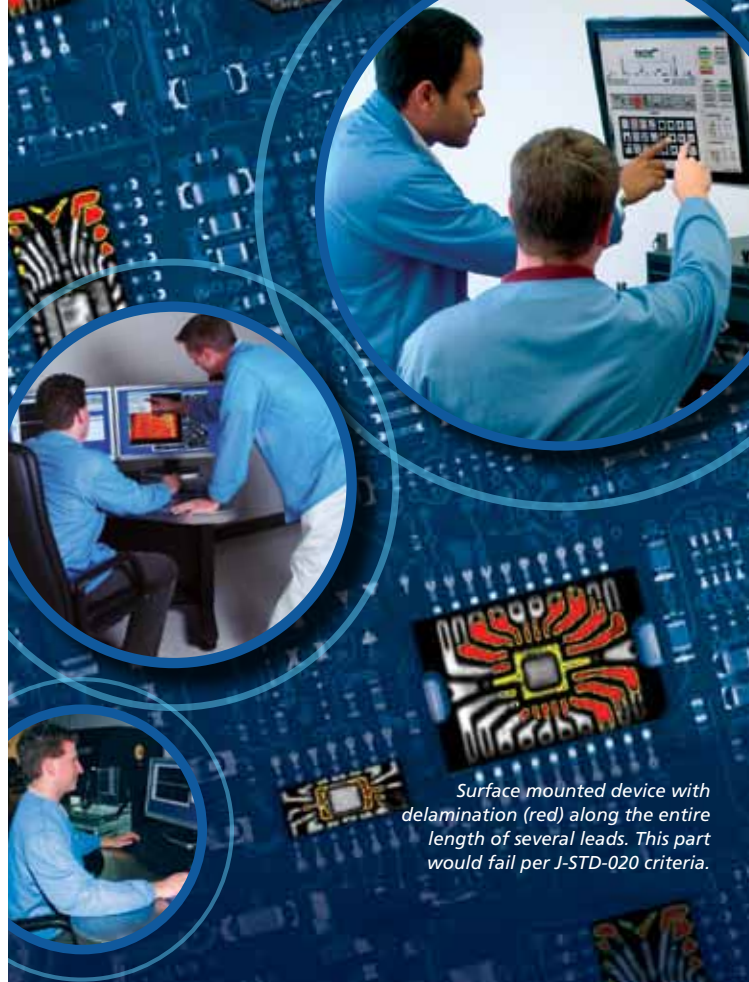
SemiProbe Marks 5th Year Anniversary

WINOOSKI, VT – Semiprobe, a global equipment supplier to the Semiconductor Industry recently celebrated their 5th year in business. Located in Winooski, VT a suburb of Burlington, SemiProbe enjoys the availability of a well educated, creative and hard working labor market. According to Denis Place, President/CEO, “This area is rich in experienced high technology workers and has for many years been a key worldwide supplier to many high technology industries with innovative products and services. We see further expansion of our products and capabilities in 2011 and look forward to building our business here in Chittenden County.”

SemiProbe finished 2010 with their best year on record with sales recorded on 5 continents. The newly patented Probe System for Life™ modular test platform has allowed customers in the semiconductor wafer probing and inspection arenas unprecedented flexibility in specifying their systems. Multiple Fortune 100 companies have selected SemiProbe product solutions as well as leading Universities and R&D centers. Concentrating on cost effective solutions to help lower their customer’s cost of test, SemiProbe anticipates an even stronger year in 2011 with recent solutions for solar cell testing, MEMS sensors, materials science studies and more.

SemiProbe was an early client member of the Vermont Center for Emerging Technologies (VCET), a Vermont high technology incubator. According to Place, “VCET provided us the early help and support we needed to get our products into the marketplace.”

More information about SemiProbe may be found at www.semiprobe.com or by calling (802) 860-7000. ♦



Surface mounted device with delamination (red) along the entire length of several leads. This part would fail per J-STD-020 criteria.

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New Die Attach Film Raises the Bar on Wetting and Molding Performance

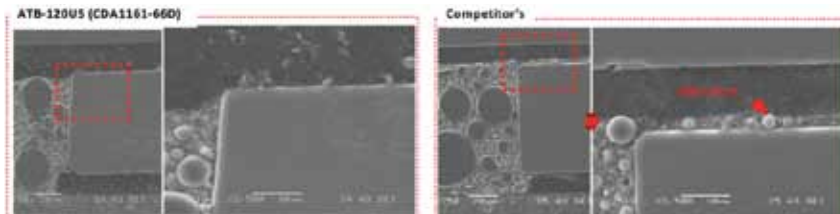
Jonathan Poo and YounSang Kim
Henkel Corporation

Complexity, functionality, miniaturization and cost-efficiency have been and continue to be the mantra of the electronics industry. Arguably, no segment is more keenly aware of this fact than the semiconductor packaging sector. As die stacks grow in number and, therefore, wafers become thinner, packaging specialists are forced to find novel materials and processes that can accommodate these demands cost-effectively. For die stacking applications that require ultra-thin bondlines and extreme uniformity, die attach film materials have emerged as one of the more robust solutions to address these device demands.

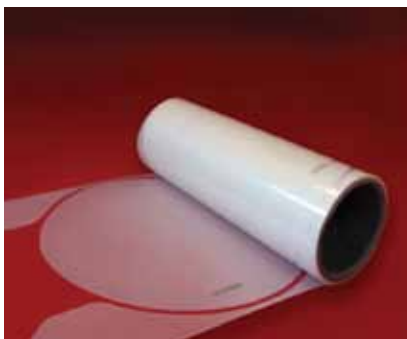
But, as die stacks have grown in number and complexity, challenges with thermal budgets, material wetting and performance during the molding process remain. For example, some films may not have good wetting performance early in the stacking and wire bonding process so wetting to the substrate is incomplete and, therefore, introduces voids into the interface. Some argue that much of the voiding can be resolved during the molding process, but reliance completely on mold pressure for void reduction is not the best approach.

Another common problem with some of today's die attach film materials is mold compound penetration. If the film is not completely adhered – all the way to the edge – to the substrate or die, mold compound materials can actually penetrate the die layers, which then causes interface adhesion strength to be weakened and results in package failure.

These hurdles, however, have been overcome with a new material innovation from Henkel. Materials scientists at the company have formulated a novel die attach film portfolio – the ABLESTIK ATB-100US series – that addresses the common performance requirements of modern die stacking processes while also delivering on some challenging characteristics such as wetting and molding performance.



ABLESTIK ATB-100US shows good mold compound penetration resistance as compared to competitive materials.



With a very long thermal budget of four hours at 175°C or 24 hours at 150°C, the ABLESTIK ATB100-US die attach film products allow for skip curing and a thermal budget long enough to ensure sufficient wetting until the last die is stacked. In fact, the ABLESTIK ATB-100US films, while shown to be competitively superior in terms of thermal budget during internal testing, are proven to have excellent wetting with minimum voids to the substrate before molding process. With this characteristic, customers do not need to be concerned about excessive voiding that molding processes may not totally eliminate.

As skip cure materials, the ABLESTIK ATB-100US products also exhibit very good resistance to molding (see image above). While the sub-par adhesion of competitive materials may allow mold compound materials to penetrate the interface, ABLESTIK-ATB100US does not. This improves device yield by eliminating any risk of adhesion weakness from the introduction of mold compound materials.

Extending cost-efficiency to manufacturers as well, ABLESTIK-ATB100US films provide excellent adhesion to copper leadframes. This is an improvement over older generation materials and allows manufacturers to reduce packaging costs by employing Cu leadframes as opposed to the more costly Alloy 42. This cost/performance value is complemented by the process flexibility the materials extend to packaging firms. The die attach materials, which have been formulated for demanding stacked die memory devices such as flash memory cards, TSOPs, BGAs and LGAs, are available in either UV or pressure sensitive (PSA) release formulations and come in a variety of thicknesses ranging from 5 microns up to 30 microns.

For memory devices manufacturers who are looking for die attach films that offer all of the requisite performance characteristics of modern die attach materials with the added advantages of extended thermal budgets, superior wetting and outstanding molding performance, they need look no further than ABLESTIK ATB-100US. Once again, Henkel has delivered on its innovation promise.

For more information on ABLESTIK-100US or any of Henkel's advanced die attach solutions, log onto www.henkel.com/electronics or call the company's headquarters at 714-368-8000. ♦




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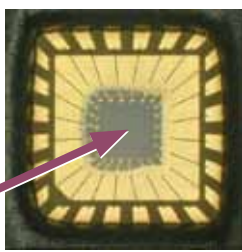
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Can We Afford Moore's Law?

Ron Jones

N-Able Group International / MEPTEC Advisory Board Member

Moore's Law is probably the most widely known characteristic of the semiconductor industry. Many are amazed at how uncannily accurate the law has proven to be. Since the law has, for many years, been used to set long term development goals, there is an alternate view that the law has become a self-fulfilling prophesy. Either way, it's had an amazing run. Gordon Moore laid down the basics of his Law in his 1965 paper. It has since been tweaked by Dr. Moore himself, and interpreted by many. He observed, "The number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years."

To those of us in the industry, we don't give it a second thought. I would guess, however, that each of us may have a little different understanding. First, it applies only to the IC chip itself. It doesn't involve packaging and it doesn't involve speed or other IC performance factors. Second, it describes an "inexpensively" cost factor. It is not what a scientist can achieve in a laboratory, but rather what can be done in a commercial environment. Third, there is the dimension of time that is not precise. Fortunately, this evens out over a period of many years.

We, as an industry, take a fierce pride in being able to do the seemingly impossible task of following Moore's Law. We can now put 10 million transistors on the head of a pin. Historical progress has caused me to focus on two main drivers for Moore's Law: wafer size and minimum feature size. In the back of my mind, I assumed you needed both to stay on target. When I started in the industry, wafer sizes were 1" and are now 12" (300 mm). Each diameter step roughly doubled the wafer area, and thus the number of chips, for around same processing cost. Over the past 35 years, geometries have gone from 8 micron (8000 nm) to

4x nm, roughly doubling the number of transistors per square inch every two years. Minimum feature size reduction has been the biggest driver of Moore's Law.

For years, there have been predictions that Moore's Law would run out of gas in x (fill in your number) years. I have always viewed being able to maintain Moore's Law from a technical capability viewpoint ... can we build and run equipment that will allow us to follow Moore's Law. I think we are beginning to reach a point where we must give serious consideration to the financial aspects of Moore's Law. Can we justify the ongoing investments to stay on the Law based on a reasonable return on investment and long term health of our industry?

For the last couple of years, we have been facing a practical decision: whether to go to 450 mm wafers or not. There is no doubt that our industry has the technical wherewithal to design, build and operate 450 mm capacity. The pesky fly in the ointment is the word "inexpensively" in Moore's Law. I have broadened this to include "total expense," which includes not only the cost of manufacturing the chips, but also the cost of designing and building the equipment and developing the processes. There is a lot of data that suggests that the industry still has not fully recouped the investment in going to 300 mm. Most of the cost of a move to 450 mm will be borne by fab equipment, fab operations and IC folks. There will, however, be some additional expense to those in the assembly/test arena, such as: probe, wafer thin, wafer bump/RDL, saw and die attach. For our industry to remain healthy, a move to 450 mm must allow vendors to recoup their investment and make a profit.

Setting 450 mm aside for a moment, these same fab vendors must continue development to allow new node jumps, which have been the main driver of the

law. The investments that have been made to drive minimum feature size have been very expensive. Over the past 15 years, we have moved from 350 nm ($.35\mu$) to <40 nm. This progress alone almost follows Moore's Law. The cost of development and equipment must also be covered by players in the supply chain for the industry to remain healthy. The outcome of this progress is that we see fabs that cost several billion dollars and mask sets that can cost many millions of dollars. There are opinions throughout the industry that the development and equipment costs for several of the recent node jumps also have yet to be recouped. There is certainly a case that can be made that a move to 450 mm with all its intendant development cost will dilute the focus and funding on node jump development to the point that no net gain will be realized.

The worst thing we could do is invest heavily to stay on Moore's Law and have several of our key companies be crippled or go out of business ... irreparably damaging the future of our industry.

There is very robust equipment infrastructure at both 200 and 300 mm. Geometries down to 5x nm can be implemented not only on 300 mm but also on 200 mm. The industry as a whole may well be better off staying at 300/200 mm and driving feature size development in the x, y and even z dimensions. No matter what, the semiconductor industry will continue to make progress so that new generations of transistors will be less expensive than their predecessors. Whether we are able to maintain adherence to Moore's Law remains to be seen. If we do start to fall off the Moore's Law curve, it will probably not be because we can't develop the technology, but more likely be because we can't justify the development and equipment cost.

◆



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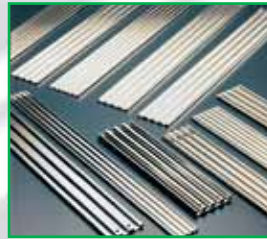
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