MEPTEC Report

FALL 2015

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 19, Number 3

MEPTEC and SEMI present

THE GREAT MINIATURIZATION:

SYSTEMS AND PACKAGING

Technology Enabling Systems in your Pocket and Beyond

NOVEMBER 10 &11 • SANTA CLARA, CA

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MEPTEC MEMBER COMPANY PROFILE

SHINKO ELECTRIC INDUSTRIES CO., LTD. is a leading manufacturer of semiconductor and microelectronic packaging products including Organic Laminate Build-up Substrates, Etched and Stamped Lead Frames, Integrated Heat Spreaders, and IC and Module Assembly.

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A Different Kind of Motivation

Jeffrey C. Demmin
MEPTEC Advisory Board Member

SALES 101 TEACHES US THAT THE key to closing a deal is knowing the motivation on the other side of the table. It could be price, performance, schedule, support … or seats in the corporate luxury box for the game next weekend. The standard answer is "all of the above," but it is usually just one of those that is the deal maker or breaker.

A good starting point in any such evaluation is money. A good price means more money in your pocket, higher performance means a higher value product, a timely schedule means earlier revenue, and good support means less internal resources needed.

The same is true on the employment side. We work for money, while other benefits and features of a job usually fill up spots 2 through N on that list. If our jobs were all fun-and-games all the time, they wouldn't have to pay us to do them.

Many people see #2 on that list of motivations as the inherent reward of building a business or contributing to the success of a company. Hopefully we have all felt that at some point, when, for example, your company mentions your project in a press release or annual report, or the stock moves because of a deal that you helped, or that critical round of funding came in because of the demo you did for the investors. I keep a file called "kudos" where I keep things like that. It's still much smaller than my "to-do" file, but at least there are a few things in there.

I recently learned something new on the motivation front, though, even at this point in a career that started at the dawn of the Fax Machine Era.

My current role is to help government agencies manage leading-edge electronics R&D programs. It is interesting to work on that kind of technology of course – interesting technology is probably in the Top Five on my motivation list – but the real pay-off has been in gaining insight into how it makes a real difference to the highest-level priorities of our nation.

Technology has become synonymous with "coding," which does a disservice to the promotion of technology among today's students. There is so much more to technology, not to mention a much broader range end uses. I have learned that with my modest contributions to technology programs for our national security.

I recently had the privilege of attending a meeting that reviewed the latest issues in electronic warfare, as well as the upcoming requirements for the components and systems for those applications. Participants included individuals with active duty assignments in the field. It was very sobering to learn about the challenges they face. Seeing exactly how the tasks that I am working on will increase the chance of those people returning from their missions really highlighted the importance of what we are trying to accomplish. Anyone who has worked in the mil/aero field knows this at some level, but putting faces to the beneficiaries of the progress was an eye-opener.

Much of the technical world these days seems to be motivated by the next killer app, where "app" is now exactly that – software that facilitates some particular activity on your smartphone. Technology has become synonymous with "coding" in the mainstream media, which I think does a disservice to the promotion of technology among today's students. There is so much more to technology – materials, optics, circuits, biotech, energy, etc. – not to mention a much broader range end uses. I have learned that in the clearest way possible with my modest contributions to technology programs for our national security. I don't mean to diminish the accomplishments or motivations of those who have contributed in other areas of our society, but I'm glad to be doing what I'm doing now. I'm not thrilled with the coat-and-tie culture in our nation's capital (especially in the temperature-and-humidity chamber of the DC summer!), but that seems like a small sacrifice in the context of the programs that I am working on.

Being driven at work by something beyond the immediate business angle is a new experience for me, and I hope that all of you get exposed to a full range of motivations over the course of your career. ◆

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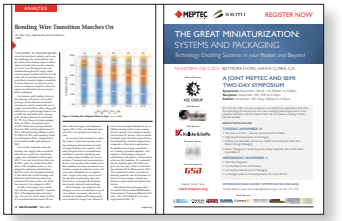
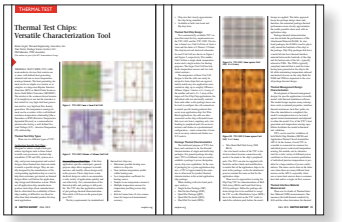
ON THE COVER

MEPTEC and SEMI jointly present *The Great Miniaturization: Systems and Packaging - Technology Enabling Systems in your Pocket and Beyond*, a two-day symposium to be held November 10th & 11th in Santa Clara, CA. The first day of this two-day symposium will address the applications that drive the technology; the second day will cover emerging technologies and a wrap-up panel discussion with the experts. Each day will feature a leading industry keynote speaker.





MEPTEC

THE NEXT GENERATION

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BETTER TECHNOLOGY STRONGER TOGETHER

JCET Completes Acquisition of STATS ChipPAC to Ascend to a Leading OSAT Player Globally

China's leading semiconductor packaging and testing company, Jiangsu Changjiang Electronics Technology (JCET, SHE: 600584), successfully completed the acquisition on Aug 5 2015 of STATS ChipPAC, a leading provider of advanced semiconductor packaging and test services headquartered in Singapore. This USD 780 mn transaction was originally announced on Dec 30 2014, and was conducted through JCET-SC (Singapore) Pte. Ltd., a subsidiary of JCET.

This acquisition will escalate the combined entities to one of the world's top outsourced semiconductor assembly and test (OSAT) players. As a combined group of companies, JCET and STATS ChipPAC offer a broader technology portfolio with significant manufacturing scale in key semiconductor geographies. The acquisition will also improve the competitiveness of the Chinese semiconductor packaging and test industry with a strong intellectual property (IP) and innovation portfolio built around advanced technologies acquired by JCET.

"The completion of our acquisition of STATS ChipPAC is an important step for us, and it presents an exciting win-win opportunity for both companies, supporting our long-term success," said Xinchao Wang, Chairman of JCET. "Post acquisition, the combined entities will provide one of the most extensive product/service portfolios to a highly diversified customer base with wide geographical coverage. Our leadership position in advanced packaging technologies will be further strengthened through the acquisition. JCET and STATS ChipPAC are working together to deliver the substantial revenue and cost synergies for our investors."

For more information, visit **www.cj-elec.com** *or* **www.statschippac.com**.

JCET

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AMKOR'S CHINA OPERATIONS TO EXPAND BY 45%

Amkor has announced plans to expand its state-of-the-art assembly and test factory in China's Shanghai Waigaoqiao Free Trade Zone. With this project, Amkor expects to increase its manufacturing facilities in China by 45%. Amkor plans to invest around $60 million for construction of the new facilities, which is scheduled to be completed by the summer of 2016.
www.amkor.com

STATS CHIPPAC APPOINTS NEW CO-PRESIDENT AND CEO

STATS ChipPAC Ltd. has announced the promotion and appointment of Dr. Han Byung Joon ("Dr. BJ Han") as Co-President and CEO, together with Mr. Tan Lay Koon. Mr. Koon and Dr. Han will both report to the Board and be jointly responsible for management, strategy and performance of the Company.
www.statschippac.com

MICRON AND INTEL PRODUCE BREAKTHROUGH MEMORY TECHNOLOGY

Intel Corp. and **Micron Technology, Inc.** have unveiled 3D XPoint™ technology, a non-volatile memory that has the potential to revolutionize any device, application or service that benefits from fast access to large sets of data. Now in production, 3D XPoint technology is a major breakthrough in memory process technology and the first new memory category since the introduction of NAND flash in 1989.
www.micron.com ◆

ASE Reports Highest-Ever August Sales

Advanced Semiconductor Engineering Inc. (ASE), has posted its highest-ever August sales, with market analysts attributing the growth to an increase in orders from Apple Inc., which is expected to unveil the next generation iPhone later in the week.

In August, ASE recorded NT$22.92 billion (US$695 million) in consolidated sales, up 5.8 percent from a month earlier and also up 9.5 percent from a year earlier.

ASE, which has been dubbed one of the important Apple concept stocks in the local equity market, said that sales generated from its IC packaging and testing operations totaled NT$13.47 billion, up 4.1 percent from a month earlier but down 3.2 percent from the same period of a year ago.

In the first eight months of this year, ASE's consolidated sales rose 16.31 percent from a year earlier to NT$179.47 billion.

Analysts said that Apple's new iPhone models, likely to be called the iPhone 6S and iPhone 6S Plus, use ASE's system-in-package (SiP) technology for the chips used in the new iPhone models.

Analysts said that ASE's consolidated sales for the third quarter could range between NT$74 billion and NT$77 billion, up 5-10 percent from the second quarter, while the company's IC packaging and testing sales are likely to grow 1-5 percent sequentially in the July-September period, and its electronics manufacturing services revenue is expected to grow 7-10 percent.

On August 21, ASE announced that it would launch a tender offer to buy a stake of up to 25 percent in Siliconware Precision Industries Co. for NT$45 per share on the open market between Aug. 24 and Sept. 22.

To fend off ASE's interest, Siliconware and Hon Hai Precision Industry Co. signed an agreement Aug. 28. Through a stock swap, Hon Hai will hold a 21.24 percent stake in Siliconware and become its largest shareholder, while Siliconware will hold a 2.2 percent stake in Hon Hai.

But ASE said that the tender offer will continue to proceed and expressed hope that the company will forge a close tie with Siliconware through the acquisition to take on escalating competition in the global IC industry.

Siliconware ranks as the third-largest IC packaging and testing firm after ASE and U.S.-based Amkor Technology Inc. ◆

Medtronic Announces Multi-Year Community Sponsorship with Minnesota Vikings

MEDTRONIC AND THE Minnesota Vikings have announced a 10-year partnership that includes the exclusive sponsorship of Medtronic Plaza, the three-acre gateway between downtown Minneapolis and U.S. Bank Stadium; a community service program with the Vikings; and a permanent display of the history of medical technology innovation that will be featured in the Medtronic Club inside the stadium.

Medtronic's partnership with the Minnesota Vikings is the latest example of the company's ongoing presence in the local community which includes supporting institutions such as the Minnesota Zoo, the Science Museum of Minnesota. ◆

Finetech Releases New Version of MiniOven for BGA Reballing and QFN Prebumping

FINETECH IS PLEASED to announce the release of a new version of the popular Martin MiniOven BGA/CSP reballing and QFN prebumping system. The MiniOven 05 provides enhanced process capability with updated firmware and increased control and temperature stability.

The highly efficient hybrid heating technology heats electronic components similar to a standard reflow oven: gently and simultaneously from all sides, ensuring process repeatability with high yields. A large 4-button front display enables fast set-up and management of multiple user-defined reballing and prebumping profiles.

Profiles are easily generated using the system's auto profile software and external thermocouple for real-time product temperature feedback. The MiniOven 05 supports inert atmospheres such as nitrogen and utilizes an advanced gas distribution system, providing an inert blanket to displace oxygen.

All of these technical innovations result in increased performance and operating simplicity. This compact, robust system is easy to use and is perfect for production and R&D environments.

For more information go to www.finetechusa.com. ◆

Qualcomm Introduces Next-Generation Fast Charging Technology with Quick Charge 3.0

Qualcomm Incorporated has announced that its subsidiary, Qualcomm Technologies, Inc., has introduced its next-generation of fast charging technology with Qualcomm® Quick Charge™ 3.0 technology. Quick Charge 3.0 is the third generation of this technology and is the first of its kind to employ Intelligent Negotiation for Optimum Voltage (INOV), a new algorithm developed by Qualcomm Technologies, designed to allow portable devices the ability to determine what power level to request at any point in time for optimum power transfer, while maximizing efficiency. With Quick Charge 3.0 you can charge a typical phone from zero to 80 percent in about 35 minutes compared to conventional mobile devices without Quick Charge that may typically require almost an hour and a half. ◆

INDUSTRY INSIGHTS

By Ron Jones

The Second SEC Conflict Minerals Filing

THE DODD-FRANK ACT REQUIRES SEC filers that use Tantalum, Tin, Tungsten or Gold (3TG) in their products to report conflict mineral information annually to the SEC. While this directly impacts public companies, it indirectly impacts private and public companies throughout their supply chain. For the semiconductor industry, fabless and IDM semiconductor companies, wafer foundries and OSAT's and many direct material suppliers are affected.

A Form SD is due each year by the end of May for the previous January 1 to December 31 compliance year.

In early August, a team from Tulane University, headed by Dr. Chris Bayer, released an analysis of the Compliance Year 2014 filings. The data was taken from publicly available information on Edgar. Please refer to table below.

On a summary level, the 2014 filings were similar to the 2013 filings in quantity and content. The quality and depth of detail on many 2014 filings were an improvement over 2013. This is to be expected as 2013 was the first filing year and there were no previous filings to reference. Almost all companies (98%) submitted their filing on or before the deadline.

Over 75% of the filers are classified as manufacturing companies, based on their SIC codes. This is not surprising as manufacturing companies would have a higher probability of using 3TG than service companies, for instance. Of interest to our industry, 113 of the 980 manufacturing filers (12%) are from SIC Code 3674 "Semiconductor and Related Devices." While this may not seem significant, semiconductors filers are the largest group and equal to the next three industry segments combined.

The minimum SEC filing for a public company that uses one or more 3TG's is a Form SD. Depending on what is discovered in performing the required Reasonable Country of Origin Inquiry (RCOI), a company may also be required to file a Conflict Minerals Report (CMR) along with their Form SD submission. Twenty percent of filers submitted only a Form SD. This generally means that they had no reason to believe that any of their 3TG was sourced from the Democratic Republic of Congo or 9 adjoining countries (DRC+9). Eighty percent of filers either knew that some materials were sourced from DRC+9 or were not able to determine that they were not. This determination triggered the need for a process called Due Diligence and required those companies to file a CMR.

For the first two filing years (2013 and 2014), companies could declare that they were not able to determine the source of their 3TG (Conflict Undeterminable). On April 29, 2014, the SEC announced that companies did not have to explicitly declare their product status based on a "First Amendment Right" challenge. Though companies did not have to specifically declare undeterminable, it was clear from filings which companies were Conflict Undeterminable, whether explicitly stated or implied. Eighty-one percent of filers were Undeterminable.

If a company is required to file a CMR, it is supposed to include information about the smelters that processed the 3TG and also the Country of Origin (CoO) where the mineral extraction took place (not always the same country as the smelter.) Only 40% of CMR filers provided the list of SoR's and only 30% provided the country of origin. This is a significant gap between the SEC requirements and what many filers were able to provide. There will be pressure going forward for companies to comply with these requirements to a greater extent.

Only 6 companies undertook Independent Private Sector Audits (IPSAs) in the 2014 filing. The original regulations said that there was a two year period where companies filing CMR's did not have to undertake an IPSA. Based on the April 29 SEC guidance, no company will ever have to undertake an IPSA unless they want to declare products to be conflict free. If the "First Amendment Right" stay is struck down, many/most companies that source 3TG from the DRC+9 will be required to undertake an IPSA. This is potentially a major disruption for public companies and the audit community. ◆

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

Categories	Number	Percent
Companies filing	1267	100%
Companies filing on time	1242	98%
Manufacturing companies filing	980	77%
Semiconductor companies filing (SIC 3674)	113	12%
Companies filing Form SD only	252	20%
Companies filing Form SD and CMR	1015	80%
CMR filers that filed Conflict Undeterminable	822	81%
CMR filers that listed SoR's	419	40%
CMR filers that reported at least one CF SoR	568	56%
CMR filers that listed Country of Origin (CoO)	326	30%
CMR filers that listed SoR's and CoO's	282	28%
CMR filers undertaking IPSA's	6	0.6%

Analysis by Tulane University

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Headlines, Trend Lines, or Expertise?

THE RECENT STOCK MARKET sell-off caused significant emotional distress to many investors who were caught off-guard. Looking past "the sky is falling" headlines, what business lessons should be learned from this "correction" as they say in market-speak? There are many parallels between the stock market and corporate strategic planning. Many of these parallels are also illustrated in the development of a new industry event, BiTS Shanghai.

The same main characters in the financial markets appear in corporate planning: the Trader, the Emotional Investor, the Professional, and the Advisor:

- The Trader has replaced seasoned investors as many financial firms have shifted from Professional Investing to Trading. Traders make money on the transactions and the volatility of the markets versus investing and growing businesses. Similarly, there are those who participate in the planning cycle as another "check the box" exercise or attempt to game it to increase their compensation.
- The Emotional Manager gets swept up in the optimism of the plans and commits many of the mistakes made by an amateur investor. The Emotional Investors were the most likely to have been lulled into a false sense of security on the basis of the trend lines mixed with emotional optimism. Like these investors, you cannot assume that short-term trends will result in long-term growth.
- The Professional (who I hope are the majority of readers) realizes that long-term value and profit requires substantial planning because "past performance is no guarantee of future results". They are planners who value objectivity to avoid the complacency of simply following trend lines.
- The Advisor provides independent strategic and tactical advice based upon their industry expertise and emotional detachment to properly value and analyze the situation. Professionals rely on Advisors because of their specific expertise combined with objectivity to counterbalance the "short-term traders" and emotional players.

Corporate strategic planning is often built on a rosy set of assumptions and linear thinking compounded by emotional attachment of the existing teams. The Emotional Investor incorrectly considers the sunk cost instead of the future and opportunity costs. These plans may fail to include possible disruptions to the overall market or the specific markets in which the company operates. **In fact, many of the disruptions that do occur are "black swan" events that could have been identified and predicted in advance.**

Why were these potential disruptors not predicted? Perhaps it is due to lack of knowledge or imagination of the current corporate team. The team may have been doing planning the same way (successfully, one would hope) for so long that they have become complacent. Or perhaps the team hasn't looked far and wide enough to see new trends or technologies. The value of an outside consultant, in the Advisor role, during the strategy planning cycle is that they can provide cross-domain expertise and perspective to avoid black swans. The Advisor's emotional detachment should also challenge the team to look beyond their default assumptions and consider new opportunities and processes.

There are amateur investors who believe betting against a company and shorting a stock is fundamentally wrong. And there are plenty of C-suite people who are not willing to plan for bad times or significant market disruption since they don't want to be a pessimist or naysayer. When the original plan fails is not the time to find out that no one considered the strategy let alone had a "Plan B" or a "Plan C". While tactics can be adjusted on the fly, proper strategy to direct the tactics takes time and considerable effort to develop. The necessary research and development of the fundamentals may take many months and cannot be rushed in the middle of a crisis.

You did not contemplate your two biggest competitors merging so you did not build relationships with others in the industry to team or merge with? A new technology just obsoleted your product and you have no blocking intellectual property or competing technology under development? ***If these unfortunate scenarios apply to your company, now is time to fix them*** *or move on before you seriously consider shorting your own stock.*

Predicting the future is very difficult. If I knew exactly what the market was going to do tomorrow, I would be too busy enjoying my retirement to write this column. **What one can and should know is the range of scenarios:** the market may go up, the market may go down, the swing may be small, or the swing may be large, etc. **And for each scenario what action should one take.** Historical data will often show the probability of each scenario which can be factored into the planning process. Like the market itself, in planning there is no guarantees of results.

Yes, there are metrics that provide indicators of a company's financial health and performance. Revenue, gross margin, inventory, P-to-E (Price/Earnings), dividend yield, etc. are all important. Investors can take these metrics into account as part of their valuation of an enterprise. Judging the quality and past performance of an organization is important in determining one's investing tactics. Having more data doesn't allow a prediction of the direction of a company's stock price but it may improve one's overall assessment of the intrinsic value and future prospects. In corporate planning one wants more data to predict the future. In this era of Big Data one can dream of having the perfect set of data to predict the future. Big Data works best when talking about large populations to predict average behavior. For example, based on tens if not hundreds of thousands of past transactions if an individual buys these two products they are likely to buy this third item 73% of the time. However, with the type of events and market specifics being forecasted in corporate planning it is unlikely that there is sufficient data such that the law of large numbers applies.

Therefore the proper corporate strategy is to prepare for all the likely scenarios and determine courses of action for each

to properly maximize each opportunity and manage the downside risk. If one doesn't, the organization will be caught unprepared when a 10% probability occurs and their biggest competitors merge or worse.

There are also plenty of situations where there is simply no relevant data available. Or the cost of obtaining that data is greater than the downside risk. In these cases, it is best to proceed with caution and limit the downside risk. A close to home example: the **Burn-in and Test Strategy (BiTS) Workshop decided that we should hold a one-day adjunct event in Shanghai China on October 21, 2015.** All the workshops in the entire sixteen-year history of BiTS have been held in the spring in Phoenix Arizona. If we chose to do another similar event in the Phoenix area we would be well prepared to estimate attendance, build a budget, and plan the event with reasonable confidence.

However, it is clear that Shanghai is not Phoenix on so many levels. **Many of our planning and some of our delivery processes were transferrable however very little of our data was applicable.** Yes, we did gauge initial support from exhibitors, sponsors, and past attendees of BiTS which was overwhelmingly positive. Even with this, we needed to be cautious due to the emotional investment of the committee and the potential participants we talked with. What we won't know until after the event is how well we did in attracting qualified attendees. With a large number of semiconductor design, packaging, and test facilities near Shanghai, we know we can fill the venue more than twice over. But a key success measure is having an audience of qualified attendees who care about the technical content of the presentations and the vendor exhibition.

BiTS Shanghai is clearly a "just do it" project for the entire BiTS committee: engage Advisors, plan to the extent possible, work hard to execute, and measure the results. The Advisors with local knowledge and expertise – not to mention contacts - have been invaluable with both the planning and execution. Without these Advisors, this event would have died in the concept stage. Yes, the first year may be "bumpy" since it is a new event but waiting longer for better data (if it is even available) would be a case of "analysis paralysis". This is where experience is more informative than data. Our processes will gather data to inform decisions for BiTS Shanghai 2016 and beyond. However, data will not assist in the short term.

Experience provides the knowledge of how to plan and not overreact emotionally. Data is used in the planning to build models that include probabilities and risk. And expertise tells you how to interpret the data, what else to consider, and how to operate when there isn't data. **It is expertise that converts data into knowledge, filters headlines, and finds meaningful trend lines.**

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.

Bonding Wire Transition Marches On

Dr. Dan Tracy, Industry Research & Statistics
SEMI

"COST-DOWN" IS A MANTRA HEARD across the electronics industry and is one that challenges the semiconductor supply chain as the industry seeks to deliver improved performance to the consumer at a lower cost. Pricing pressures are abundant throughout the supply chain and can impact material selection in both wafer fab and package manufacturing. A particularly dramatic change in materials has been observed over the past seven years as companies sought to reduce the impact of gold metal costs in semiconductor packaging.

For decades gold bonding wire was the mainstay material in wire-bonded packages. Semiconductor manufacturers began to closely examine the use of copper wire material to offset rising gold metal prices as gold pricing began to rise in 2006. By September 2011, average gold pricing peaked at its record high, $1,772/ Troy Ounce (trz) and remained above $1,660/trz throughout much of 2012. Gold metal pricing subsided from late 2012 and throughout most of 2013, with gold pricing falling to below $1,300/trz in 2013 and remaining at this level throughout 2014—though still at levels almost double gold pricing in 2007.

As a result, companies along the bonding wire supply chain invested in alternatives to gold wire, specifically copper wire, palladium-coated copper (PCC) wire, and silver/silver alloy wire. In 2007, gold wire totaled about 98% share of the 16 billion meters of wire shipped to packaging manufacturers. By 2013, gold wire shipments declined to just about half of total bonding wire shipments and further declined to an estimated 44% share of the over 20 billion meters of wire shipped in 2014.

In 2014, total copper wire, including both bare copper and PCC, captured 48% of the shipment share and silver-type wire grew to an 8% share. In 2015, it is forecasted that this trend will continue with total copper wire shipments topping 50% of the total shipment share and silver wire gaining some share as well.

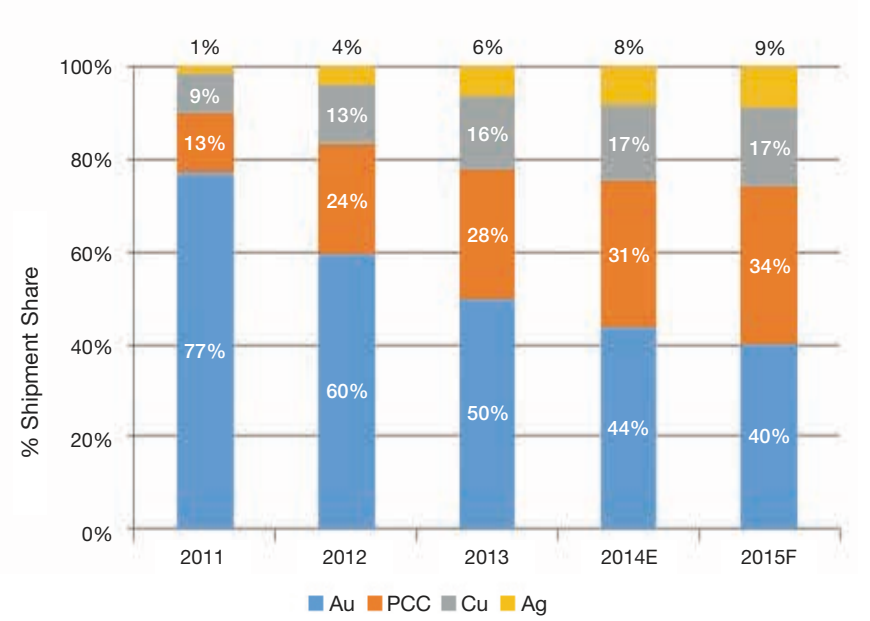

Figure 1. Bonding Wire Shipment Share by Type. *(Source: SEMI)*

To succeed at this transition to reduce the impact of gold metal pricing, leading packaging subcontractors invested in copper bonding wire capacity, with many integrated device manufacturers and fabless customers qualifying and now using copper bonding wire in new products. Consumer and communication devices were products that initially drove this transition but usage and interest now includes a range of industrial, server, and even some automotive device applications. Copper wire usage occurs across the spectrum of packaging types and form factors, covering both leadframe and organic substrate-based packages.

Silver bonding wire usage has also emerged as a low cost alternative to gold wire without, necessarily, the need for investments in high-end bonding equipment needed for copper wire. Interest in silver wire developed initially for use in LED packaging and for some memory devices, though it has ramped in production for other IC devices, such as mobile baseband chips. The latter typically have less demanding reliability requirements compared to other device applications. In addition to packaging manufacturers, bonding equipment suppliers, wire suppliers, and bonding component manufacturers all played a critical role in achieving this transition. It is estimated that the industry spent $2.8 billion on gold wire last year, which is well below the estimated $5.5 billion spent in 2011. This collaborative effort succeeded in reducing material costs in electronics in the face of increasingly complex performance requirements and tighter form factors.

Interested in the packaging materials market? Please seethe SEMI Global Semiconductor Packaging Materials Outlook—2013-2014 Edition (www.semi.org/en/node/45446) ◆

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A JOINT MEPTEC AND SEMI TWO-DAY SYMPOSIUM

Symposium: November 10th & 11th, 8:00am to 5:00pm
Reception: November 10th, 5:00 to 6:30pm
Exhibits: November 10th Only, 10:00am to 6:30pm

The first day of this two-day symposium will address the applications that drive the technology; the second day will cover emerging technologies and a wrap-up panel discussion with the experts. Each day will feature a leading industry keynote speaker.

SESSION TOPICS INCLUDE:

TUESDAY, NOVEMBER 10

- The Genius of Cars – and why Semiconductors Matter
- High Speed Components and Packaging
- Medical and Wearables for Human Health: Connecting the Dots from Silicon through Packaging
- Power Management and Energy Harvesting: Opposite sides of the Same Coin Battery?

WEDNESDAY, NOVEMBER 11

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- On the Road to SiP and Modules
- Carrying the Standard(s) for Packaging
- IC-Package-System Co-Development in the New SIP Era

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SHINKO

Interconnecting our Future

SHINKO Headquarters in Nagano, Japan

SHINKO ELECTRIC INDUSTRIES CO., LTD. is a leading manufacturer of semiconductor and microelectronic packaging products including Organic Laminate Build-up Substrates, Etched and Stamped Lead Frames, Integrated Heat Spreaders, and IC and Module Assembly.

Founded in Nagano, Japan in 1946, SHINKO initially developed a technology to recycle light bulbs; this beginning was the inspiration behind the SHINKO name, which means "new light" in Japanese Kanji. Since then, Shinko has evolved and built success through technology leadership, state of the art manufacturing, and by offering a wide variety of high quality products for diverse markets in the semiconductor industry.

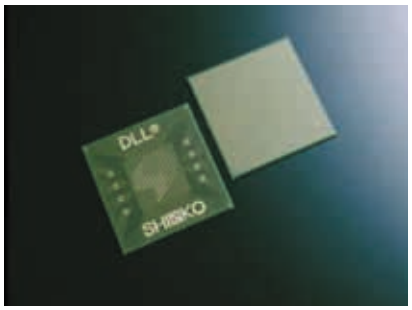
ORGANIC LAMINATE BUILD-UP SUBSTRATES

SHINKO became the first company in the world to provide DLL® FC-BGA substrates for the packaging of IC's in 1999. DLL® substrates are appropriate for a number of applications including; servers, MPU, GPU, chipsets, memory and ASIC's.

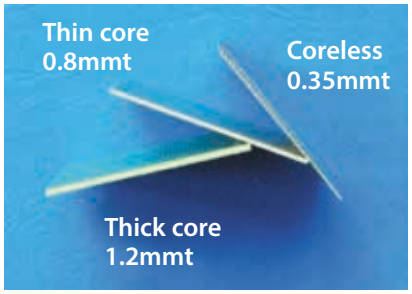
SHINKO maintains its position as a world leader with advanced design rules and unmatched quality and reliability. DLL® substrates can be found in the latest PC's, laptops, mobile devices, and gaming consoles. SHINKO can provide high performance solutions for any application utilizing the latest low CTE and low loss materials.

For higher density and low z-height, SHINKO's DLL3® coreless substrates can reduce layer count, package height and cost compared to equivalent cored substrates. SHINKO established themselves as a leading supplier of coreless DLL3® substrates in 2010 with the start of high volume manufacturing (HVM). DLL3® offers improved design flexibility, low loop inductance and fine C4 bump pitches. Available structures are from 5 to 13 layers.

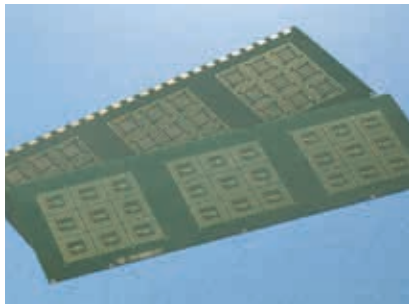
SHINKO's IVH and IVH3 pre-preg substrates are the perfect solution for low power and mobile applications. Utilizing the latest in ultra-thin core and ultra-low CTE materials, these substrates can meet increased market demands for thinner packages while maintaining warpage control. IVH (cored) and IVH3 (coreless) are perfect for mobile processors, PoP memory, and SiP. Available in strip format, SHINKO can customize layouts to maximize HVM throughput for FC or Wire-bond assembly.



DLL® "Direct Laser Laminate" Substrate.



DLL3® Substrate.



IVH and IVH3 Interstitial Via Hole Substrate.

IC ASSEMBLY

SHINKO offers unique solutions for high performance packaging technologies across a wide range of markets. From mobile, to industrial, to automotive; SHINKO provides high yielding, quality packages designed to exceed the requirements for each application.

SHINKO's innovative MCeP® (Molded Core embedded Package) technology utilizes the know-how of today's FCBGA packaging to create a unique and robust embedded die solution. MCeP® allows for high performance, vertical stack solutions while reducing the package footprint simultaneously.

SHINKO's 300mm Cu Pillar bumping can also be utilized to achieve a fine pitch flip chip connection such as 50μm inline and 30/60μm staggered. For applications requiring multiple component solutions, SHINKO offers SiP/Module design and IC assembly.

Simulation services are also available to help guide a path towards warpage control or optimizing electrical/signal performance, depending upon the application.

As an ISO/TS16949 certified facility, SHINKO is well-suited to providing total solutions for design, assembly and testing on a wide range of package configurations.

LEAD FRAMES

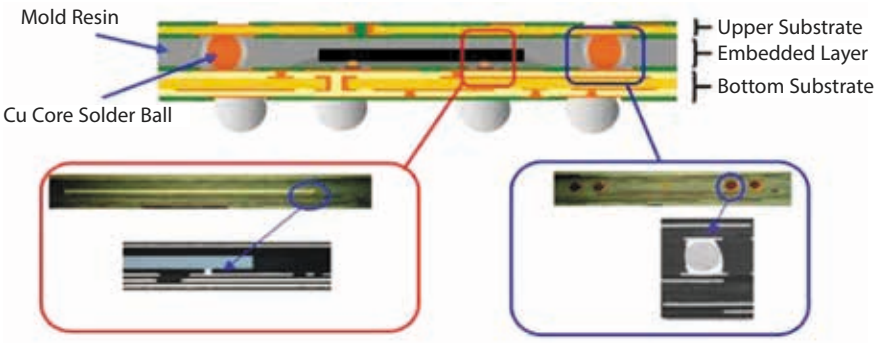
SHINKO has manufactured Lead Frames for almost 50 years and continues to lead the industry in advancing Lead Frame manufacturing technology.

SHINKO's expertise in pre-plated, selective Ag, and roughened plating can help to enable MSL1 level reliable packaging solutions for automotive, industrial and other high-end applications.

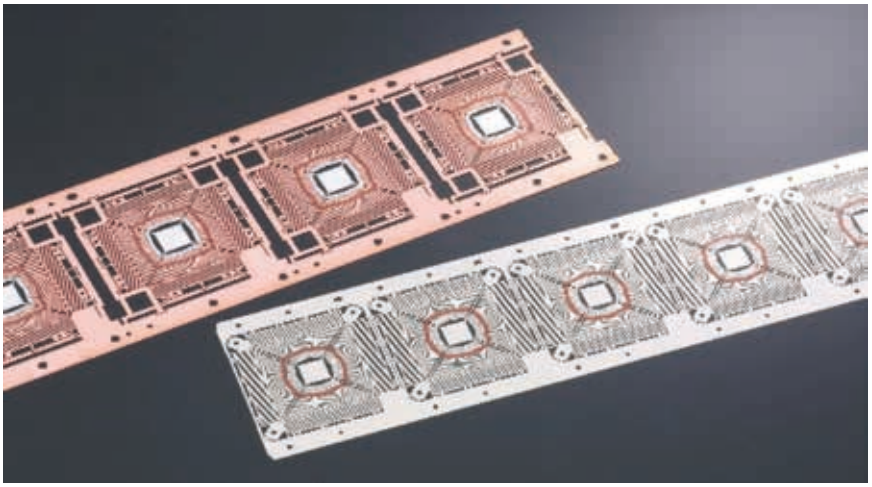
The trend towards strip size expansion continues and SHINKO supports ultra-wide 100x300mm strips and beyond.

SHINKO is also a global leader in QFN (Quad Flat Non-Lead Package) Lead Frame solutions (i.e. ≤ 5mil, wide strip, dual row, advanced QFN type) for applications requiring small footprint, high power and efficient heat dissipation. Super fine pitch (110μm "SFP") stamped Lead Frames from SHINKO also help to reduce Au/Cu wire costs and improve electrical performance by bringing leads closer to the die.

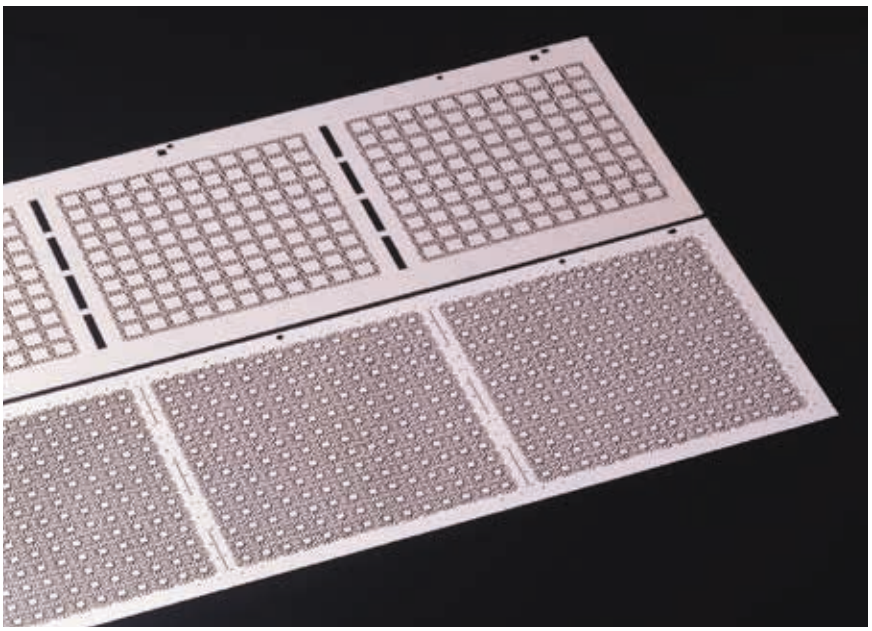
A wide variety of Lead Frames (P-DIP, PLCC, QFP, SOP, etc.) are available uti-



Cross-section of MCeP®.



QFP Lead Frames.

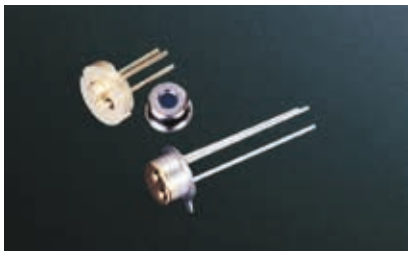


QFP Lead Frames.

lizing open tooling. SHINKO designs and manufactures custom Lead Frames made to order for specific customer needs. From roughened to riveting, SHINKO is a one-stop shop for Lead Frame solutions.

GLASS TO METAL SEALS

SHINKO was founded to recycle light bulbs and the technology for sealing glass to metal enabled it. Today, SHINKO continues to innovate this technology to better manage the Coefficient of Thermal Expansion (CTE) differential of the materials to ensure proper wetting of the molten glass to the metal is done efficiently and reliably during the manufacturing process.



ø5.6mm-type package and TO-18 package.

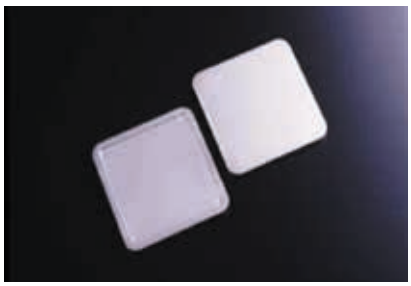
SHINKO's high quality glass-to-metal seal is characterized by its hermeticity and superior electrical characteristics. It is used widely in areas such as laser diodes for optical communications and sensors for in-car use. SHINKO provides both matched and compression type seals.

SHINKO offers not only the industry standard ø5.6mm-type packages for laser diodes for optical pickups, but also caps with stems or window-glass designed to meet the changing needs of customers. Reacting flexibly to diversifying customer needs, SHINKO is able to carry out all the integrated production processes (from product design, mold design, stamping, to plating), utilizing an intensive quality management regime.

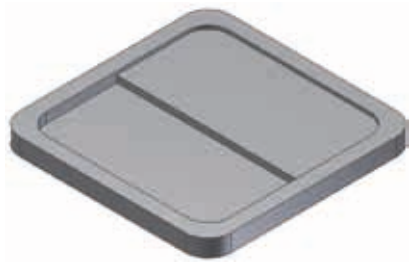
HEAT SPREADERS

As IC's release more and more heat as a result of power consumption, "Thermal Management" is of greater and greater concern. This heating up of the chip can adversely affect the speed and lifetime of the device. The Heat Spreader ensures the safe operation of the electronic circuit by efficiently diffusing the heat released and preventing overheating of the chip. The cavity depth and flatness are key to the efficient thermal dissipation properties of the heat spreader. SHINKO's in-house design simulation, stamping tool production, and surface plating expertise yield an unsurpassed level of quality and usability.

New trends for multi-die packages and die stacking are driving the need for even larger heat spreaders with tiered surfaces. SHINKO's latest capabilities incorporate a high tonnage press for high precision stamping of larger body sizes. The cavity surface can be engineered and stamped with high precision to accommodate new assembly techniques.



A Ni Plated Cu Integrated Heat Spreader for a large format organic laminate substrate.



Heat Spreader for multi-die package.

RESEARCH AND DEVELOPMENT

SHINKO is committed to delivering innovative technologies and high quality products to the marketplace, through continued focus in R&D. In addition, SHINKO continuously seeks to expand into new markets and enhance core competencies to the meet the dynamic needs of customers. Fine trace line and space width, organic interposers and optical waveguides are just a few technologies that SHINKO R&D is working on to lead the next generation device interconnection. ◆

For more information about SHINKO please contact Rick MacDonald at 408-232-0482 or visit the SHINKO website at www.shinko.co.jp.

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Thermal Test Chips: Versatile Characterization Tool

Bernie Siegal, Thermal Engineering Associates, Inc.
Tom Tarter, Package Science Services LLC
Phil Marcoux, PPM Associates
(The authors are part of the BPT Semiconductor Group)

THERMAL TEST CHIPS (TTC) ARE semiconductor devices that contain one or more well-defined heat generating elements and one or more temperature sensing elements. The heat generating element can be as simple as a resistor or as complex as a large area Bipolar Junction Transistor (BJT) or Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The resistor is the common choice because of its simplicity in use but the transistor is best suited for very high total heat generation and for very high heat flux density generation. The temperature sensing element can be a resistor with a well-defined resistance-temperature relationship [like a thermistor or RTD (Resistive Temperature-dependent Device)] or a semiconductor junction also having a well-defined Forward Voltage (VF) – Junction Temperature (TJ) relationship.

Thermal Test Chip Types

There are two different types of TTC:

Application Specific Test Chips – Designed to mimic complex heat generation topologies such as those found in multi-core processors, stacked chip assemblies (2.5D and 3D), system-on-a-chip, and power management and control designs, these thermal test chips are made to match a specific design. They are usually designed by the manufacturer of the corresponding application chip as a tool to help their customers get started on thermal design efforts well before the application chip design and fabrication is done. While not all application chip manufacturers produce such chips, those manufacturers that do often limit the availability of these chips making it difficult to use them for other than their intended product development application.

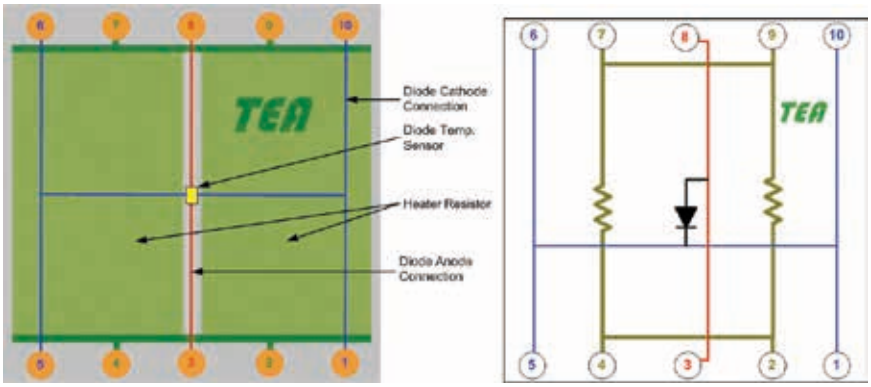

Figure 1. TTC-1001 1mm x 1mm Unit Cell.

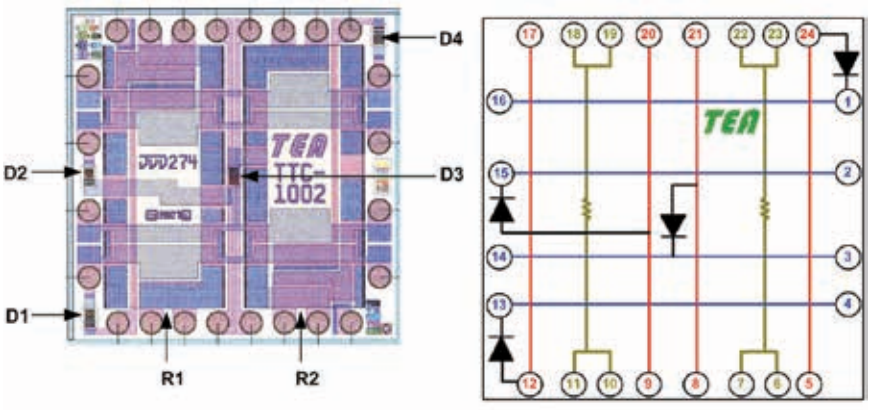

Figure 2. TTC-1002 2.54mm x 2.54mm Unit Cell.

General Purpose Test Chips – Like their application specific counterpart, general purpose chips allow engineers to model, measure, and modify silicon design early in the process. These chips have a standardized design in order to accommodate a wide variety of applications quickly and cost effectively. Yet, customization of the thermal profile and package is still possible. The TTC also has application outside of just package thermal characterization. This article will focus on the general purpose TTC.

The key requirements for standardized thermal test chips are:

- Maximum possible heating area relative to chip size
- Near uniform temperature profile within heating area
- Low temperature coefficient for heating source
- Simple-to-use temperature sensor(s)
- Multiple temperature sensors for temperature profiling across chip surface
- Kelvin Connections (4-wire connections) for improved measurement accuracy

- Chip size that closely approximates the chip being simulated
- Available in both wire bond and flip chip form

Thermal Test Chip Design

Two commercially-available TTC versions that meet the key requirements are the TTC-1001 and the TTC-1002. The former is based on a Unit Cell size of 1mm x 1mm and the latter is 2.54mm x 2.54mm. The chip layout and electrical schematic for each Unit Cell are shown in Figure 1 and Figure 2, respectively. The smaller Unit Cell has a single diode temperature sensor and a single resistor for heating purposes. The larger Unit Cell has four diode temperature sensors and two individual resistors.

The uniqueness of these Unit Cell designs is that the cells can easily be arrayed to form chips that can approximately match any size application semiconductor chip, up to roughly 100mm x 100mm. Figure 3 shows a 4 x 4 array of the smaller cell and a 2 x 3 array of the larger cell. For Flip Chip applications, the individual cells are electrically isolated from each other so the package traces can be used to configure the cell connections to match specific heating patterns that occur in an application chip. For Wire Bond applications, the cells are interconnected on the chip with metal traces that cross saw lanes, requiring only wire bonding to peripheral pads for access to resistors and diodes in a predetermined configuration – series connection of resistors in an array column and diodes in a X-Y matrix.

Package Thermal Characterization

The traditional purpose of TTCs has been, and continues to be, the thermal characterization of single and multi-chip packages. For general package development, TTCs of different size are used to establish a package's power dissipation versus chip-size capabilities. In the case of packaging for a given application chip size, a TTC of approximately the same size is often used for product thermal characterization in the actual application chip package.

When dealing with wire bond packages, such as –

- Single In-line Package (SIP),
- Dual In-line Package (DIP),
- Quad Flat Package (QFP),
- Quad-Flat No-leads (QFN),
- Dual-Flat No-leads (DFN),

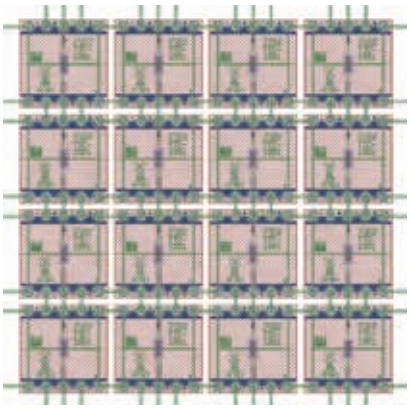

Figure 3A. TTC-1001 (1mm square Unit Cell) 4 x 4 Array.

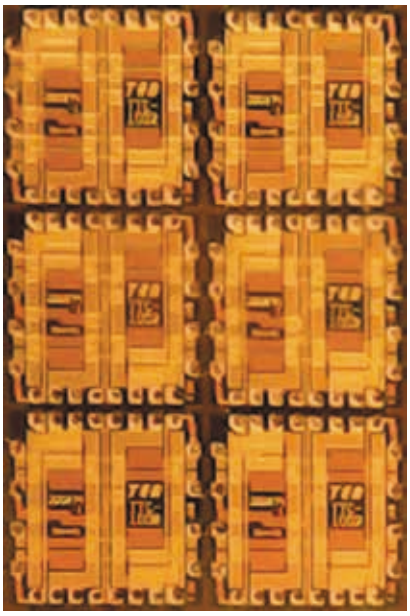

Figure 3B. TTC-1002 (2.5mm square Unit Cell) 2 x 3 Array.

- Wire Bond Ball Grid Array (WB BGA)

– the wire bond version of the TTC is the obvious choice because connection only needs to be made to the chip's peripheral pads. The TTC can also be supplied with backside surface finish and metallization to match that of the application chips to be used in the package, so the die attachment process remains the same as that for the application chips.

There are two approaches to using the Flip Chip TTC for characterization of Ball Grid Array (BGA) and Land Grid Array (LGA) packages. Either the package substrate design has to be modified to accept the TTC or a Re-Distribution Layer (RDL) has to be fabricated on the TTC wafer to match the substrate pads before the metal bumps are applied. The latter approach keeps the package design intact and, therefore, the measured package thermal performance more closely approximates the results possible when used with an application chip.

Package thermal characterization can also include the performance of Die Attachment Material (DAM). In wire-bond packages, the DAM is used to physically mount the backside of the chip to the package. Flip Chip packages that have a metal lid also have thermal interface material between the backside of the chip and the bottom side of the lid – typically referred at TIM_1. The TIM is typically compliant material that is used for transferring heat generated in the chip to the lid while minimizing temperature-induced mechanical stresses on the chip. Both the DAM and TIM are important to the overall package thermal design.

Thermal Management Design Characterization

Development of thermal management designs for specific applications is usually started with thermal simulation software. The model design requires many assumptions, such as material properties, interface thermal resistances, heat flow paths, etc. Once the simulation is completed, the model's assumptions have to be tested against actual measurements and adjusted to refine the model. Use of the TTC's heat generation and temperature sensing capabilities facilitates the model refinement and validation.

TTCs can be used for validation of both Multi-Chip Modules (MCM) and Application Printed Circuit Assemblies APCA. In the former, if each TTC in a module is connected in a manner for individual power control and temperature sensing, the module can be characterized for a wide variety of different power conditions so that an accurate predication of individual junction temperatures is possible for a large number of power combinations. The same can be done in the latter case when there are many different heat sources on the APCA, especially when one or more heat sources share a common heat sink and/or a single air flow sources.

Thermal Interface Material Measurement

There are two kinds of Thermal Interface Material (TIM) measurements. One measures the bulk thermal conductivity ($k\theta$) and the other determines the thermal

resistance (Θ) in an application-oriented configuration. The former is usually standards-based (like ASME ASTM D5470), while the latter includes the interface resistance between the TIM and measurement reference surfaces.

A good way to accomplish the latter at relatively low cost is with a TTC mounted directly to a measurement board, as shown in Figure 4A. Adding the rest of the fixturing – copper heat spreader block with imbedded temperature sensor, heat sink with spring pressure apparatus, and metal backing plate – results in the complete mechanical assembly shown in Figure 4B. The measurement setup thermal portion is shown in Figure 5; the heating power supply and temperature sensor measurement equipment are not shown.

Thermal Interface Material Reliability Characterization

The same assembly shown in Figure 4 can be used for TIM reliability studies. The entire assembly can be subjected to temperatures up to 120ºC to study the effect of high temperature bake and temperature cycling as a function of time. Consistency or changes in measured thermal resistance at specific time or cycle intervals will indicate TIM reliability. The same apparatus can be used for power cycling, in which the power to the TTC

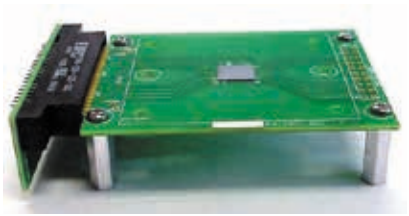

Figure 4A. TTV-4101 (TTC mounted on TTB) with mating edge connector.

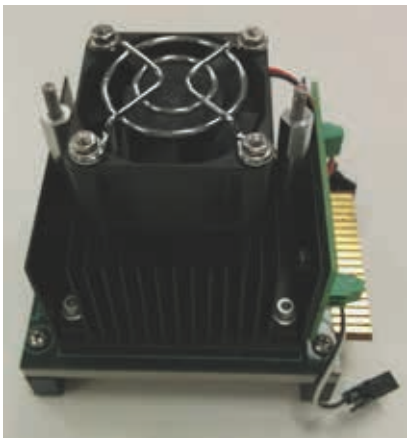

Figure 4B. TTV-4101 Assembly.

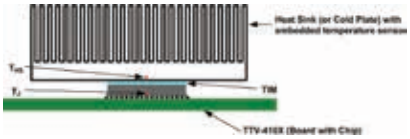

Figure 5. TIM Measurement Setup.

is adjusted to reach a specific junction temperature and then turned on and off for a large number of cycles. Monitoring the junction temperature on a cycle-by-cycle basis will reveal TIM reliability as a function of the number of cycles.

Hot Spot Thermal Management

Very few application chips have uniform temperature distribution from a spatial or time consideration. Flip Chip TTCs, with access to individual heating resistors and temperature sensors can generate power maps as shown in Figure 6A and Figure 6B.

The approximately 5.3mm square chip shown in Figure 6A contains a 5 x 5 array of 1mm square Unit Cells that contains 25 isolated heating elements (the light blue area in each cell) and 25 diode temperature sensors.(the red dot in each cell). This area provides the latitude of powering all the heating elements to 3W each (i.e., 75W total) or powering each element differently to produce a power map to mimic a real application chip's power topography. The large number of diode temperature sensors produce an accurate representation of the temperature distribution for either uniform or hot spot heating.

Similarly, Figure 6B shows a 7.2mm square TTC-1002 3X3 array chip that has 18 distinct isolated heating elements that can handle up to 108W for uniform power or some lower power on most elements but higher power on specific elements to generate a specific power map. As there are four diode temperature sensors per cell (the red dots), the 64 sensor can be used to monitor a single cell temperature or all the sensors used to produce a temperature topography map of the entire chip.

Considering Figures 6A and 6B, the same concept is applicable to chips of much larger sizes. For example, a chip of approximately 26.84mm x 26.84 size made up of a 25 x 25 array of 1mm square Unit Cells would have 400 heating elements and 400 diode temperature sensors. Total power dissipation capability would be over 1KW if operated in a well managed thermal environment.

Temperature Controlled Stage

One potential TTC application area not fully explored is the use of the chip as a temperature-controlled stage. The ability to measure the chip temperature, in one or more regions, to drive a feedback circuit to apply power to the heating resistors, provides an opportunity to precisely control the chip backside temperature. Such an application would possibly find service in the field of temperature-dependent chemical analysis material characterization.

Conclusion

Thermal Test Chips offer a versatile and convenient method for estimating the thermal properties and performance of complex ICs and stacked IC assemblies. The TTC chip size options allow the design engineer the ability to estimate course or fine thermal properties. The availability of wire bond or flip chip versions allow the TTC to be used in a wide variety of packages, configurations, and applications. ◆

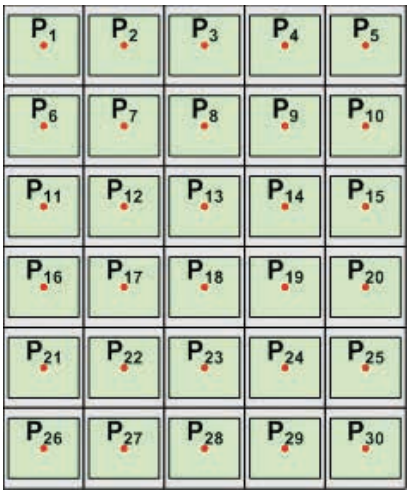

Figure 6A. TTC-1001 5 x 5 Array Power Mapping Layout.

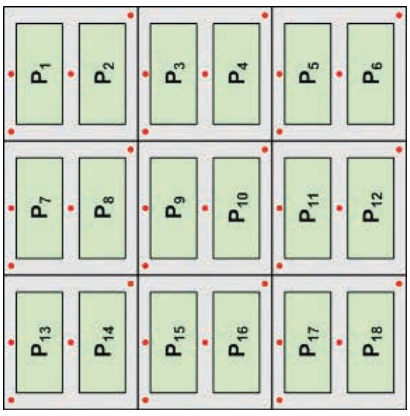

Figure 6B. TTC-1002 3 x 3 Array Power Mapping.

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Silicon-based Flexible Electronics Enabled by HANAflex

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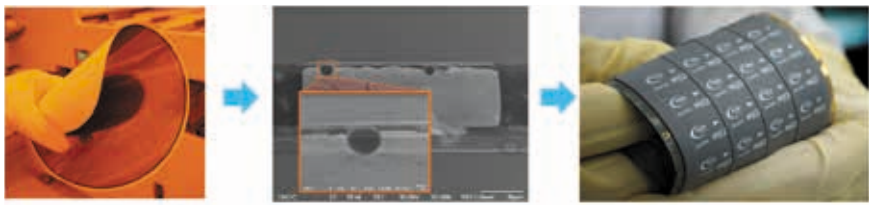


Overview of HANAflex Process.

Advent of Flexible Electronics

At MWC 2015, Samsung introduced the Galaxy S6 edge, where the screen is curved around the longer sides to offer "immersive viewing experience" by continuing the interface around its edges. Although the previous curved smartphones were experimental, Galaxy S6 edge has received near-universal praise for its sleek design. Leading-edge consumer electronics (CE) companies have been perfecting their manufacturing technologies for flexible electronics and in the near future we will be able to witness commercial foldable tablets.

As consumers want devices to be more conformal and flexible to their usage applications, more electronic parts, especially displays are necessary to be flexible. Printed organic integrated circuits (IC) have been around and been intensively researched as enabling technology for truly flexible electronics. However, due to their poor electrical property, low reliability and high cost per transistor, printed organic devices are proven to be unsuitable for computational purposes. Although printed organic ICs may find their sweet spot at large-area sensor applications, the applications such as memory, RF connectivity, MCU, high resolution image sensor and display driver ICs (DDI) still require the analog amplification efficiencies, the digital computational power and the transistor density of silicon(Si)-based IC technology.

HANAflex

With flexible electronics becoming a next-big-thing-type-trend, HANA Micron has been developing HANAflex, the world's first mass-production-ready flexible packaging solution for Si-based IC chips. HANAflex is a promising IC packaging technology for smartphones, tablets, wearables and even medical devices. The technology enables companies to preserve and extend IC chips they have spent years developing. HANAflex negates the need for specialized front-end fabrication technologies customized for flexible electronics and avoids costly and complex approaches like Silicon-On-Insulator (SOI) or Si transfer on foils. HANAflex can be offered as an additional package option, besides QFN, WLCSP and BGA, for existing products.

Wafer Level Roll Transfer Equipment.

Flexible Ultra-Thin Si Wafer

Si is generally considered as rigid and brittle material. However, the flexibility in Si can be achieved by reducing the thickness of Si wafer down to less than 100μm. In stacked-die memory products, normally the back side of Si wafers are ground and routinely they are thinned down to 50μm. 50μm-thick Si wafers are very flexible, and theoretically it can withstand the strain from the bending radius of 4mm. While there exist various potential enabling technologies for generating ultra-thin Si wafers, the conventional back-grinding method seems to be the most viable and the only mass-production-ready solution at this moment. A series of innovative manufacturing process is developed to handle and package ultra-thin Si dies while keeping their conformity. Using HANAflex technology, the mass production of the world's first flexible x-ray image sensors with 50μm-thick Si dies has started in 2Q 2015.

Wafer Level Roll Transfer

Handling of ultra-thin Si wafers is extremely difficult. Even very small impact can easily damage the wafer. In order to protect and handle the ultra-thin wafers, a patented wafer-level-roll-transfer system has been newly designed. With the new roll-transfer system, Si wafers are laminated with stretchable adhesive films, while retaining their flexibility. This lamination strategy has beneficial influences not only on handling purpose itself but also on minimizing the possible change in electric characteristics of circuits fabricated on the wafers. The electric characteristics of both active and passive devices on wafers are affected by mechanical stress level. When a film having a crying shape or a smile shape, there exists the neutral plane in the cross section of the film along which there are no longitudinal stresses or strains. By adjusting the thickness, the thermal expansion coefficient or other mechanical properties of the laminated adhesive film as tuning knobs, the neutral

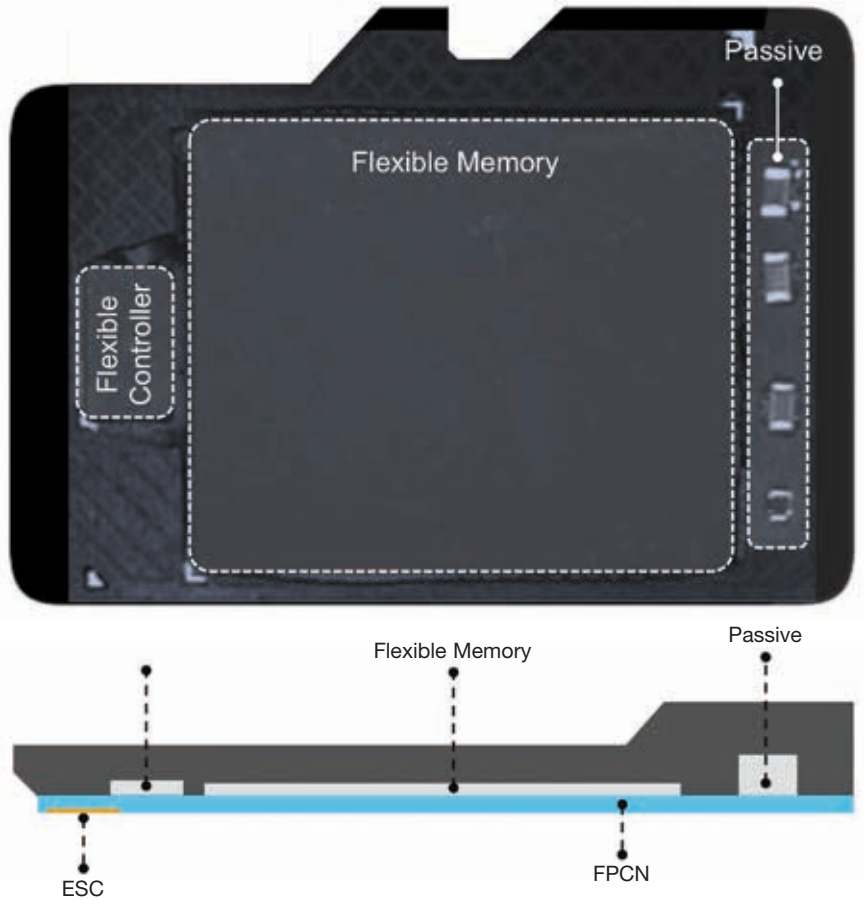
plane can be placed near the thin Si die layer so that the mechanical strains in Si semiconductor layer are minimized.

Interconnect

A sophisticated sawing technique is developed to carefully separate the laminated ultra-thin wafers into individual dies. After the separation process, bumped laminated dies can be stored in tray and directly supplied to customers. Separated dies can also go through further processes where they are attached to flexible printed circuit board (PCB) for fan-out purpose or for System-in-Package (SiP) configuration. Due to various market demands, HANAflex currently offers both gold wire bonding and flip chip bonding as interconnect options. The flip chip bonding option utilizes anisotropic conductive films (ACF), which is commonly used in liquid crystal display (LCD) manufacturing to make the electrical and mechanical connections from the driver electronics to the glass substrates of the LCD (Chip-on-Glass) or to flex substrate (Chip-on-Flex). ACF bonding has the advantages of low temperature process, fewer processing steps without underfill, and the fine pitch capability. Flip chip bonding with 28μm bump pitch has been achieved and has passed a series of process qualification tests. A product with fine bump pitch is scheduled to start high-volume production in 4Q 2015 and will be the world's first case of flexible Si IC ever being adopted to mainstream CE products. Metallurgical flip-chip bonding with solder bumps is currently being developed for applications that do not need large flexibility but require extremely thin form-factor, lower cost and lower contact resistance. After the interconnection stage, flexible molding is applied to provide mechanical protection to flexible dies, surface mounted passive components and substrates, while keeping the thickness of entire package under 0.4mm.

Reliability

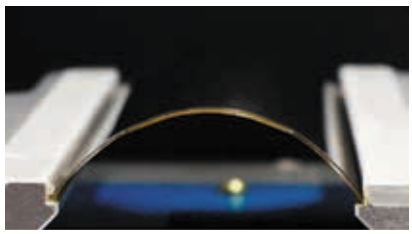
Using the HANAflex technology, a 4GB flexible microSD card which consists of a controller IC, a NAND flash and 4 capacitors has been developed. The microSD storages are fully functional at bending radius of 10mm and have passed environmental reliability tests such as high temperature storage test, temperature cycle test, moisture sensitivity level test, highly accelerated stress test (HAST) and temperature humidity storage test. Bending fatigue test has shown that the SiP can survive over 25,000 cycles of bending at room temperature and at high temperature of 125°C it survives over 7,000 cycles of bending. The highly reliable SiP package is made possible by innovative material engineering and clever layer design. HANA Micron has utilized its simulation capability as a way to analyze the mechanical characteristics of the flexible electronics structure. The outcomes help us optimize the film configuration so that the minimum bending radius has been ensured, while minimizing the possibility of resulting any harms to the package.



4GB Flexible microSD Card.

Author

Dr. Kim is currently the Vice Director of the R&D Center at HANA Micron. Before joining HANA Micron, he developed 14nm FinFET SOC logic technology, 20nm Gate-Last High-K Metal-Gate technology and 28nm Gate-First High-K Metal-Gate technology at Samsung Electronics. He has multiple patents and holds the Ph.D. degree in Electrical Engineering from Stanford University.



Bending Fatigue Test.

About HANA Micron

HANA Micron provides a "turnkey-key solution" for semiconductor packaging and test manufacturing services. Over 15 years, HANA Micron has successfully served key customers including Samsung, SK Hynix, and leading IDM (Integrated Device Manufacturer) and fabless companies. As today's market evolves toward mobile devices, HANA Micron have been focused on advanced packaging technologies such as MMC, MCP, LGA, Flip-chip and WLP as well as providing comprehensive test services on RF, SOC, PMIC, Analog and Logic chips.

Please contact HANA Micron at HANAflex@hanamicron.com for further information. For media inquiries, contact James Cho at pr@hanamicron.com. ◆

PacTech - Packaging Technologies
is a worldwide leader in both Wafer Level Bumping & Packaging Services and in Advanced Packaging Equipment Manufacturing.

Prime Manufacturer of Leading-edge Technology Equipment & Processes for the Advanced Packaging Industry

ALMOST 40 KILOMETERS NORTHwest of Germany's capital, Berlin, is the city of Nauen where PacTech has its headquarters. Founded as a spin-off of the federal scientific Fraunhofer IZM in 1995, the company consists of two business units:

1. Manufacturer of advanced wafer level packaging and wafer bumping production equipment.

2. Provider of high-quality, subcontract manufacturing services.

With subsidiaries in California and Malaysia, the corporation supplies its outstanding solutions in these relevant business regions.

PacTech has continually grown, and the company is to date the biggest high-tech employer in the region with a staff of some 350 people.

In Europe, the U.S. and Malaysia, the full enterprise portfolio of different manufacturing services is available, as well as all of the backend solutions. The advanced equipment manufacturing operations is located at the German HQ. All machinery, sold originates from the headquarters and carries the well-known brand: "Made in Germany"!

The company's main target area is now the Asian markets, which consume the lion's share of products and services.

With more than 20 years of experience, PacTech is a prime manufacturer of leading-edge technology equipment and processes for the advanced packaging industry. PacTech designs, manufactures and supports solder jetting equipment, wafer-level solder ball transfer systems, wafer-level solder rework equipment, laser assisted flip-chip bonders and automatic plating tools for high volume electro-less Ni/Au and Ni/Pd/Au Under Bump Metallurgy (UBM) and Over Pad Metallurgy (OPM) through its global sales network.

In its worldwide sales and application centers PacTech offers demonstration capabilities, including assembly of samples and prototyping under ISO certified production conditions. Moreover, PacTech has a unique dual business model in which it offers its customers with new chip designs or initial low volume requirements the option to use in the initial phase PacTech's demo centers for services. After qualification of the product the customer has the option of further cost reduction by utilizing PacTech's full turnkey solution: Equipment, Process and Technology. This reduces the cost of customers new product introductions and at the same time gives the customer the option to qualify and intensively study the technology, and understand the cost of ownership. Together with its partner and main shareholder NAGASE, PacTech is also developing embedding technologies for wafer and substrate level CSP technologies. The solder ball jetting equipment addresses markets like Hard Disk Drive, Camera Module, Sensors and Stacked TSV chip packages. The electro-less plating line addresses applications in power MOSFET devices for clip attach, contactless RFID devices, high reliability power devices, and for Wire Bonding applications using Ni/Au, Ni/Pd respectively, including Ni/Pd/Au for Over Pad Metallization, and many other applications. Ni/Pd Metallization is qualified for volume production of low cost Cu Wire Bonding over active pad. The new Ultra SB² tool is addressing all wafer and substrate-related solder ball applications for high volume mass production. PacTech has leading edge technology for Solder Ball Transfer, Minimum Solder Ball diameter is 30 μm. For the electro-less Plating Tool, PacTech is the worldwide leader with more than 20 Automatic Tools installed worldwide.

Since its inception, PacTech has received more than 110 patents for products developed in areas relating to wafer bumping, flip-chip and chip-scale packaging, and laser-bonding technology.

Also PacTech is providing all chemicals for wet Chemical Pad Protection and Pad Metallization as part of a turnkey solution for electro-less Wafer Bumping. Additional analytical services and support to customers is available.

It is PacTech's mission to provide the highest level of innovative technology solutions with an unparalleled degree of customer service orientation, corporate integrity and attention to its clients' individual technology demands.

More information is available at the PacTech website at www.pactech.de. ◆

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Wafer Backside Metallization
- Wafer Thinning
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- TiNiAg & TiNiAu Evaporation

Backend & Die Sort
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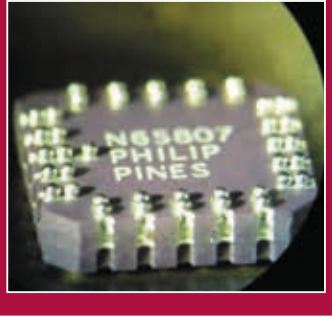

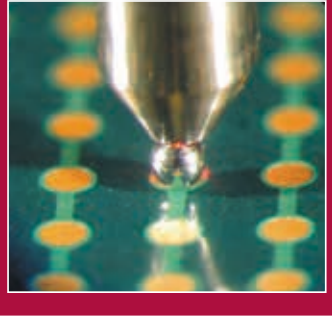

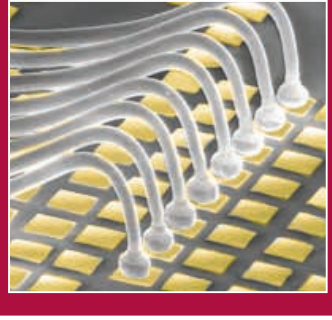

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Enhancing Reliability of Fine-Pitch Flip Chip Devices

Matthew Hayward
Henkel Electronic Materials, LLC

WITH UNYIELDING CONSUMER demand for higher functioning products in ever-smaller footprints, the electronics packaging industry is witnessing an accelerated shift from traditional wire-bonded devices to flip chip technology. Flip chips have many advantages including the ability to incorporate higher I/O counts, facilitate package integration and allow for tighter bump pitches. Increasingly found in consumer, mobile/handheld, high power computing, as well as Internet of Things (IOT) applications, flip chips offer broad appeal because of their compact form and high function. In addition to flip chip proliferation in general, there has also been significant growth in copper pillar flip chip technology, which is a key enabler of finer bumps and tighter pitches.

The decreasing bump pitches, gaps and widths inherent with copper pillar technology have made robust flip chip device protection more challenging than ever before. Most packaging specialists prefer the use of capillary underfill systems, but the higher density dimensions of emerging flip chip architectures place new demands on these materials to deliver complete coverage for robust interconnect protection and long-term device reliability. Alternatives to capillary underfill processes – non-conductive pastes with thermal compression bonding, for example – are currently recommended for flip chips with bump pitches below 80 μm, gaps less than 35 μm and bump widths less than 40 μm. But, for everything above these dimensions, capillary underfills are still the materials of choice.

Designing a high-performance capillary underfill system capable of providing all of the flip chip processability benefits required, while delivering on the increasingly demanding performance needs is no small feat. Improving on its well-known LOCTITE ECCOBOND UF 8830 material, Henkel has developed a completely new underfill system designed for emerging copper pillar flip chip designs. The new material, LOCTITE ECCOBOND UF 8830S, is a fast flow material with a brand new resin system and filler package formulated to accommodate the challenging dimensions of today's flip chip designs.

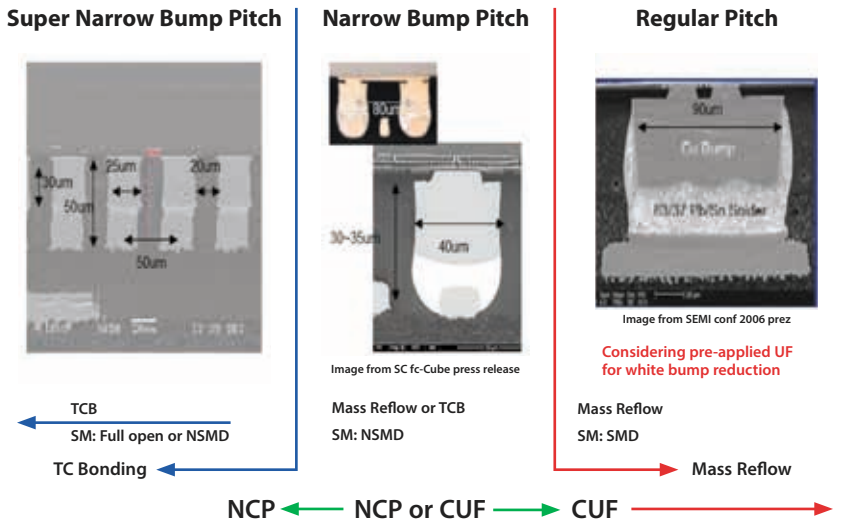
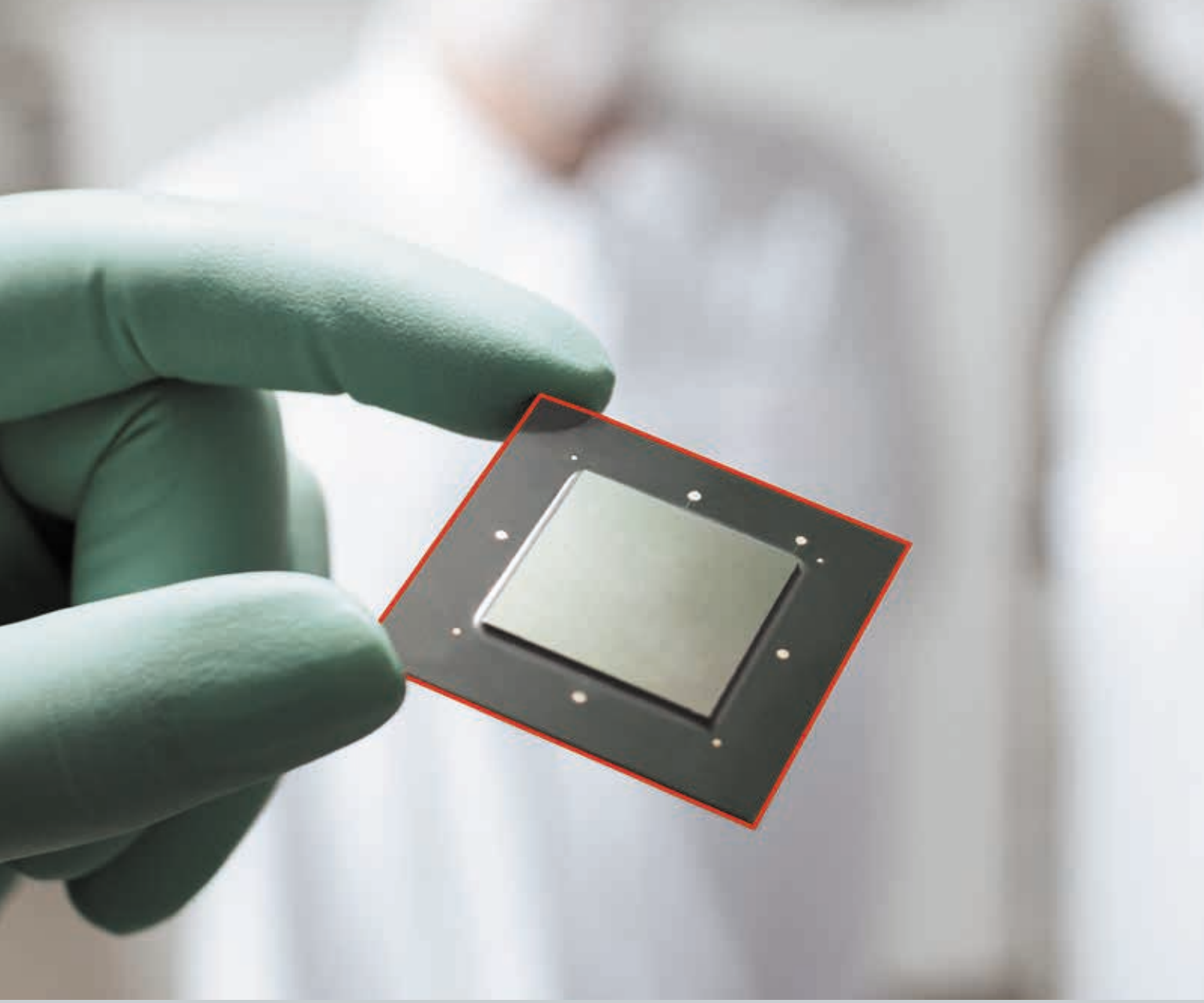


Figure 1. When to use NCP or CUF.

As compared to one of the more popular Japanese underfill materials, LOCTITE ECCOBOND UF 8830S delivers better performance in several areas. The Henkel underfill system offers users a much longer work life, with minimal viscosity increase after 72 hours. This is in comparison to other materials that ranged from a 45% to a 108% increase in viscosity during the same time period. In terms of reliability, LOCTITE ECCOBOND UF 8830S also outperforms other package- level underfill materials. With a higher, more stable glass transition temperature (Tg), the Henkel material provides a higher reliability option. When tested against competitive systems, LOCTITE ECCOBOND UF 8830S maintained very stable Tg levels even after exposure to high temperature for extended periods of time. Competitive materials, however, have wide swings in Tg as temperature exposure increases, leading to instability and potential device warpage.

As package dimensions decrease, the keep out zone – or footprint of the package and surrounding material – becomes increasingly important. Here, too, LOCTITE ECCOBOND UF 8830S outperforms other underfill products. With a shorter dispensing tongue and less resin bleed out than competitive underfills, LOCTITE ECCOBOND UF 8830S

continued on page 28



The smaller the device - the more solutions

No matter where you are or what your process requires, you can count on Henkel‘s expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel‘s world-class global team ensures your success and guarantees a low-risk partnership proposition.

Henkel Excellence is our Passion

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gives manufacturers little concern about material moving beyond the defined area. Likewise, the integrity of the material is superb, with no filler/resin separation whatsoever, which is in stark contrast to other materials where x-ray analysis very clearly shows areas where resin-only protection is observed (see figure 2). This can lead to differing coefficient of thermal expansion (CTE) rates, which can create high stress areas and potential failures.

Priced competitively, LOCTITE ECCOBOND UF 8830S offers packaging specialists an exceptional underfill material with notable gains over competitive products. And, Henkel isn't stopping here; the development of next generation of capillary underfill materials for ultra-fine-pitch flip chips is already underway. The ambitious Henkel underfill technology roadmap, in combination with a well-trained global team to facilitate world-class support and process integration, provides customers with a solid materials partner to progress flip chip technology well into the future.

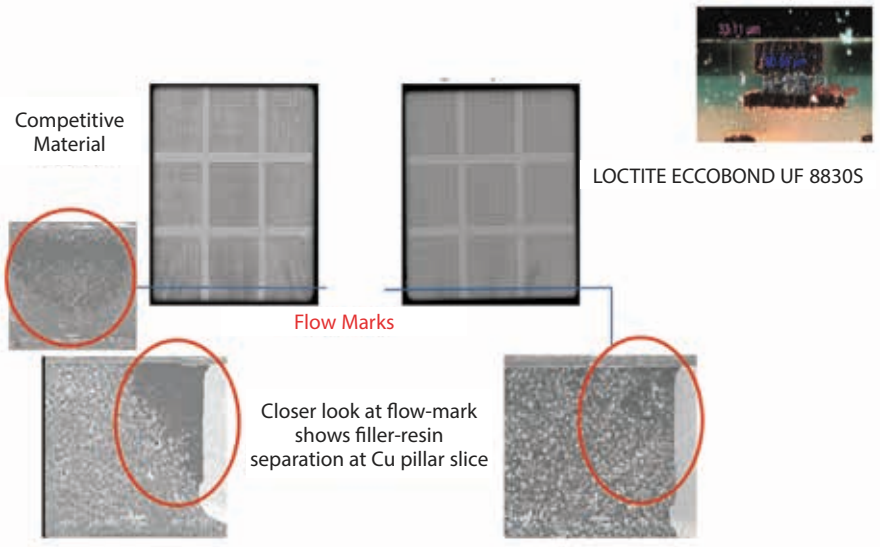

Figure 2. Flow Mark (15 x 15mm x 30µm gap).

For more information, visit www.henkel.com/electronics or call +1-714-368-8000. ◆

OPINION

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visions need to be turned into bite-sized action items for sub-markets such as environmental sensors, gas and optical sensors, biosensors for unobtrusive health sensing, ultra-high-volume low-cost sensors and electronics — made possible by roll to roll printing capabilities on a mass scale not yet seen and other enabling technologies.

MEMS Industry Group in conjunction with MEPCOM (the organization that runs MEPTEC) plans to take a deeper dive into the mechanisms that will spawn the trillion sensors required to help us attain Abundance during TSensors Summit, Dec 9-10, 2015 in Orlando Florida. More than 30 leading technology experts from around the world will begin to put the pieces together of the roadmap that will lead us to TSensors. Why not join us on this exciting journey to a trillion sensors and put Moore's Law and More than Moore into action for Even More. ◆

1 2014 vision from Foundation for Economic Trends http://www.huffingtonpost.com/jeremy-rifkin/obamas-climate-change-plan_b_5427656.html)

2 http://www.zdnet.com/article/internet-of-things-market-to-hit-7-1-trillion-by-2020-idc/ and https://www.visiongain.com/Report/1429/Mobile-Health-%28mHealth%29-Market-Forecast-2015-2020

3 https://datafloq.com/read/the-great-sensor-era-brontobytes-will-change-socie/211

4 http://www.slideshare.net/vangeest/exponential-organizations-h

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IWLPC Conference: October 13–14 IWLPC Exhibits: October 13–14 Tutorials: October 15

EVENT SCHEDULE

Tuesday, October 13 – Wednesday, October 14

Exhibition, Panel Discussion and Technical Presentations on 3D, WLP and MEMS

Thursday, October 15

Professional Tutorials

T1: Introduction to Fan-Out Wafer-Level Packaging

T2: 3D IC Integration and 3D IC Packaging

T3: Adhesion Science & Practice with an Emphasis on Temporary Bonding of Electronics (Wafers, Displays, Devices)

T4: Wafer-Level Packaging for MEMS and Microsystems Technologies for Size and Cost Reductions

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CONFERENCE SPECIAL EVENTS

Tuesday, October 13

Keynote Breakfast Address
High Density Fan-Out: Evolution or Revolution
Rama Alapati, *GLOBALFOUNDRIES*

Panel Discussion
Fan-Out WLP Panel Processing: Will it happen and What will it be?
Moderator: Jan Vardaman, *TechSearch International*

Exhibitor Reception
Join us in the Bayshore Ballroom for the Exhibitor Reception where over 60 exhibitors will showcase the latest products and technologies offered by leading companies in the semiconductor packaging industry. This evening reception offers attendees numerous opportunities for networking and discussion with colleagues.

Wednesday, October 14

Keynote Address
2.5D/3D IC – Examining Low Cost Alternatives
Sitaram Arkalgud, Ph.D., *Invensas Corporation*

Panel Discussion
Interposers, 3D TSVs and Alternatives: What are the Options and Where do They Fit?
Moderator: Françoise von Trapp, *3DInCites*

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For more information about the conference, or exhibit and sponsorship opportunities, contact Tanya Martin at 952-920-7682 or tanya@smta.org. www.iwlpc.com

Moore and More than Moore as a Foundation for Even More

Stephen Whalley
Chief Strategy Officer, MEMS Industry Group

HAVING SPENT 30 PLUS YEARS IN various aspects of the mainstream semiconductor industry, it was certainly an interesting change when I delved into MEMS and sensors a mere five years ago. I was hooked when I saw my first chip photograph of an accelerometer – so much more simple than a multi billion transistor microprocessor – yet none the less a feat of engineering, manufacturing and wonder. And then when you see what an accelerometer, gyro and magnetometer can do buried away in a smart phone; unleashing a vast potential in new applications that were once just destined for military, aerospace, automotive and other industrial applications, it quickly draws you in further.

The excitement about MEMS and sensors continues to grow in me five years on. Unlike the cyclical nature of the semiconductor business driven by the ups and downs of PCs, servers, memories and the general economy, the MEMS and sensor industry has seen steady double digit growth for the past decade. This growth has been fueled by smart phones, ink jet printers, game controllers, automotive and the catch all Internet of Everything. While it's been a great ride so far, the best is yet to come for MEMS and sensors. There does not seem to be a new category of devices launched these days without some form of sensing capability built in. Wearables, personal health devices, environmental sensing, food and agriculture technologies, clean energy sources, drones, autonomous vehicles, smart buildings, smart cities and smart everything essentially means sensing is exploding.

Before I get too carried away with myself though on the opportunities, there are challenges ahead not surprisingly in markets this big. Many of these challenges have been faced and overcome before though in the semiconductor business. Challenges such as all that comes with keeping pace with Moore's Law, standards and best known methods for process repeatability and scaling, advanced packaging and testing, lower power, security, interoperability and monolithic systems on a chip to name just a few. While there are many diverse aspects of these two industries, common challenges certainly exist that would benefit from a sharing of learnings and a coming together of the supply chains where relevant to work on scaling for growth together. "More than Moore" efforts are underway around the world but I am not sure if the Moore and the More than Moore brethren are coming together anymore (if they ever did) or perhaps we have all succumbed to less is more doctrine these days. OK, no more of that! Suffice to say, it might be a small step but MEMS Industry Group and SEMI have been collaborating in this area since the Spring of this year and have a task force in place addressing some of the issues above.

> Multiple visions have emerged for a trillion sensors (TSensors) market, with the largest forecasting 100 trillion sensors by the year 2030

Now, back to the opportunities and the exciting things happening with sensors in a multitude of different markets. Beyond the continued growth in the general consumer electronics and industrial markets that is driving volume today, it's clear there is a vast array of emerging applications that we need to pay attention to, some of which are mentioned above. There is also a rising tide in 3D printing and ultimately large area printing of processors, sensors, radios, power sources and passive components. Add to that sensing capability in smart fibers and we have a textile base that could usher in dramatic new capabilities in our home, transport and work environments. And all this could be a reality in the next few years.

Multiple visions have emerged for a trillion sensors (TSensors) market, with the largest forecasting 100 trillion sensors by 2030[1]. The explosive connectivity growth of "all things" is obviously not just about the hardware however; it's also about the explosion of sensor-driven data, which Datafloq predicts will reach brontobytes in the 2020s. Such volume of data creates unprecedented business opportunities for data generation (sensors), services, analytics and visualization.

The promise of trillions of sensors clearly excites the juices of sensor supply chain executives. There is also something else for all of us to get excited about in this future. In 2012 Bestselling Author Peter Diamandis, founder of XPrize Foundation and Singularity University, co-wrote the book *Abundance – The Future is Better than You Think*. In this book, Diamandis introduced the concept of "Abundance," the utopian vision for a world with no hunger, no pollution, affordable medical care and clean energy for all. Remarkably, claims Diamandis, Abundance is expected to come in just about 20 years, enabled mainly by eight exponential technologies producing goods and services on Earth faster than the global demand. One of those technologies is connected sensors.

Will just identifying the road to massive device units, data and revenue allow us to tackle our greatest humanitarian issues? Clearly not. These high-level

continued on page 28

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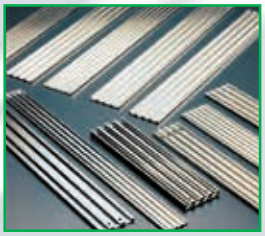
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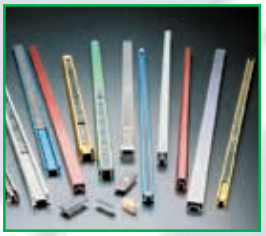
I. C. Tubes and Rails


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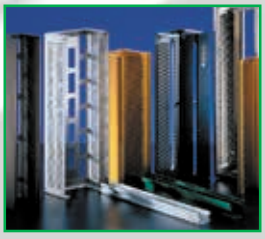
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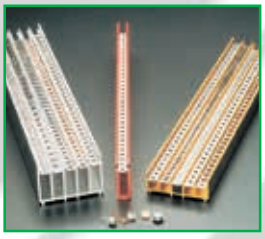
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