MEPTEC Report

SUMMER 2017

A Quarterly Publication of the Microelectronics Packaging & Test Engineering Council

Volume 21, Number 2

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A Tool for Developing New MEMS Sensors
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MEPTEC MEMBER COMPANY PROFILE
Located in Itasca, IL, just outside of Chicago, Kester's center of excellence houses their global manufacturing for many of their products as well as centralized R & D staff and application equipment, technical support labs and product management capabilities.
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ASE GROUP

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Wire Bond	Flip Chip	WLP	2.5D & 3D	Fanout	SiP

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The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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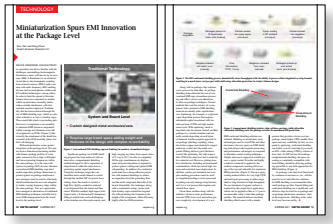
ON THE COVER

Failure analysis is an effective tool for the development of new MEMS sensors products. It can be used to understand the behavior of a part in the given application environment. A life test profile evaluates the effects of the environmental conditions against the design objectives and a developed manufacturing process. Functional testing and non-destructive/destructive analysis provides the lessons learned where immediate inputs to the new product development cycle can reduce development costs and increase the time to market.

Cover Photo Courtesy of SMART Microsystems Ltd.



TSMC PROMOTES DAVE KELLER TO PRESIDENT, TSMC NORTH AMERICA

TSMC has announced the promotion of a veteran executive, Dave Keller to President, TSMC North America. Rick Cassidy remains as Chief Executive Officer, TSMC North America.

As President, Keller is responsible for managing the North America business, which is a wholly owned subsidiary of TSMC and accounted for over 60 percent of TSMC's 2016 sales of $29.4 billion. Cassidy, in his role as CEO, will be strategic in guiding the North America organization on its technical, financial and human resources matters.
www.tsmc.com

MICRON APPOINTS SANJAY MEHROTRA AS PRESIDENT/CEO

Micron Technology, Inc. has appointed Sanjay Mehrotra as President and Chief Executive Officer and a member of the Board of Directors, effective May 8, 2017. Mehrotra succeeds Mark Durcan and joins Micron at a time of increasing opportunity for memory and storage technologies and solutions as the key enablers for the next-generation of computing architectures.

Mehrotra was a co-founder of SanDisk and served as its president and CEO from 2011 to 2016. He drove the growth of the company from a start-up in 1988 to an industry-leading Fortune 500 company with revenues that reached $6.6 billion, and ultimately culminated in a sale for $16 billion to Western Digi-

Xilinx and IBM First to Double Interconnect Performance for Accelerated Cloud Computing with New PCI Express Standard

XILINX HAS ANNOUNCED an achievement in PCI Express® Gen4 capability. Together with IBM, the two companies are first to double interconnect performance between an accelerator and CPU through the use of PCI Express Gen4 compared to the existing widely-deployed PCI Express Gen3 standard. Gen4 doubles the bandwidth between CPUs and accelerators to 16 Gbps per lane, thereby accelerating performance in demanding data center applications such as artificial intelligence and data analytics.

Since the introduction of PCI Express in 2003, Xilinx has been a leader in PCI™ interconnect-based solutions, offering PCI Express compliance across its All Programmable FPGA families. Today IBM and Xilinx have achieved Gen4 interoperability between Xilinx® 16nm UltraScale+™ devices and IBM POWER9 processors, demonstrating the first-ever PCIe Gen4 capability in a programmable device.

"This leadership in PCI Express is another reason that POWER architecture is being deployed in modern data centers," said Bradley McCredie, vice president and fellow at IBM. "IBM is excited to leverage the underlying performance of PCIe Express Gen4 for CAPI 2.0 which eases the programming experience for application developers."

"We believe in open standards," said Ivo Bolsens, CTO at Xilinx. "It's gratifying to see this milestone between our companies that will alleviate significant performance bottlenecks in accelerated computing, particularly for data center computing."

Xilinx is the leading provider of All Programmable semiconductor products, including FPGAs, SoCs, MPSoCs, RFSoCs, and 3D ICs. Xilinx uniquely enables applications that are both software defined and hardware optimized – powering industry advancements in Cloud Computing, 5G Wireless, Embedded Vision, and Industrial IoT.

For more information, visit www.xilinx.com. ◆

CORWIL Technology Invests in Portable Clean Environment for Wafer Sort

TO SATISFY CUSTOMER DEMAND FOR ultra-clean environments for wafer sort, CORWIL Technology (CORWIL) has added a Portable Clean Environment for wafer sort that is good to Class 1000. CORWIL's one-stop solution from wafer sort, die prep, assembly, Package Test and Reliability provides the ability to understand how different pieces of the backend process affect each other in terms of yield.

Joe Foerstel, Vice President of Test for CORWIL said, "Customers have found that wafer sort in a very clean environment improves yield, especially when using certain RF probe technologies or probing devices with sensitive surface structures; particularly for our customers in the communications and medical industries."

"We have seen dramatic improvement of yields at Second Optical when customer's wafers arrive from a cleaner environment, especially when back grind is one of the steps in the process," added Jonny Corrao, CORWIL's Director of Die Prep.

For more information on CORWIL's wafer sort capabilities and the Portable Clean Environment please contact CORWIL 408.618.8700. ◆

Intel Named to DARPA Project Focused on Machine Learning and Artificial Intelligence

INTEL HAS BEEN SELECTED by DARPA to collaborate on the development of a powerful new data-handling and computing platform that will leverage machine learning and other artificial intelligence (AI) techniques.

The notion of Big Data emerges from the observation that 90 percent of the data available today has been created in just the past two years. From devices at the edge to large data centers crunching everything from corporate clouds to future energy technology simulations, the world is awash in data – being stored, indexed and accessed.

DARPA's Microsystems Technology Office created the Hierarchical Identify Verify & Exploit (HIVE) program to develop new technologies to realize 1,000x performance-per-watt gains in the ability to handle graph analytics.

Intel's Data Center Group (DCG), Platform Engineering Group (PEG) and Intel Labs will work as one of the hardware architecture research performers for DARPA HIVE, with a joint research program between Intel and DARPA valued at more than $100 million during a 4½-year effort.

"By mid-2021, the goal of HIVE is to provide a 16-node demonstration platform showcasing 1,000x performance-per-watt improvement over today's best-in-class hardware and software for graph analytics workloads," said Dhiraj Mallick, vice president of the Data Center Group and general manager of the Innovation Pathfinding and Architecture Group at Intel. "Intel's interest and focus in the area may lead to earlier commercial products featuring components of this pathfinding technology much sooner." ◆

ASE Records Purchase of 15.2 Million KwH Green Power in Past 4 Years

ADVANCED SEMICONDUCTOR ENGINEERING, INC. HAS announced that its Taiwan facilities in Kaohsiung and Chung Li, had purchased 4.5 million KwH green power in 2017 from Taiwan Power Company (Taipower), a state-owned electrical power utility company. Since 2014, the company has purchased an accumulated total of 15.2 million KwH (Kilowatt Hours) green power - reducing 8,025 metric tons of carbon emissions into the atmosphere and equivalent to the carbon sequestration from 660,800 trees.

Green power refers to environmentally-friendly energy and energy technologies derived from natural resources that replenish themselves over short periods of time, including the sun, wind, moving water, organic plant and waste material (biomass), and the Earth's heat (geothermal). By purchasing green power, households and businesses commit their green power providers to purchasing the equivalent amount of electricity from accredited renewable energy generators, which generate electricity from sources like wind, solar, water and bioenergy. As part of a national sustainability strategy, the Ministry of Economic Affairs rolled out the Pilot Program for Voluntary Purchase of Green Power in mid-2014. ASE was one of the early volunteers and have gradually increased the amount of green power purchased annually. Taiwan's main renewable energy sources come from solar and wind power. ◆

tal Corporation in 2016. His team pioneered a diversified and comprehensive portfolio of flash storage solutions that included removable products, embedded mobile solutions, client and enterprise solid state drives and innovative enterprise system solutions.
www.micron.com

MST RECEIVES ITAR REGISTRATION

Micro Systems Technologies, Inc., located in Mesa, Arizona, is now qualified to work on projects which are subject to ITAR or EAR regulations. Their offering includes ultra-HDI/microvia flex, rigid-flex or rigid PCBs and LCP based substrates for aerospace & defense applications requiring the highest reliability and performance. The sophisticated solutions are manufactured according to the EN 9100:2009 standard, guaranteeing highly effective processes and 100% traceability.

Micro Systems Technologies, Inc. is part of the MST group consisting of four technology companies that provide innovative components and services for medical technology, aerospace & defense, telecommunication, and other high-reliability/high-performance industries.
www.mst.com

DISCO RECEIVES INTEL'S PREFERRED QUALITY SUPPLIER AWARD

DISCO Corporation has been recognized by Intel as a 2016 Preferred Quality Supplier (PQS) award winner.

The PQS award celebrates exceptional, per-

Intel to Invest US$178 Million to Advance its R&D Innovation in India

REINFORCING ITS COMmitment to advance cutting-edge research and development (R&D) and innovation in India, Intel Corporation has announced it will invest US$178 million to expand its R&D presence and build a new state-of-the-art design house in Bengaluru. The proposed facility will be located at Intel's 44-acre campus on Sarjapur Ring Road (SRR) in Bengaluru, Karnataka.

With approximately 620,000 sq. ft. of space, including lab capacity, the new building with specialized infrastructure will be used for chip design and verification purposes. This additional capacity will help Intel India consolidate its R&D operations to a large extent at the SRR campus.

Designed to be a "smart and green" building, the upcoming facility, SRR4, will be constructed using innovative "One High Technology," with each floor being built on the ground, then lifted and attached to the of the building, and then built from the roof downward. This technology will enable the reduction of scheduled construction time by 30 percent as compared to traditional construction methods. The second such building in India, it will be constructed entirely by local contractors, will be equipped with IoT-based smart features, including smart lights and real-time occupancy management, and will use renewable energy sources like fuel cell-based power.

To meet the growing need for vehicle parking space at its Bengaluru campus, Intel is also building a multilevel car parking (MLCP) facility. The construction material for the MLCP have been locally sourced, with a majority being recycled.

Intel has consistently invested in growing its R&D and innovation presence in India. It has invested in hiring and developing talent, state-of-the-art facilities, and innovation and entrepreneurship programs. Intel India is engaged in cutting-edge engineering work such as chip/system-on-chip design, graphics, software and platform for the cloud, devices and IoT markets involving advanced technology areas such as artificial intelligence, virtual reality and 5G. ◆

Varioptic Acquired by Invenios LLC

Invenios LLC, an advanced technology micro-fabrication foundry specializing in glass structuring, micro glass packaging, and glass bonding, has successfully completed the acquisition of Varioptic.

Varioptic is the pioneer and a world leader in the liquid lens technology which enables variable focus, variable tilt, or variable cylindrical lenses with no moving parts.

Invenios has been working on improving Varioptic's OIS lens (Optical Image Stabilization), with an enhanced, low cost and scalable design. This acquisition will streamline liquid lens development efforts, and enable broader market access with an extended product portfolio.

For more information, visit: www.invenios.com. ◆

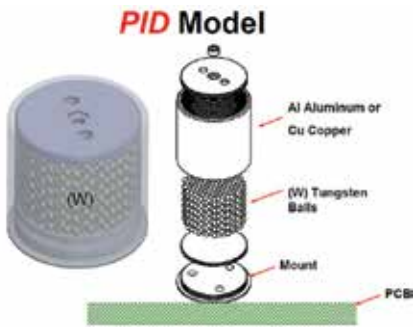
TopLine and NASA to Jointly Present Particle Damping (PID) Paper at PCB West

TOPLINE AND NASA WILL PRESENT a joint paper, titled "Practical Design Considerations for Particle Impact Dampers (PID) to Prevent Random Vibration Failures in Printed Circuit Boards," at the PCB West Conference, Sept 12 – 14, 2017, in Santa Clara, California.

TopLine was recently granted an exclusive worldwide license by NASA to manufacture "Particle Damping for Vibration Mitigation for Circuit Cards."

Presenters will be Ron Hunt from the NASA Marshall Space Flight Center, and Martin Hart, President of TopLine Corporation. Ron Hunt is the inventor of this new PID technology that attenuates destructive vibratory forces to reduce damage in PCBAs. This innovation extends the life of the assembly, including IC packages that operate under harsh environmental conditions including thermal stress and vibration.

The presentation will explain a novel way to attenuate vibrations in PCBs by using a simple component known as a PID (Particle Impact Damper) that is attached directly to the PC board. The PID itself is filled with Tungsten spheres that deflect the board in the opposite direction while the board is vibrating. The PID helps keep the board remain stable

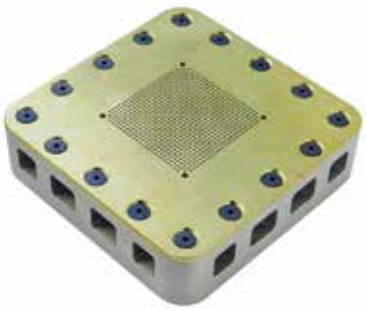


during massive random vibration. NASA made a technology transfer of the Patent US9521753 B1 to TopLine in September 2016.

PIDs are commercially-available COTS components. Mounting methods include surface mount soldering, snap-in through-hole, screw mounting, and epoxy mounting with permanent adhesives. Engineering development kits are currently under development. To learn more, visit http://www.topline.tv/vibration_damping.html, and visit the TopLine booth #210 at PCB West.

For more information, contact TopLine Corporation, Tel (800) 776-9888; Email: sales@TopLine.tv ◆

TopLine Offers Column Planarizing Tool for Trimming CCGA Solder Columns



TOPLINE ANNOUNCES AN UPGRADED Column Planarizing Tool for precise trimming of CCGA Solder Columns to ensure planarity across the CCGA with 1 mil accuracy. Planarity ensures robust, reliable and uniform connections when the CCGA component is mounted to its footprint on an electronic assembly. TopLine CCGA Column Grid Array IC packages are made with high temperature solder columns for Surface Mount (SMT) soldering on Printed Circuit Boards. CCGA packages provide more compliancy than BGA solder balls to absorb stress caused by CTE mismatch and increase solder joint reliability under harsh operating conditions.

The TopLine Column Planarizing Tool securely locks the CCGA in place while columns are safely planarized.

Trimming or lapping is required for CCGA packages with Pb90/Sn10 and Pb80/Sn20 copper-wrapped solder columns. Utilizing the TopLine Column Planarizing Tool is a demonstrated best practice for planarizing solder columns to bring the CCGA into coplanarity.

For more information, visit http://www.topline.tv/CCGA_Planar.html. ◆

sistent performance and the continuous pursuit of excellence. Suppliers have exceeded expectations and performance goals in quality, cost, availability, technology, customer service, labor and ethics systems, and environmental sustainability.

The PQS award is part of Intel's SCQI program, which encourages Intel's key suppliers to strive for best-in-class levels of excellence and continuous improvement.
www.intel.com/go/quality

TOSHIBA MATERIALS AND KYOCERA TO COLLABORATE

Toshiba Materials Co., Ltd. and **Kyocera Corp.** have announced that the two companies have agreed to start full-scale collaboration on development and production of nitride ceramic components.

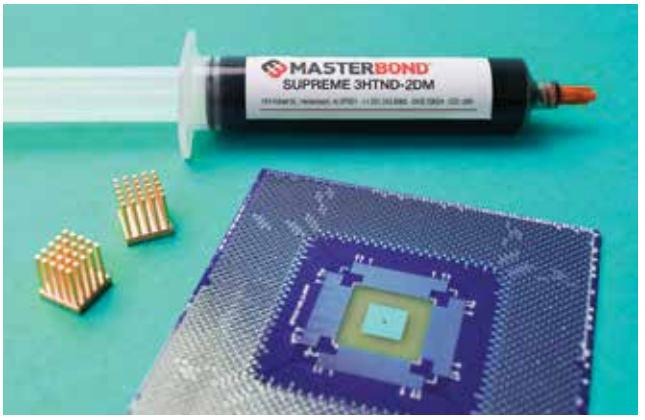
Used as heat-dissipating and insulating parts in power semiconductors, demand is increasing for nitride ceramic components possessing excellent thermal conductivity and mechanical properties as energy-saving requirements heighten in the automotive and railway industries. It is also expected that adoption of nitride ceramics will expand in semiconductor production equipment (SPE) as they enable precise temperature control at higher temperatures in the production process.

The two companies decided to work together in order to blend the material technologies on nitride ceramics possessed by Toshiba Materials with the special ceramic processing technologies possessed by Kyocera.
www.kyocera.com ◆

One Part, Toughened Epoxy for Specialty Dam-and-Fill Encapsulation

MASTER BOND SUPREME 3HTND-2DM is a rapid curing, toughened, one part epoxy system used for the dam-and-fill method for chip-on-board encapsulation. Essentially, there are two methods to protect chips and their wire bonds. One method is referred to as glob top, where the encapsulating system is dispensed and applied directly to the area to be protected. The dam-and-fill method entails dispensing the damming material around the area to be encapsulated. This material will cure in place and will not run, in essence forming a dam. Then an encapsulating material is applied to cover the remaining area to be protected. This system can be cured in thicknesses up to 1/4 inch.

Supreme 3HTND-2DM passes ASTM E595 specifications for NASA low outgassing enabling it to be used in vacuum, aerospace, electro-optic and other related applications. This high performance compound bonds well to a wide variety of substrates used in electronics including silicon and other semiconductors, metals, ceramics and many plastics. Most importantly, Supreme 3HTND-2DM has enhanced dimensional stability and has a tensile strength of 6,000-7,500 psi at room temperature. It also maintains its Shore D hardness of 85 after withstanding 1,000 hours at 85°C/85% RH.



As a toughened system, Supreme 3HTND-2DM resists rigorous thermal cycling. This epoxy withstands exposure to water and chemicals such as acids, bases, fuels and a number of common solvents.

This single component system is easy to handle and offers "unlimited" working life at room temperature. It cures readily at 250°F in 20-30 minutes or 5-10 minutes at 300°F. It is serviceable from -100°F to +400°F [-73°C to +204°C]. Supreme 3HTND-2DM is available for use in syringes, cartridges and jars. For more information visit www.masterbond.com. ◆

Amkor Technology Completes Acquisition of NANIUM

AMKOR HAS ANNOUNCED THAT IT HAS completed the acquisition of NANIUM S.A., a world class provider of wafer-level fan-out (WLFO) semiconductor packaging solutions.

The acquisition of NANIUM will strengthen Amkor's position in the fast growing market of wafer-level packaging for smartphones, tablets and other applications. NANIUM has developed a high-yielding, reliable WLFO technology, and has successfully ramped that technology to high volume production.

"Amkor is a leader in wafer-level CSP and high-density integrated fan-out technologies," said Steve Kelley, Amkor's president and chief executive officer. "With the acquisition of NANIUM, we will have an equally compelling value proposition in the low-density fan-out area. NANIUM is widely viewed as the fan-out technology leader as well as a very capable manufacturer, having shipped more than one billion WLFO packages utilizing a state-of-the-art 300mm wafer-level packaging production line."

NANIUM employs approximately 650 people and is based in Porto, Portugal.

Amkor Technology, Inc. is one of the world's largest providers of outsourced semiconductor packaging and test services. Founded in 1968, Amkor pioneered the outsourcing of IC packaging and test, and is now a strategic manufacturing partner for more than 250 of the world's leading semiconductor companies, foundries and electronics OEMs. Amkor's operational base includes 10 million square feet of floor space with production facilities, product development centers, and sales and support offices located in key electronics manufacturing regions in Asia, Europe and the U.S.

For more information visit the Amkor website at www.amkor.com. ◆

Xilinx Invests in Machine Learning Pioneer DeePhi Tech

XILINX HAS ANNOUNCED THAT it has invested in DeePhi Tech, a recognized leader in machine learning specializing in deep compression, compiling toolchain, and system-level optimization. Leveraging the architectural advantages of Xilinx® devices for machine learning, DeePhi provides inference platforms from edge to cloud for the coming wave of AI products and services in the industry.

DeePhi Tech was founded by researchers from Tsinghua University and Stanford University known for their pioneering research in machine learning and numerous papers published at top AI conferences around the world. Members of the DeePhi Tech team recently received the Best Paper Award at FPGA2017 for breakthrough results with a highly efficient FPGA-accelerated speech recognition engine achieving 43x the performance and 40x the performance per watt compared to a CPU; 3x the performance and 11x the performance per watt compared to a GPU.

"Xilinx FPGAs and MPSoCs provide the ideal combination of low latency and reconfigurability required for our inference solutions," said Yao Song, CEO at DeePhi Tech. "Xilinx's powerful platforms are already being used by DeePhi in commercial products from edge to cloud in smart surveillance and data center applications."

"Empowered by Xilinx technology and expertise, DeePhi solutions provide breakthroughs in efficiency through techniques like network pruning, compression and use of reduced precision data types," said Nazeem Noordeen, CVP of Acceleration and IP Solutions at Xilinx. "Our investment in DeePhi is further evidence of our commitment to provide our customers with industry-leading accelerated computing products."

Xilinx investments for accelerated computing target solutions for applications such as machine learning, image and video processing, and storage and network acceleration. To learn more about DeePhi Tech, visit www.deephi.com.

Xilinx is the leading provider of All Programmable semiconductor products, including FPGAs, SoCs, MPSoCs, RFSoCs, and 3D ICs. Xilinx uniquely enables applications that are both software defined and hardware optimized – powering industry advancements in Cloud Computing, 5G Wireless, Embedded Vision, and Industrial IoT.

For more about Xilinx products visit www.xilinx.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Smoke and Mirrors? A Failure in Three Acts

WOW, THAT'S COOL AND I really want one! In fact it is a perfect solution to _____. Those are typically my first right-brain thoughts when watching a slick "use case" video on crowd-funded sites like Kickstarter.com. Then a few seconds later my logical left-brain reminds my creative right-brain **whoa, not so fast**. In the case of Plastc, I almost fell for it at $155!

I've accumulated a few too many credit cards over the years to pick up points and other perks. And Plastc certainly looked like a cool way to slim down my wallet to just one card. One card to rule them all! (Apologies to J.R.R. Tolkien.) After reading a "write-up" and watching their really cool video at the time of the public launch in late September 2014 I almost placed a "pre-order". (Pre-orders in the crowd-funded world are the **euphemism for thanks for funding us and we'll be happy to ship you the product if we ever get it working**.)

How did my left-brain stop me from joining the herd which reportedly funded Plastc to the tune of $13.3 million? Business Insider reports they raised $9 M in pre-orders and $4.3 M from venture capitalists (VCs). My left-brain said I should know better and not even be tempted since there were several red flags. It now appears that Plastc was flawed in three areas: marketing, technology, and management. Any one of these flaws can be fatal but the combination of all three creates the perfect storm that presents impossible odds of surviving.

Flaw 1 - Marketing

As a marketer, I know that slick ads and product placements can drive demand, especially for a consumer product. And not just because there is a "sucker born every minute" as is misattributed to P.T. Barnum. When you have the right mix of compelling story or use case along with something that magically solves a problem – or even better removes a pain point – you get customer interest. I was "almost sold" by their impressive advertising and promotion. However, marketing communications (aka marcom - ads, press releases, trade shows, etc.) is only a part of marketing.

Many people, especially outside of marketing, confuse the two and believe marcom is all there is to marketing. These people don't realize that marketing is really about how to manage "exchange relationships" – i.e. exchanging goods and services for compensation. This includes product management (defining what is to be exchanged now and in the future), creating these goods and services, communicating with customers (marcom), delivering goods and services to provide value (product realization), and working with customers to define what is of value.

I'm all for marketing driving product management and setting BHAGs (Big Hairy Audacious Goals) to drive innovation. Plastc required innovation simultaneously on two fronts - technology (see Flaw 2) and changing the consumer usage model – which is very difficult even for the most established (read: successful and well-funded) companies to manage. It is far better – especially for a startup – to successfully disrupt one area and then worry about the second later.

Once they had their technology functioning, Plastc would have **had to convince customers to switch to their better mousetrap and to pay for this privilege**. At the end of the day, was there a sufficient market to support these cards at a level which would achieve economies of scale? Clearly there was a market since they had approximately fifty-eight thousand pre-orders (totaling $9M, at $155 each). But this pales with the millions, if not billions, of credit cards issued in the United States alone. Needing to disrupt on the technology and usage model fronts at the same time raised the overall risk and greatly reduced the likelihood of Plastc being successful.

Beyond the required innovation, the shifting landscape of the market was the far larger concern not addressed by the marketing team. Earlier the very same month (September 2014) that Plastc announced, Apple introduced Apple Pay. This was in addition to Google's on-going developments in their Wallet product family that were publicly shown multiple times staring in 2011. Knowing that these two giant disruptors were entering the payment market should have caused any seasoned marketing team to prod the executive team to immediately work on a business plan pivot.

One last glaring oversight was the market shift to implement Europay Mastercard Visa (EMV) "smart cards" which we have now as "chip and signature". The shift to these new more secure cards was started in Europe (as "chip and pin") but announced as early as 2011 in the US. Implementation in the US of the EMV standard was accelerated after the Target data breach in 2013. The switch over in liability - the "carrot" being used to "encourage" retailers to implement EMV readers - was set as October 2015. This date was no secret and was known several years in advance. Yes, Plastc gets credit for claiming that their product would include EMV support but this would create additional technology challenges discussed below. It is amazing that a competitor (Swyp) brazenly launched later in January 2015 with magnetic strip only – i.e. without EMV – joining the overflowing field of those attempting universal credit cards.

Flaw 2 – Technology

Here at Feldman Engineering we often get involved in "Technical Marketing", a deep understanding of the relevant technology versus the customers' needs. When the fundamental technology is not well understood, it is too easy to oversell what the technology can do in terms of product specifications or product roadmap. We dislike having to occasionally ask "what law of physics are you going to suspend" when reviewing what has been over-promised by over-eager product managers or marketers who don't understand the limitations of their own technology. What is worse is when other team members – who have the science and engineering background to know better – start believing their own company's marketing sales pitch.

The technical challenge of system integration that the Plastc universal credit card proposed was substantial: electromagnetic rewriteable "magnetic" stripe; high-resolution e-ink display; Near Field Communication (NFC) and/or Bluetooth connectivity – and a microprocessor. And don't forget sufficient battery power in a credit card size

that was rugged enough to survive daily use and abuse. **This level of engineering and integration is not the typical design (mostly aesthetic style / fashion) and supply chain exercise of many successful crowd funded goods like clothing and suitcases.** The non-recurring engineering costs of custom integrated circuits (ASICs or FPGAs), if required, could easily have been 5- to 10-times what they "raised".

Added to this integration challenge was how to support the required EMV functionality. On credit cards today, EMV is implemented with a secure microcontroller (MCU) whose input-output terminals are the gold pads you see you on the face of your credit card. These MCUs are standardized for a small handful of suppliers and are designed to do one thing very securely. The Plastc engineering team would have needed to figure out how to build a EMV MCU with "multiple personality disorder" to switch between your twenty-five different credit cards. And anyone thinking that the banks would consider sharing the encryption keys that prevent your credit card from being "cloned" should think again. At the end of the day, there is little difference between you cloning your credit card to Plastc, Swyp, Coin, Stratos, etc. and a criminal counterfeiting your card.

Flaw 3 – Management

I am not yet ready to jump on the bandwagon to label Plastc as a scam or pyramid scheme which would result from dishonest management. However, additional details may come to light especially if a class action lawsuit proceeds.

Management would be clearly at fault if there was only a Marcom team and not a marketing team to drive product management. Perhaps they were as confused as others are to the difference? (See Flaw 1.) However, assuming there was a real marketing team, having failures in both Marketing and technology (Engineering) is clearly a management failure. The management team needs to be smart enough and strong enough to know when either or both functions are not up to the challenge. Yes, Engineering and Marketing may disagree but neither should be bullied to agreeing to do the impossible. Difficult and challenging yes, impossible no. Functioning and responsible management needs to step in and moderate as required.

It has been reported that there were VCs who did fund Plastc. "Surprisingly" it is difficult to find those VCs investments listed now that Plastc failed to close a Series A funding round and has filed for Chapter 7 (liquidation) bankruptcy. Assuming there was VC participation, with typical representation on the company board of directors, this would be an additional layer of management failure. The VCs should have been smart enough to hire marketing professionals and technology consultants to perform due diligence and provide guidance to the startup. Of course, the VCs' right-brains may have also been taken in by the hyperbole and glitzy Marcom and successfully overruled their left-brains.

There were two additional "yellow flags" - cautionary items for crowd funding of future technology: be aware of "press release journalism" and non-community based fund raising platforms. Looking back at all the glowing news – from reputable "news" outlets – it was clear that they were mostly retelling the information provided by Plastc and not reporting on their actual usage of prototypes or products. **Yes, the product appeared to have great potential on paper.** Lastly, Plastc did their pre-orders direct and not through a platform or community such as Kickstarter. Although Kickstarter does not guarantee delivery or quality of items that are funded, they do attempt to manage risk on the basis of team reputations and by providing additional transparency.

It is true that the risk to the individuals (read "amateurs" who could not fully evaluate the product) who "pre-ordered" was not great. That is the beauty of crowd funding. However, the buyer still needs to beware since there is often little to no recourse to obtain a refund. And **in this story, the professionals failed.** If there was a marketing team they were not capable or able to do their job. Engineering did not speak up at the right time or in a meaningful way. And, clearly, management did not lead.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

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INDUSTRY INSIGHTS

By Ron Jones

Tips if You Decide to Look

HAVING BEEN IN THE RECRUITING business for more than 20 years, it feels like there are two states:

- Infinite number of available candidates and zero open positions.
- Infinite number of open positions and zero available candidates.

Being cyclical, it also seems like we go from one state to the other over a period of about 15 minutes.

We do a lot of due diligence work for companies that are looking at making investments in the semiconductor industry. One of the first questions invariably is "What is the outlook for the industry?" and our response, in true consultant fashion, is "It depends." We're not being evasive or flippant . . . the semiconductor industry is far from homogeneous.

There are IDM and fabless device companies; foundry and OSAT manufacturing companies; equipment and materials companies. There are end markets like computer, smart devices, automotive and of course the new buzz . . . IoT. Typically there are several product categories that are experiencing real growth and the others are static or shrinking. There are technologies like fab processes and geometries as well as assembly 2.5/3D, WLP, fanout/in, etc. These myriad parts overall may generally be headed up, down or static, but they certainly don't all run in synch like a clock. As you peel the onion, you see major differences. Closely related to company and industry growth is headcount.

I'm going out on a limb and saying that "generally" the jobs outlook for our industry is currently on a positive trend. There is still a relatively high level of M&A consolidation, which can cause personnel surpluses. Now that the election is over, companies are beginning to move ahead with plans for the future. This doesn't mean that there aren't reservations or concerns, but I am guardedly optimistic.

I have included some thoughts on what we see on a regular basis in the semiconductor hiring space. These are mainly aimed at people who have been in the industry for a number of years, not for those in their first few years out of school.

Residence Versus Work Location

Companies have varying levels of flexibility about allowing employees to work from home. Some companies are fine with an employee having local accommodations near the company during the week but traveling home on weekends, while others are not.

Job Hopping

Many hiring managers are sensitive to candidates who have had a number of short stays, either recently or in a row. They fear the candidate may not be a good investment unless they plan to stay for several years. In some cases, a person may have joined a startup that runs out of money for instance. In those cases, it may be wise to put a short sentence stating the circumstances of why you left.

Recruiting Process

Most companies in the semiconductor industry use a pragmatic, no nonsense approach to recruiting. They review candidate documentation and select those to move forward. They typically do an initial phone screen, then move promising candidates through one or two interview sessions. They identify a short list and move to an offer for the top candidate. The speed with which this happens depends to some degree with the number and availability of the involved people on the company side.

Recruiting Cycle Time

Our experience is that it takes about a month to identify and vet a sufficient quantity of contenders to ensure there are adequate viable candidates. It takes about a month to perform interviews and narrow to a candidate that receives an offer. We plan another month for the candidate to give notice and report to work. We have had searches that completed in a few weeks and some that have gone on a LONG time, for various reasons.

Age

It is illegal for companies to ask about or discriminate on age. If you want to appear younger, a common ploy is to drop early career jobs from your resume and not list dates for your education. This works fine as long as there aren't public sources that tell the rest of the story such as a LinkedIn profile with all your jobs or a Facebook account that lists your upcoming high school reunion. I have had candidates that said up front that they wanted to be evaluated on their capabilities and energy before divulging their age.

Relocation

Relocation reimbursement involving a home sale seems to be less common these days. Some level of moving reimbursement is not unusual. In some cases, the company only wants to consider local candidates

Resumes

We have grown up hearing about the importance of first impressions. In the employment arena, the resume often makes that critical first impression. Opinions about what constitutes a good resume are like noses . . . everybody has one. So here are mine:

- Clarity - It's not how much you can cram on a page, but rather how easily a reader can glean your key strengths and experience.
- Length - I recommend that a resume not go beyond 2 pages. If you have lots of patents or papers that are important, include them or do a separate attachment.
- Bullets - I prefer bulleted resumes that make it easy to see individual items. A large paragraph about what you did at a company is very difficult for the reader to sort out and interpret.
- Type font - My preference is for a relatively plain font like Calibri, with Times New Roman being second. Under no circumstances should you use something like Courier New, lest you be relegated to the nerd squad immediately.
- Contact Information - I recommend name, phone (home and cell), personal e-mail and home address (at least city and state). If it's not there, how will you be contacted?
- Job being sought – Opinions abound regarding a first section that states what you are seeking in a job. If you want to make it specific, that is probably OK. If you say you want a job that utilizes your talents and experience, better to say nothing at all.
- Box score - I usually like a section

before the list of jobs that has 3 or 4 columns and several rows with words or short phrases about your expertise or strengths.

- Employment history - For each employer, I recommend stating the name of the company (and possibly a short phrase on the nature of their business), the period of employment in beginning/ending format and the title of your position. If you had several positions, list the company once and then have the job title and from/to date for each.
- Education - Generally, you should list your educational achievements and special training undertaken. Time periods are optional.
- Personal Information - Information about marital status, children, military service, health, hobbies, etc. may be appropriate for some positions and less so for others.
- References - Almost always stated as available upon request.

Interviews

Do your homework! Be prepared! Spend time on the internet learning all you can about the company, its products and services, its history and culture and its financial condition. Talk to colleagues with knowledge about the company. Find out all you can about the hiring manager and others that may interview you using Linked In, Facebook or colleagues.

N-Able Group

We are always looking for experienced people that might be a fit for our client's positions. Please send along your resume. It will be help in strict confidence and not shared without your express permission.

If you are a company in the semiconductor industry that is looking to grow and needs people, please contact us to learn more about our services. ◆

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group also utilizes deep semi supply chain knowledge to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain. Email ron.jones@n-ablegroup.com.

2017 Semiconductor Industry Equipment and Materials Outlook

Dan Tracy, Sr., Ph.D. Director, Industry Research & Statistics
SEMI

THE SEMICONDUCTOR INDUSTRY turned in a surprisingly strong finish to 2016, especially given that growth expectations in the beginning of the year pointed towards possible contractions for a number industry segments. The strong close to 2016 coupled with slowly improving global GDP growth forecasts has resulted in an increasingly more positive outlook for 2017. Some industry analysts are now forecasting double-digit growth for both semiconductor revenues and capital spending.

The solid growth outlook for 2017 is based on a stronger outlook for the memory sector and for sensor devices. Storage, industrial, automotive, and wireless applications are driving this year's growth and will be key factors for longer term prospects for the industry.

Semiconductor Equipment Outlook

SEMI is forecasting about 12% growth in the overall semiconductor equipment market for the year, driven by investments for leading edge foundry technology, 3D NAND Flash, and advanced packaging applications. China will be a key market for capital spending, though especially in 2018 and beyond as the new fab projects there ramp up in earnest. While only three months of collected data is on-hand, the trends currently point to very solid year-over-year growth (see table above), with double-digit and even triple-digit year-over-year growth observed for most regions we track in our data collection program.

Overall, SEMI forecasts 12% growth in the equipment market for this year, and spending on fab equipment is expected to reach an industry all-time record. Current analysis based on the SEMI World Fab Forecast shows the record will be broken again in 2018.

Fab equipment spending is mainly directed towards memory (3D NAND

Region	2017 Year-to-Date (March)	2016 Year-to-Date (March)	Y/Y % Change
Europe	$940	$354	166.0%
Japan	1,245	1,237	0.6%
North America	1,256	1,006	24.9%
Korea	3,603	1,681	114.3%
Taiwan	3,554	1,887	88.3%
China	1,990	1,604	24.1%
ROW	616	506	21.6%
Total	**$13,205**	**$8,276**	**59.6%**

Source: SEMI/SEAJ Worldwide Semiconductor Equipment Market Statistics Report

Worldwide SEMS Billing Trends (US Dollars in Millions).

	2010	2011	2012	2013	2014	2015	2016	2017F	2018F
Wafer Fab	$23,046	$24,219	$23,464	$22,975	$24,250	$23,952	$24,705	$25,650	$26,845
% Annual Growth		5.1%	-3.1%	-2.1%	5.5%	-1.2%	3.1%	3.8%	4.7%
Packaging	$21,799	$22,861	$21,357	$20,293	$19,790	$19,338	$19,613	$19,701	$19,854
% Annual Growth		4.9%	-6.6%	-5.0%	-2.5%	-2.3%	1.4%	0.4%	0.8%
Total	**$44,845**	**$47,080**	**$44,821**	**$43,268**	**$44,040**	**$43,290**	**$44,318**	**$45,351**	**$46,699**
		5.0%	-4.8%	-3.5%	1.8%	-1.7%	2.4%	2.3%	3.0%

Source: SEMI Industry Research & Statistics Group, April 2017

SEMI Materials Forecast by Segment (US Dollars in Millions).

and DRAM), Foundry and MPU. Other strong product segments are Discrete (including LED and Power), Logic, MEMS (with MEMS/RF), and Analog/ Mixed Signal. By region, Taiwan and Korea will spend the most, though China is forecasted to be the third largest spending region for equipment and is likely to emerge as the largest spending region by 2019.

SEMI is tracking 20 new fab projects from 2016 onwards in China, with the Memory (3D NAND) and Foundry segments investing the most. While foreign investment historically accounts for the bulk of China investment, indigenous players will represent the majority of investment over the next several years.

Semiconductor Materials Outlook

Throughout the history of the semiconductor industry, annual equipment spending has proven to be more volatile compared to annual semiconductor materials growth as manufacturers need for capacity and technology affect the ramp expectations driving capital investment. Overall semiconductor industry output, in terms of units, tends to follow a more modest path in terms of year-over-year growth, and, in turn, the materials market trends track by SEMI typically reflect the more modest annual growth patterns, and 2017 will follow this trend.

Overall, we are currently tracking just over 2% revenue growth for total semiconductor materials, with a higher revenue growth forecast for fab materials compared to packaging materials. Material revenue growth overall should trend below semiconductor device revenue growth as the device growth comes from higher average selling prices expected in the memory sector. While downward pricing pressures abound across the materials supply chain, there is some upside to the forecast with overall improvements in the semiconductor market outlook and anticipated solid unit growth for devices. Some materials segments will benefit from improved pricing as well.

Revenue growth for fab materials will approach 4% for this year to reach over $25 billion globally. The strongest annual growth rates will be in China and Southeast Asia, respectively, as new capacity ramps up, off a smaller base compared to other regions. Strong single-digit growth will also occur in Korea and Taiwan as advanced fabs continue to ramp in those regions.

For packaging materials, the strongest growth this year will be in the China market as it has been over the past decade. The China market growth is based on the rising capabilities of the China OSAT companies and on-going package assembly investments by overseas OSATs and IDMs. An increasing number of companies in China are capable in delivery solutions for advanced packaging needs.

Summary

2017 will be a solid growth year for the global semiconductor industry, with storage, industrial, automotive, and wireless (connectivity) applications being the dominant drivers. Investments in the semiconductor industry will grow by double-digits for the year; and these end market segments will be key for industry growth for the foreseeable future. Advancements in semiconductor technology will enable innovations that will continue to transform and to disrupt many industries.

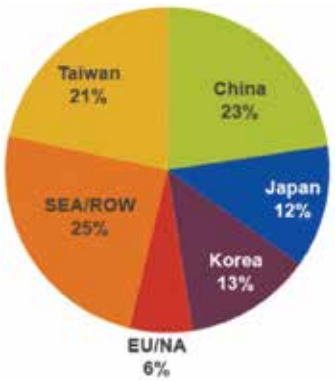
Foundry, 3D NAND, and advanced packaging are driving the growth for fab equipment. 2017 will mark the second year in a row of solid spending growth for semiconductor capital equipment and current projections indicate 2018 fab investment levels will increase over 2017 levels. The semiconductor materials market will increase as well. There are prospects that some material segments will experience some increases in average selling prices, and this trend could further boost the revenue growth for materials in 2017. ◆

2016 = $24.7 billion

Region	2016F $US B	2017F $US B	% Change
China	$2.09	$2.26	7.8%
Europe	2.49	2.54	2.1%
Japan	4.36	4.39	0.8%
Korea	4.62	4.48	4.7%
North America	4.30	4.40	2.2%
SEA/ROW	1.29	1.38	6.6%
Taiwan	5.56	5.85	5.2%
Total	**$24.7**	**$25.7**	**3.8%**

Totals may not add due to rounding.
Source: SEMI Materials Market Data Subscription, April 2017

Revenue Growth for Fab Materials.



2016 = $19.6 billion

Region	2016F $US B	2017F $US B	% Change
China	$4.44	$4.63	4.3%
Japan	2.39	2.36	-0.9%
Korea	2.49	2.47	-0.6%
EU/N. America	1.23	1.22	-0.9%
SEA/ROW	4.83	4.79	-0.8%
Taiwan	4.24	4.23	-0.2%
Total	**$19.6**	**$19.7**	**0.4%**

Totals may not add due to rounding.
Source: SEMI Materials Market Data Subscription, April 2017

Revenue Growth for Packaging Materials.

OVERVIEW

KESTER IS A GLOBAL SUPPLIER OF assembly materials to the electronic assembly and semiconductor industries. Their products include an array of industry standard and high-tech attachment materials including traditional soldering such as chemicals, paste, wire, and bar to more customer-specific solutions such as tacky solder fluxes and One Step Chip Attach materials. Their innovative products serve a worldwide customer base with supporting facilities and staff in North America, Europe and Asia.

Kester was founded in 1899 as the Chicago Solder Company to produce flux-cored solder wire. This patented Kester manufacturing process continues to have a major impact in the electronics industry to this day. Throughout the years, the Kester product portfolio grew to incorporate the product lines available today. Through strategic acquisitions, Kester was able to get close to electronics industry leaders and leverage new products. Working closely with key customers, Kester has continued to innovate in step with the evolving electronics market by supplying VOC-free wave fluxes for through hole applications in the 70s, solder paste during the adoption of SMT technology in the 80s, lead-free alloys during the 90s and 2000s, and continues with halogen-free offerings today.

Kester believes in building a global company with strong local presence. Hence, over the years, Kester has established local sales and support teams in North America, Europe and Asia, as well as manufacturing facilities in the US, Germany and China that enable Kester to be closer to their customers in each region.

In 2006, Kester was acquired by Illinois Tool Works (ITW). ITW is one of the world's leading diversified manufacturers of specialized industrial equipment, consumables and related service businesses. ITW businesses serve local customers and markets around the globe, with a significant presence in developed as well as emerging markets. The company has operations in 57 countries that employ more than 50,000 women and men who adhere to the highest ethical standards. These talented individuals, many of whom have specialized engineering or scientific expertise, contribute to their global leadership in innovation. They are proud of their broad portfolio of more than 17,500 granted and pending patents.

Kester is now part of ITW's Test & Measurement and Electronics business segment. ITW's Electronics business provides manufacturing and maintenance, repair, and operations (MRO) solutions that serve the semiconductor, industrial, life sciences and automotive industries among others. Strong brands such as Kester, Simco-ion, Texwipe, MPM, Camalot and Electrovert deliver quality performance and products that improve customers' productivity and quality. ◆

Kester's Facilities

Kester is headquartered in Itasca, IL, just outside of Chicago. This facility is Kester's center of excellence, housing global manufacturing for many of their products as well as centralized Research & Development staff and application equipment, technical support laboratories and product management capabilities.

In 2015, Kester opened a new facility in Wujiang, China. This plant, with best-in-class equipment and automation processes, has expanded Kester's global capacity. Kester invested heavily to adhere to China's strict regulatory demands and continues to focus on safety and environmental issues.

Kester also invested in their manufacturing hub to service and support the European market in 2015. This facility is based in Gernlinden, Germany (just outside Munich) and has been a Kester site since 1972. Kester has also been adding resources to their sales and technical support team in key regions, including Asia-Pacific and Europe.

Throughout the world, Kester's products are known for their high-quality and advanced technology. Kester's ISO-14001 and ISO-9001 certifications assure Kester's partners of this dedication to quality and environmental responsibility in every region in which their products are manufactured or supplied.

Kester's New Product Development Strategy

Kester strives to continually develop new products based on understanding their customers' pain points and needs. Using a robust New Product Development process, Kester is able to engage all functions of the organization in the creation of new products. Sales, Product Managers, and R&D Scientists work to understand trends and driving forces with the industry. Working closely with customer partners is essential to developing a product that will truly satisfy the needs of the industry. After thorough understanding of the customer pain points, Kester is able to leverage internal experience and scientific knowledge of staff with over 35 years of experience. In addition, Kester is able to engage resources from ITW and outside universities and academic institutions. After development, the product is brought to industry scale with their global manufacturing and quality network, ensuring customers from around the world will receive consistent quality products. Kester's sales team, technical application

engineers and distribution partners then make sure to aid customers in selection, qualification and continued support of products. Before and after product launch, Kester supports customers with in-depth product performance analysis in their fully equipped application laboratory. Even with a full SMT line and equipment to support semiconductor packaging, Kester continues to invest in equipment and expertise to better meet customer needs.

Product Line Overview

Kester products are solution-driven, reliable and backed by unparalleled customer service. Kester offers the following solutions:

- Tacky Solder Flux (TSF)
- SE-CURE™ Advanced Materials for Semiconductor Packaging
- One Step Chip Attach Materials
- Solder Paste
- Liquid Solder Flux
- Solder Wire
- Preforms
- Bar Solder
- A full spectrum of global customer technical support

Tacky Solder Flux

Kester TSF products are the industrial standard for Flip Chip and BGA Sphere Attach. With viscosities optimized for high speed application and holding of a chip or sphere in place prior to reflow, Kester TSFs enable wide process windows for their users. Known for their active soldering, Kester TSFs ensure good electrical connections on known good die and components. Kester's TSF portfolio includes solutions for no-clean and water soluble assemblies, with both rosin-based and synthetic rosin-free formulations. Kester offers options to meet both halogen-free and more stringent zero-halogen requirements of their customers.

One Step Chip Attach Materials for Use in Mass Reflow

Kester's new OSCA-R product line combines Flux and Underfill Technology for Flip Chip and Cu-Pillar Die Attach processes. This advanced material solution enables process simplification by eliminating separate cleaning and underfill dispensing steps of the process. Therefore, the material can improve throughput for a faster process, helping customers to increase profitability by increasing UPH. Multiple versions of OSCA-R provide cure kinetics customized to individual processing needs, including versions that immediately and completely cure curing mass reflow, or those that delay the final curing to a heat cycle after reflow, thereby allowing integration of post-reflow processes. By working closely with customers in their specific applications, Kester can tailor OSCA-R materials by adjusting filler type (silica or alumina, filler size (nanometer to micrometer and filler loading (0 to 60%). As an extension of the OSCA-R technology, Kester has also demonstrated material solutions for underfill and coating applications.

Soldering Made Easy with High-Reliability Products for Demanding Applications

Recently, the manufacturers in the Electronic Assembly industry have expressed concern over no-clean flux residue and its influence on reliability. This concern has been heightened by miniaturization simultaneous with high density board design trends.

To ensure high reliability, Kester has followed specific experimental procedures based on simple chemical fundamentals. These protocols discriminate two primary chemical mechanisms causing reliability failures: corrosion and electrochemical migration. Including industry standards and customer-specific testing, Kester is proud to present their series of chemically reliable products.

Solder Paste Products

Kester offers a complete line of solder paste to fit the needs of the electronic assembly market and cover the complete range of application types including no-clean, water-soluble, halogen-free and lead-free.

Liquid Flux Products

Lead-free wave and selective soldering systems require exposing the flux to slightly higher soldering temperatures. Lead-free alloys traditionally wet metal surfaces more slowly than tin-lead. Kester liquid fluxes for lead-free assembly have new activator packages to enable rapid wetting and holefilling, ensuring reliable product output.

Solder Wire

Kester wire products have been developed to provide superior performance for robotic soldering and hand soldering in the industrial and electronics industries. Kester wire is available in sizes down to 0.25mm and in silver-free, lead-free and leaded alloys in either solid solder or internally cored with fluxes optimized for specific applications. Kester's 100 years of history have enabled optimized production processes to eliminate flux voiding in solder, maximizing yields for end customers.

Preforms

Kester preforms are used for the assembly of components that cannot be assembled (or conveniently assembled) using traditional SMT reflow e.g. heat sensitive components and through-hole devices. Preforms are solder stampings that can be custom made in a very wide variety of forms and sizes. Common preform shapes include washers, discs and rectangles with either internal or externally applied flux. A full list of shapes and dimensional capabilities is available at www.kester.com.

Preforms can be supplied loose in bulk, stacked or in tape-and-reel packaging. Depending on customer specifications, alloy type, flux core or coating and packaging requirements, the combination of variables is nearly endless. Kester preforms are ideal for automotive electronic, selective soldering, die attach, thermal fuse and connector/wire harness assembly applications.

Kester and Industry Trends

At Kester, they believe in working closely with their key customers to understand their pain points and drive the customer back innovation process to provide innovative interconnect solutions to their customers in the electronic assembly and semiconductor industry.

In the age of IoT (Internet of things) and Big Data, reliability of the electronic devices is becoming more important. Besides automotive electronics, military and medical devices, more and more consumer products are considering the issue of reliability in electronics as continuous data capturing and processing becomes more critical.

Over the past few years, Kester has published technical papers that showcase their unique product solutions to the industry. These articles, including *"Assembly of Copper Pillar Devices using One Step Chip Attach Materials (OSCA-R) and Conventional Mass Reflow Processing"*, *"Electrochemical migration under low stand-off components"* and *"Dendritic growth from chemical contamination and partial cleaning"* can be found on their website at www.kester.com.

Kester's product innovations evolve around providing the best interconnect technology and solutions to their customers to ensure high reliability of the interconnect that translate into high reliable end products. They believe that with their unique advance knowledge in flux chemical, polymer technology as well as strong metal alloy know how, Kester is well positioned to provide an innovative solution to the industry. ◆

Kester Wire Products

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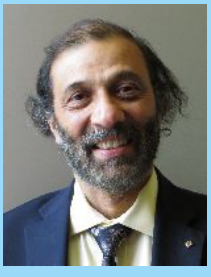

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Miniaturization Spurs EMI Innovation at the Package Level

Jinu Choi and Doug Dixon
Henkel Electronic Materials LLC

DEVICE DESIGNERS AND ELECTRONics specialists are all too familiar with the challenges surrounding electromagnetic interference, more well-known by its acronym, EMI. A disturbance to an electrical circuit due to electromagnetic coupling from external sources, EMI is quite common with radio-frequency (RF) emitting devices such as smartphones, tablets and IoT-enabled technologies, among others. In order to limit the spread of the interference from one component to another within an electronics assembly and/or reduce outside interference, effective isolation must be employed. Traditionally, this has been achieved through the use of EMI shielding caps, which are also often referred to as cans or faraday cages. These metal lids attach to grounding pads that cover a component or an assembly to minimize EMI between components within a design and eliminate cross talk of components on PCBs. (Figure 1) Historically, the attachment of the shield has occurred at the PCB assembly phase, but that's all changing.

With miniaturization comes greater integration at the package level. Not only are device dimensions becoming smaller with thinner package profiles, it's also quite common to have chips with higher and lower operating frequencies within the same package, as is the case with system-in-package (SiP) devices. Because conventional EMI shielding caps don't enable super-thin package dimensions or protect against in-package interference, new strategies must be used to effectively shield miniaturized devices and adequately isolate varying frequency chips within the same package. Two new approaches have emerged as alternatives to traditional EMI shielding techniques and effectively move EMI management from the board level to the package level.

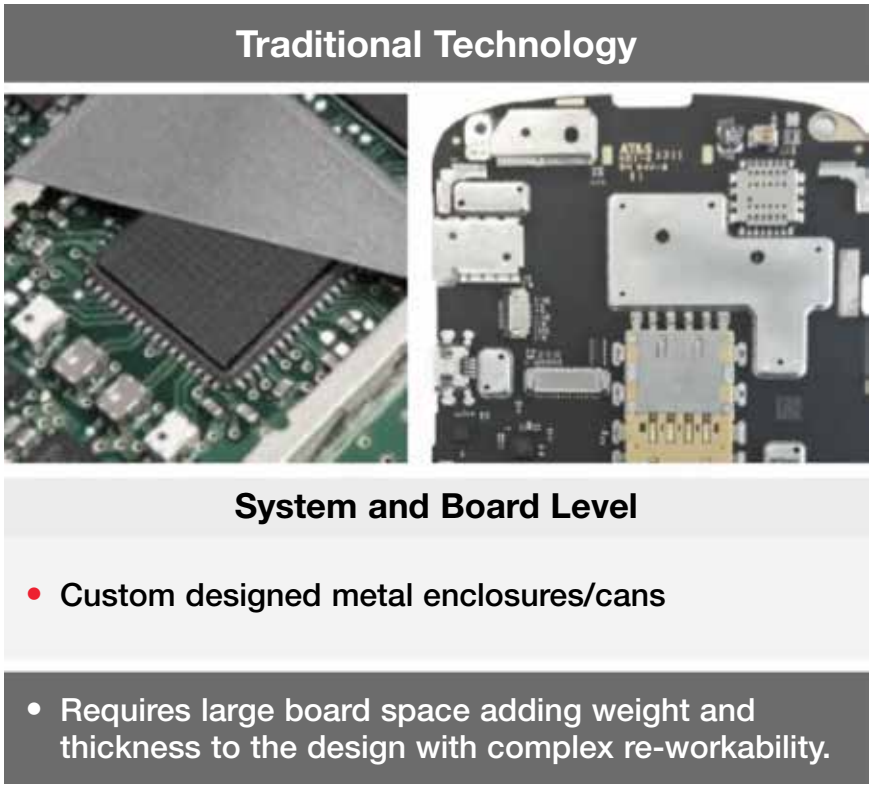

Figure 1. Conventional EMI shielding caps are limiting for modern, streamlined designs.

Significant package-level EMI shielding progress has been achieved with an innovative, compartmental shielding method designed to allow separation of chips housed within the same device, protecting against signal interference. Using this technique, target dies are identified and a small channel is routed through the molded SiP via precise laser cutting. Once the trench is created, a high-flow, highly-conductive material is jet-dispensed into the trench and then cured. With this method, high aspect ratio (aspect ratio = X dimension/Y dimension) filling is critical and can be challenging, as the trenches are often quite narrow and high, ranging anywhere from aspect ratios of 5:1 up to 10:1. In order to completely fill the gap, simultaneous air displacement and paste deposition is required to protect against voiding and optimal EMI safeguarding. In addition, the conductive paste must have strong adhesion properties with minimal shrinkage to ensure no separation from the grounding floor and the mold compound sidewalls of the trench. Essentially, this technique, along with a conformal coating, creates multiple faraday cages around the targeted die without altering the footprint or the height of the component, while delivering highly-effective EMI protection.

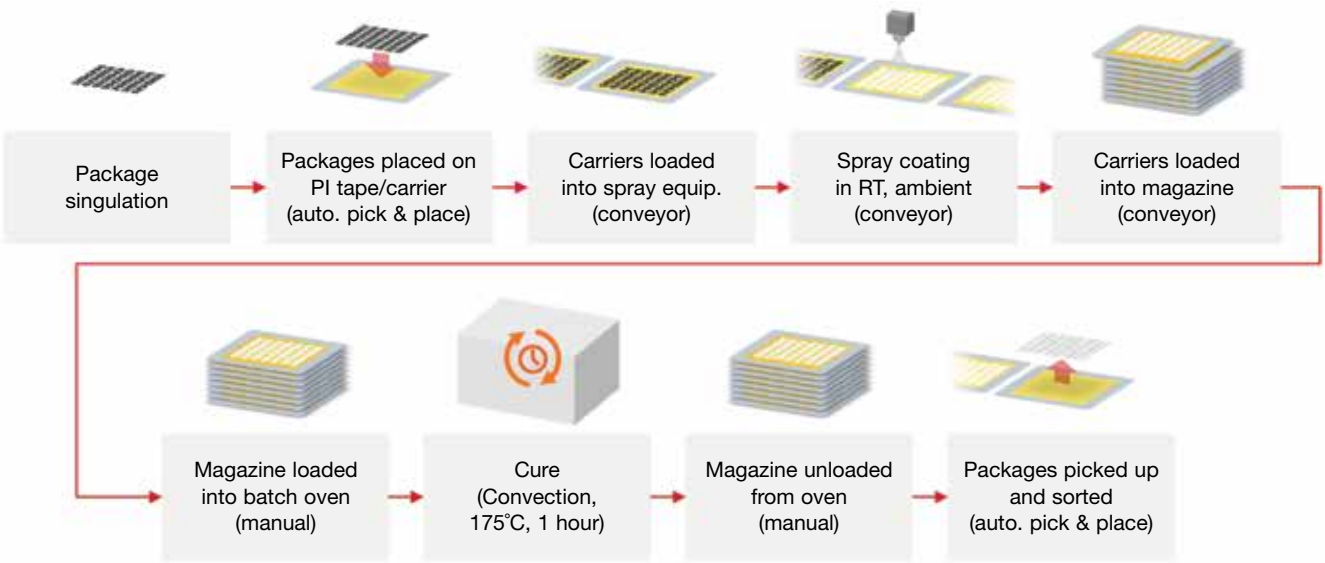

Figure 2. The EMI conformal shielding process dramatically raises throughput with the ability to process either singulated or strip formats, resulting in a much lower cost per part while delivering ultra-thin protection for today's thinner designs.

Along with in-package chip isolation, a new process for ultra-thin, on-package shielding helps eliminate the use of conventional EMI caps, streamlines processing and offers a lower-cost alternative to other on-package techniques. Current methods that coat the exterior of a component with a protective EMI shielding material are usually quite capital-intensive. Sputtering, for example, is a physical vapor deposition process that requires substantial capital investment with low units per hour (UPH) and high maintenance costs. With sputtering, metal is deposited onto the plasma treated, molded package in a vacuum chamber and normally entails depositing several layers of material. Another popular approach to on-package shielding is plating, where electroless copper and electrolytic copper/nickel are coated onto the mold compound. Plating delivers good thickness control like sputtering, but with respectable UPH at the strip level and a relatively low material cost. However, plating does have drawbacks, including environmental contamination which has raised high concerns and restricted mass deployment. In addition, surface pre-treatment and complex masking procedures must be used; no singulated packages can be processed as plating can only manage strip formats; and, it is a wet process that requires substantial floor space.

Given these realities along with the industry's desire to raise performance, increase UPH, lower cost and reduce process complexity, development of a new

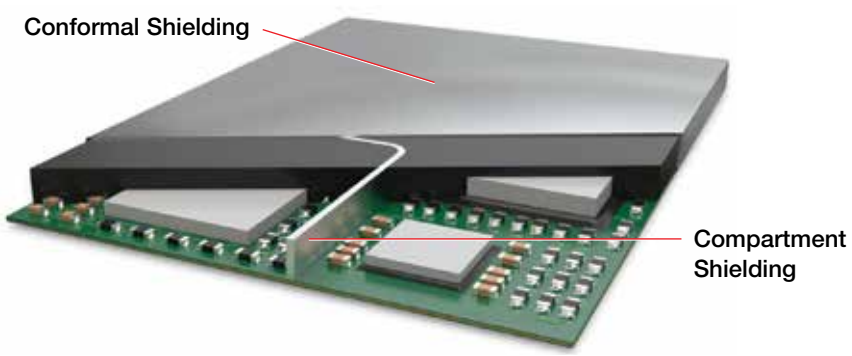

Figure 3. Compartment shielding isolates chips within a package, while ultra-thin conformal shielding coats the package exterior for maximum EMI protection.

EMI conformal shielding solution was initiated. Building on atomization spray technologies used to coat PCBs and other electronics, the new spray-on EMI shielding material provides superior processing and performance advantages as compared to alternative metal coating techniques. Simple and easy to support in a batch process, a spray-coated, flowable and highly conductive material is applied to the molded component, ensuring full coverage of the top and sidewalls for maximum EMI protection. (Figure 2) The new spray coating method allows for very high UPH and multi-part processing in either singulated or strip formats for high throughput. No pre-treatment of organic surfaces is required for this single-layer application, which can be applied as thin as 3-5 μm to accommodate today's ultra-thin package profiles. The material delivers excellent shielding effectiveness with a simple process that provides a lower cost per package, much higher UPH, smaller floor space and easy scalability. In fact, as compared to sputtering, conformal shielding can reduce cost of ownership by as much as 60%, while raising UPH by a factor of four. And, for SiP devices that undergo compartmental shielding, the spray-on coating is completely compatible with trench filling materials, allowing packaging specialists to use both approaches for EMI shielding. (Figure 3)

As package- and chip-level functionality continues to increase so, too, will the need for novel and effective solutions for EMI shielding to accommodate ultra-small package profiles. Trench filling and conformal shielding are a significant, cost-effective step forward for in-package and on-package interference resistance. And, in the longer-term, shielding at the wafer level may become reality. ◆

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Are Trade Secrets a Better Alternative to Patents for Protecting IC Packaging Inventions?

Kevin Roe, Intellectual Property Attorney and Phil Marcoux, Packaging IP Strategist

WITH THE MYRIAD OF CHANGES to the protection of US patents over that past five years they may have reached the point that they aren't worth the ink to print them. The normally staid world of IC packaging has not been able to avoid the impact of these changes. This is particularly troublesome at a time when IC packaging has become more critical.

The changes have occurred within the US Patent Office, within the US Courts, and throughout the world.

Some of the most impacted IC packaging areas include interconnections, such as via usage in various substrates, e.g. silicon, glass, metal; component stacking, and material development to improve performance.

Since the *Alice Corp. Pt. Ltd. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014) decision of the Supreme Court in June 2014, a vast number (several hundreds) of patents have been invalidated in the US federal courts, before the patent infringement litigation phase could even begin. Nominally, the original Supreme Court *Alice* test was composed of two parts (1) a determination if a patent claim had such a vast legal scope that it potentially caused legal preemption of an abstract idea, principle, or scientific law, and (2) a determination of whether such a patent claim had any redeeming inventive (i.e., novel) concept that distinguished and limited the scope of the patent claim to make it still legally enforceable. If all the patent claims failed this two-part test, then the entire patent could be invalidated. However, in the original *Alice* decision, even the US Supreme Court itself was able to recognize and observe ***that all inventions at their heart, if examined deeply enough, actually apply abstract ideas, principles, or scientific laws***, and as a result, the original *Alice* decision cautioned US federal courts to keep this in mind and not invalidate patent claims and entire patents merely because of this fundamental fact regarding all inventions.

However, the warning notice in the *Alice* decision was totally ignored by almost all US federal courts, except for a few exceptions on rare occasions. So the use or application of an abstract idea, principle or scientific law by any patent claim became automatic presumptive proof of preemption as far the US Court of Appeals for the Federal Circuit was concerned, and this viewpoint was adopted by the US District Courts as well. This was the first mutation of the *Alice* decision. Then the US Court of Appeals for the Federal Circuit mutated the *Alice* test in a second way - ***if the patent application did not re-teach in a vacuum all the already known prior art technology used by the invention all over again, then the inventive concepts in the patent claims are irrelevant to meeting the second part of the Alice test, and do not need to be considered at all and the patent is automatically invalid based on the presumption of preemption***. To see how unjust this second mutation is, consider the following analogy. If you were to invent a new internal combustion car engine that uses conventional spark plugs, ignition wires, fuel injectors, cylinder heads, and so forth, then this second mutation means that your patent automatically fails the *Alice* test if your patent does not go back and re-teach in a vacuum all the details of how to make and install spark plugs, ignition wires, fuel injectors, cylinder heads and all the rest. In other words, under the second mutation of the *Alice* test, any patent that does not regurgitate all the already known prior art technology all over again is automatically invalid and can be declared invalid by summary judgment - even if your patent lists several prior art patents that already teach the prior art technology in detail that you use in your invention. If you find this to be so idiotic as to be absolutely astounding, see US Supreme Court case docket number 15-1201, which has a petition that describes the use of these two mutations to invalidate an actual patent.

Therefore, virtually any patent litigated in the US is now at great risk of being invalidated by an opposing party that merely makes a false accusation of abstract idea preemption by the patent claims, even without a shred of factual evidence in reality. Typically, the patent will be declared invalid (without even a full consideration of the extra inventive concepts in the patent claims) in a US District Court's summary judgment and no evidence will need to be presented by the accuser to prove preemption of an abstract idea.

The net result of all the preceding is that a US patent application can now be a waste of time and money for inventions in many cases, especially inventions having any software component. The original incentive of filing a patent application in the first place was that if the inventor taught their invention to the entire world, the inventor would at least get a time-limited monopoly to the invention in the US under US patent law as a reward for teaching the invention to all competitors around the world, so that the invention could used as a stepping stone to advance the field of technology even beyond the invention disclosed. Now, without a valid patent that can be legally enforced, the entire exercise of filing a patent application and obtaining a patent is a waste of time and money for inventors, especially individual inventors and small companies.

However, there is an alternative way to protect inventions and it's one that should apply very successfully for the IC packaging industry. Trade secret law can be enforced in state courts as well as federal courts, and trade secrets in many cases offer many advantages, compared to published patents that instantly teach an invention to every competitor in the

continued on page 32

Failure Analysis – A Tool for Developing New MEMS Sensors

William Boyce
SMART Microsystems Ltd.

IN THE WORLD OF MEMS SENSORS new product development, failure analysis is a tool that can reduce costs and accelerate time to market. Failure analysis can be used to achieve a better understanding of the behavior of a MEMS sensor product after being stressed by the conditions from its application environment. In a thoughtful design, the environmental conditions in which a product is intended to function need to be considered carefully. Once these conditions have been determined, a life test profile is defined in order to simulate the environmental conditions in which the product will need to survive. When the life test profile is completed, a functional test is performed to evaluate whether the product is still operating according to customer specifications. The next step is to perform destructive and/or non-destructive analysis of the product to identify its strengths and weaknesses. Analysis should always be conducted regardless of whether or not there is a confirmed failure. Finally, the lessons learned from the analysis must be fed back to the product design team to improve the product, lower the cost, or both.

Environmental Conditions

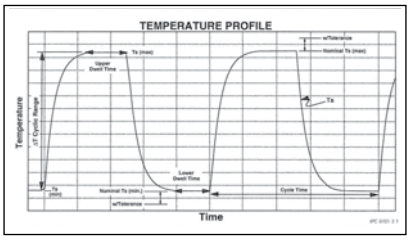
The environmental conditions for a MEMS sensor product are requirements driven by the customer. An automotive application for example, will have a different set of requirements than a part with an aerospace application. The end user or customer typically has a good understanding of how the part will be used and the environment in which it must survive. High temperature endurance, low temperature endurance, and UV exposure are examples of tests that are used to replicate common environmental conditions.

Life Test Profile

A life test profile is developed by the customer in an effort to simulate the environmental conditions to which the part will be subjected during use. These tests, or series of tests, are intended to accelerate the life exposure of the product and can sometimes be harsher than the actual operating conditions of the product. For example, air to air thermal shock exposure is a commonly performed test that can stress a mechanical MEMS sensor package to premature failure. The life test profile includes tests that represent both actual environmental conditions and accelerated environmental conditions in order to create learning about failures, potential failures, or both.[1]

Super UV Test Chamber.

Thermal Shock and Thermal Cycle Chambers.



Sample Thermal Cycle Test.

Functional Test

Functional tests can vary widely and are driven by the operating requirements of the product. This can include visual inspection, measurements taken after the life test profile, and/or measurements taken during certain tests. In the case of a MEMS pressure sensor, the functional test will typically include current draw, output as a response to applied pressure (characteristic curve), and a leak test. In many cases, monitoring the sensor output function throughout testing is required to determine the exact moment of failure—if and when it occurs. There is also typically a mechanical package inspection requirement to determine if any physical damage to the package occurred as a result of the life test profile.

Destructive / Non-Destructive Analysis

If a functional failure does occur from the life test profile, analysis should be performed to determine the root cause of the failure. Non-destructive analysis techniques include optical microscope inspection, 3D X-ray, and acoustic microscopy. Destructive disassembly follows which could include shear/pull testing, cross sections, scanning electron microscopy (SEM), optical microscopy, and elemental surface analysis such as emission dispersive spectroscopy (EDS).

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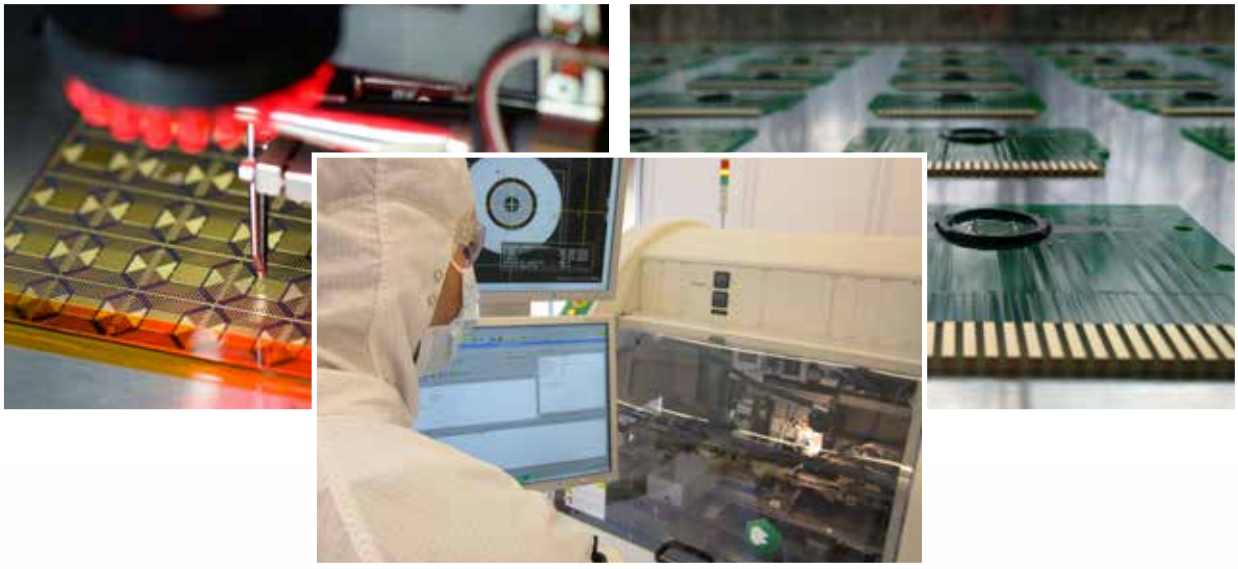

PROTOTYPE DEVELOPMENT • ENVIRONMENTAL LIFE TEST • MANUFACTURING SERVICES

MEMS sensors are a platform technology that measure environmental stimuli – for example, pressure, gas, temperature, motion – and can be used in a wide variety of different application areas. MEMS sensors are attractive because they deliver higher performance at lower cost plus they are smaller, have less weight, and use less power than other technologies. New combinations of packaging materials and semiconductor components add complexity; therefore the advantages can only be realized with custom microelectronic process development in order to ensure the performance requirements, the manufacturability, and the cost targets for the specific application.

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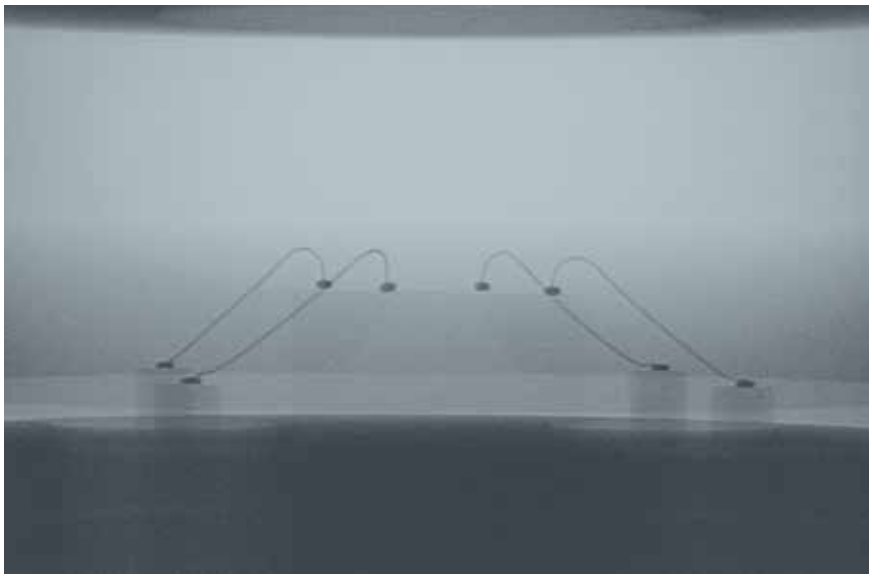


X-ray of Die and Wire Bonds.

3D X-ray System.

If all of the parts on test survive the entire life test profile without a failure, a complete post-test analysis should still be conducted in order to determine if there are any parts near failure or areas for improvement. Additionally, it is recommended that non-destructive analysis techniques should be used to capture images of parts before the life test profile, so that there is a base line for comparison once testing is complete. In some instances, design and process improvements can be identified by uncovering potential weaknesses after the life test profile, even without a demonstrated failure.

Lessons Learned

In this stage of the new product development cycle a complete "lessons learned" review is in order. It is important to use all collected data to drive design and process improvements. This aligns with proven new product development strategies such as: test early, test often and concurrent engineering. The idea is to create early learning using failure analysis results in order to implement improvements before freezing the product design. The results of this "lessons learned" review drive action in the form of a Risk Analysis, PFMEA, DFMEA, other six sigma techniques and quality methods.[2]

Failure analysis is an effective tool for the development of new MEMS sensors products. It can be used to understand the behavior of a part in the given application environment. A life test profile evaluates the effects of the environmental conditions against the design objectives and a developed manufacturing process. Functional testing and non-destructive/destructive analysis provides the lessons learned where immediate inputs to the new product development cycle can reduce development costs and time to market. ◆

Fatigued/Deformed Wire Bond.

Scanning Electron Microscope.

William Boyce is the Engineering Manager at SMART Microsystems. He is detail-oriented and is a hands-on engineering leader with a wide range of diverse skills from his background in automotive sensing.

He has served in senior engineering roles over the last 19 years with accomplishments that include manufactured automotive sensors. He also led new product development teams that created over $25 million in new revenue per year. He is certified in EIT and Six Sigma Green Belt and is an industry recognized expert in Al wire bonding. Additionally, he designed and led the metrology lab and machine shop at Sensata.

Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has been a member of the IMAPS New England Chapter for over 10 years.

References

[1] "Environmental Test Strategies for MEMS Sensors Product Development", MEPTEC Report, Spring 2017, Volume 21, Number 1.

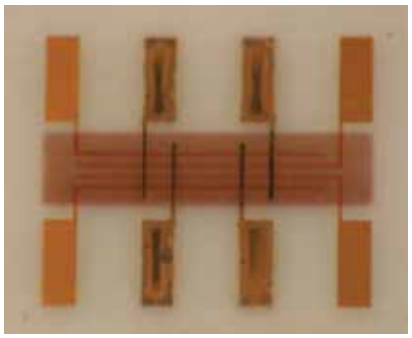
[2] "Engineering that Begins with the End in Mind", MEPTEC Report, Spring 2016, Volume 20, Number 1.

State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to include this new feature to the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

REMIT University (Australia) has developed a revolutionary process using nano-printing of liquid metal to create integrated circuits that are only atoms thick, allowing reliable production of large wafers 1.5 nanometers in depth. Other techniques have proven unreliable in terms of quality, scale up and function only at very high temperatures. The surface of the wafer can be pre-treated to form individual transistors. Researchers used this process to develop transistors and photo-detectors of very high gain and reliability. *(IEEC file #9887, Science Daily, 2/16/17)*



Duke University researchers have developed a "spray-on" digital memory device that can significantly lower cost flexible electronics. The technique utilizes an aerosol jet printer and nanoparticle inks. The created 4-bit flash drive device is the first fully-printed digital memory. Potential applications include environmental sensors or RFID tags. The process compatible with building electronic devices on bendable materials like plastic or fabric. *(IEEC file #9971, R&D, 4/3/17)*

Rutgers University researchers are exploring using graphene for cooling of computer chips in electrical devices such as smartphones. Graphene is a very thin, 2-D material that can be miniaturized to cool local hot spots. They achieved a power factor two times higher than thermoelectric coolers. Graphene also conducts electricity better than copper, quickly diffuses heat and is 100 times stronger than steel. *(IEEC file #9964, R&D, 3/28/17).*

Linköping University researchers have developed the world's first heat-driven transistor. This logic circuit transistor is controlled by a heat signal instead of an electrical signal. Potential applications include monitoring medical dressings and monitoring the healing process. Only a single connector is needed from the heat-sensitive sensor, to the transistor circuit. (IEEC file #9861, ECN, 1/31/17)

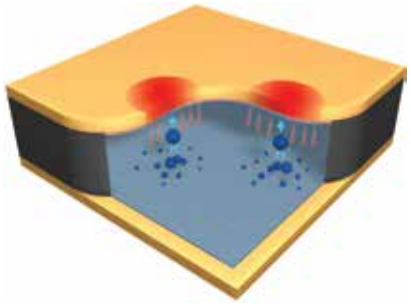
New low cost, eco-friendly flash memory device using a hybrid of graphene oxide and titanium oxide has been developed by University of Exeter engineers. This technique could lead to flexible and transparent electronics applications such as flexible electronic devices, intelligent' clothing, 'bendable' mobile phone, computer and television screens. *(IEEC file #9970, Solid State Technology, 3/31/17).*

The University of British Columbia has developed a flexible sensor for foldable electronics. It is constructed with two layers of silicone, and a layer of conductive gel. In the stretched condition, it can detect varying degrees of human touch, such as swiping or taping. This sensor can also be used as a component in artificial skin. If the sensor acts as an outer layer in robotic designs, it could potentially increase the safety of human-robot interactions, relaying body movement data and vital signs. *(IEEC file #9947, ECN, 3/20/17)*

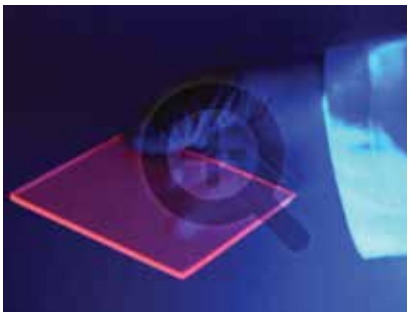
Carnegie Mellon University researchers have developed "Thubber", a thermally conductive rubber material that represents a breakthrough for creating soft, stretchable machines and electronics. The new composite material is electrically insulating and has metal-like thermal conductivity. Its elasticity can stretch over six times its initial length. Applications includes athletic wear & sports medicine, energy, transportation are other areas which could use stretchable electronic material. *(IEEC file #9881, Product Design & Development, 2/14/17)*

University of Illinois researchers found that "bubble-recoil" can be harnessed to mix liquid coolant around high-power microelectronics in space applications. Researchers demonstrated this capability by taking two heat-generating chips and sandwiching them while alternating the power to the two chips. This enabled a test apparatus to swing back and forth through the coolant. *(IEEC file #9922, Science Daily, 3/6/17)*

University of Exeter researchers have developed a breakthrough method in the production of vital new optoelectronic materials that could 'revolutionize' materials and methods used for a wide range of future optoelectronic devices. The team used microfluidics technology, in which a series of channels controls the flow and direction of small amounts of fluid containing graphene oxide flakes. *(IEEC file #9921, New Electronics, 3/6/17)*



Researchers at Duke University are using a new technique utilizing "jumping droplets" to help solve the problems with local device hotspots. They demonstrated that when two water droplets merge together on a water-repellant surface, the merged droplet spontaneously jumps perpendicular to that surface. The out-of-plane jumping motion is driven by surface energy initially stored on the droplets and released upon drop coalescence, which can locally cool hot spots. When a hotspot appears on a surface saturated with water, it drives the working fluid to vaporize This enables continuous operation of the vapor chamber to dissipate heat. *(IEEC file #9972, R&D, 4/4/17)*



University of Minnesota researchers using silicon nanoparticles have developed an approach to energy collecting windows. Windows that can collect solar energy are the next considered an important extension to renewable energy technologies. They embedded the silicon nanoparticles into luminescent solar concentrators (LSCs). When light shines through the surface, the useful frequencies of light are trapped inside and concentrated to the edges where small solar cells can be put in place to capture the energy. *(IEEC file #9907, Printed Electronics World, 2/28/17)*

Researchers at Jülich Supercomputing Center have found a novel combination of graphite and barium manganese oxide for use in spin-based transistors. Spin transistors require significantly less energy than conventional transistors. The hybrid material allows both precise spin alignment and good spin transport, as demonstrated by simulations on supercomputers. *(IEEC file #9837, EIN 007, 1/18/17)*

MARKET TRENDS

Global MEMS market projected to be $26.8 billion by 2022, growing at a CAGR of 11% from 2016 to 2022. The Asia-Pacific region contained the major share in the market, and is projected to continue its dominance through 2022. The global MEMS market high growth rate is due to development and high usage in smartphones, major growth in portable electronic market and increase in popularity of Internet of Things (IoT), and demand in automation industry. Further, emerging trend of wearable devices, connected cars, and others are expected to offer new opportunities for market growth. *(IEEC file #9954, Sensors, 3/15/17)*

A $600 million stretchable electronics market is expected by 2027. The electronic industry is in a major paradigm shift. Resulting novel form factors are emerging, ranging from the introduction of limited stretchability, through to ultra-elastic and conformable electronics. This transfiguration has been in the making for more than a decade but it is only now that it is beginning to make a substantial commercial impact. *(IEEC file #9958, Printed Electronics World, 3/22/17)*

The transparent conductive film (TCF) market is projected to be $400+ million by 2027. This industry is entering a new phase as new market opportunities are emerging. Some ITO alternatives have matured, receiving increasing market adoption. The consumer electronic touch screen market is the primary market driver for TCFs. Other new market opportunities are emerging such as touch surfaces in the form of whiteboards, tablets, and other interactive surfaces. Automotive displays will also pay a significant part. These market opportunities are forecasted to represent nearly 45% of the total TCF market by 2027. *(IEEC file #9935, IDTechEx, 3/13/17)*

The 3D and 2.5D IC packaging market is projected to be $170 billion by 2022, with 38 % CAGR of between 2016 and 2022. The drivers for this market are the increasing need for advanced architecture in electronic products, rising trend of miniaturization, and growing market for tablets, smartphones, and gaming devices. The 3D TSV market is expected to grow at the highest CAGR. The major factors driving the 3D IC and 2.5D IC packaging market for 3D TSV include highest interconnect density and greater space efficiencies in 3D TSV compared to all other types of advanced packaging such as 3D WLCSP. *(IEEC file #9911, Solid State Technology, 2/22/17)*

Global smart sensor market is forecasted to be $60 billion by 2022, growing at a CAGR of 19.2% from 2016 to 2022. Automotive industry dominated the smart sensors market in 2015. In the same year, Europe led the global market, accounting for 32% market share. Smart sensors transmit data over all the available networks, and enable features such as digital processing, data conversion, and interaction with external devices. Such sensors hold significant importance in the current scenario, owing to the augmented usage across various application verticals such as consumer electronics, automotive, and healthcare. *(IEEC file #9888, Sensors, 1/20/17)*

The Flexible Battery Market was valued at $70 Million in 2015 and is estimated to increase to $958 Million by 2022, at a CAGR of 46.6% between 2016 and 2022. Smart packaging application held the largest market size in the overall flexible battery market during the forecast period. The smart packaging application of the flexible battery held the largest market size in terms of value in 2015. Smart packaging includes printed electronics products such as disposable batteries, sensors, printed displays, and circuits as well as other electronic features such as anti-theft tags, RFID tags, and smart labels. *(IEEC file #9843, Sensors, 1/9/17*

RECENT PATENTS

Air-cooled heatsink for cooling inte-grated circuits *(Assignee: IBM Corp.) Patent No.– 9,609,785*. A system includes an integrated circuit and a heatsink mounted thereon. The heatsink includes a flat base plate thermally coupled to a top surface of the integrated circuit, thermally-conductive solid metal posts mounted perpendicularly on the base plate, and flat metal fins. Each of the fins has holes fitted about the posts such that the fins are mounted on the posts in vertically-spaced, parallel alignment relative to each other.

Double-sided chip on film packaging structure *(Assignee: Raydium Semiconductor Corp.) Patent No.– 9,589,883*. A double-sided chip on film (COF) packaging structure and a manufacturing method thereof are disclosed. The double-sided COF structure includes a metal layer, a first insulating layer, a second insulating layer, a chip, and an encapsulant. The first insulating layer and second insulating layer are disposed on a first surface and a second surface of metal layer respectively. The first surface and second surface are opposite. The first insulating layer includes a first part and a second part separated from each other. An accommodating space is existed between the first part and the second part and a part of the first surface is exposed.

Electrically stackable semiconductor wafer and chip packages *(Assignee: Invensas Corp.) Patent No.– 9,601,474*. A wafer-leveled chip packaging method, comprising the steps of: providing a wafer; attaching at least one first chip to the wafer; forming a first insulating layer on the wafer; forming a plurality of first conductive vias penetrating the first insulating layer, wherein parts of the first conductive vias are electrically connected with the first chip; forming a conductive pattern layer on the surface of the first insulating layer wherein the conductive pattern layer is electrically connected with the first conductive vias.

Thermally Conductive Circuit Board Substrate *(Assignee: Klein Raul) Patent No.– 15/369762*. Thermally conductive efficient substrate for use in an electrical circuit board assembly (ECBA) preferably having at least one LED component. The substrate is constructed of a thermally conductive efficient material such that the substrate functions both as a substrate and as a heat sink for the PCB. The substrate allows a PCB to function without a dedicated auxiliary heat sink. The substrate preferably includes a plurality of raised pads formed such that open channels are formed between, and such that the upper surfaces of the pads are preferably substantially coplanar.

Distribution of power vias in a multi-layer circuit board *(Assignee: IBM Corp.) Patent No.– 14/717,026*. One aspect is a method that includes identifying, by a power via placement tool executing on a processor of a circuit design system, a source and a sink of a voltage domain of a multi-layer circuit board based on a design file defining a layout of the multi-layer circuit board. A number of power vias to support a maximum current demand from the source to the sink is determined. Positions of a plurality of the power vias are determined at locations of the multi-layer circuit board forming paths through the power vias between the source and the sink and having a substantially equal total path length.

Semiconductor package with high density die to die connection (Assignee: Qualcomm Inc.) Patent No.– 9,595,494. A semiconductor package according to some examples of the disclosure may include a substrate having a bridge embedded in the substrate, a first and second die coupled to the substrate, and a plurality of electrically conductive bridge interconnects in the substrate coupling the bridge to the first and second die. The plurality of electrically conductive bridge interconnects may have a first bridge contact layer directly coupled to the bridge, a first solder layer on the first bridge contact layer, a second bridge contact layer on the first solder layer, a second solder layer on the second bridge contact layer, and a die contact directly coupled.

Binghamton University *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications.* ◆

continued from page 34

product needs to incorporate the phases of product acceptance into their plan and implement a supply chain to accomplish these demands. Many of us have heard the horror stories of landfill sites filled with unsold Atari games. Neither large nor small companies are immune from excitement bubbles. This excitement is best calibrated by external experts.

Regulatory requirements need to be considered from the very start of any product. Consider the medical device market: the FDA has stringent requirements for design documentation. If these are ignored early on with the thought that they can be "back filled", it can mean expensive and time consuming re-engineering of documentation and testing. A consulting FDA specialist can help establish the proper processes and documentation to enable timely submission and approvals and/or clearances by the FDA. Start-ups may be advised to use existing certified manufacturers to avoid costly non-compliance issues.

Standard operating procedures are not first and foremost in the thoughts of founding individuals of the company. Yet, standard operating procedures and Quality Management programs refined for the particular company are essential. Trying to establish these later can mean more complex procedures and compliance fixes. If established early and designed for use specific to the company, these procedures can operate seamlessly, interwoven into daily activities.

The complexities mentioned above can be simplified and risks mitigated by employing the right talent at the right time. This talent can be utilized on an as needed basis without building a cumbersome infrastructure of personnel. An organization of professional consultants such as the IEEE Consultants Network of Silicon Valley (IEEE-CNSV, California-Consultants.org) is one way to find the talent needed. It consists of individual consultants with a myriad of talents. These groups offer a searchable resource for the correct experts for the tasks. They are also a network of individuals capable of aligning experts in other areas outside their expertise. Consulting resources are one of the best answers for emerging technologies and markets. ◆

Advanced Packaging Technologies Get Reliability Boost from NCF Material

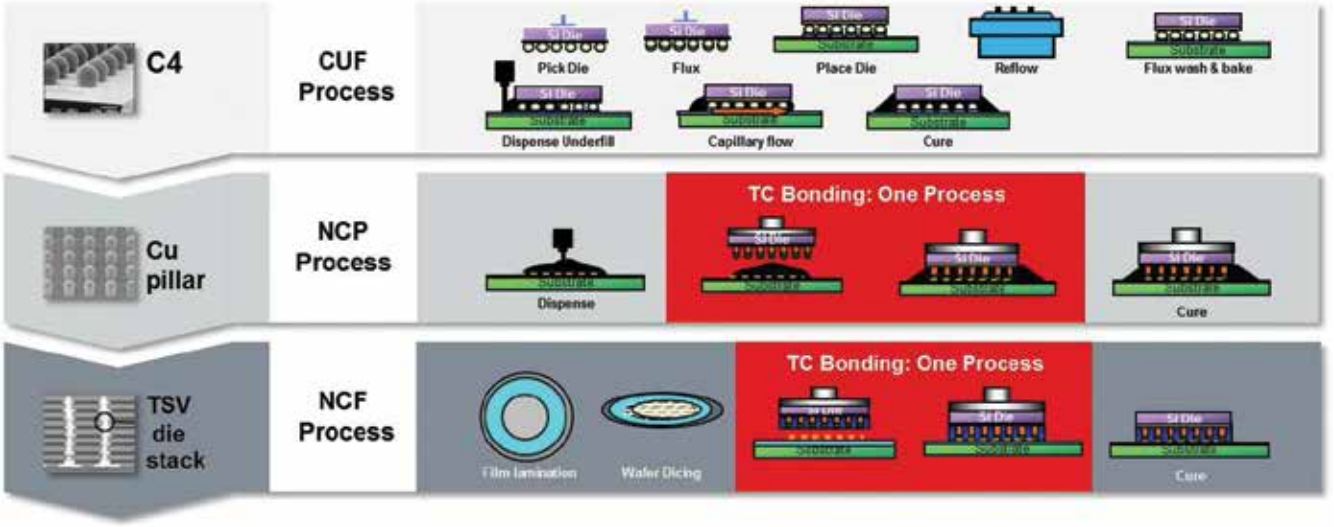
Rose Guino, Henkel Electronic Materials LLC

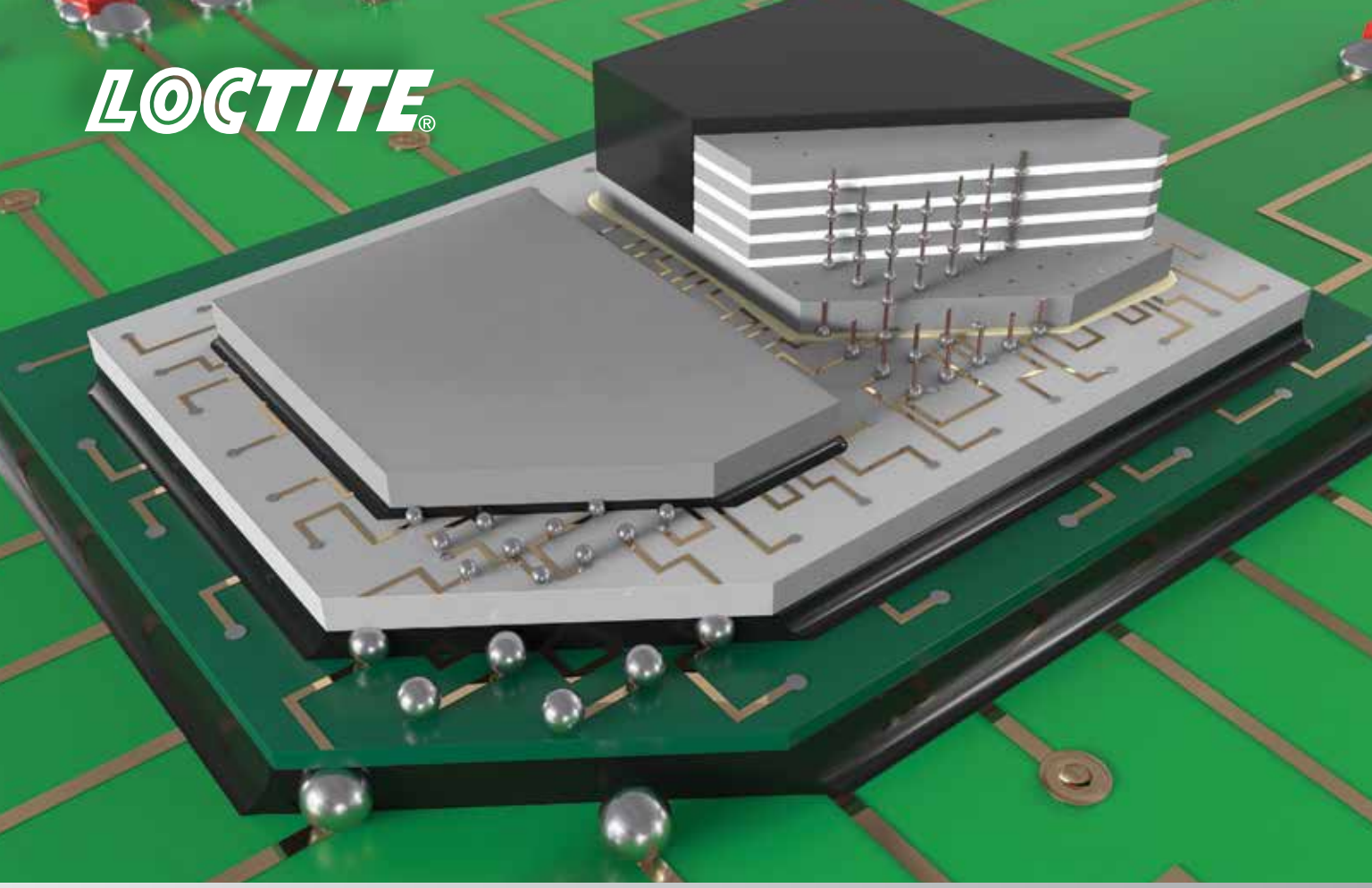
THE PAST DECADE HAS WITNESSED dramatic growth in mobile and computing technology, a market dynamic that has driven the development and adoption of various interconnect solutions. Traditionally, transistor scaling has been the technique used to advance form and function, but this method has become increasingly challenging and costly. Therefore, many device designers are considering new advanced packaging techniques to address the continued requirement for high performance and increased functionality. Modern package designs include increased I/O, system-in-package and higher interconnect densities, among others.

As newer packages become thinner and smaller with more I/O for greater function, ensuring the reliability of the designs becomes essential to long-term performance. Stress management and structural bump protection are critical factors, as chips are more fragile than ever with lower silicon nodes and ultra-low dielectric layers. Wafers and dies with through silicon vias (TSVs) are thinner to accommodate 3D stacking and thinner substrates are already available, making handling and warpage control more challenging. Achieving higher functionality for a given die size has also given rise to copper (Cu) pillar technology. This technique allows designers to place Cu pillar bumps in higher density, enabling increased I/O and utilizing wafer functionality. But, like other challenging designs, Cu pillar bump pitches of less than 50 µm and narrow sub-40 µm bondline gaps make conventional bump protection methods increasingly problematic. Traditional capillary underfills (CUFs), for example, are hard-pressed to flow in and around the tight dimensions. Because flux cleaning under the tight spaces is also challenging, underfill compatibility with flux residues is a growing concern. In addition, new substrate solder mask designs such as partial or full solder mask openings (SMOs) are making the underfill process more complex and void-prone due to the added substrate topography.

Because of these realities, non-conductive paste (NCP) and non-conductive film (NCF) – also referred to as wafer-applied underfill (WAUF) – materials have emerged as the most reliable underfill solutions for Cu pillar and TSV packaging approaches. Both NCP and NCF materials offer excellent bump-pad alignment accuracy through thermal compression bonding, as shown in the process diagram below.

In the memory market, however, where 3D TSV stacking applications have evolved into the dominant packaging technique, TSV die applications less than 100 µm thick are challenging for thermal compression bonding of paste materials. Because of the potential for die top and bonding tool contamination with NCPs, packaging specialists have moved toward the use of NCF for die structures – including TSV and Cu pillar – where more controlled flow and fillet formation are required. As illustrated in the diagram on page 32, the NCF is applied via lamination and not only protects the bumps on





NON CONDUCTIVE FILM

Advanced Packaging Technologies Get Reliability Boost From NCF Material

Today's smaller footprint, greater I/O package designs dictate use of emerging technologies like through-silicon via (TSV) and copper pillar to address form factor requirements. With this come thinner dies for 3D stacking and higher-density bump, driving the need for greater protection to ensure reliability. In the memory market, where TSV applications with die less than 100 µm thick are common, Henkel's new non-conductive film (NCF) technology provides controlled flow, stability and protection without the concerns associated with paste-based underfill materials and challenges posed by thermal compression bonding.

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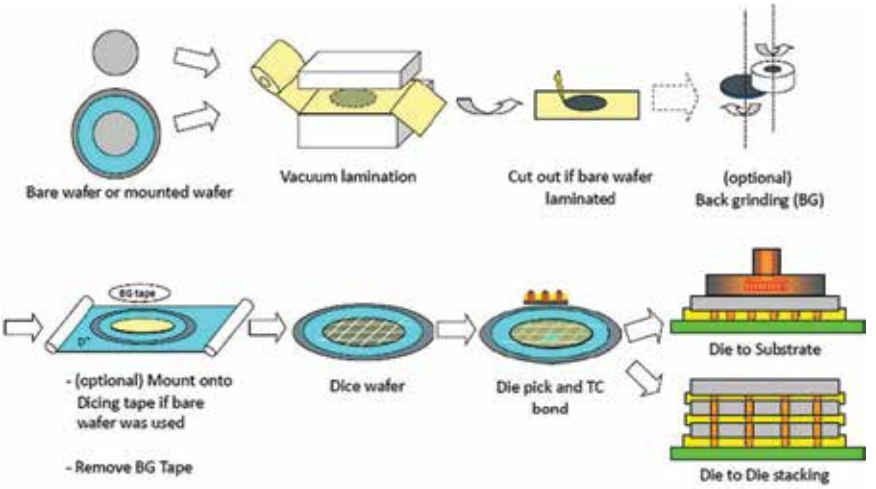
the wafer, but also serves as additional support for wafer handling and successive processing. Bump protection is achieved immediately following thermal compression bonding, and die stacking of TSV dies is highly viable.

The latest NCF material to be introduced to market is a 2-in-1 wafer-applied underfill film from Henkel. Henkel's NCF has been developed to facilitate die processing for die that are less than 60 µm thick and, as compared to previous generation materials, the new NCF has a long work life of 8 weeks; 6 weeks with the backgrinding tape and an additional 2 weeks once the backgrinding tape is removed. Not only does the backgrinding tape facilitate wafer thinning when required, it also delivers handling stability and enables complete NCF gap filling and coverage for maximum bump protection. The material has lower melt viscosity which allows for lower bond force processing, exceptionally fast three-second cure, a four-month shelf life and no outgassing during processing. Henkel's NCF has been designed to balance flow behavior and cure



kinetics to achieve good joints without entrapment or solder extrusion, provide good fillet coverage and complete gap filling.

In addition to all of the performance and reliability benefits afforded by NCF, film-based materials are ideal for the requirements of memory chip processing and, even for non-memory applications, enable the close placement of die, which is not achievable with paste-based materials. As the industry moves toward more challenging designs and 3D integration, advanced materials such as Henkel's new non-conductive film will be essential for robust wafer processing and long-term package reliability.

Email rose.guino@henkel.com for more about NCF benefits. For Henkel info visit www.henkel.com/electronics. ◆

IP PROTECTION

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entire world. Trade secrets can be legally protected as long as they are not widely known and give a business advantage as long as the trade secret owner and any business "partners" licensing the trade secret make strong efforts to maintain the confidentiality of the trade secret. There is no time limit to trade secret enforcement and some trade secrets have been kept confidential for centuries. Since trade secrets are confidential by their nature, there is far less danger of trade secret theft than the deliberate infringement of a patent by a "non-partner" competitor anywhere else in the world. Trade secrets can be defended in courts around the world without the requirement that a patent application be filed and a patent obtained in each and every country where the inventor wants to legally protect their invention.

The biggest drawbacks to trade secrets are that the reverse engineering or the independent discovery of a trade secret are legal and either of these events gives the discoverer the right to implement the trade secret. However, it is still possible to actually make reverse engineering of a trade secret very difficult in many cases, and it is also still possible that independent discovery of a trade secret may not actually happen for many years. Examples that come to mind in IC packaging would be the chemical compositions of mold compounds or the protective measures used to prevent mold bleed on lead-frames.

The licensing of trade secrets is possible. And trade secrets also offer an advantage over patents for the licensing of inventions. The licensing of patents has the drawback that since a patent is published and can be read by competitors around the world, patent infringement of valuable patented inventions is far more likely that infringement of a confidential trade secret - that can only happen by trade secret theft, independent discovery, or reverse engineering. This reduced risk of infringement of an invention that would otherwise require expensive legal patent litigation expense can make a trade secret more practical and more desirable than a patent to a potential licensee.

It is possible that a second entity may ultimately discover a trade secret invention and file a patent application for it, but if the original trade invention owner can prove commercial use of the trade secret invention before the date that the second entity filed a patent application, then any patent obtained by the second entity can be invalidated on these legal grounds as well as all the other available legal grounds for patent invalidation. And as a practical matter, if the trade secret was well hidden by the original entity to avoid detection or reverse engineering by anyone else, infringement of a later patent by the original entity may likely never be asserted by the second entity.

The scope of inventions in the IC packaging world that can be protected as trade secrets is quite large. And there are several techniques to make the reverse engineering of trade secrets difficult. Even inventions that at first sight appear to be impractical candidates for trade secret protection, can with imagination and skill, be hidden and legally maintained as trade secrets. ◆

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Bridging the Gap

Dennis Falkenstein, President, iOnTrends, Inc.
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YOUR PROJECT DUE DATE IS approaching and now your team tells you they have encountered problems. This is a familiar situation to everyone who has been involved in a technology and resource challenged environment. The demands are escalating as cost containment and speed to market are competitively driven. As engineers push the envelope there is often the need for a "help button" or YouTube "how to do it" equivalent. But, of course, these problems would never reach the manager if it were this easy.

The demand for external consultants is growing as evidenced by reports from Technovia Consulting and others. Companies are reluctant to add full-time personnel even if they are experiencing growth. They may not be bullish on the continued growth and opt to take a temporary resource measure. This temporary resource may include consulting personnel. Why consultants? The best answer is cost effective and successful results. It is a way to minimize the potential risk that managers and companies encounter.

Let's examine some of the strategies that provide cost effective results. First, an experienced individual can be brought on board without the normal hiring delays of searching and attracting someone from an existing position at your competitor or a similar industry. Hiring a junior employee does not assure the desired experience and thus adds a delay for training. They may not bring domain knowledge with them and certainly have no concept for the emerging trends of your industry. The consultant can be contracted without the fear of leaving for a competitor and is exempt from the employee benefits package. The budgetary or salary guideline restraints tend to make it very difficult to hire experienced personnel.

A consultant can be hired with more credible references; human resource laws usually discourage companies from providing a negative reference on previous employees. However, a consultant can provide references based on contracted results. Hiring a consultant usually does not threaten current full-time employees. If the consultant is a consideration for long term employment, they can first prove their capability and chemistry with other workers.

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The consultant can be focused on a specific project and therefore is less likely to be diverted by other activities or company personnel issues. Many times engineers can be diverted from new design projects to solve service or manufacturing issues. Conversely, consultants with experience in older technologies can solve problems faster and more effectively with the company's legacy products. This relieves the company engineers to work on new, more motivating, projects. Likewise, new products may have to interface or upgrade older legacy products. Consultants with knowledge of older technologies can help to strategize transition and design specifications to new technologies more smoothly.

Consulting personnel are not just for the immediate fixes as in the opening paragraph of this editorial. Companies are taking advantage of consulting professionals for co-creation of managerial and strategic plans to gain external knowledge. These co-creative ventures include everything from market analysis and product definition and launch up to C-level forecasting and budgeting. Consultants can offer unbiased and experienced input for company executives while ensuring confidentiality. This can be very important to minimize day to day operational disruption.

The competitive environment and emerging disruptive technologies require outside influence from leading consultants. Artificial intelligence, big data, Blockchain security, and IoT compatibility are a few of the game changing catalysts that cannot be ignored. Companies need robust strategies to implement solutions in this new environment.

Many consultants have also worked for startup companies as well as having large corporate experience. The startup experience can mitigate many risks of the unknown when entering new and existing markets. Company founders can be overly convinced of their perceived superior concepts. While budding enthusiasm is great, grounding in reality is critical when pursuing funding. It is imperative that the milestones established in the funding process be realistic and achievable with the estimated resources. Too many companies "burn" through funding faster than planned. No investor wants to see their initial investment become diluted by desperate requests for additional funds to meet the original goals.

The founding technical experts in a startup need to incorporate the intricacies of "going to market". The best conceived

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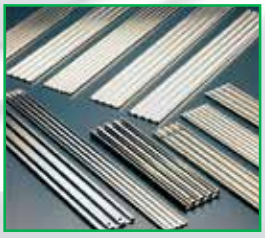
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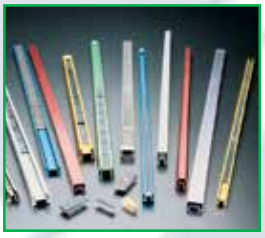
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