MEPTEC Report

WINTER 2015

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 19, Number 4

14th ANNUAL MEPTEC

MEMS TECHNOLOGY SYMPOSIUM

Advancing MEMS and Sensors for Today's Exploding Demands

Wednesday, May 11, 2016
San Jose, California

page 22

+

The Great Miniaturization Symposium Follow-Up

page 15

MEPTEC MEMBER COMPANY PROFILE

Now in its 43rd year, SHENMAO TECHNOLOGY INC., the leading solder material provider globally, started by manufacturing resin flux cored solder wire and solder bar in 1973 at its Taiwan Headquarters, continuously expanding since 1998 to 10 worldwide locations.

page 18

INSIDE THIS ISSUE

ASE GROUP

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The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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ON THE COVER

MEPTEC presents its 14th Annual MEMS Technology Symposium titled "Advancing MEMS and Sensors for Today's Exploding Demands" on Wednesday, May 11 2016 at the Holiday Inn - San Jose Airport in San Jose, California. Invited speakers will focus on the fundamental MEMS technologies and manufacturing techniques to address this explosive growth short to medium term, but also take a peek at what's coming longer term that we all need to be aware of today.

HENKEL APPOINTS HANS VAN BYLEN TO SUCCEED KASPER RORSTED AS CEO

Hans Van Bylen

Henkel has announced that CEO Kasper Rorsted, who has decided not to renew his current contract beyond 2017, will leave the company at his own request as of April 30, 2016. He served on the Henkel Management Board for 11 years, thereof 8 years as CEO. Effective May 1, 2016, Hans Van Bylen has been appointed as his successor. His successful career at Henkel started in 1984 and he has served as member of the Management Board since 2005. The appointment to CEO this spring will enable him to lead the development of the new strategy which Henkel will announce at the end of this year and drive its successful execution.
www.henkel.com

ALTERA'S NEW QUARTUS PRIME DESIGN SOFTWARE EXTENDS LEADERSHIP IN DESIGN PERFORMANCE AND PRODUCTIVITY

Signaling a new era in design productivity for a new generation of programmable logic devices, **Altera Corporation** has released the Quartus®

SHENMAO Introduces PF606-P133 Solder Paste for Laser Soldering

SHENMAO PF606-P133 Solder Paste is designed for selective laser soldering on tiny solder joints (1.5mm or smaller), especially on expensive, temperature-sensitive components and assemblies. In the past, such a small solder joint is not suitable for standard reflow processes and has to be soldered manually. With PF606-P133 Solder Paste, automatic laser soldering can easily be accomplished.

Within only several seconds of heating after dispensing, solder joint is well-formed with minimal flux residue and without splash or solder ball. Process time can be greatly reduced with extremely high yield rate.

PF606-P133 is approved by world leading electronic component manufacturers.

For more information, contact SHENMAO America at 408-943-1755, e-mail usa@shenmao.com, or visit www.shenmao.com. ◆

SMART Microsystems Now ISO 9001 Certified

SMART MICROSYSTEMS, located in Northern Ohio, creates turn-key solutions for microelectronic package assembly challenges to move MEMS sensor technology from development to production. As a newly certified ISO 9001 manufacturer, SMART Microsystems incorporates design-for-manufacturing into the initial stages of development. By working concurrently with their customer's design team and suppliers they are able to implement process specifications, design-to-cost goals, and on-time delivery objectives efficiently, reducing overall time and cost.

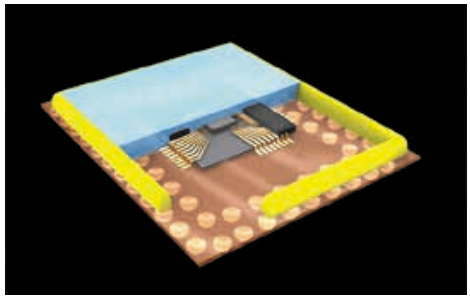
More information about SMART Microsystems capabilities and services is available at www.smartmicrosystems.com. ◆

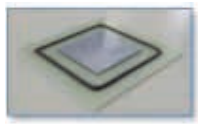
NAMICS Corporation Develops Improved Dam-and-Fill Encapsulants

NAMICS CORPORATION HAS DEVELOPED an epoxy dam material (CHIPCOAT G8345D) and an accompanying epoxy fill material (CHIPCOAT G8345-6) for the semiconductor market. Dam-and-Fill materials encapsulate your wire bonded device as an electrically insulating material. Dispensing a high-viscosity dam followed by a low-viscosity fill, will create a completed encapsulated package for your CSP and BGA. CHIPCOAT G8345D and G8345-6 are fast curing, low CTE (low stress), offer high package reliability and reduced warpage.

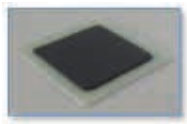
CHIPCOAT G8345D and G8345-6 are in full production and are available for sampling. Standard packaging is frozen syringes with 50 grams in a 30cc syringe; larger cartridges are available.

NAMICS CORPORATION is a leading source for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Singapore, Korea, Taiwan and China,





G8354D (Dam)



G8345D & G8345-6 (Dam & Fill)

NAMICS serves its worldwide customers with enabling products for leading edge applications.

To find out more about these NAMICS Dam-and-Fill materials, please visit www.namics.co.jp/e/product/chipcoat04.html or contact your local NAMICS sales representative. ◆

InvenSense Announces Sensor-Based SaaS Fitness Tracking Platform For Mobile and Wearable Application Developers

Coursa Sports Employs Sensor Enhanced Positioning and GNSS Duty-Cycling to Provide More Accurate Speed, Distance and Route Tracking at Reduced Power Consumption

INVENSENSE, INC., A leading provider of MEMS sensor platform solutions, announced Coursa Sports, a cloud-based Software as a Service (SaaS) fitness tracking platform for smartphone and smartwatch health and fitness applications. The platform is designed to provide more accurate and always available speed, distance, and route tracking and at least a 3X improvement in relative elevation reporting for walking, hiking and running at up to 50% reduced power consumption. Coursa Sports is comprised of an SDK for integration into a mobile application and a cloud server. Mobile and wearable application developers can download the Coursa Sports SDK today from www.coursasports.com.

As use of mobile fitness applications increases, so does the expectation of battery efficiency and accuracy enabling users to get full credit for their exercise sessions. Most fitness apps use GNSS (such as GPS) to track the speed, distance and route of activity. However, on forest running trails or in deep urban canyon environments, GNSS can be inaccurate or unavailable, resulting in lost or inaccurate fitness data.

The Coursa Sports SDK uses advanced algorithms that take sensor data from the mobile device gyroscope, accelerometer, and barometric pressure sensor to generate an inertial tracking data flow that is combined with GNSS data. The addition of the inertial tracking system, together with GNSS, improves customer experience by increasing the continuity and accuracy of the fitness data when GNSS signals are weak or unavailable.

Coursa Sports improves mobile device battery life by up to 50% during workouts by frequently turning GNSS off (duty-cycling). During duty-cycling, the lower power sensors are used to track fitness data at the same accuracy as GNSS. This feature extends battery life during fitness tracking, and enables developers to migrate their smartphone apps to smartwatch devices, where smaller batteries and the high power consumption of GNSS previously prohibited fitness tracking use cases.

"InvenSense has made significant investments in human context and location tracking algorithm development to serve our OEM customers," said Eitan Medina vice president marketing and product management, InvenSense. "Now, for the first time, we are enabling application developers to take advantage of these technology advances in their apps. Coursa Sports is the first commercially available SDK and SaaS platform designed to help fitness and health application developers provide more accurate and reliable fitness metrics to their customers through the use of MEMS inertial sensor data."

The Coursa Sports SDK supports iOS, Android and Android Wear platforms. More information is available at www.coursasports.com or contact InvenSense Sales at sales@invensense.com. ◆

Prime design software. Altera's new software environment builds upon the company's proven, user-friendly Quartus II software and incorporates the new productivity-centric Spectra-Q™ engine. The new Quartus Prime design software is optimized to enhance the FPGA and SoC FPGA design process by reducing design iterations, delivering the industry's fastest compile times, and accelerating silicon performance.
www.altera.com

ASE RECEIVES 2015 BSI GRC AWARD

ASE announced that it has received the BSI (British Standards Institute) 'Inclusive Green Growth Award' and the 'GRC (governance, risk management and compliance) Award'. This is the fourth year in a row since 2012 that ASE has received recognition from the BSI Group Taiwan. The BSI Group, also known as the British Standards Institution, is a business standards company that develops standards and provides its services to companies to improve performance, reduce risk and achieve sustainability.
www.aseglobal.com

DCG SOLVES LOCALIZATION OF ELECTRICAL SHORTS WITH EBIRCH™ TECHNOLOGY

In conjunction with the 41st International Symposium for Testing and Failure Analysis (ISTFA), **DCG Systems** announced the release of EBIRCH™, a new, unique technology for localizing shorts and other low-resistance faults that may reside in the inter-

Infineon OPTIGA™ TPM Chips Protect Latest Microsoft Surface Devices

MICROSOFT puts emphasis on hardware based security to protect sensitive user data stored on connected devices. The company integrates OPTIGA™ TPMs (Trusted Platform Modules) from Infineon Technologies AG into its latest personal computing devices. Among these are the new Surface Pro 4 tablet and the Surface Book, the first Microsoft branded laptop.

TPMs are dedicated security chips to store sensitive data such as keys, certificates and passwords separated from the main processor. This increases protection of the computing device from unauthorized access, manipulation and data theft. For example, the key and password of the Microsoft BitLocker Drive Encryption application are securely stored inside the TPM.

Infineon is recognized as the world's leading supplier of security solutions for Trusted Computing. Microsoft's personal computing devices rely on the OPTIGA™ TPM SLB 9665, the industry's first certified security controller based on the latest TPM 2.0 standard. This standard was defined by the Trusted Computing Group (TCG), an international standardization group with members such as Intel and Google. TPM 2.0 specifications are based on most advanced cryptography and security mechanisms. In addition, they particularly address mobile computing such as notebooks and tablets as well as IoT devices with special security requirements. ◆

FINEPLACER® Coreplus BGA Rework Station

The FINEPLACER® coreplus is a dedicated rework system that offers a level of professionalism that exceeds its attractive price. The system offers Finetech's long proven rework technology for a wide spectrum of SMD components, ranging in size from 01005 to 90 mm x 90 mm.

The FINEPLACER® coreplus meets the needs of single system, high mix rework, or multiple system production environments where process portability and reproducibility is crucial.

Visit www.finetechusa.com for more information. ◆

Promex Industries, Inc. Hires Rosie Medina as Director of Sales and Marketing

Former Med Tech Business Development Director Joins Silicon Valley EMS to Promote Contract Manufacturing Services for Medical and Bioscience Products

PROMEX INDUSTRIES Inc., an electronic manufacturing services (EMS) provider that integrates conventional SMT with semiconductor microelectronic packaging and assembly, has hired Rosie Medina as its new director of sales and marketing.

Formerly the director of medical technology business development at CORWIL Technology (Milpitas, CA), Ms. Medina has close to 30 years of experience in the semiconductor industry. She has worked with a variety of companies around the world, ranging from new startups to major corporations in the commercial, medical, and mil-aero markets.

"Rosie knows what it takes to fast track new medical and bioscience products from prototype to volume production," said Promex President and CEO Richard Otte. "She understands the importance of quality and repeatable processes in PCB assembly – especially for Class III implantable devices and other complex multi-technology medical devices. Her skills in business development, sales and marketing in the contract manufacturing sector position her well to lead the Promex sales team."

In her new position, Ms. Medina will be responsible for supporting the rapid growth of Promex by enhancing sales, marketing and customer support, among other responsibilities. Ms. Medina will also work closely with executive management on new strategic engineering and manufacturing initiatives.

Founded in 1975, Promex Industries Inc. provides a broad range of assembly services to the medical, bioscience, commercial semiconductor and military markets.

More information is available at the Promex website www.promex-ind.com or by calling +1-408-496-0222. ◆

Amkor Technology Announces Acquisition of Remaining Shares of J-Devices

AMKOR TECHNOLOGY INC., A LEADER in semiconductor packaging, assembly and test services, has announced that on December 30, 2015, it increased its ownership interest in J-Devices Corporation from 65.7% to 100% through the exercise of previously disclosed options.

"Amkor will consolidate the financial results of J-Devices beginning in 2016, initially adding about $800 million of annual revenue to our top line," said Steve Kelley, Amkor's president and chief executive officer. "This transaction cements Amkor's position as the world's second largest OSAT, well ahead of the next two players. We also become the largest OSAT for the automotive market, with roughly $750 million in combined automotive-based revenues in 2015."

"Fully combining J-Devices and Amkor is the logical next step in our joint venture relationship that was begun more than six years ago," said Yoshifumi Nakaya, J-Devices' chief executive officer. "We are fully committed to our customers in Japan, and we see exciting opportunities to expand our business worldwide by capitalizing on our leadership position in automotive ICs."

J-Devices is the largest OSAT in Japan and the sixth largest in the world. For the 12 months ended September 30, 2015, J-Devices generated revenues of $832 million, EBITDA of $113 million and net income of $26 million.

Amkor Technology Inc. is one of the world's largest providers of semiconductor packaging, assembly and test services. Founded in 1968, Amkor pioneered the outsourcing of IC assembly and test and is now a strategic manufacturing partner for more than 250 of the world's leading semiconductor companies, foundries and electronics OEMs. Amkor's operational base encompasses more than 7 million square feet of floor space with production facilities, product development centers and sales & support offices located in key electronics manufacturing regions in Asia, Europe and the USA. For more information visit www.amkor.com. ◆

connect structures or the polysilicon base layer of integrated circuits. Named for Electron Beam Induced Resistance Change, EBIRCH offers fault analysis (FA) engineers and yield experts the ability to detect and isolate low-resistance electrical faults without resorting to brute-force binary search approaches that rely on successive Focused Ion Beam cuts. Its unparalleled ability to quickly isolate low-resistance faults enables EBIRCH to boost the success rate of physical failure analysis (PFA) imaging techniques to well above 90%, accelerating time-to-results and establishing the FA lab as a critical partner organization in solving yield and reliability problems. *www.dcgsystems.com*

UTAC AND MCUBE ANNOUNCE PRODUCTION RAMP OF MEMS 3-AXIS ACCELEROMETERS

UTAC Holdings Ltd. a Singapore-based semiconductor assembly and test services provider and **mCube, Inc.**, provider of the world's smallest microelectromechanical systems (MEMS) motion sensors have jointly announced the successful qualification and production ramp of mCube's new MEMS 3-axis accelerometers in small packages ranging from 2x2 mm to 3x3 mm at UTAC's Thailand factory. These accelerometers feature mCube's monolithic single-chip motion sensor technology which enables small die size, ultra-low power consumption, and high-performance inertial sensors. These sensors

are optimized in a portfolio of products that are specifically targeted for mobile phones, wearables, and IoT devices.
www.mcubemems.com
www.utacgroup.com

STATS CHIPPAC RANKED IN TOP 10 SEMICONDUCTOR EQUIPMENT MANUFACTURERS BY IEEE FOR PATENT INNOVATIONS

STATS ChipPAC Ltd. has announced that it has been ranked among the world's top 10 semiconductor equipment manufacturing companies in the 2015 Patent Power Scorecards published by the Institute of Electrical and Electronics Engineers (IEEE). This is the sixth consecutive year that STATS ChipPAC has been recognized in the annual scorecards.

STATS ChipPAC was ranked seventh in the Semiconductor Equipment Manufacturing category. This is the highest ranking ever received by an Outsourced Semiconductor Assembly and Test (OSAT) provider.

In August 2015, Jiangsu Changjiang Electronics Technology Co. Ltd. ("JCET") acquired the entire shareholding of STATS ChipPAC. With over 1,500 patents issued by the USPTO as of the end of 2015 and 784 patents granted by the State Intellectual Property Office of China, the JCET Group has a combined IP portfolio that is unmatched in the OSAT industry with a deep knowledge base that provides a powerful competitive advantage for customers in the marketplace.
www.statschippac.com
www.cj-elec.com ◆

11th Annual Global Technology Awards

GLOBAL SMT & PACKAGING SUCCESSfully held the 11th Annual Global Technology Awards at Productronica 2015 in Munich. The star-studded event featured the very latest innovative products produced by suppliers of EMS manufacturing equipment and materials over the last 12 months. Videos describing the winning products and why their product stood out compared to the other entries was played during the presentation ceremony.

The Global Technology Awards are held annually and rotate every second year between Productronica, Germany and SMTAi, USA. Next year, the awards contest will accept entries from March 1st, 2016.

The awards ceremony will be held at SMTAi in Chicago, USA on Tuesday, September 27th, 2016. For further information, please visit http://globalsmt.net/global-technology-awards/ ◆

Category	Winning Company	Winning Product
Adhesives/Coatings/Encapsulants	YINCAE Advanced Materials LLC	SMT 256
Assembly Tools	Panasonic Factory Automation	Multi-recognition camera
Best Manufacturers Rep/Distributor	Horizon Sales	David Trail
Best Product – Asia	MIRTEC	MV-6 OMNI 3D
Best Product - Europe	GEN 3 Systems	GM Series of Contaminometers
Best Product - Americas	Indium Corporation	InFORMS®
Bonding Equipment	Nordson DAGE	4800 Bondtester
Cleaning Materials	Kyzen Corporation	AQUANOX® A4708
Contract Services $25 - $50 Million	Computrol	Contractor
Dispensing Equipment	Nordson ASYMTEK	Spectrum II with tilt & rotate
Environmentally-friendly Products	CAMTEK	Gryphon SL
Inspection - AOI	Cyberoptics	SQ3000™ 3D AOI System
Inspection - SPI	Test Research Inc	TR7007Q 3D Solder Paste Inspection System
Inspection - x-ray	ViTrox	V810 S2EXi In-line 3D Advanced X-Ray Inspection system
Placement - high Volume	ASM Assembly Systems	SIPLACE TX
Placement-low to medium volume	Mycronic AB	Agilis Smart Bin System
Printing Equipment	ITW Speedline	MPM Edison
Programming	Data I/O	LumenX
Rework and Repair	METCAL	Scarab Site Cleaning System
Software - Process Control	JUKI and Cogiscan	JUKI Line Solution Software
Software - Production	MIRTEC and YXLON	Smart Loop
Solder Paste	Henkel	GC10
Soldering Equipment	kurtz ersa	SMARTFLOW 2020
Stencils, Nano coatings	FCT Companies	Nanoslic
Storage Systems	Totech Super Dry	Dry Tower
Test Equipment	VJ Electronix	XQuick
Test Services	Datest	Datest Reverse Engineering Service
Editor's Choice Award	JUKI and ESSEGI	JUKI and Essegi Storage Soltions

INDUSTRY INSIGHTS

By Ron Jones

Who's Next on the Dance Floor

IF IT SEEMS LIKE YOU'RE HEARING a lot of talk these days about mergers and acquisitions in the semiconductor industry, it's not your imagination. There has been an explosion in level of activity and there is no sign of things slowing down as we approach the end of 2015.

According to IC Insights, the average M&A for the years 2010-2014 was $12.3 B. In the first half of 2015, they report we have already reached $72.6 B, roughly 6x the previous annual average. Reuters has reported more than $80B through September and there are estimates that the year may hit $100-120 B when the final buzzer sounds.

Year	Semi M&A
2010	$ 7.7 B
2011	$ 17.0 B
2012	$ 8.5 B
2013	$ 11.5 B
2014	$ 16.9 B
2015 (1st half)	$72.6 B

Table 1. *(Source: IC Insights)*

Deals range in size from small (i.e. 10's of millions) to very large ($37 B for Broadcom). Avago alone has made four acquisitions (LSI, PLX, Emulex, and Broadcom) over the past couple of years that total $45 B.

Table 2 lists some acquisitions/mergers that have either closed or are well along in 2015. Some dates are closings, others are announcements and everything in between.

(Please realize that I am submitting this article in early December and you will be reading it in mid-February, 2016... a 75 day delay.)

There are other semiconductor companies that are surely on the radar screen for merger or acquisition. See Table 3.

A reasonable question would be why M&A activity in the industry has taken off like a rocket this year. To some degree, it is driven by trends that have been going on for years, such as the increasing cost of mask sets. It is not unusual for leading edge designs to run in excess of $100 million, and that is just for the masks. Many designs continue to go up in complexity, taking them beyond the technical reach of smaller fabless companies.

The Internet of Things (IoT) and other smart technologies are finally beginning to creep out of the shadows and toward the center of the radar screen for a lot of companies. It is not a matter of whether IoT will happen, but rather in what myriad configurations it will reveal itself and how quickly it will grow over the next several years.

Though IoT is currently small, many semiconductor companies have an eye on broadening their portfolio of products, technology and IP to position them for a market that is expected to experience rapid growth over the next five years. Having been in the industry for several decades and watching the fabless model create hundreds and hundreds of new companies over the past 25 years, it will be interesting to watch as consolidation reverses the trend to some degree with a growing number of mega fabless/IDM companies. Seems that our most consistent trend is change. ◆

Acquirer	Acquiree	Amount	Date
Avago	Emulex	$606 M	05/2015
Avago	Broadcom	$37,000 M	05/2015
Cypress	Spansion	$4,000 M	03/2015
Dialog	Atmel	$4,600 M	09/2015
Hua Capital	OmniVision Technologies	$1,900 M	6/2015
Intel	Altera	$16,700 M	10/2015
Lattice	Silicon Image	$600 M	03/2015
NXP	Freescale	$11,800 M	03/2015
ON	Fairchild	$2,500 M	11/2015
Qualcomm	Ikanos	$47 M	08/2015
Qualcomm	CSR	$2,400 M	08/2015
Uphill Capital	ISSI	$640 M	11/2015
Western Digital	SanDisk	$19,000 M	11/2015
Total		**$101,793 M**	

Table 2.

Potential Targets	Potential Suitors
PMC-Sierra	Skyworks and Microsemi are in play now
Maxim	TI, ADI, . . .
Lattice	Xilinx, Qualcomm, Marvell, Microsemi, . . .
Cavium	Intel, Qualcomm, Avago, Marvell . . .
Xilinx	
M/A-Com Technology	
Skyworks	

Table 3.

RON JONES is CEO of N-Able Group International. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Engineering: The Solution to Software Quality!

WHO IS AN ENGINEER? IN A RECENT Atlantic article, "Programmers: Stop Calling Yourselves Engineers", Ian Bogost argues strongly that software developers should not be called engineers based upon several factors including quality, professional licensure, and liability. Mr. Bogost includes examples of where software has failed even as it has become critical infrastructure. Having struck a nerve, there are several notable rebuttal articles and thousands of comments on the original article.

But instead of arguing over who should be called an Engineer or which honorific should be used for Mr. Bogost based on his doctorate in Comparative Literature, we should be asking the bigger question: **How can engineering solve software quality problems?**

Engineering is now practiced in far more areas than the classical dictionary list of endeavors that could be characterized as the engines of the Industrial Revolution. Wikipedia does a better job of describing what is built in terms of function than specific devices. As such it incorporates the essence of our current information technology revolution by including tools and processes.

What is common to both definitions of engineering is practicality, i.e. making something useful. The key to achieving practicality is to make sure that the true requirements are fully understood and the end result is tested against these requirements. **A good engineer takes the time to understand the true requirements** including transforming implicit assumptions into documented requirements.

At the same time, **quality is often stated as an expectation versus a measurable goal.** For example, Ford's now discontinued slogan of "Quality is Job 1" is meaningless without specific, measurable, achievable, realistic, and time based ("SMART") goals to implement it. Having meaningful goals allowed Ford to focus on the required transformations that positioned them well compared to their competitors.

Clearly there is a difference between a software developer who attacks a problem in a structured manner versus one who cobbles together something "quick and dirty" that "works". Using a structured process to ensure that all the requirements are addressed is the best engineering approach. Even though a "code sprint", often used by Agile methodology practitioners, allows for focused effort to make forward progress in code development, it is essential to know the destination and the requirements. There is no sense in "running" around and either missing the destination or solving the wrong problem, right?

Beyond a requirements issue, software has three unique aspects that are not present in tangible products that contribute to quality issues: **feature creep, perception of "simple" fixes, and scale.**

Off-the-shelf software is often selected on the basis of what it promises to do and not on reliability. So, product marketers continually identify new features to attract new users while the average user may use only a very small percentage of existing features. Even if you do know most of the features of a common program such as Microsoft Excel or Word, it is highly unlikely you regularly use more than a small fraction of these features. These extra features therefore "bloat" the software and may contribute to lower overall reliability due to the added complexity. And, of course, increased product complexity makes it more difficult to comprehensively test each new release of the software.

Unlike hardware, the "penalty" for fixing a bug in software at the first order level is minimal. A mistake in a semiconductor photolithography mask set could easily cost tens of millions of dollars to generate a corrected mask set. This cost is incurred before the actual production to replace the defective parts and before the costs to repair or replace the parts in end products. The actual cost of fixing a software bug? Simply the development and test teams' time to fix the error and retest the software release. And today's digital delivery requires no physical media. (This ignores the often-significant business costs of the software error, i.e. customer support costs, lost revenue due to time to market delay, etc.) Clearly the "stakes" are often much lower due to the low cost to repair software. Additionally, many web-based companies release new versions of their software daily eliminating the issue of infrequent or delayed update cycles.

Lastly, where hardware technology aims for very low – typically single digit part per million (ppm) - defect rates, these rates may be too "high" for Internet scale software. Facebook currently has over 1.4 billion monthly users so a 1 ppm defect could easily be seen by 1,400 users in a month. Internet scale applications like Facebook need extremely low defect rates on the order of 10 to 100's parts per billion (ppb) for critical functionality due to the multiplier of the number of users and transactions. Regardless of the actual defect rate, software defects are quickly exposed.

But are the software failures, especially those for "infrastructure" that Mr. Bogost finds the most alarming, a product of feature creep, simple fixes, or scale challenges? Clearly the defects are more visible when the scale of usage is very large. **However, there is more to the situation than just feature creep and "patch it later" mentality on the part of the software team responsible for these failures. It is corporate culture.**

Facebook's previous motto of "Move Fast And Break Things" was appropriate for the race to scale as quickly as possible to attract additional users and advertisers. This set the tone for their corporate hacker culture. To shift the culture to focus on how to do things more reliably at scale, especially in their core platform and services, Facebook changed their motto last year to "Move Fast With Stable Infra[structure]".

To do their job correctly – finding practical solutions that meet the business needs – **software developers need to fully comprehend the requirements and test the solution thoroughly against these requirements. And there must be a corporate culture that supports innovation and quality.** Arguing about whether programmers are true engineers will not solve the issues of quality. What is important is that the developers

think and are treated like engineers and that management assigns them clearly defined projects that don't easily change scope. (This implies a healthy relationship between marketing and engineering, which of its own, is a worthy discussion.) Let's focus on the corporate culture and not on job titles to improve the quality of software.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.

An Inside Look at the System-on-a-Chip (SoC) Market

Rich Wawrzyniak
Semico Research Corp.

THE SOC MARKET HAS BEEN growing and evolving for the last 15 - 20 years and is a very complex combination of semiconductor solutions that fills every possible niche in the electronics market today. Semico Research Corp. looks at this market on a regular basis and publishes research on its makeup, direction and evolution.

To get a better understanding of the SoC market, it is important to understand where it came from and what its roots are.

As Figure 1 shows, the origin of the ASIC market was the rise of what were called full custom designs in the mid-1970s. These devices were usually produced by large IDMs only for specific customers. In most cases, the customer supplied the design to the IDM. The customer consumed all the output of the IDM and used the parts internally. As the semiconductor market grew, new types of devices arose to help meet the needs of customers and markets alike.

Around 1980, the ASIC market fragmented into three basic types: Gate Arrays, Standard Cells and Programmable Logic. Later, as the demand grew for certain types of systems, the Application Specific Standard Product category arose. This class of device filled a gap between the three standard types of ASIC.

In the mid-1990s, the ASIC market again reached a point where the standard approaches for creating an ASIC were no longer satisfying customer or market needs, and another wave of innovation and fragmentation started with the advent of the SoC. From a single type of SoC, we now have moved to a market environment where it is possible for different types of SoC to co-exist to fill necessary market niches.

A major component of the SoC market is the use of 3rd Party Semiconductor Intellectual Property (SIP) and SIP that was created for reuse internally by the designers to be used in the creation of these designs. To track this market accurately, Semico has created a paper definition that details the three main classes of SoC in the market today. (see Figure 2)

The reason for the market evolution to create a separate SoC segment was to provide designers with more flexibility to

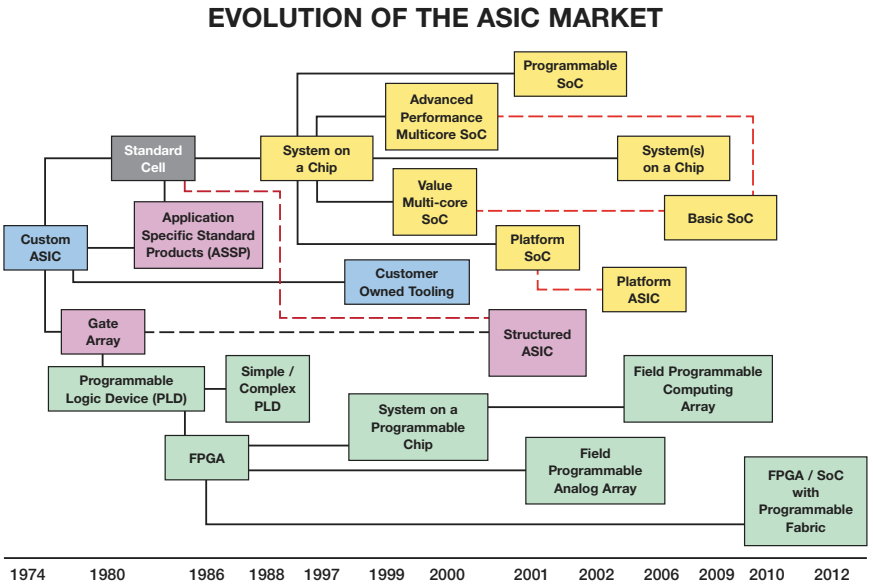


Figure 1. History of the ASIC Market. *(Source: Semico Research Corp.)*

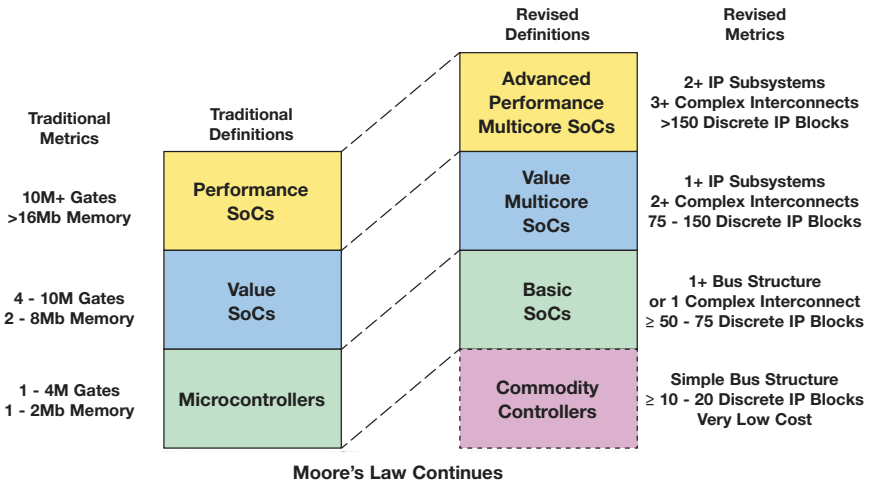


Figure 2. SoC Definition by Complexity. *(Source: Semico Research Corp.)*

aid in the creation of their silicon solutions. New market segments like mobile computing and communications, the Internet, wireless connectivity and now the emerging Internet of Things (IoT) all put new demands on designers to provide more functionality and richer feature sets to users of the devices. The 3rd Party SIP industry grew up to support these efforts, and that is why Semico created the definitions you see in Figure 2 – to provide a greater granularity in understanding the composition of the market and a way of easily separating one SoC type from another.

Revenue for this market will grow from $103.4 billion in 2015 to $192.0 billion by 2019, a CAGR (compound annual growth rate) of 13.2%. Over the next five years, higher revenues will continue to be driven by the following factors:

1. Many silicon solutions that previously used older design methodologies have switched over to using an SoC approach.
2. Many of the off-the-shelf 'catalog' parts found in the product portfolios of large IDMs (Independent Device Manufacturers) are using the SoC design methodology when they are refreshed by the manufacturers.
3. The drive to add connectivity to all mobile devices has pushed silicon designers to use the SoC approach to incorporate the necessary functionality through the use of 3rd Party SIP blocks.
4. The new capability and functionality found on mobile devices has caused the users of those devices to consume ever-greater amounts of bandwidth.
5. This has caused service providers of both wired and wireless solutions to increase the bandwidth available in their networks, and to choose the SoC methodology to meet the changing market requirements.

The net impact of these trends is to push both the revenues of SoC devices and the unit shipments of these devices to increased levels. Over time, the SoC design methodology will be responsible for the majority of the revenue in the integrated circuit portion of the semiconductor market.

Figure 3 looks at the revenue forecast for the three main types of SoC along with some of the more minor variants. The SoC type responsible for the largest revenue is the Advanced Performance Multicore SoC with the Value Multicore SoC in second place and the Basic SoC in third position. The Basic SoC category is going to be where most of the IoT solutions are going to reside and will exhibit the fastest growth rate over the forecast period. While the unit volumes projected for IoT are going to be very high, the ASPs of these devices will be fairly low compared to the other SoC types. This will act to hold down the overall revenues for the Basic SoC category compared to the other SoC categories.

The story of the SoC market is one of innovation and design expertise coming together to create new market segments and industries. The pace of market evolution is accelerating as new process geometries enter the market providing silicon architects with new tools and capabilities to fulfill ever more stringent end market requirements. While one can argue that the pace of evolution may slow down at some point, the profound impact of the various SoC product types on the semiconductor and electronics industries is indisputable and has been very positive. This is a trend that will continue for the foreseeable future. ◆

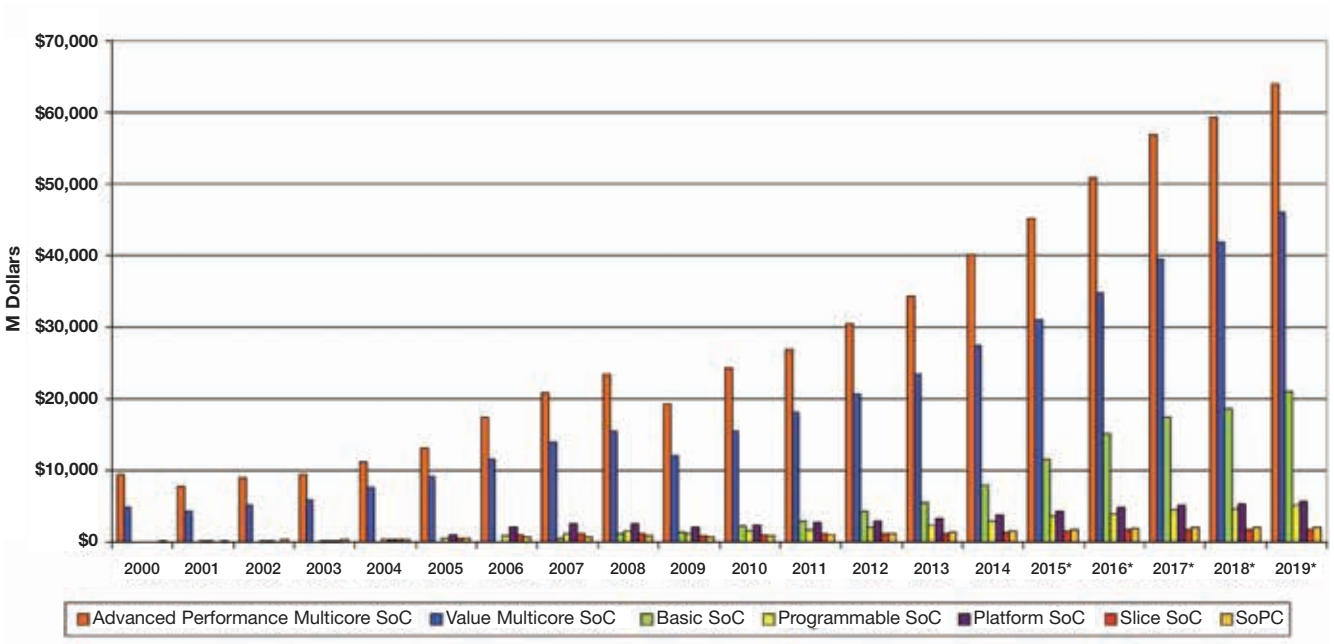


Figure 3. Worldwide SoC Forecast by Device Type. *(Source: Semico Research Corp.)*

THE GREAT MINIATURIZATION: SYSTEMS AND PACKAGING

Technology Enabling Systems in your Pocket and Beyond

Joel Camarda, SemiOps

I RECENTLY HAD THE PRIVILEGE of co-chairing the MEPTEC-SEMI symposium, November 10-11, along with Rich Rice of ASE. Our thanks to all our distinguished individual session leaders. They really did a terrific job recruiting all of our speakers and shaping the message of each session. Of course, a great thanks to our speakers, all recognized experts in their fields. For all involved, this means putting some time aside from their already busy schedules. In some cases, there is the added time and expense of travel. Herein is the most gratifying aspect of MEPTEC: recognized, accomplished professionals sharing their experience and expertise with colleagues, and, hopefully, the next generation of colleagues.

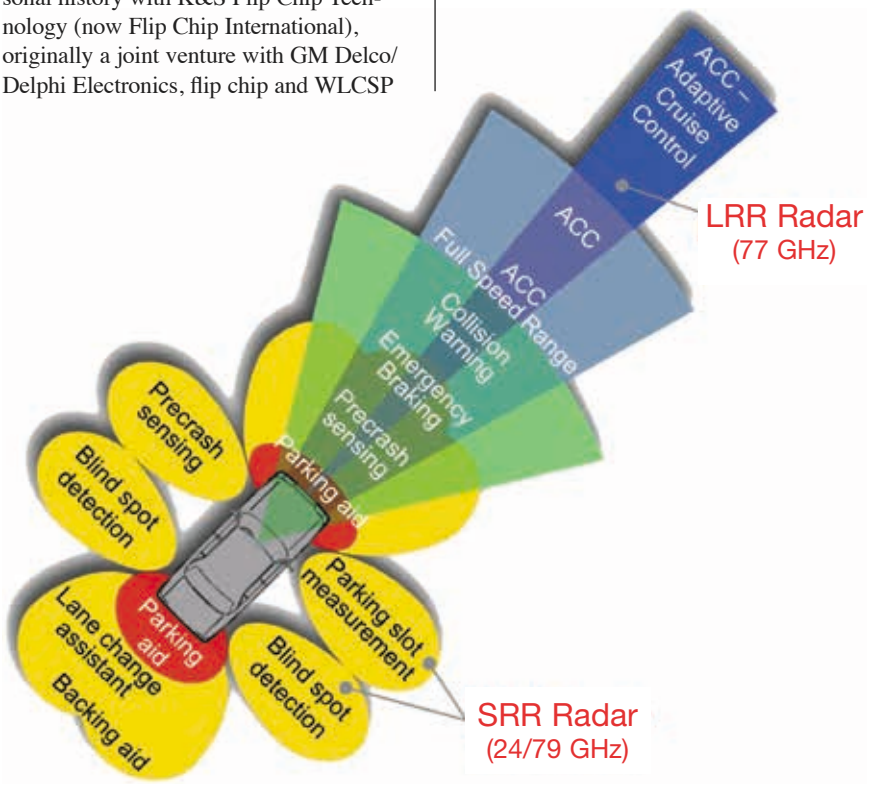
Our symposium this year, was subtitled "Systems in your Pocket" obviously borrowing from some popular acronyms, SOC, SIP, POP. We have embarked on a new level of electronics system personal mobility: a smart phone in your pocket; a smart watch on your wrist; a biomedical monitoring device inside your body; an infotainment system inside your automobile glove box; sensors and transmission devices in your automobile tires and under the hood; a driverless automobile (!); sensors in your clothing.

The advancement of IC device integration, Moore's law in silicon, is a significant factor. Fewer, smaller chips, have more functionality. However, as device geometries approach single atom thicknesses, Moore's law is losing some steam, and encountering more expensive barriers to entry of the next node. The next (or current) venue for Moore's law may well be packaging: multi-chip SiP, 2.5 D, 3D, TSV, etc. Frankly, some silicon level technologies do not always integrate well onto a single chip, at least not cost effectively: analog vs. digital; MEMS sensors vs. signal processing; power drivers vs. anything. More on this topic later in Ivor Barber's paper.

DAY 1

SESSION 1: The Genius of Cars – and Why Semiconductors Matter

Prasad Dhond, of Amkor Technology introduced us to some of the more stringent quality controls of package manufacturing for the automotive market. To my surprise, most of the Amkor automotive package manufacturing is wire bonded, and copper is well accepted. In my personal history with K&S Flip Chip Technology (now Flip Chip International), originally a joint venture with GM Delco/ Delphi Electronics, flip chip and WLCSP have been extensively used in automobiles. In more recent published papers, I have read that, for low lead counts, QFN-type packaging can be cost and profile competitive with WLCSP, especially if Cu wire is used. The automotive IC market is forecasted to reach $28 B in 2017, up from $19 B in 2012. Professor Rao Tummala, of Georgia Tech, presented *Systems Scaling A New Fundamental Electronics Frontier Technology*. From 1970 to 2010, silicon node scaling progress has outpaced system line spacing by 200 to 1. Mobile electronics systems are driving SiP type solutions including fine pitch and TSV



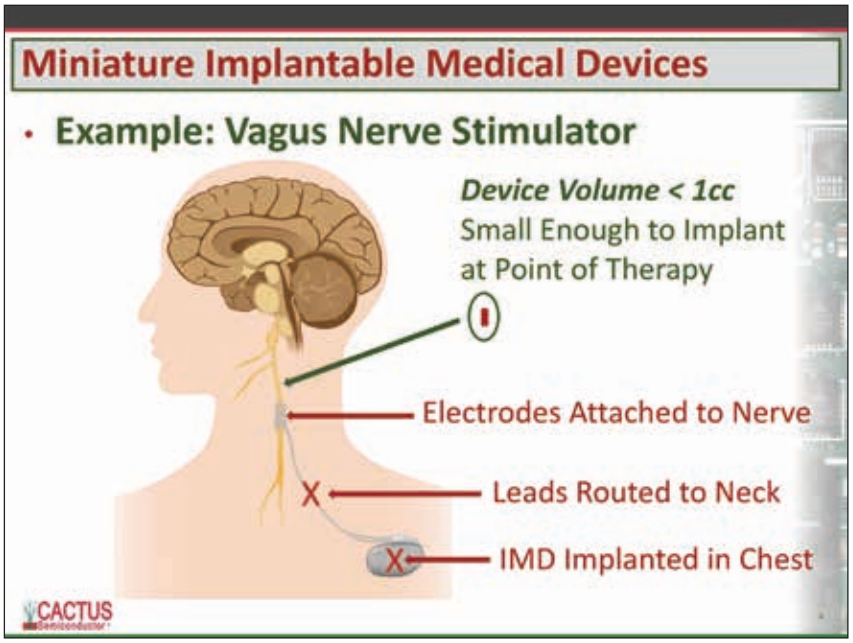
Sensor Technologies for Driver Assistance Systems. *(Source: Freescale)*

interposers. Georgia Tech, working with Shinko and Unimicron, has developed new glass interposer technology

In SESSION 2: High Speed Components and Packaging, our speakers were Dr. Larry Zhu of Sarcina Technology; Ou Li, of ASE Group; and Dr. Hong Shi of Xilinx. Dr. Zhu discussed the cost and time to market advantages of mulit-chip and multi-package ASIC systems, and the particular interconnection challenges for 25 Gbps+ SerDes, where even BGA ball heights create significant differential impedance variations. Ou Li discussed chip-packaging-system co-design and the "tool box" to create virtual SOC. Dr. Shi took us one step further to 1TB data paths requiring 56 Gps transceivers.

Our Tuesday keynote speaker was Dr. Joan Vrtis, CTO of Multek, a division of Flextronics, presenting ***Enabling a Connected World in the Age of Intelligence***. Multek and Flex are spearheading wearable electronics, and were recently featured in an article in BusinessWeek. By 2025 connectivity is forecasted to be reach $2 T value, including consumer, agriculture, transportation, energy, and healthcare applications. This work starts with a vision of creating new opportunities in otherwise legacy markets. Packaging and circuit technologies are key enablers. A small example: Multek has developed a shoe sole with sensors that can determine foot pronation. A challenge for wearable electronics: does it have to be washable? There is also an interactive dance floor which generates electricity. Dr. Vrtis quoted Daan Roosegarde's "3 phases of innovation": (1) Cannot be done; (2) Is not allowed, and (3) Why didn't you think of this before? I might also add, Costs too much.

SESSION 3: Medical and Wearables for Human Health: Connecting the Dots from Silicon to Packaging. Wow, this session really got to the heart (and the ear) of *system in your whatever*. Kurt Koester, of Advanced Bionics, presented *Miniaturization of Cochlear implants*. Andrew Kelly, of Cactus Semiconductor, discussed *I.C. Design for Miniature Implantable Medical Devices*. I personally know some one with a cochlear implant, who was previously deaf. It is life changing gift, and packaging, a combination of implanted, and body worn components, makes it possible. Andrew Kelly explained how MEMS devices, solid state



battery technology, ICs, system design integration, and packaging of all have enabled new generations of miniature, less invasive, implantable devices/systems. MIMDs (Miniaturized Implantable Medical Devices) have reduced module sizes from 15-50 cc's, historically, to < 4 cc's. Smaller devices can also be implanted closer to the point of therapy.

SESSION 4: Power Management and Energy Harvesting, Opposite Sides of the Same Coin Battery? Professor Debbie Senesky, of Stanford University, presented *Gallium Nitride: A New Multifunctional Sensing Platform*. The unique structure of GaN may enable a multitude of device and sensors applications, and offers temperature range and rad-hard advantages vs. silicon. Tim Dry (representing Dr. Jamie Schaefer), of Global Foundries, presented *22DFDX Technology Enables Energy Harvesting Solutions*. 22FDX = 22 nm fully depleted SOI, promising FinFET performance for the cost equivalent of 28 nm silicon processing. Dr. Douglas Tham, of Silicium Technologies presented *Energy Harvesting Technology Based on Next-Generation Thermoelectric Devices*. Body heat may provide the electrical power for the next generation of wearable devices.

Day 2

Our second day started off with **SESSION 5: Multi Die Integration**, including presentations by Trevor Yancey of Techsearch International, Ivor Barber of Xilinx (also session leader), and Vincent Liao, of ASE. Trevor Yancey discussed *Cost Effective Multi Die Integration Solutions for IOT*, including extensive OSAT SIP offerings in leadframes, substrates, FOWLCSPs, etc. For automotive, there are 3 levels of driver assist in automation: (1) Assist, include driver action; (2) Partially automated, i.e. driver copilot; (3) Fully automated, i.e. driverless. Interestingly, 200 mm foundries are providing the majority of IOT devices, specifically MEMS sensors and RF. Ivor Barbor gave us a lesson on single device integration cost vs. multi-device SIP. Packaging cost is higher for multi-chip, especially with TSV interposers. However, given the physics of defect density and yield per wafer for very large, advanced geometry node ICs, the die cost can be less for smaller, better yielding chips. So two (or more) chips, with interposer, vs. single SOC, can be the more cost effective solution. Xilinx is a leader in SSIT (stacked silicon interposer technology) with TSV. Advanced geometry nodes down to 65 nm are available in interposers. Wafer bumping and micro-bumping (Cu post) is also advancing to finer and finer pitches. Vincent Liao introduced us to package level conformal EMS and antenna on package via metal sputter over mold compound.

SESSION 6: On the Road to SIP and Modules. Mike DeLaus, of Analog Devices, discussed how ADI, traditionally known as a single chip analog, mixed signal and DSP devices supplier, has a

roadmap for SiP and multi-device *Heterogeneous Integration*. One potential example: MEMS accelerometer, gyroscope, and ASIC in single package. Dr. Harrison Chang, of ASE, presented *Co-Design for High Density SiP*. The high density integration of heterogeneous SIP module for IoT, wearables, and 5G, is driving the IC houses and OSATs to collaborate on design for function, manufacturability, and testing methodology. This drives the OSAT to new expertise levels on EE/RF design, substrate layout, simulation, and system validation. Dr. Ilyas Mohammad, of Jawbone discussed *SiP from a Systems Perspective*. The current state of wearables includes on person computing (watches, glasses); on person health; and in person health. Are we progressing to a sensor in your baby's diaper, to tell you it's time to change?

On our second day, Wednesday, the key note speaker, Dr. Tarun Verma, a Partner at Silicon Catalyst, discussed ***Enabling the Next Generation of Semiconductor Startups***. Dr. Verma has been a long time contributor to MEPTEC in his former role as Sr. Director of Packaging at Altera. The number of Seed/Series A deals for semiconductor startups per year is down 90% from year 2000. Silicon Catalyst is an incubator for new startups, offering an array of strategic supplier partnering and professional mentoring, a virtual ecosystem of silicon experts encompassing design tools, testing, tape-out, fab & packaging production, and financing. This minimizes the need to raise large seed cap and makes cash investment more impactful. Silicon Catalyst has been awarded the EDN/EE Times ACE (A Champion in Education) 2015 Startup Company of the Year Award. Si Catalyst has selected 5 startups (from 50 applicants) in 2015 to work with, including Silicium in Session 4.

SESSION 7: IC-Package Co-Development in the New SIP Era. Presenters were Hui Liu, Altera, *Product Co-Development in the New SIP Era*; Tom Whipple, Cadence Design, *Chip-Package-Board Pathway Design Optimization*; and Tomoyuki Yamada, Kyocera, *Advanced Organic Package Technologies, Interposer and Embedded*. Hui Liu discussed *Product Co-Development in the SiP Era*. Front end and back end product co-development, including engineering and marketing, is supplanting traditional separations. An impressive example is the *Stratex 10 SiP*, which includes 5 M logic elements, 10 B transistors, 1640 IO's, FPGA, 64 bit ARM and transceiver on Si interposer. Tom Whipple, from the CAD tool perspective, expounded further on this integration of manufacturing disciplines and design tools, including the Pathways design environment, facilitating more optimum layouts and package pin assignment with more flexible personnel skill levels. Tomoyuki Yamada introduced us to new low CTE organic laminate 2.5 D interposer in development, fine pitch flip chip and line-space (6μ) capable, with build up to 5-2-5 levels.

SESSION 8: Wrap Up Panel Discussion: The Great Consolidation. Paul Werbaneth of Intevac led this panel, including speakers and session leaders from both days. We are seeing M&A from both the IC manufacturer side (Intel-Altera, Dialog-Atmel, TI-NS, Microchip-Micrel) and the OSAT-Foundry side (JCET-STATS-ChipPaC, ASE-?, Global-Charter). Who is going to be left? This trend is not unique to the semiconductor world. Since 1996, 37 different financial institutions, globally, have been merged into 4. ◆

SHENMAO Technology Inc.

SHENMAO TECHNOLOGY INC. offers total solutions of Solder Materials to customers by meeting and exceeding their quality and reliability requirements with products and service satisfaction accumulated over four decades of research and development experience. In the meantime, SHENMAO works closely with customers to develop new application products on nanotechnology for the electronics and other industries. From production to shipment, strictly controlling each step, SHENMAO insists on using high quality raw materials to produce high quality products. Through continuous improvement, cost reduction, swift sales and service, SHENMAO keeps making efforts to help customers to be competitive, creating a Win-Win situation.

SHENMAO Technology Inc., as the third largest Solder Materials provider founded in 1973, produces and markets SMT Solder Paste, Semiconductor Packaging Solder Spheres, Wafer Bumping Solder Paste, Dipping Flux, Wave Solder Bar, Solder Wire, Flux and Solder Preforms distributed from 10 worldwide locations as the strategic manufacturing partner of leading OSAT's, the top EMS and OEM's.

SHENMAO Technology Inc. strives to offer the best quality without compromising cost and time-to-market while providing maximum value to all customers, always by superior customer service and technical support. Customer satisfaction and sustainable high quality are always SHENMAO's priority.

Now in its 43rd year, SHENMAO Technology Inc., founded by Mr. San Lian Lee, Chairman and CEO of the globally leading solder material provider, started by manufacturing resin flux cored solder wire and solder bar in 1973 at its Taiwan Headquarters, first for Taiwan and then for the Asian market, continuously expanding since 1998 to 10 worldwide locations.

SHENMAO MICRO MATERIAL INSTITUTE

In order to research and develop the next generation of Solder Material products, SHENMAO established the SHENMAO MICRO MATERIAL INSTITUTE (SMMI) in 2003. The main purpose of the institute is to study and focus on the development and improvement of Micro Lead Free Materials with the highest Quality and Performance. The 1,500 square meter (16,146 Sq. Ft.) SMMI is staffed with 36 engineers (3 PhDs, 8 Masters) continuously developing Innovative New Lead Free Solder Alloys, New Lead Free Solder Paste and Fluxes. SMMI's mission is to improve on the ability of Product Development for a total solution through technological innovation. SMMI has been working closely with electronic manufacturers, universities, and research organizations in the field for innovated material, technology, and failure analysis.

SHENMAO HISTORY

1973 Established SHENMAO incorporation to manufacture Resin Flux Solder Wire and Solder Bar.

1978 Expanded Plant and changed company Name to SHENMAO Industry Co. Ltd.

1982 SHENMAO received CNS Certificate Honor No. 3423 & 3424 for best quality Resin Flux Cored Solder Wire and Solder Bar.

1986 Invited solder expert Mr. Akiyama from Japan to take charge as Advisor.

1987 Obtained Japan Industry Standard (JIS) Certification TW # 8716 & 8717.

1989 Pooled capital with "JSKL" to set up an office in Hong Kong and expanded by setting up a plant in Guangdong, China.

1990 Set up an office and plant of "Shen Mao (M) Sdn. Bdh" in Penang, Malaysia.

1997 SHENMAO obtained ISO 9002 Certification.

1999 Expanded operations with a second plant in Suzhou China for mass production for the ever growing demand of high quality Solder Materials to serve the expanding electronic manufacturing service companies. In cooperation with ITRI, developed the process to manufacture solder spheres.

2001 SHENMAO set up a factory to produce Solder Powder and with the cooperation of JOINT, Japan, to manufacture BGA and Micro BGA Solder Spheres up to a capacity of 60 Billion per month. Obtained ISO 14000 Environment Accreditation.

2002 SHENMAO launched the latest Lead Free solder products featuring environmental concerns, obtained a sub-license from Iowa State University Research Foundation's Pb-free Patent No.5527628.

2003 Established SHENMAO MICRO MATERIAL INSTITUTE for up-to-date soldering technology research. Obtained ISO 9001 Quality Certification. Obtained FUJI ELECTRIC CO., LTD., JAPAN 5 Elements alloy solder (Sn-Ag-Cu-Ni-Ge) Japanese Patent No.3296289; U.S. Patent No.6179935B1.

2004 HP and Dell approved SHENMAO Lead-Free Solder Paste. Moved SHENMAO Headquarters to Taoyuan and expanded the manufacturing plant.

2006 Set up "SHENMAO Technology (Thailand) Co., Ltd.", plant and office in Thailand and "SHENMAO Europe GmbH" in Munich, Germany.

2007 Signed a contract with SMIC for licensing the patent of Sn-Ag-Cu Lead-Free Solder. Awarded OHSAS 18001 Certification. Awarded ISO/TS 16949 Quality Certification. Established Dongguan Shen Yang Micro Material Co., Ltd. in China.

2008 Lead-Free Solder Paste approved by Continental AG. Obtained "Taiwan Industrial Sustainable Excellence Award 2008", Signed up Distributor "White Solder Ltda." in Brazil and "Persang Alloy Industries Pvt. Ltd." in India. Listed SHENMAO Technology Inc. on the Taiwan Stock Exchange.

2009 Introduced Wafer Bumping Solder Paste for Semiconductor Industry. Established SHENMAO America, Inc. subsidiary in San Jose, CA, USA to manufacture solder paste locally for the North American market. Signed up "NEVO GmbH" as European Distributor in Germany and the Czech Republic. Founded SHENMAO subsidiary SOLARJOIN TECHNOLOGY, Inc. in Taiwan to provide the best PV Ribbon, Flux, for the Solar Industry.

2011 Obtained HP re-approval of Halogen Free Lead Free Solder Paste and Halogen Free Liquid Flux. Invested and set up Shenmao Electronics Technology (Chongqing) Limited in Chong Quing City, China P.R.C.

2012 HP re-approved existing Low Silver Content Solder Materials.

2013 Introduced Solder Paste and Flux for PoP (Package on Package) applications. Founded the SHENMAO Technology Inc. Branch Office in Japan.

2014 Started production of Solder Preform made available in Tape and Reel.

2015 Put into production Micro BGA Solder Spheres sizes 55µ and 50µ available in six different Alloys. Released Novel Laser Soldering Solder Paste and developed machine to Dispense and Laser Soldering. Released Novel Laser Soldering Solder Wire.

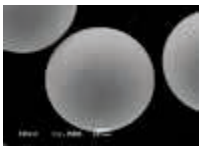
2016 SHENMAO Technology Inc. HQ and plant in Taoyuan, Taiwan will expand adding a near-by new plant currently under construction with the ability to smelt large quantity Tin Ore, providing SHENMAO with its own Tin supply.

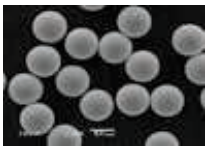
SHENMAO HEALTH, SAFETY AND ENVIRONMENT CONCEPTS

SHENMAO Technology has achieved and is maintaining the ISO 9001, ISO 14001, TS 16949, OHSAS 18001 and QC 080000 Standards. In the future, SHENMAO Technology Inc. and their subsidiaries will continue to follow existing regulations, and seek different international standard to pursue the best quality and fulfill the commitment to environmental protection. SHENMAO Technology has continually researched and developed green products which are more able to be recycled in order to meet ROHS environment protection regulations. The responsibilities of SHENMAO are to reduce the impact on the environment, protect the safety of its employees and customers, and support the communities where SHENMAO does business.

SHENMAO PRODUCTS

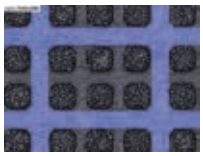
Semiconductor Packaging Material



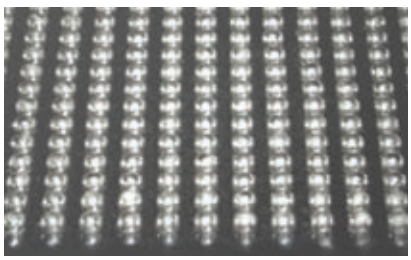


BGA and Micro BGA Solder Spheres

SHENMAO BGA Solder Spheres for PBGA, CBGA, TBGA, CSP and Flip Chip Assemblies are made by UMT (Ultra Micron Technology) from highly pure metals produced to various exact Alloy compositions using Piezoelectric Droplet Jet Technology in high volumes to accurate diameter uniformity, bright shiny surface finishes and high quality sphericity. Various diameters (from 0.76 mm to as small as 0.05 mm) are available at affordable low cost from 10 worldwide SHENMAO locations. SHENMAO High Drop-Resistance Alloy PF902-S (SAC0307X) greatly increases reliability and performance of portable electronic devices drop test.



Bumping Solder Paste
SHENMAO Bumping Solder Paste PF608-PI-21 (Sn/Ag4.0/Cu0.5/x) and PF606-P-BS1 (Sn/Ag3.0/Cu0.5/x) aim to decrease voids in wafer bumping process to yield excellent bump height uniformity. SHENMAO Micro Material Institute applications engineers focused on developing the Bumping Solder Paste Formula with excellent stencil printing transfer rate and the lowest Void to optimize manufacturing process performance. The world's largest IC Packaging and Test Service OSAT's utilize SHENMAO Bumping Solder Paste in production.



Wafer Bumping Flux
SHENMAO SMF-WB02 / SMF-WB51 Water Soluble Flux are made locally in the USA and with the same quality in 8 other worldwide locations. It is said their low viscosity (easy to apply), high tackiness (slump resistant), consistent printability for BGA and Micro BGA Ball Assemblies and excellent wash ability after high temperature reflow (255ºC and 60 seconds over 220ºC) create highly reliable solder joints with optimum maximized quality. A large chipset producer consistently uses SHENMAO SMF-WB02 / SMF-WB51 Water Soluble Flux to achieve ultimately reliable and residue clean ball attach connections.

Package on Package Solder Paste
SHENMAO Package on Package Solder Paste provides excellent tacky property, great dipping, soldering and voiding performance.

SMT Assembly Materials

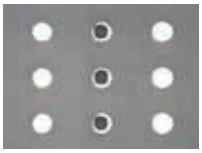
SHENMAO Offers a Variety of Solder Paste Solutions

Tin Lead Solder Paste
Tin Lead Solder Pastes are made from high purity metal ingot (Tin, Lead) with guaranteed high quality. SHENMAO produces solder powder and flux in house. Strict production and quality control, strong technical and development team result in reasonable price to meet each customer's specific needs.

Lead Free Solder Paste
SHENMAO provides Halide-containing and Halide-free Solder Paste Fluxes together with Lead Free Solder Powder sizes from 2, 3, 4, 4.5, 5, 6, 7 and 8 to offer full selection of solder paste.

Water Soluble Solder Paste
SHENMAO Technology offers a full line of Water Soluble Fluxes and Water Soluble Solder Paste for SMT and IC packaging applications. Halide-containing and Halide-free Fluxes for Tin/Lead as well as Lead-Free Solder Alloys. Our formulations, with wide process window, have been proven to be excellent in shell life, stencil life, wetting and clean-ability.

Halogen Free Solder Paste
SHENMAO PF606-P26 No-Clean / Zero Halogen Solder Paste is made locally in the USA and with the same quality in 8 other worldwide locations. It is said to prevent BGA Non-Wet Opens and Head on Pillow defects if there is oxidation on BGA Balls or PCB Pads. In case BGA components are warped, PF606-P26 thru excellent printability, wetting and solder ability can create highly reliable solder joints that greatly reduce their failure rate. A Major Chipset Producer is recommending the use of SHENMAO PF606-P26 Solder Paste to achieve ultimately reliable connections to the PCB.



Laser Soldering Solder Paste
SHENMAO developed Novel Solder Paste for Laser Soldering with good dispensing performance, low flux residue, low spattering and no solder ball.

Solder Preform
SHENMAO Solder Preforms offers accurate solder deposition for various soldering processes. Reel packaging provides opportunity of automation for efficient application. Custom Material may be formulated to unique material and dimensional requirements.

Wave Solder Assembly Materials

Solder Bar
SHENMAO Solder Bar is made solely from high purity metal, produces a low proportion of dross and is suitable for dip and wave soldering. The quality meets J-STD-006 and JIS-Z-3282 standards. Solder Bar is available specification in A grade, S grade, Anti-oxide Bar, Silver added Bar, Pure Tin Bar and other Lead Free Solder Bars.

Core Solder Wire
SHENMAO Cored Solder Wire is specially designed with low residue, high solder ability for Hand/Automatic soldering applications. Solder Wire is available in both Lead Free and Tin Lead alloy compositions. No Clean, Water Soluble, Halogen Free, RMA (Rosin Mild Activated), High Activity (for soldering on stainless steel, nickel, and aluminum surfaces) types are available for a variety of soldering processes.

Paste Flux and Liquid Flux
Full line of Water Soluble Fluxes and No-Clean Flux for SMT, IC packaging and PCB Wave solder applications including Halide-containing and Halide-free Fluxes for Lead-Free Solder Alloys. Shenmao Lead Free Liquid Flux has been approved by HP and Dell Computer.

Solar Application Materials

Solder Ribbon
High quality Solder Ribbon manufactured by SHENMAO is available in many standard alloys and sizes. It has the lowest flow temperature, best wetting and best flow characteristics. Formulated to unique alloy and dimensional requirements.

Solder PV Ribbon and Plated Copper Wire
SHENMAO subsidiary company Solarjoin Technology, Inc. produces quality PV Ribbon, Copper Wire and Flux to meet highest reliability requirements. Special ribbon sizes and alloys are available depending on customer requests.

SHENMAO LOCATIONS

TAIWAN HEADQUARTERS
SHENMAO Technology Inc.

SHENMAO Technology Inc.

NORTH AMERICA
SHENMAO America Inc., San Jose, CA

SHENMAO America Inc.

CHINA P.R.C.
SHENMAO Solder Material (Suzhou) Co., Ltd.

Dong Guan SHEN MAO Soldering Tin Co., Ltd.

Dong Guan SHENYANG Solder Material Co., Ltd.

SHENMAO Electronics Technology (Chongqing) Ltd. Sales Office
Chong Qing City

EUROPE
NeVo GmbH, Brno, Czech Republic

INDIA
Persang Alloy Industries PVT Ltd.
Waghodia, India

JAPAN
SHENMAO Tokyo Sales Office

MALAYSIA
SHENMAO Solder (Malaysia) Sdn. Bhd

SOUTH AMERICA
White Solder, Ltda.
Mariana, Ribeirao Preto – SP. Brazil

TAIWAN
SolarJoin Technology Inc.

THAILAND
SHENMAO Technology (Thailand) Co., Ltd.

For more information about SHENMAO Technology and their products please visit their website at www.shenmao.com. ◆

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MEMS TECHNOLOGY SYMPOSIUM

Advancing MEMS and Sensors for Today's Exploding Demands

Wednesday, May 11, 2016
San Jose, California

If you are involved in the MEMS and Sensors Industry today, or are thinking about entering it, you are in the right place at the right time. Double digit growth fueled by inertial and other sensors in smartphones, wearables, and a plethora of IOT applications have garnered the attention of many who not only see the financial rewards but also the possibilities of new and exciting markets.

With this renewed growth comes a desire to reduce costs, decrease throughput times, scale to much larger volumes faster and continually innovate with existing MEMS and sensors while preparing for the untapped broader markets. Linear technical innovations in design, processes, materials, packaging and test are enabling widespread commercialization of breakthrough MEMS products. While this is absolutely necessary to meet today's demands, will it be sufficient for the future five to ten years from now? If we believe the analysts and commercial companies predicating tens of billions of connected nodes and sensor arrays by 2020, can our industry keep up by sticking to the path we are on?

MEMS sensing applications will track growth in CE, mobile, wearable's, medical, food and agriculture, environmental, energy and the catch all IOT/IOE markets. The 14th Annual MEPTEC MEMS Technology Symposium will focus on the fundamental MEMS technologies and manufacturing techniques to address this explosive growth short to medium term but also take a peek at what's coming longer term that we all need to be aware of today. If you are involved in MEMS and Sensors design, processes, packaging, test and system integration you will not want to miss this one-day action packed and informative event.

Topics to include:

MEMS Design – reusability and enabling faster time to market
Process Technologies – from prototypes to production better, faster cheaper
Packaging – current and advanced techniques to scale more devices and functional in one package
Test – design for MEMS testing and future trends
Emerging Technologies – flexible, hybrid and printed MEMS and sensors

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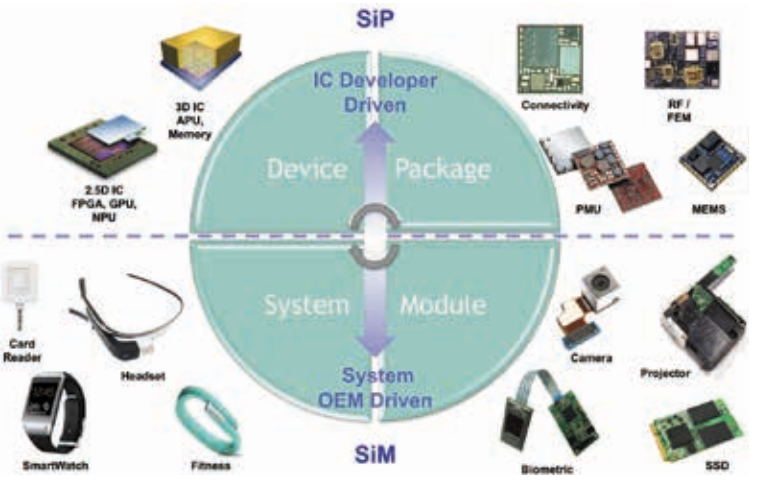
System-in-Package (SiP) – Shifting the Market

William Chen, Senior Technical Advisor
ASE Group

AS WE MOVE TOWARDS A MARKET that's becoming dominated by personal devices, we are seeing extensive creation and proliferation of connected devices and systems. How will this impact both industry and society in order to meet related requirements? One reinterpretation of the promise of integration is moving towards heterogeneous integration through System-in-Package (SiP).

SiP module packaging provides an alternative and complementary solution to System-on-Chip (SoC) for system integration and miniaturization, while reducing development time, design cost, time to market, and total cost of ownership. The sophistication of consumer products emerging today demands more diverse functionality – logic, memory, MEMS, sensors, mixed signal, RF, power, and passives, all heterogeneous components – integrated into a single package with a smaller and lighter form factor. Besides the traditional SoC solutions, SiP is now increasingly being explored and implemented by design houses and system companies to meet new requirements for their product development.

According to the ASE Group, SiP can be defined as "a package or module that contains a functional electronic system or subsystem that is integrated and miniaturized through IC assembly technologies." Essentially, the subsystems are made up of individual dies that are manufactured separately, each using its own most cost-effective node. For example, the ASIC (a SoC) could be in one technology node, additional memories in different nodes, peripherals in still another node, together with discrete and integrated passives, MEMS, and different sensors. These components can be successfully assembled inside the package through a variety of established techniques – perhaps together with additional features such as antennas and shielding – in existing high-volume manufacturing infrastructures. SiP is still in its early stages. There are many compelling industry dynamics driving SiP adoption within mainstream semiconductor manufacturing. Chief among these are the rapid development and implementation of new and innovative IoT and mobile products requiring heterogeneous components and affordable development costs, as well as the creation of differentiated platform solutions through system integration and optimization.



Crossing Boundaries – SiP to Modules

Some leading players within the Outsourced Assembly and Test (OSAT) community are moving beyond their established core competencies and are positioning themselves to serve the industry's SiP needs through leveraging advanced IC packaging technologies to enable new generations of miniaturized electronic systems. Recent developments in advanced packaging technologies – wafer level packaging, fanout chip-first and chip-last, embedding packaging, TSV 2.5D, wirebond and flip chip re-inventions – have great potential for addressing a broad spectrum of SiP applications. Through established expertise in core competencies, IC packaging technology enables highly integrated and miniaturized modular products. In addition, it is crucial to understand the different market segments and to provide SiP co-design and co-development initiatives to support OEM product roadmap execution in these segments. With this understanding, it is possible to deliver rapidly scalable, high-quality, high-precision, and cost-effective SiP manufacturing capacity.

There are many compelling reasons why SiP is currently stimulating heightened interest and discussion across the expanding electronics ecosystem. Many ecosystem players are coming to realize the numerous benefits, including integrated/embedded passives, heterogeneous components, smaller and simplified system boards, reduced power consumption, and decreased component size and thickness. Further simplification is achieved through module level test and qualification, reduced system BOM and complexity, as well as the significant fact that SiP technology is flexible, re-usable, and re-configurable. SiP technology flexibility is particularly important to design in product functionality and differentiation, and perhaps generating innovation in contributing to solutions that address concerns relating to privacy and security.

In summary, the industry is driving towards functional diversification, heterogeneous integration and miniaturization, with SiP establishing itself across the industry, supply chain, and ecosystem. The drive for heterogeneous device integration, decreased size, lower cost, and reduced time to market and revenue is leading many established and emerging players to explore the value proposition of SiP. As an industry, we are at an early stage of a collaborative work-in-process. There is much work that needs to be done in the ecosystem to innovate new ideas and to implement new solutions to bring SiP fully into the mainstream. ◆

Closing the MEMS Sensor Product Life Cycle Gap from Development to Production

MICROELECTRONIC PACKAGE assembly is a key part of the $16.5B commercial MEMS sensor market representing 22% of the market. In terms of unit growth, the MEMS microelectronic package assembly market is growing *twice as fast* as the IC package assembly market, but the needs of the entire life cycle of a MEMS product are not met. From development of initial manufacturing processes and materials selection, to prototype development, to environmental life test qualification, to volume production, SMART Microsystems provides the lowest overall development time and cost to satisfy the full life cycle requirements of MEMS sensor products.

Relatively common MEMS devices—such as pressure, chemical, and optical sensors—require custom package development when being integrated into a sub-assembly for niche applications. And while many service providers (who focus on microelectronic package assembly of ICs) often underestimate MEMS sensor development projects, SMART Microsystems **focuses on microelectronic package assembly of MEMS sensor products** to appropriately scope projects. This reduces delays and increases the ability to solve complicated process issues. SMART Microsystems provides companies throughout the United States and Canada with MEMS sensor prototypes and has successfully brought several new development programs to production readiness. Customers include producers, manufacturers, and suppliers who require microelectronic sub-assemblies for sensor products. With expertise and a focus on MEMS sensor products, the SMART Microsystems engineering team has solved many MEMS process challenges and understands the nuances of MEMS sensor product development needs.

Located in Northern Ohio, SMART Microsystems opened a new facility with over 15,000 square feet of ISO 6 (class 1000) and ISO 5 (class 100) cleanrooms. This state of the art facility, furnished with flexible equipment capabilities for assembling a high mix of materials and products, creates a **turn-key solution for microelectronic package assembly of MEMS sensors**. From prototyping all

MEMS Product Life Cycle Captured at SMART Microsystems.

the way through market entry, SMART Microsystems is a single supplier, reducing the total cost of product development. Prototype development and manufacturing capabilities include dicing, die attach/flip chip, vacuum solder reflow, wire bonding (ball and fine/heavy gauge wedge with both wire and ribbon) and encapsulation (adhesive dispense, lid seal and parylene coating). Environmental life testing capabilities at SMART Microsystems include HAST, thermal shock, thermal/humidity cycling, high temperature storage and accelerated UV durability. Advanced inspection equipment is comprised of an acoustic microscope, 3D X-ray, interferometer and a scanning electron microscope (SEM).

Equipment capabilities at SMART Microsystems deliver manufacturable and sustainable solutions. As a **certified ISO-9001 manufacturer**, SMART Microsystems incorporates design-for-manufacturing into the initial stages of development—this decreases process iterations and reduces time needed as the product moves into volume production. By working concurrently with the customer's design team and suppliers, SMART Microsystems is able to implement process specifications, design-to-cost goals, and on-time delivery objectives efficiently, reducing overall time and cost. SMART Microsystems applies this approach to aerospace, industrial, medical, and other markets and supports the package format—QFN, DIP, TO-can, chip-on-board, flip chip, or custom housings—that is needed for the application. In all situations, incorporating manufacturing objectives early reduces the development time and cost, enabling SMART Microsystems to scale-up quickly, support volume production, and meet quality assurance requirements.

SMART Microsystems is located near Cleveland, in a Midwest manufacturing hub. Nearby access to an international airport allows for fast and easy transportation to support medical, aerospace and other markets that require the high-value, low-volume applications for MEMS sensors. With a focus on MEMS package assembly and a certified ISO-9001 status, SMART Microsystems creates the turn-key solution for customers. Accomplishing the full life cycle requirements of MEMS sensor products, SMART Microsystems takes a design from prototype, through qualification, to volume production at the lowest overall development time and cost.

More information about SMART Microsystems services can be found at www.smartmicrosystems.com. ◆

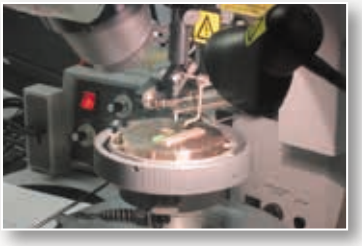
Industrial Controls

Medical Applications

Aerospace Systems

The SMART Advantage.

Lowest Overall Development Time and Cost



SMART PROTOTYPE DEVELOPMENT

As a turn-key solution, SMART Microsystems builds early proof-of-concept samples as well as feasibility studies to help you avoid challenges that appear early in process development. SMART Microsystems engineering team's expertise in MEMS sensor products has solved many of these challenges.

SMART ENVIRONMENTAL LIFE TEST

SMART Microsystems' environmental life testing identifies reliability issues early in your MEMS sensor product development. As part of a turn-key solution, reliability study, or on an as-needed basis for overflow/bandwidth, SMART Microsystems can solve your issues before they become a problem in the field.

SMART MANUFACTURING SERVICES

With the SMART Microsystems investment in state-of-the-art facilities and an experienced team, we are able to scale-up manufacturing quickly, support low-volume production, and meet your quality assurance requirements.

SMART Microsystems creates turn-key solutions for microelectronic package assembly challenges to move your MEMS sensor technology from development to production. With an engineering team experienced in manufacturing and state-of-the-art facilities, SMART Microsystems accelerates the transition of your new MEMS sensor product to the market.

Call us today at **440-366-4203** or visit our website at www.smartmicrosystems.com for more information about SMART Microsystems capabilities and services.

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Packaging and Assembly Technology for the Internet of Things Era

Jayna Sheats, CEO
Terecircuits Corporation

IT IS NOW RATHER WIDELY RECOGnized that the technology of integrated circuit (IC) packaging has overtaken chip fabrication as the focal point of innovation in electronic fabrication. Technical trade journals are replete with articles about the latest advances in 2.5D, 3D and even 3.5D packaging, and various forms of chip scale and wafer level packaging (WLP). System-in-package (SiP) modules, such as Freescale's SCM-i.MX 6Dual, Samsung's Artik series, or the proprietary but strategically important Apple S1 (iWatch) occupy center stage for designers. A recent (November 2015) Yole report projects FOWLP as supplying the majority of the industry's growth during the next several years.

The impetus for this shift is with little doubt a consequence of the inexorable approach of the end of Moore's Law, an event that astute observers have known had to arrive at some point (for reasons of atomic scale if no other). There are very few apparently viable options for introducing major inventions into IC fabrication, and even those currently in development are horrendously expensive and complex. Packaging, on the other hand, affords many attractive options at more customary costs.

It is important to remember, however, that "More than Moore" does not offer the same advantages as Moore's Law did. The latter, while originally expressed in terms of transistor count per chip, was most fundamentally an economic phenomenon: the marketplace supported the cost of the fantastic advances in equipment and processes because they facilitated making transistors cheaper, not because they made them run faster. Higher speed transistors fabricated from III-V materials have been available for decades, but that is not the prevailing techology for most products because it is appreciably more expensive.

The current palate of "advanced packaging" including fan-in and fan-out WLP, interposers, and monolithic as well as through-silicon via (TSV)-based 3D integration, offers routes to increasing a product's performance (e.g. clock frequency or power), but not lower cost per basic computing element (logic gate). The success of Moore's Law fundamentally stems from the magic of planar processing and the genius of lithographers: as tools were developed to process smaller features, the cost of those tools rose more slowly than dimensions fell. In combination with larger wafers, the result has been (until recently) close to a constant cost per unit area of silicon processed, and hence steady (exponential) reduction in cost per transistor. Short of some futuristic scenario with holographic processing of volume elements, there is simply no way to do this in the third dimension. Stacking chips in 3D today means stacking chips whose cost arose from the manufacturing structure of planar processing, and can only give a product whose transistors cost more, not less.

There are many reasons to pursue non-planar packaging despite the added cost. For example, these same transistors may be able to work faster, or consume less power. As die size increases in conventional scaling, global *RC* delay increases as the 4th power of the scaling factor. *RC*-related signal delay for global interconnects increases even at constant die size because dielectric and conductor thicknesses decrease, while local interconnect delays remain constant. Since the longest lines are getting longer, resistive power consumption also increases. (In practice, line and dielectric thickness have not decreased with the chip scaling factor, but there is only so far one can go with aspect ratio, so the problem remains.) These prominent issues for on-chip signals pertain also to interchip connections along with other issues (e.g. wirebond inductance).

The clarity and simplicity of Moore's Law notwithstanding, what matters for the consumer is computing "power" (an unfortunately subjective metric) per dollar, not transistors *per se*. Predicting how to achieve increases in this metric is much more complicated. It is clear, however, that shortening interconnects is vital, provided cost efficacy is maintained.

The shortest possible connections between two chips are obviously obtained by stacking (ideally face to face; TSVs being a close second). Doing this cost-effectively has proved to be a formidable undertaking, having only recently achieved significant commercial success after 15 – 20 years of intensive industrial development (taking ALLVIA to be the pioneer of this stage). While progress will continue, it is worth asking if any other approach can be effective.

For example, what might happen if the distinction between packaging of chips and assembly of circuit boards were eliminated? Conceptually, the architecture of a printed circuit board (PCB) corresponds to that of a chip: functional elements are connected by wiring. In the case of ICs, one first forms the active elements, and then the interconnects. Arguably, at the time when interconnects were made with discrete wires, this is how PCBs were constructed: finished components were placed on the board and then wired together.

The Challenge

There are both historical and practical reasons why this is not done today. In practice, the wide range of component

sizes which may be encountered, e.g. 01005 capacitors and transformers, would make it very difficult to move the populated board through any integrated wiring process. Many products do not have this large range, but a conventional assembly company must be prepared to handle all possibilities.

Second, the historically rooted supply chain and infrastructure of the industry does not readily embrace or facilitate change. PCBs predate modern IC architectures; they were already used with vacuum tubes, and 4-layer PCBs were in production at about the same time Jack Kilby came to Texas Instruments. Thus the technology for fabricating them in a process (and typically location) separate from where components would be added was already well entrenched. At the same time, the sensitive and easily damaged ICs were packaged for protection and convenient insertion (in most cases) into the through-holes of those boards.

The modern incarnation of this legacy will not go away anytime soon, but there are numerous products, including typical wireless sensor modules, embedded controllers, and many of the components of mobile phones which contain only surface mount devices (ICs, sensors and passives). These products, which comprise the foundation of the IoT, give us an opportunity to depart from conventional practices. At Terecircuits we have developed the technologies for an IC-like approach: place unpackaged or minimally packaged components onto a single substrate, interconnect them, and encapsulate the entire circuit at once. This simple architecture has the potential to cut the number of process steps for such a product by 80% or more, with concomitant reduction in materials use. Most importantly, it enables us to achieve a great deal of what 3D integration is designed for, but with a process that is poised to actually reduce costs.

Process Details

The process can be divided into three parts: placement, embedding (which is roughly equivalent to the molding in conventional packaging), and interconnection. The placement step in Terecircuits' process replaces the mechanical pick and place tool with a novel photopolymer transfer operation: an entire array of components is adhered to a transparent polymer-coated plate which is then aligned in close proximity to the target (in a tool similar to a contact aligner); irradiation of the polymer (through the plate) behind selected components with a dose typical for microlithography and attendant mild heating causes its vaporization and release of the components.

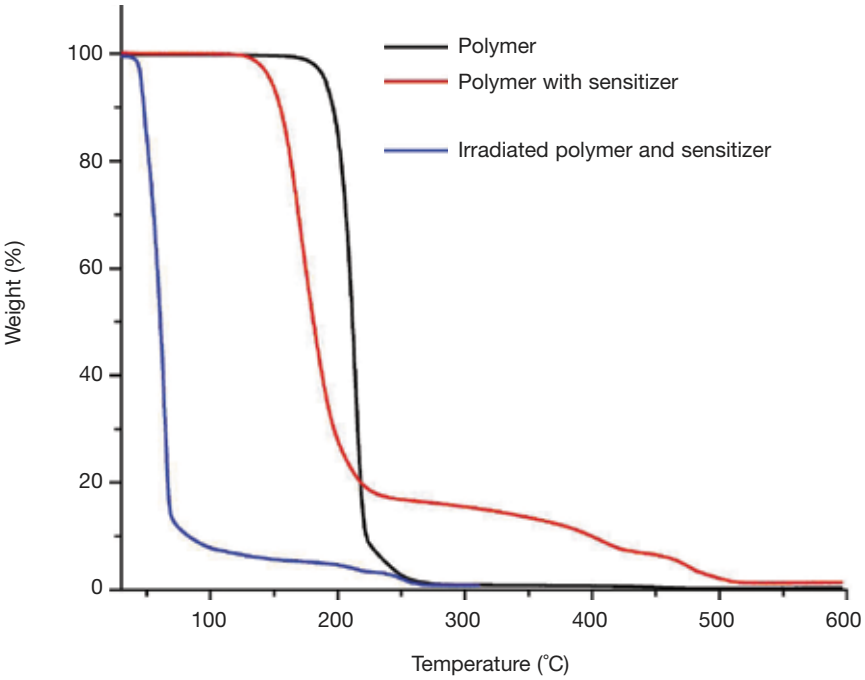


Figure 1. Thermogravimetric analysis of the materials used in the photopolymer component transfer process; heating rate 10C/min. Faster heating eliminates the residue in the exposed material which in the TGA requires >100C to decompose.

This critical step allows the otherwise delicate bare dice to be handled at high throughput with near-zero risk of damage. Ultrathin (25 microns or less) and extremely small (effectively limited only by the optical system) components are readily accommodated. Because of the array processing, throughput can be many times greater than present pick and place tools with comparable capital and labor costs.

Figure 1 shows the process window between unirradiated and irradiated polymer; it makes process control substantially easier than for stamp transfer printing (which relies on relatively small differences in adhesion between components, stamp and substrate) or laser ablation (where a narrow threshold margin separates ablated and unablated material). That control is critical for achieving precision, close-spaced placement in a parallel (array) process with small components.

High-resolution interconnects are best made on a planar surface. This is obtained by placing the components face down on a release layer and embedding them in a reflowable polymer which then becomes the substrate and matrix. Such partial molding processes are certainly not new, and have been the subject of several publications by Matti Mäntysalo and colleagues at Tampere University in Finland, among others. Compared to conventional molding, embedding allows consideration of a wider selection of polymers, optimizing for example the coefficient of thermal expansion.

Releasing this "front end" laminate from the temporary substrate and turning it over affords a substrate as flat as the chips themselves on which interconnects with resolution of a few microns can then be built up as desired. In essence the wiring of the "PCB" is simply a continuation of that in the chips. Without a package surrounding the chips, their edges can be placed nearly contiguous (within a few microns), resulting in a product rather like one big chip (which of course could never be made monolithically for a host of reasons). We might call it a "composite chip".

continued on page 32

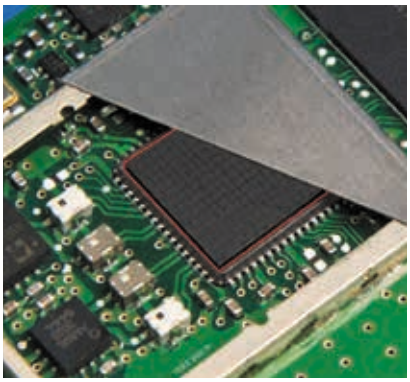
Uniting Thermal Control and EMI Absorption

Scott King
Henkel Electronic Materials, LLC

THE SHRINKING DIMENSIONS AND increasing functional capability of modern electronic devices place continual demands on effective control of heat and electromagnetic interference (EMI). Not only are new component and printed circuit board (PCB) designs adhering to the miniaturization trend, but higher density assemblies that place parts with different operating frequencies closer to each other are also becoming prolific. All of these factors combine to place additional stress on conventional EMI and thermal management protocols.

Like heat management, EMI has been analyzed by electronics specialists for decades and is well-understood. If not controlled, EMI – which is a disturbance to an electrical circuit due to electromagnetic coupling from external sources – can compromise or inhibit the function of a circuit, degrading signal integrity and impacting system performance and efficiency. In order to protect against EMI, the most common approach is the use of EMI shielding caps – metal lids attached to grounding pads – to prevent outside interference, minimize interference between components within a design and to prevent crosstalk of components on printed circuit boards (PCBs). This solution has traditionally been highly effective. However, as PCB component density becomes more challenging, the success of shielding caps – also known as Faraday cages – to control EMI may require supplemental EMI absorption to make conductive shielding for electromagnetic compatibility (EMC) even more robust. In fact, widely recognized industry standards defined to control applications that use multiple frequencies dictate effective EMI and heat transfer control for end product acceptance and reliability.

These requirements were the driving factors behind the development of a groundbreaking product that satisfies the need for both thermal control and EMI management. Henkel's GAP PAD® thermal interface materials portfolio, long



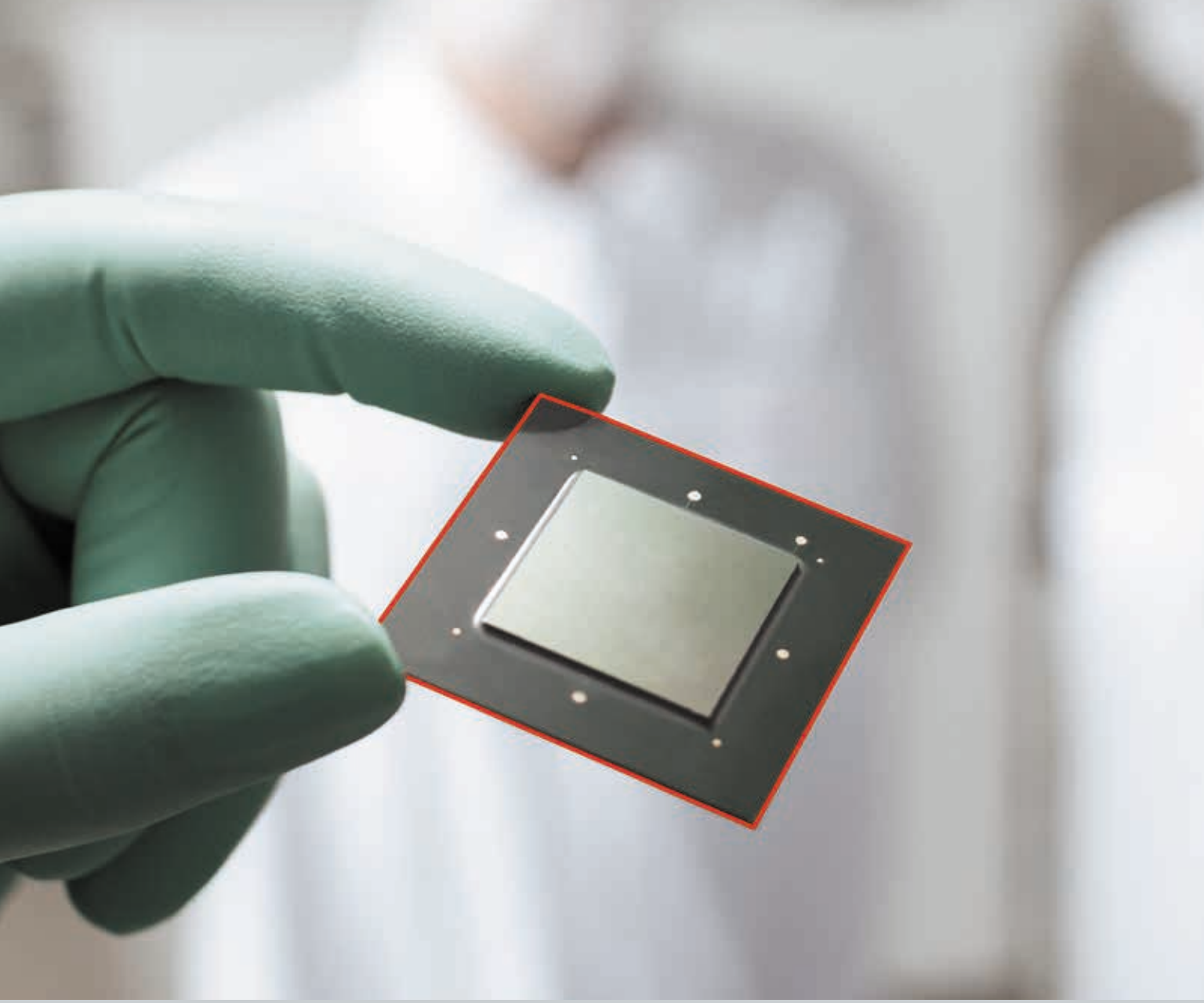
recognized as the market's most effective gap filling thermal management product line, has been extended with the addition of a dual-function material. GAP PAD EMI 1.0 is the market's first-ever extremely low stress thermal interface material that unites thermal conductivity and EMI absorption capabilities in a single product.

With thermal conductivity of 1.0 W/m-K and EMI absorption for frequencies above 1GHz, GAP PAD EMI 1.0 provides robust thermal management control and an added level of EMI protection. Because of its improved wet-out at the interface, GAP PAD EMI 1.0 results in thermal performance that is superior to other competitive materials with a similar rating. Thermal conductivity is also enhanced by the material's natural tack on one side, which eliminates the requirement for any thermally-impeding adhesive layers and also makes component rework simple. Uniquely, EMI absorption capabilities of 0.28 dB/mm at 2.4 GHz and 0.55 dB/mm @ 5 GHz have been exhibited with GAP PAD EMI 1.0. (Note: As material thickness, part size and shape and other factors can largely influence EMI performance it is always recommended that GAP PAD EMI 1.0 be tested in the application for the best result.)

In addition to its impressive thermal dissipation and EMI absorption performance, GAP PAD EMI 1.0 is the softest and most compliant thermal interface material on the market. Its ability to easily conform to various topographies and provide a high degree of flexibility ensures very low stress on solder joints. As compared to traditional EMI materials with high modulus, GAP PAD EMI 1.0 helps improve reliability by reducing in-field failures caused by solder joint stress and fractures.

While its potential applications are broad, GAP PAD EMI 1.0 is particularly well-suited for products in the consumer electronics, telecommunications, and PC sectors. ASICs and DSPs can also benefit from use of GAP PAD EMI 1.0. The material is available in sheet and die-cut formats, various thicknesses, custom part sizes, and can be applied manually or by automated placement. For electronics specialists who are working with PCBs that challenge conventional approaches to heat management and effective EMI control, GAP PAD EMI 1.0 is the ideal solution.

For more information, visit www.bergquistcompany.com. ◆



The smaller the device - the more solutions

No matter where you are or what your process requires, you can count on Henkel‘s expertise. Our unmatched portfolio of advanced materials for the semiconductor and assembly markets all backed by the innovation, knowledge and support of Henkel‘s world-class global team ensures your success and guarantees a low-risk partnership proposition.

Henkel Excellence is our Passion

PacTech - Packaging Technologies
is a worldwide leader in both Wafer Level Bumping & Packaging Services and in Advanced Packaging Equipment Manufacturing.

Prime Manufacturer of Leading-edge Technology Equipment & Processes for the Advanced Packaging Industry

ALMOST 40 KILOMETERS NORTHwest of Germany's capital, Berlin, is the city of Nauen where PacTech has its headquarters. Founded as a spin-off of the federal scientific Fraunhofer IZM in 1995, the company consists of two business units:

1. Manufacturer of advanced wafer level packaging and wafer bumping production equipment.

2. Provider of high-quality, subcontract manufacturing services.

With subsidiaries in California and Malaysia, the corporation supplies its outstanding solutions in these relevant business regions.

PacTech has continually grown, and the company is to date the biggest high-tech employer in the region with a staff of some 350 people.

In Europe, the U.S. and Malaysia, the full enterprise portfolio of different manufacturing services is available, as well as all of the backend solutions. The advanced equipment manufacturing operations is located at the German HQ. All machinery, sold originates from the headquarters and carries the well-known brand: "Made in Germany"!

The company's main target area is now the Asian markets, which consume the lion's share of products and services.

With more than 20 years of experience, PacTech is a prime manufacturer of leading-edge technology equipment and processes for the advanced packaging industry. PacTech designs, manufactures and supports solder jetting equipment, wafer-level solder ball transfer systems, wafer-level solder rework equipment, laser assisted flip-chip bonders and automatic plating tools for high volume electro-less Ni/Au and Ni/Pd/Au Under Bump Metallurgy (UBM) and Over Pad Metallurgy (OPM) through its global sales network.

In its worldwide sales and application centers PacTech offers demonstration capabilities, including assembly of samples and prototyping under ISO certified production conditions. Moreover, PacTech has a unique dual business model in which it offers its customers with new chip designs or initial low volume requirements the option to use in the initial phase PacTech's demo centers for services. After qualification of the product the customer has the option of further cost reduction by utilizing PacTech's full turnkey solution: Equipment, Process and Technology. This reduces the cost of customers new product introductions and at the same time gives the customer the option to qualify and intensively study the technology, and understand the cost of ownership. Together with its partner and main shareholder NAGASE, PacTech is also developing embedding technologies for wafer and substrate level CSP technologies. The solder ball jetting equipment addresses markets like Hard Disk Drive, Camera Module, Sensors and Stacked TSV chip packages.

The electro-less plating line addresses applications in power MOSFET devices for clip attach, contactless RFID devices, high reliability power devices, and for Wire Bonding applications using Ni/Au, Ni/Pd respectively, including Ni/Pd/Au for Over Pad Metallization, and many other applications. Ni/Pd Metallization is qualified for volume production of low cost Cu Wire Bonding over active pad. The new Ultra SB² tool is addressing all wafer and substrate-related solder ball applications for high volume mass production. PacTech has leading edge technology for Solder Ball Transfer, Minimum Solder Ball diameter is 30 μm. For the electro-less Plating Tool, PacTech is the worldwide leader with more than 20 Automatic Tools installed worldwide.

Since its inception, PacTech has received more than 110 patents for products developed in areas relating to wafer bumping, flip-chip and chip-scale packaging, and laser-bonding technology.

Also PacTech is providing all chemicals for wet Chemical Pad Protection and Pad Metallization as part of a turnkey solution for electro-less Wafer Bumping. Additional analytical services and support to customers is available.

It is PacTech's mission to provide the highest level of innovative technology solutions with an unparalleled degree of customer service orientation, corporate integrity and attention to its clients' individual technology demands.

More information is available at the PacTech website at www.pactech.de. ◆

PacTech
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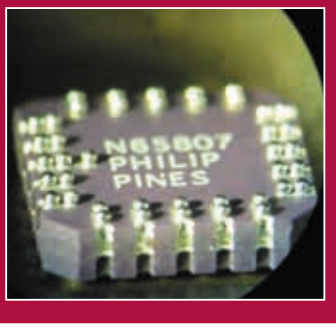
Your Partner for Advanced Packaging

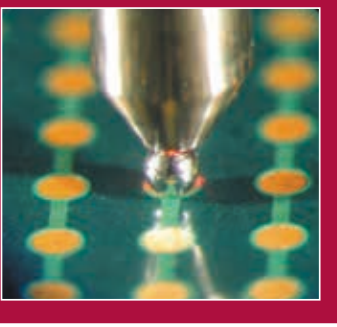
Our Services

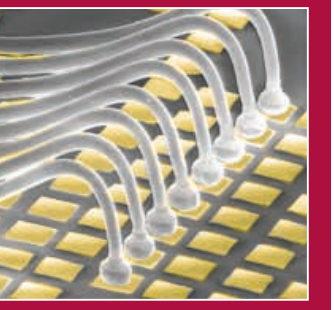
Wafer Bumping
- UBM & OPM Plating, e.g. eless NiAu & NiPdAu, e-plate Cu & Au
- NiFe Plating for MEMS
- Solder Ball Attach / Solder Jetting
- Wafer Level RDL (Low Volume)
- CSP & BGA Ball Rework

Wafer Backside Metallization
- Wafer Thinning
- Single Wafer Etch
- TiNiAg & TiNiAu Evaporation

Backend & Die Sort
- Laser Marking, Sawing, Electrical Test
- Tape & Reel
- FC-Assembly







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TECHNOLOGY

continued from page 27

The "composite chip"

Such a composite chip in practice requires bare dice, however; even the best CSPs will give component separations one to two orders of magnitude larger. But bare dice are problematic to handle with pick and place tooling and are hard to connect due to irregular pad locations (these points were emphasized by Joseph Fjelstad, of Verdant Electronics, in a recent article in The PCB Design Magazine). The Terecircuits photoprinting component transfer process uniquely enables such structures. With it, close, precise positioning of components such that lithographic connections can be made is not only possible, but actually cheaper than conventional packaging (cost modeling predicts a reduction of more than 10x).

There is one more problem with bare dice (also emphasized in Fjelstad's article), which is testing and burn-in, or the availability of KGD (known good die). Fortunately, the smaller the die, the greater the yield (based on exogenous defects; process variation follows a different curve) and the less testing is required. Device infant mortality which is the main reason for burn-in can be brought below 0.5% by proper refinement of the process. Finally, wafer-level testing (including non-contact approaches) is an actively developing field; the same issues apply in general to all 3D stacking architectures.

The "composite chip" may sound a lot like what has been called a Multichip Module (MCM), and indeed it is one variety (at Terecircuits, we refer to them as "integrated multichip circuits", or IMCs). MCMs were discussed with thoroughness and great clarity nearly 20 years ago in "Roadmaps of Packaging Technology" by Bogatin, Potter and Peters (Integrated Circuit Engineering Corp., 1997), who noted that "MCMs did not become the vehicle that made single chip packages obsolete. They did not take over all of electronics. However, they represent over a $1B market today." The main impediment was identified as the KGD issue. By using high-quality interconnects (especially eliminating wirebonding), smaller dice, and mature processes for die fabrication, this issue can be managed (as it must be also for any sort of 3D packaging).

Photoprinting component transfer can also be used to stack devices; the subsequent interconnect processes and problems are the same as for any 3D system. Both in-plane and vertical placements may be advantageous for a given product.

Conclusion

The innovations emerging in packaging today could have been useful at almost any stage in the last few decades, but they were far less compelling when price per functionality could be decreased at the same time that product performance increased. Now both of these trends are slowing or reversing. Stacking (either monolithically or by some form of bonding and wafer-to-wafer interconnect) addresses the latter issue directly. However, it will be quite some time, if ever, before the cost per gate of a finished product (what is on the PCB) is decreased by these techniques. The technology presented here, while perhaps not attaining the highest performance levels, still offers the potential for meaningful cost reductions along with substantial performance improvements. ◆

OPINION

continued from page 34

Europe and the SEMICON Taiwan SiP Global Summit. However, in the last few years, we have seen a noticeable expansion in participation from companies across the electronics supply chain. From system integrators, with Cisco, Microsoft, Huawei, Xaomi and other, through fabless, IDM, foundry, OSAT, EDA, equipment and materials suppliers – all segments of the supply chain are now represented in SEMI Advanced Packaging Committees around the world.

To add to this intensity in the packaging industry, it has become clear that very few packages are single die any more. The growth drivers in packaging – 2.5D, 3D, Fan-out Wafer Level Packaging (FOWLP), SiP – are pushing towards a higher level of integration, and ultimately, system-scaling. To add to the complexity, the push from end-use customers in various verticals keeps the industry on its innovating edge, creating a wide assortment of new options within these technologies.

Another trend over the last few years has been the shift in end-use markets for semiconductors. Already, more semiconductors are sold into consumer products than into IT infrastructure. The industry is faced with a new set of time-to-market demands along with new pressures on cost, performance and form-factor and companies involved in the packaging segment are on the front line in addressing these needs. Co-design has become the new norm and companies are collaborating – not just with the supply chain segments on either side of them – but with their customers' customer and sub-suppliers as well.

To enable efficiencies across this complex network of technologies and constituents, the advanced packaging community is already working towards convergence on a Standards platform. SEMI is adapting its International Standards efforts in packaging – focusing on multi-die integration and developing new standards in such areas as materials characterization for novel materials, wafer thinning and bond/de-bond, TSV characterization, automation for back-end facilities, and more.

In combination, the transformative changes the industry is encountering – from M&As, ecosystems shifts, strategic partnerships, IoT-fueled opportunity and growth, and international standards efforts – all of these efforts will help enable advanced packaging to deliver on the promise of system-scaling and drive innovation well into the 2020s.

As SEMI, our members and partners get ready to tackle another year of navigating a rapidly changing ecosystem, we look forward to doing more together with industry stakeholders and associations alike. There is great power in collaboration and community-building. We have seen it in our Standards task forces, our Special Interest Groups and our events, and it's the most effective and sustainable way of keeping our promise – to advance the growth and prosperity of our members. To you and yours, Happy Holidays and a prosperous 2016! ◆

Driving Innovation Through Transformative Change

Bettina Weiss and Tom Salmon
SEMI

THE NUMBER OF MERGERS AND acquisitions (M&As) last year has been truly staggering. M&As and the subsequent shifts in the semiconductor ecosystem have had a profound impact on all parts of the supply chain. Suppliers feel the pinch of a smaller but more demanding customer base, and must broaden their product portfolios to remain competitive, while the entire semiconductor industry is forecast to grow by only single digits for the next few years. Customers may now be system integrators or consumer electronics manufacturers who have an entirely different culture and way of doing business.

As 2015 came to a close, at SEMI, we reflected on an exceptional year. SEMI, serving the electronics supply chain, has seen its industry supply chains undergo a transformative change – and trade associations are changing as a direct result of these new dynamics.

Strategic Partnerships a Key to Expansion

What does this mean for regional and global associations? For SEMI, the changes in the semiconductor industry make it critically important to partner to increase value for our members. Value means broadening engagement platforms, deepening technical expertise, and offering focused Standards and education initiatives and events that bring stakeholders together, both to network and solve problems. We also realized that nobody can go it alone because "organic growth" for companies and associations alike often takes too long and lags behind innovation. To this end, SEMI has developed the Strategic Association Partnership concept, a model that allows for a more formalized partnership with other associations and organizations, especially in adjacent markets.

On October 7, SEMI announced its first such partnership with the FlexTech Alliance (www.semi.org/en/node/58856). FlexTech will continue to pursue its mission of fostering the growth of the emerging flexible, hybrid and printed electronics (FHE) industry – now, as part of SEMI, while SEMI broadens its community in this sector. FHE is high priority for SEMI members, especially in the context of the Industry of Things (IoT), because it combines elements of traditional IC manufacturing with high-growth markets in the areas of wearables, medtech, smart manufacturing and "smart manufacturing." Both organizations recognized that its activities were complementary and by leveraging each other's strengths, their collective membership would benefit through access to more resources, global platforms and new industry communities for collaboration, R&D initiatives, new supplier-customer interactions and deeper engagement in Standards development.

For SEMI, the changes in the semiconductor industry make it critically important to partner to increase value for our members.

IoT to the Rescue?

Internet of Things (IoT) is a tremendous opportunity for many companies in the ecosystem. This is good news for many companies: MEMS and sensors on flexible substrates for IoT and novel consumer products open the door to new markets and customers. Highly automated and IT-driven, "smart" manufacturing is gaining momentum, and self-driving cars are no longer science fiction. All this – the Internet of Everything – needs semiconductor devices.

Based on the exploding number of internet-enabled mobile devices and the emergence of the IoT, demand for sensors, MEMS, analog, power and related semiconductor devices is rapidly growing. While these devices are critical to enable the new era of computing, the applications do not require leading-edge manufacturing capability, and this demand is "breathing new life" into 200mm fabs.

According to SEMI's recently published "Global 200mm Fab Outlook to 2018," worldwide 200mm semiconductor wafer fab capacity is forecast at 5.2 million wafer starts per month (wspm) in 2015 and expanding to 5.4 million wspm in 2018 – largely a reflection of IoT activity.

Shift from Chip Scaling to System Scaling

So while consolidation is reducing the number of companies in the leading-edge digital space, opportunities and growth still abound in emerging markets, fueled by IoT and new technology needs of vertical markets such as automotive, biomedical and industrial automation. One strong trend we see emerging, and something that was discussed in depth at the recent MEPTEC/SEMI symposium (see page 15), is the shift from chip-scaling to system-scaling. The focal point of this trend is solidly in the advanced packaging space.

SEMI has provided a platform for programs in semiconductor packaging for a number of years – from work on packaging Standards and collaboration with JEDEC, IEEE and others in the early 1990's to recent standards work on 3D-IC and events like the SEMI 3D Summit in

continued on page 32

Connecting People and Technology

Customer demand for highly sophisticated products has made semiconductor packaging an important factor in system performance. As one of the world's largest suppliers of outsourced semiconductor packaging design, assembly and test services, Amkor helps make "next generation" products a reality.

Founded in 1968, Amkor's continuous path of innovation, improvement and growth has led us to be a strategic and trusted manufacturing partner for many of the world's leading semiconductor companies. As the industry moves aggressively toward new and more complex technologies, our unique expertise in high-volume manufacturing techniques and the ability to solve technological challenges are among our greatest strengths.

Customers also benefit from our extensive and expanding global footprint, enabling us to easily handle large orders and offer quick turnaround times. Amkor is positioned to deliver end-to-end solutions that meet the requirements for a broad range of product designs today, and in the future.

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Grip Rings


Grip Ring Magazines


Grip Ring Shippers


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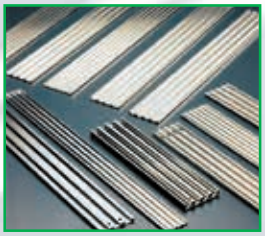
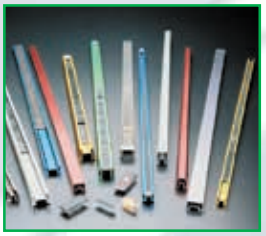
Stack Magazines - E.O.L.

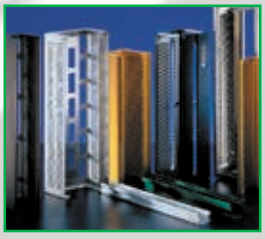

Process Carriers (Boats)

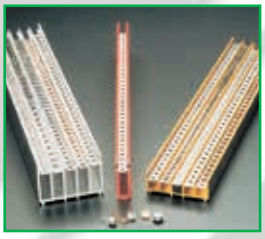

Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines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