MEPTECReport

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 20, Number 4

GEL DISPENSE FOR ENCAPSULATION OF MEMS PRESSURE SENSORS

Gel Encapsulation Poses Unique Challenges in Packaging

page 24

Everything-Proof: The Future of Mobile and Wearable Devices

MEPTEC MEMBER COMPANY PROFILE Established in 1997, UTAC's customers span across all vertical markets including: mobile phone and communication, consumer, computing, automotive, security banking, and security identity, industrial

and medical applications.

page 12



The success of Fan-Out packaging platforms is so undeniable today.



Epoxy paste adhesives have historically been the sole epoxy material available for die attach.

20

In an industry that is accustomed to many package options, consolidation could produce "The Big Five" advanced packaging platforms.

30

IC Designers, EDA and IP Vendors, Foundries and Assembly Houses Can Work Together.

page 28







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Volume 20, Number 4

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ON THE COVER



MEPTECReport

As the MEMS-based sensing industry grows, the environmental conditions in which these sensors must perform grow with it. Pressure sensing is one application where particularly harsh environments can be present. Unlike previous technology, the MEMS-based technology offers the ability to place the microscopic sense element and wire bond interconnects directly in the fluid path. It is often necessary to protect the sense element and interconnects with products such as encapsulation gels.

Cover Photo Courtesy of SMART Microsystems Ltd.

ANALYSIS – 2016 was a turning point for the Fan-Out packaging market since both leaders, Apple and TSMC changed the game and may create a trend of acceptance of Fan-Out packages. Yole is analyzing the current market and technologies trends and offers you to discover these results within a new report.

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PROFILE – UTAC is a leading independent provider of semiconductor assembly and test services for a broad range of integrated circuits including analog, mixed-signal, logic, memory and radio frequency. UTAC is the 6th largest OSAT in the world and among full-service assembly and test providers, UTAC's test percent of revenue is the highest in the industry.

MEMBER COMPANY PROFILE

6 APPLICATIONS – Plasma dicing is a chemical-etching process that does not chip or crack the silicon. The gentle dicing process can be controlled to deliver extremely smooth sidewalls and has been proven to yield the highest die strength from all dicing methods.

UTAC





20 TECHNOLOGY – Over the past few years, there has been a significant shift from PCs and notebooks to smartphones and tablets as drivers of advanced packaging innovation. In an industry segment that has grown accustomed to a multitude of package options, consolidation could produce "The Big Five" advanced packaging platforms.

RON HUEMOELLER, ADRIAN ARCEDERA AND RAMA ALAPATI AMKOR TECHNOLOGY

DEPARTMENTS

ANNETTE TENG PROMEX INDUSTRIES

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MEMBER NEWS

► AMKOR COMPLETES QUALIFICATION OF SWIFT[™] PACKAGING FOR ADVANCED MOBILE, NETWORKING & SIP APPLICATIONS

Amkor Technology Inc. has recently announced completion of product qualification for its innovative new Silicon Wafer Integrated Fan-Out Technology (SWIFT[™]). SWIFT is designed to handle the demanding requirements of today's advanced mobile, networking and system-inpackage (SiP) applications.

SWIFT was named the "Device of the Year" at the 3D InCites Awards ceremony in 2016. It was recognized for being "uniquely developed to deliver a high yielding, high-performance package with the thinnest profile in the industry."

SWIFT is targeted for production in the second half of 2017 at K5, Amkor's state-of-the-art manufacturing, research and development center in Incheon, South Korea. www.amkor.com

ASE RECEIVES ISO 26262 CERTIFICATION FOR ITS KAOHSIUNG FACILITY

ASE has announced that its Kaohsiung, Taiwan facility has received the ISO 26262 certification from TÜV NORD, a technical service provider that helps companies to validate the safety of products and services. ISO 26262 is a standard related to the safety of electrical and electronic systems within a car and addresses possible hazards caused by malfunctioning behavior of safety-related systems, including interaction of these systems. www.aseglobal.com

Namics Technologies Announces Plans for New Manufacturing Facility



NAMICS TECHNOLOGIES has developed a plan to construct a new upgraded manufacturing facility on the same property as their current head office factory in Niigata City, Japan. Construction began in March 2016 with completion targeted for April 2017.

The current manufacturing building has been in use for many years and needs to be replaced with an upgraded building that incorporates the latest construction standards for withstanding

natural disasters. The new building will enhance their stability of supply and create an improved manufacturing environment. When the construction of the new building is complete and manufacturing equipment installed, Namics will begin sampling products for qualification of the new facility. Once all products from the new facility have been qualified by their customers, they will decommission the current facility and remove the building.

Namics will maintain product quality and consistency throughout this relocation as all raw materials, type of equipment, operators, manufacturing process flow and parameters, manufacturing environment and outgoing inspection procedures will remain the same for both facilities. In addition, Namics will strictly maintain product traceability of all manufactured lots before. during and after the transition.

Namics is committed to providing the highest quality products with superior support in order to meet their primary goal of total customer satisfaction.

Contact Regional Manager Brian Schmaltz at schmaltz@namics-usa.com or call 408-516-4611 for more information. ◆

Master Bond's Thermally Conductive, High Temperature Resistant Epoxy Passes NASA Low Outgassing Tests

CERTIFIED TO MEET ASTM E595 NASA low outgassing standards, Master Bond EP46HT-2AO Black is well suited for the aerospace, electronic, opto-electronic industries and can be used vacuum environments. This two component system blends thermal stability with a high strength profile for a variety of bonding, sealing and encapsulation applications.

EP46HT-2AO Black combines superior thermal conductivity of 9-10 BTU•in/ft²•hr•°F [1.2981-1.4423 W/(m·K)] and reliable electrical insulation with a volume resistivity exceeding 1014 ohm-cm at room temperature. It has a glass transition temperature of 200-210°C and is serviceable over the wide temperature range of -100°F to +500°F [-73°C to +260°C]. This dimensionally stable system delivers a tensile strength of 6,000-7,000 psi, compressive strength of 26,000-28,000 psi and tensile lap shear strength of 1,400-1,600 psi at 75°F. EP46HT-2AO Black also withstands a variety of chemicals including oils, water, acids, bases and fuels.

Unlike most traditional two part epoxies, EP46HT-2AO Black cures with the addition of



heat, which allows it to have a working life of over 24 hours. It has a forgiving 100 to 30-35 mix ratio by weight and upon mixing, this thixotropic system has a viscosity of 140,000-280,000 cps. It bonds well to metals, composites, glass, ceramics, rubbers and many plastics.

Master Bond EP46HT-2AO Black is thermally conductive and electrically insulative adhesive, sealant and potting compound that meets NASA low outgassing requirements. Read more about Master Bond's heat resistant adhesives at www.masterbond.com or contact Tech Support at technical@masterbond.com. ◆

Industry Veteran Nick Leonardi Joins SMART Microsystems Team to Expand Next Generation MEMS Sensors Packaging and Assembly



NICHOLAS LEONARDI has been retained by SMART Microsystems in the role of Business Development, bringing over 25 years of industry experience with positions ranging from product development and manufacturing to sales and marketing, in start-ups to the Fortune 100. Mr. Leonardi gained valuable technical sales, marketing and applications management experience with companies such as General Electric and National Semiconductor. The transition to business development followed years in manufacturing and development engineering with companies such as LSI Logic and Advanced Micro Devices. Current industry activities include his participation on the MEPTEC Advisory Board, Arizona State University Bio-Medical Engineering School Advisory Board and memberships with other Electronics Industry Organizations. Mr. Leonardi received a B.S. Degree in Materials Engineering from Alfred University, in New York State.

SMART Microsystems has gained momentum and is well positioned in MEMS Packaging and Assembly, supporting demand for next generation sensor related technologies, with focus on Medical, Auto and the Mil/Aero industries.

For more about SMART Microsystems capabilities and services contact Nick Leonardi, Director of Business Development, at nleonardi@ smartmicrosystems.com, call 440-366-4203, or visit the company website at smartmicrosystems.com. ◆

KYOCERA Optical Blood-Flow Sensor is Among World's Smallest for Wearable Devices, Smartphones

KYOCERA CORPORATION HAS announced that it has developed one of the smallest known optical blood-flow sensors, which measures the volume of blood flow in subcutaneous tissue. With the sensor, Kyocera is researching a



variety of mobile health (mHealth) applications such as monitoring stress levels or preventing dehydration, heatstroke and altitude sickness by studying trends or changes in blood-flow volume as alerts for these conditions and developing algorithms for detection.

Leveraging Kyocera's expertise in miniaturization, the sensor – only 1mm high, 1.6mm long and 3.2mm wide – is designed for use in small devices such as mobile phones and wearable devices. The company will offer sensor module samples starting April 2017, and aims to commercialize the technology as a device by March 2018. Visit www.kyocera.com for more information. \blacklozenge



Surface mounted device with delamination (red) along the entire length of several leads. This part would fail per J-STD-020 criteria.

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EXAR APPOINTS DIVISION VP OF CORPORATE QUALITY AND RELIABILITY

Exar Corporation has named David Matteucci Division Vice President of Corporate Quality and Reliability. Mr. Matteucci will be central to managing Exar's Quality and Reliability function as well as supporting tier 1 engagements.

Mr. Matteucci has over 30 years of experience in the semiconductor industry, having held executive positions at Power Integrations, Nano Nexus Inc., Zoran Corporation, Galileo Technology, National Semiconductor, as well as previously at Exar Corporation, where he served as Vice President of Operations Engineering and Quality and Reliability. www.exar.com

TESSERA HOLDING CORP. COMPLETES ACQUISITION OF DTS

Tessera Holding Corporation announced that it has completed the acquisition of DTS, Inc. The Company's combined portfolio of products and technologies uniquely positions it to deliver smart sight and sound solutions and nextgeneration 3D semiconductor interconnect solutions for mobile devices, consumer electronics, and automotive markets - while also addressing the growing potential of emerging technologies such as IoT and AR/VR. The Company's team of world-class engineers will focus on the vision of creating core technologies that power intelligent, immersive and personalized digital experiences.

tesseraholdingcorporation.com

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Intel Unveils Compute Card, a Credit Card-Sized Compute Platform

INTEL HAS ANNOUNCED

a new modular compute platform called the Intel® Compute Card along with a range of partners who will be working with Intel to help accelerate the ecosystem of solutions based on the Intel Compute Card. Intel has been a leader in delivering technology to help realize the benefits of the Internet of Things and enable more smart and connected devices. The Intel Compute Card is being developed with that in mind, to transform the way compute and connectivity can be integrated and used in future devices.

The Intel Compute Card has all the elements of a full computer, including Intel SoC, memory, storage and wireless connectivity with flexible I/O options so hard-

ware manufacturers can optimize for their

Intel. particular solutions - from interactive refrigerators and smart kiosks to security cameras and IoT gateways. Device makers simply design a standard Intel Compute Card slot into their device and then utilize the best Intel Compute Card for their performance and price needs. This reduces the time and resources needed to design and validate the compute block and helps speed up innovation to bring the power of intelligence into an ever wider range of devices.

Intel is working with a wide range of partners who share their vision that the Intel Compute Card could significantly change the way they and the rest of the industry design and productize a wide range of solutions in the near future. The Intel Compute Card will be available in mid 2017 and

be available in mid-2017 and will come with a range of processors options, including the latest 7th Gen Intel[®] Core[™] processors. For more information and to stay up to date on the Intel Compute Card, visit www.intel.com/ ComputeCard. ◆

Mendoza Elected Chairman of JEDEC Microelectronics Committee

BEN MENDOZA, VICE President and General Manager of Golden Altos Corporation, and newly elected Chairman of the JEDEC JC-13.2 Microelectronic Devices Committee, begins his term at this month's JEDEC meeting in San Antonio, Texas.

Joining JEDEC in the 1990s, Mr. Mendoza began representing the semiconductor industry and now leads the microelectronic devices section of this Government Liaison committee. In addition to being a member of JEDEC, Mr. Mendoza participates in other industry task groups. These include Copper Wire (Bonding), Plastic Encapsulated Microcircuits Flow for Space Applications, and the Mission Assurance Improvement Working Group. \blacklozenge

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MST Expands Its Sales Organization for US East Coast

THE MICRO SYSTEMS TECHNOLOGIES (MST) Group, a global provider of innovative components and manufacturing services for high-reliability / highperformance industries, such as medical technology and aerospace & defense has experienced strong market growth in recent years. The group's customer focused strategy and growing demand have resulted in a decision to expand their US organization. MST is pleased to welcome Robert F. Baker to the company.

Effective October 10, 2016, Robert F. Baker was appointed Eastern Regional Account Manager for Micro Systems Technologies, Inc. Prior to joining MST, Robert was Business Development Manager for Janco Electronics, Inc. Bringing a wealth of relevant industry technical experience to the company, Robert will focus his sales and technical support activities in the Eastern United States.

Visit www.mst.com for more information about Micro Systems Technologies products and services. \blacklozenge

SMART Microsystems Purchases Mitutoyo Programmable Measurement System for MEMS Sensors Packaging



SMART MICROSYSTEMS HAS announced the recent purchase of a new Mitutoyo Quick Vision ELF Coordinate Measurement Machine (CMM). As an ISO9001 certified supplier to their valued customers, SMART has an obligation to insure, monitor, and maintain the quality of all incoming materials. This highly accurate programmable non-contact and contact measurement system will allow SMART to measure and certify incoming material in a fraction of the time it would take by conventional means. Lot basis geometric measurements can be performed in minutes. With machine accuracy greater than 2+3L/1000, they will also be using this system to perform contract precision measurement services to customers at a highly competitive rate with very rapid turnaround times.

SMART Microsystems creates turnkey solutions for microelectronic package assembly challenges to move your MEMS sensor technology from development to production. With an engineering team experienced in manufacturing and state-of-the-art facilities, SMART Microsystems accelerates the transition of your new MEMS sensor product to the market.

For more about SMART Microsystems capabilities and services contact Nick Leonardi, Director of Business Development, at nleonardi@smartmicrosystems. com, call 440-366-4203, or visit the company website at smartmicrosystems.com.



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COLUMN

COUPLING & CROSSTALK



By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Quality, Meet Safety & Security!

▶ WHAT CAN BE SIMPLER TO specify or install than a light bulb controlled by a wall switch? Overengineered versions, especially when developed without engineers, can really cause you to lose sleep. However, the real nightmare is the danger of simple products being hijacked by the Internet.

What keeps me up at night? Many things... When I'm focused on a client's product requirements, it is making sure they match true market needs. Plus, dozens of other non-work related things like my children, the recent presidential election, the economy, ... Thankfully I easily fall asleep shortly after my mind starts to rundown this very long list.

What *actually* kept me awake on my recent business trip? Poor product quality, improper system design, and a lack of planning for failure. At a brand-new hotel the fancy multi-button bedside controls for the room lights and curtains failed in two different rooms. In the first room, the lights would intermittently not switch off. And in the second room, the multiple ceiling mounted spotlights over the bed would not switch off - at all when I attempted to go to sleep. There was a considerable delay at midnight to get a maintenance person to disconnect the wiring in the hidden electrical control panel. Unlike a desktop or floor lamp, these lights were too difficult to reach to unplug or unscrew without a ladder. I admit I was not thinking kind thoughts at that moment about the engineer who designed the system, the supplier of the

system, nor the company that installed it.

This may have been both a quality control failure or "escape" at the supplier and at the time of installation. Quality is essential for any product or service. It is critical to determine how to assess and control the quality of any manufacturing or delivery process. Without proper quality systems, one does not know if the process is out of control which may result in big surprises later on. In the case of the hotel lights, it is clear that there was a quality failure – either in the physical hardware or during installation - since the system was clearly not operating as designed. Or, at least, how most "reasonable" users would expect. Perhaps there was a local tradition of punishing those who go to bed after 11 PM?

Luckily, enlightened product managers and designers do place quality on their list of product requirements. **But do they always add safety and security?** It depends on the perceived risk and complexity of the product in addition to regulatory requirements (if any). Where most will agree that quality control is an essential cost – especially when in the long run it may save money – some tradeoff or fail to consider safety and security in order to reduce cost.

In the case of the hotel lighting system failure, there was clearly a lack of quality in the design process at either the control system or hotel design level since the designers failed to consider the system failure modes. (Who knows if there were actual engineers on the design team?) [And yes, this is a recursive thought since there is both quality of the manufacturing and delivery process in addition to the quality of the design process itself.] Done properly the system design would have included a Failure Mode Effect Analysis (FMEA) to identify most, if not all, possible failure modes along with countermeasures to eliminate or reduce the impact of the failures. Clearly the system was not designed to fail in a "safe mode".

Failure of a switch? Use another switch for the same function. Failure of a curtain motor? Manually close the curtain. Failure of the logic control system? If the system could detect this, it should have turned itself off. But not every device can be "self aware" to detect proper operation. This is where the designers failed to provide a way for the user – not the maintenance technician – to override the system. Yes, there was a "Master" switch bedside but it was a master on/off "request" switch versus one that actually removed power from the entire system. Requiring a screwdriver to remove the back panel of the closet to access the logic control system to unscrew wires is neither user friendly nor the best design. This approach may have enabled the product or the system installation to hit the desired aesthetic and cost targets, but clearly it wasn't designed for failure.

Many organizations "design" or plan for success but they don't consider designing for failures in quality, safety, or security. We have come a long way in product design over the last twenty years. However, it is not clear that progress has been made in a user's ability to remove the power source from many electronic devices. In the "real old days" of vacuum tubes almost all devices had a true "Mains" switch that cut the input power to the power transformer -i.e. the same as unplugging it. Because we are impatient and desire "instant television", sets moved from truly turning off to going into standby mode. The television was really on (consuming power keeping the tubes powered up) but simply not displaying a picture on the cathode ray tube (CRT) to eliminate the need to "warm up". Today, LCD screens use very little energy so there is little concern about them being powered up all the time. Since most new TV's are connected to the Internet, perhaps we should instead worry about their capability of watching the viewers! (Read again: George Orwell's 1984.)

History has repeated itself with smartphones. In the quest for making them thinner and smaller, most leading brands have removed the ability to remove the battery. Smartphones are never really off and a "hard reset" is a request to reset versus a true power on/off cycle. As Samsung just discovered with the Note 7 battery issues, changing to a non-removable battery led to their being banned from airplanes as these phones could not be safely carried in a true "power off" state.

As products and devices become more complicated, the digital circuitry and software become significantly difficult to thoroughly test. As such, the probability of security holes, test escapes, or latent defects (possibly introduced after test) increase with complexity. Even presuming robust quality and security processes, defects will occur. Therefore, it is essential for products to "fail safe" with unam-

biguous methods so that a user can shut down or reset a compromised or malfunctioning device. Without these capabilities, beyond mere inconveniences, we are putting ourselves at grave risk as the number of autonomous devices increase by the day - everything from self-driving cars to drones. This risk is compounded by the sheer number of devices that comprise the Internet of Things (IoT). The recent distributed denial of service (DDoS) attacks using approximately 100,000 compromised web and security cameras demonstrated the power of a small number (relative to the projected billions of the IoT) of simple devices. It is estimated that there are over half a million of these infected devices due to the manufacturer(s) shipping them with the same default password and the users choosing not to change them

Researchers at the Weizmann Institute of Science recently demonstrated the ability to spread a worm among Internet connected light bulbs via their ZigBee mesh radio network. The worm allowed them to take control of the light bulbs and to spread to neighboring bulbs that were not

configured on the same network. In this case, the researchers were able to bypass the manufacturer's security using sophisticated techniques. They speculated on the ability to use a similar security breach to cause mayhem from power grid failures to epileptic seizure. In theory, these bulbs are simpler "things" than web and security cameras with no user controlled security features.

Combine these issues and add paranoia to keep us all up at night? How about a worm/virus that takes control of your smartphone and changes the battery charging parameters causing your battery to exploding or ignite?

In the development and design process, product designers, engineers, and product managers need to think about failure modes and ways to make their products safe and secure. We need to add security and safety to design for manufacturing, quality, support, etc. that is known as "DFx". Beyond making a product elegant and intuitive to use, the design team needs to worry about how their product could be misused and what to do in case things go wrong. As it is said "Murphy was an optimist"...

In industries and product categories that do not have governmental nor voluntary safety and security standards, another role(s) should be added to the crossfunctional design team to focus on safety and security. Either an internal resource or, better yet, an external resource who can provide the required perspective and breadth of experience to take an independent view is required. Yes, quality has fought hard for a seat at the product development table and now it is time for safety and security to join too!

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. \blacklozenge

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COLUMN

INDUSTRY INSIGHTS



By Ron Jones

They're Still Dancing

A YEAR AGO, I WROTE AN ARTICLE titled "Who's Next on the Dance Floor." It's focus was on the rapid rise in the level of M&A activity in the semiconductor industry.

For several years, semiconductor M&A had been averaging about \$12 billion per year. (See Table 1.)

Year	Semi M&A
2010	\$ 7.7 B
2011	\$ 17.0 B
2012	\$ 8.5 B
2013	\$ 11.5 B
2014	\$ 16.9 B
2015 (approx.)	\$120.0 B
Table 1.	Source: IC Insights

I added up the deals in November, 2015 and the total was just north of \$100 billion. You can't get an exact count because not all deal sizes are disclosed and there is a time lapse between when deals are announced and when they close ... or don't close. It's a bit like counting a room full of white cats. The general consensus is 2015 came in around \$120 billion.

I don't think there was any expectation that deals would stop just because we rolled from 2015 to 2016 . . . and that was indeed the case.

It is the end of the year again and the M&A tally is shown in the Table 2.

At this point in time, it looks like 2016 will be similar to 2015 in number of deals in each size category and in total dollars. I excluded smaller deals that had no given deal size. (See Table 3.

As last year, the growth to some degree is driven by trends that have been going on for years, such as the increasing cost of mask sets. It is not unusual for leading edge designs to run in excess of \$100 million, and that is just for the

Acquirer	Acquiree	Amount
ON	Anadigics	\$32 M
Microsemi	PMC-Sierra	\$2,500 M
Micron Tech	Inotera Memories	\$3,200 M
Microchip Tech	Atmel	\$3,600 M
Sony	Altair Semiconductor	\$220 M
Cisco Systems	Leaba Semiconductor	\$320 M
GigOptics	Magnum	\$54 M
Cypress	Broadcom wireless IoT	\$550 M
Cavium	QLogic	\$1,360 M
Softbank	ARM, Inc.	\$32,000 M
Analog Devices	Linear Tech Corp (LTC)	\$14,800 M
Renesas	Intersil	\$3,200 M
Beijing Mgmt	Analolgix	\$500 M
Inphi	Clarify	\$275 M
Qualcomm	NXP	\$38,500 M
TOTAL		\$101,111 M

Table 2.

masks. Many designs continue to go up in complexity, taking them beyond the technical reach of smaller fabless companies.

The Internet of Things (IoT) and other smart technologies are continuing to grow and are becoming a focus for a lot of companies. To that end, companies are acquiring other companies that have enabling products, technology or IP to position them for a market that is expected to experience rapid growth. It is not a matter of whether IoT will happen, but rather in what myriad configurations it will reveal itself and how quickly it will grow over the next several years.

A new driver this year is the rapid rise in smart, autonomous vehicles of all sizes. Great strides have been made in the last year and lots of companies

2015	2016
4	3
5	5
4	7
	2015 4 5 4

(Top 3 accounted for almost 85%)

Table 3. Number of Deals by Deal Size

Source: GSA Market Watch and Press Releases

want to get a piece of the pie. I believe the major factor in Qualcomm's decision to acquire NXP is its penetration in the automotive market to bolster Qualcomm's small presence.

Having been in the industry for several decades and watching the fabless model create hundreds and hundreds of new companies over the past 25 years, it is interesting to watch as consolidation reverses the trend to some degree with a growing number of mega fabless/IDM companies. Nothing is forever . . . except change. \blacklozenge

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Visit www.n-ablegroup.com or email ron.jones@n-ablegroup.com for more information.

ANALYSIS

Will Fan-Out Packaging be Sustainable Long-Term?

Jean-Christophe Eloy Yole Développement

2016 WAS A TURNING POINT FOR the Fan-Out packaging market since both leaders, Apple and TSMC changed the game and may create a trend of acceptance of Fan-Out packages. Yole Développement (Yole) is analyzing the current market and technologies trends and offers you to discover these results within a new report entitled *Fan-Out: Technologies & Market Trends 2016.*

TSMC investment in Fan-Out Wafer Level Packaging (FOWLP) and development of its Integrated Fan-Out (InFO) changed the wafer level packaging (WLP) landscape. Following high volume adoption of InFO and further development of embedded Wafer Level Ball grid array (eWLB) technology, a wave of new players and FO WLP technologies may enter the market. TSMC's FO WLP solution called InFO will be used to package the Apple A10 application processor, implemented in the new iPhone 7 series... The success of FO packaging platforms is so undeniable today. What will be the status of the market tomorrow? What are the next steps of the leading FO players? Which technology will be the winning solutions?

"Production starts in 2016 and represents a big change in the Fan-Out industry for several reasons", confirms Jérôme Azémar, Market & Technology Analyst, Advanced Packaging & Manufacturing at Yole. And he explains:

- First of all, in terms of volume, capturing the Apple processor market is a big asset for Fan-Out technology. iPhone 7 phones are expected to be sold in more than 200 million units.
- In terms of technology capability,

Fan-Out History: A Long Development and a Recent Hype



Source: Fan-Out Technologies & Market Trends 2016 report, Yole Développement.

it is also a major turn: processors require thousands of connections while the FO market was essentially focused on limited IO count applications so far.

• Eventually, the potential for market spread is very high: the Apple brand brings more interest to the FO platform.

According to Yole's advanced packaging & semiconductor manufacturing team, the market will actually be split into two types:

- The "core" market of FO, including single die applications such as Baseband, Power management, RF transceivers, etc. This is the main pool for FO WLP solutions and will keep growing.
- The "high-density" FO market, started by Apple application processor engine (APE) that will include larger I/O count applications such as proces-

sors, memories, etc. This market is more uncertain and will require new integration solutions and high performing FO packages but has a very high potential.

Apart from TSMC, STATS ChipPAC is willing to make further investments powered by JCET, ASE extends its partnership with Deca Technologies while Amkor, SPIL, and Powertech are in development phase eyeing future production. Samsung is seemingly lagging behind and is considering its options to raise competitiveness.

"With such a high potential for the high-density FO and solid growth of the core FO, the supply chain is also expected to evolve with a considerable amount of investment in Fan-Out packaging capabilities", asserts Jérôme Azemar from Yole. Several players are already offering FO WLP while many others are developing their competitive Fan-Out platforms to enter the Fan-Out landscape and enlarge their portfolio.

PROFILE



UTAC HOLDINGS LTD AND ITS

subsidiaries (UTAC), is a leading independent provider of semiconductor assembly and test services for a broad range of integrated circuits including analog, mixed-signal, logic, memory and radio frequency. UTAC is the 6th largest OSAT in the world and among full-service assembly and test providers, UTAC's test percent of revenue is the highest in the industry.

The Group offers a full range of package and test development, engineering and manufacturing services and solutions to customers who are primarily integrated device manufacturers (IDMs), fabless semiconductor companies, and wafer foundries.

First established in 1997, the Group's customers span across all vertical markets including: mobile phone and communication, consumer, computing, automotive, security banking, and security identity, industrial and medical applications. Striving to maintain diversity across end markets not only helps to provide balance in the ebb & flow of product demand, it also positions them for growth in the overall industry with significant benefits from the proliferation of the Internet of Things (IoT).

As more devices become connected to the IoT, the need to safeguard information from cyber assaults is driving an increased demand for secure creation and management of devices and data. As a leading supplier of assembly and test services, UTAC plays a vital role in their customer's manufacturing flow. Similar to quality initiatives, security compliance is regulated using industry standards and is administered at the UTAC corporate level. Today, 50% of UTAC's factories are certified with EAL 6 / ISO standard ISO1540.



UTAC - SINGAPORE - TEST CENTER OF EXCELLENCE

- Experienced Team (average years on the job) Final Test, Wafer Probe & Post-Test Processes:
 Engineering Managers 15 Years & Test Engineers 10 Years
- World Class Systems for OEE & Factory Systems with Online & Offline Engineering Analysis
- Operations with intrinsic ownership for Quality & Pervasive Continuous Improvement Culture.
- Proven Project Management methodology used for NPI Qualification, Safe Launch, Pre/Mass Production Release
- Driving on-going Innovations, Benchmarking & Value Creations with solide alignment with ATE & Systems Solutions Suppliers
- Wide range of configurations for Components, Integrated & Complex RF/Mixed Signal testing solutions
- Sophisticated and Competitive Technical Roadmap for higher pin count and higher parallelism
- Superior WLCSP engineering experience including BSP, Side-Wall Protection & AVI/EOL

Medical / Automotive / Consumer / Industrial / Mobile Phone / Security



KEY FACTS & FIGURES

- Revenue \$878 M (2015)
- Established in 1997
- HQ in Singapore
- Operations in 6 countries, 10 factories
- Approximately 12,000 employees

QFN Dual Row

• Worldwide Sales Team

QFN Single Row

• Services: Assembly 65% / Test 35%

KEY SERVICES

- Assembly Research & Development
- Package Assembly
- Test Engineering & Development
- Test Services
- Quality Assurance
- Reliability & Failure Analysis
- End of Line & Drop Ship



Flip Chip QFN

Expose Die fcQFN



Top Expose Pad QFN



ASSEMBLY SERVICES

UTAC offers a wide range of semiconductor assembly services to meet customers' needs and the increasing market demand for next generation devices. UTAC has a diverse capability spanning across ten factories, in six countries in the Asia Pacific region. Their packaging capability includes Leadless Packages, Wafer Level Packages, System in Package (SiP), Laminate Packages, Leaded Packages and Security Smart Card Module and Smart Card Inlay.

To complement their packaging solutions they have state-of-the-art design and package characterization capabilities to help customers achieve both performance and cost objectives. UTAC engineering teams collaborate closely with customers to understand the performance requirements and utilize proprietary calculators and design tools to accelerate the package design phase. Once the design is approved, UTAC uses a proven project management methodology to facilitate the new product introduction, taking the product through a rigorous phase gate process to ensure first time qualification.

TEST SERVICES

UTAC is a world leader in integrated circuits testing with more than 1,600 installed testers and a team of more than 300 experienced test engineers. Among full-service assembly and test providers, UTAC's test percent of revenue is the highest in the industry. UTAC has wafer sort and final test capability in every factory location to provide a full-turnkey product flow.

UTAC has extensive experience and capability to test all semiconductor device types in the industry: analog, mixed signal, logic, memory, CMOS image sensors, accelerometer MEMS sensors, radio frequency (RF) for radar, near field communications (NFC) and other RFID devices. Their test solutions include wafer probe (ambient, hot and cold), security black box wafer level encryption, final test, O/S test, reliability and failure analysis. With a centralized test development engineering team, UTAC provides test development (TD) services to customers worldwide. TD engineers work closely with customers to reduce costs and streamline process flows by ensuring test programs are optimized with the most effective test coverage and enable the shortest test times.





D2-fcFBGA (Hybrid)

Smart Card Module



LGA-SiP (Multichip RF)



Cu Clip QFN Module 2 FET + Clip + Controller







UTAC is a world leader in IC testing with more than 1,600 installed testers and a team of more than 300 experienced test engineers. *Photo: UTAC Test Operation in Thailand.*

PROFILE

UTAC'S OFFERINGS

Assembly Capability

- Leadless Packages: QFN, multi-row QFN, thin QFN, side-lead plating QFN, Cavity QFN, MEMS, Image Sensor and Cu Clip/ Power
- Wafer Level Packages: wafer thinning, protective coating, saw & laser dicing
- System in Package (SiP): Laminate, Leadless, FC-SiP, QFN-SiP, Multi-Die SiP
- Laminate Packages: PBGA, FCBGA, CSP, FBGA, WCSP,
- Leaded Packages: PDIP, SOT, SOIC, TO, QFP Laser Diode
- Smart Card Module Assembly & Inlay w/ EAL 6 Common Criteria Site Certification



Test Services

- High Volume Wafer Probe (Tri-Temp)
- High Volume Final Test (Tri-Temp)
- Security Black Box Testing/Encryption w/ EAL 6 Site Level Certification
- Burn-In Services
- Reliability & Failure Analysis Testing
- Production & Package Qualification

Research & Development (Assembly / Test)

- Package Design Consultation
- Thermal, Mechanical & Electrical Modelling
- Package Prototyping
- Material Selection & Benchmarking
- Test Program Development
- Test Program Conversion
- Test Hardware Design & Layout



UTAC Design Centers provide one-stop design service for full range of packages.

SOLUTIONS & PARTNERS

- 3-D Embedded Partners
- WLCSP Fan-In, Fan–Out and Solder Pillar Bump



UTAC has established agreements with several IC Bump companies to provide seamless, complete turnkey backend solutions for Fan-In and Fan-Out WLCSP as well as Solder Pillar Bump for Flip Chip. This seamless solution begins with state-of-the-art Bump technology through UTAC Wafer Sort, End-of-Line Processing and Ship.



UTAC GROWTH MILESTONES

1997 United Test & Assembly Center Incorporated in Singapore (UTAC)

- 1998 Developed memory & DRAM turnkey test & assembly services
- 1999 Acquired test operations Fujitsu Microelectronics Asia
 - **2003** Established China footprint in Shanghai
 - **2005** Acquired Ultra Corp. to establish presence in Taiwan and add memory test and assembly services
 - **2006** Acquired NS Electronics Bangkok to penetrate the Analog assembly market
 - **2010** Acquired ASAT and its subsidiary in Dongguan, to enhance China footprint
- **2014** Acquired 3 Panasonic Plants; Singapore, Malaysia, & Indonesia; Launched Japan Sales Region and Offices
- **2015** Organic growth through product development and site certifications in key areas: MEMS, Cu Clip, Automotive & Security

2016 Qualification & high volume production ramp: MEMS, GQFN, Cu Clip, Automotive (SLP), & Security products: Smart Card Inlay, Smart Card Module, Secure IC Encryption Wafer Sort

UTAC FACILITY SNAPSHOT

Continues

Dongguan, China

Package Type

- QFN
- QFP
- FPBGA
- FCQFN
- MODULE
- LGA

Operational Certs:

OHSAS18001, ISO14001, ISO9001:4003, TS16949, QC08000

Shanghai, China

Package Type:

- LGA
- BGA
- QFN

Operational Certs:

ISO 9001:2005, ISO 14001:2008, OHSAS18001:2012

Karawang, Indonesia

- Package Type:
- QFP
- SOP
- TO
- F-LD
- TAPE/TAG

Operational Certs:

ISO9001 (1999), ISO14001 (2000), ISO27001 (2009), OHSAS18000 (2011), EAL 6 Site

Malacca, Malaysia

Package Type: • SOT(SMD)

- TO(Power)
- nonational Co

Operational Certs: ISO9001:2008 (2012), TS16949:2009 (2012), ISO14001:2004 (2013),

ISO18001:2007

Serangoon, Singapore

Package Type:

- WLCSP
- FCCSP
- FCCSP 95mm Singulation Saw
- Cap
- FCBGA
- BGA

• COB/CVM

Operational Certs:

ISO 9001, TS16949, ISO14001,18001, AEC-Q100, ISO/IEC27001, ISO/IEC17025, EAL 6 Site

Ang Mo Kio, Singapore

Package Type:

- CLCC/LGA
- BGA
- QFN
- SOP
- LDHU
- TO

Operational Certs:

ISO9001:2008, S16949:2009, ISO14001:2004, O18001:2007

Bangkok, Thailand

Package Type:

- QFN
- FCQFN
- GQFN
- SMD
- FCSMD

Operational Certs:

OHSAS18001, ROHS, Certified Sony Green Partner, TS16949, ISO14001, EAL 6 Site

Hsinchu City, Taiwan

Package Type:

- WLCSP
- BGA
- LGA

Operational Certs:

ISO9001/QS9000, OHSAS18001, TQM, ISO14000, QC080000, ISO9001, ISO/TS16949, ANSI ESD S20.20

APPLICATIONS

Die Attach Film Applications

Annette Teng Chief Technology Officer Promex Industries

DIE ATTACH FILM (DAF) AND DICING die attach film (DDAF) have been commercially available since 2000. Epoxy paste adhesives have historically been the sole epoxy material available for die attach, an integral part of component assembly, in particular for wire-bonded devices, but not quite applicable for flip chip assembly. DAF and DDAF are epoxy adhesives which are film based instead of paste based and are attached to the back of the wafer prior to dicing. DAF is sold by the supplier without a support dicing tape, whereas DDAF is sold by the supplier on a stretchable support dicing tape which is partially sawn and subsequently poked by ejector needles during automated die pick. DDAF has gained popularity due to the many advantages of film over paste, driven especially by the growth of stacked die architecture. Because there is no re-shaping of adhesive material from a drop-shape to a thin 2 dimensional layer, the process window for film is much wider than for paste material. Engineering intensive processes to control fillet shape, overflow, under-coverage and voiding are eliminated by the use of films. For very thin dies as well as for stacked dies, it is imperative to use film.

There are a handful of suppliers of wafer level DAF. Major suppliers provide the circular DAF sheets in rolls for automatic machine lamination such as shown in Figure 1. DAF can also be sourced as sheets for non-automated lamination. DDAF and DAF material have a shelf life of 6 to 12 months when stored at 0-10°C. They can also be stored at room temperature, but the expiration date is shortened by about half. Hence, the material is only made to order and major suppliers impose a minimum order of up to 300 sheets or 3 rolls. A nonconductive 8" DDAF is around \$8/wafer but the conductive version is an order of magnitude higher in cost. One major



Figure 1. Photo provided by Lintec.



Figure 2. 7-die stack with high thermal conductive DAF.



Figure 3. DDAF dicing on dual spindle saw.

manufacturer that has a silver filled DAF product will only sell to high volume users offshore. This limit on suppliers can make DAF less cost effective unless they use a subcontractor who has a wellstocked inventory. The cost per wafer of silver filled DAF may be higher, but with the savings in process steps and yield improvement, the cost is very comparable to paste.

Currently both conductive and nonconductive DDAF films are commercially available at various thicknesses. Most suppliers provide 20 to 25μ m as a standard thickness option. Lower $10\mu m$ thickness DAF is available but maybe a challenge to procure for low volume users. Electrically and thermally conductive silver filled films are also available at 20-25 μ m thickness and have been deployed at Promex for many QFN device assemblies. QFNs with silver DDAF have passed JEDEC MSL3 for 8x8mm QFN from Promex. However, many high-end applications require higher thermal conductivity and have resorted to DAF with diamond fillers instead.

Promex has been assembling multidie stacks with diamond filled DAF successfully. Figure 2 shows a cross-section of a 7-die stack die device using a diamond filled film. The silicon wafers have been thinned to 200μ m before laminating onto the diamond filled DAF. The die on the device wafers with DAF were singulated using a dual spindle dicing saw as shown in Figure 3. Saws with single spindle are not recommended as adhesive stringers and conjoining of die may result. After singulation, die attach using a Datacon 2200 with a heated stage was performed. Each die is pressed down on a heated substrate at a force recommended by the supplier which keeps the die firmly anchored in place. An example of a wafer with silver epoxy DAF during Datacon pick is shown in Figure 4. All DAF'ed die must be subsequently cured at higher temperatures around 150-165°C for 1 hour. One of the biggest advantage of film over paste is the absence of outgassing or void formation during oven



Figure 4. Singulated die on Silver filled DDAF being picked by the Datacon.

cure. The effect on die tilt and die shifting caused by void formation has been a challenge for paste users, particularly for large dies. The bondlines of stacked die of various DAF brands after cure are found to be consistently uniform.

High yield can be attained by good quality control of DDAF material and wafer backside cleanliness. Contaminants either from mishandled DAF or a mishandled wafer can result in problems with missing adhesive film as shown in



Figure 5. Adhesive presence on backside of die.

Figure 5. Poor adhesion may be traced to contaminants such as polydimethylsiloxane (PDMS)^[1] which can be removed by Argon gas plasma cleaning. A pass/ fail criteria set at greater than 95% DAF visible on die backside is acceptable for good die shear strength.

Wafers with DAF that are diced with improper dicing parameters may exhibit adhesive stringers in the saw streets as shown Fig 6. This is rejectable as the stringers may cover bond pad openings



Figure 6. DAF stringer.

affecting wirebond integrity. Saw dicing parameters must be optimized to eliminate such stringers. Another reject is conjoined die found during pick which is caused by inadequate adhesive singulation due to improper blade depth or worn out blades. Lasers can be used for the singulation of DAF wafers however, this is only cost effective for high volume manufacturing.

Die attach films can also be applied to non-die attach processes such as lid

ADVANTAGE COM	PARISON	DIE ATTACH FILM	DIE ATTACH PASTE
Paste Dispense machine set-up Requirement of dies/wafers		None (less set-up dies)	Engineering intensive & more set-up dies/wafers
Batch oven curing 1hr at 150C-165C UPH improvement		Partial cure OK with full cure during wirebond	Must Cure 100% prior to wirebond
Die to pad size ratio		1.0	Less than 0.9
Die strength during pick		Reinforced by DAF	No reinforcement
Wafer warpage during handling		Reinforced by DAF	No reinforcement
Bondline		Consistent	Must monitor
Die pick Issues	Con-joined dies Missing adhesive Stringers	Must control during saw Must control during prep Must control during saw	None None None
Die tilt and fillet issues		None	Must monitor
Pot life before cure		Hours/day	Minutes<4hrs
DA Cure Issues	Voiding Bleed out Shrinkage at corners	None None None	Must control Must control Must dispense proper amount

Table 1.

APPLICATIONS

sealing and wafer bonding. At Quik-pak, where Open molded cavity plastic packages (OmPP) are made in array form as shown in Figure 7, various DAF materials were evaluated for sealing a large panel lid. OmPP are made by molding walls on QFN lead frames with standard thermoset mold compounds. OmPP packages can be temporarily sealed to provide engineers with the flexibility to test and debug rapidly. They can also be effectively overmolded by dispensing epoxy to fill the cavity and curing. And, these cavity packages can be lid-sealed for MEMS and sensor products. Lid sealing can be done either individually or in panel form utilizing DAF, with a preference for the latter for cost savings.

A comparison of 5 DAF types from several suppliers showed one DAF type that produced 100% yield on lid seal integrity. For each DAF type, a panel of OmPP packages, namely, QFNs, was panel lid sealed under thermal compression and then saw singulated. One DAF product yielded 108/108 pass on visual in 10X magnification with no voids on all 4 sides of the singulated QFNs. Figures 8a and 8b shows the sidewall of the ceramic lid over the QFN with a very uniform bondline of 20-25 μ m in thickness of DAF. 15/15 units passed after been subjected to a Fluorinert[™] leak test (Mil. Std. 883 Method 1014 Condition C1) with no preconditioning to catch leakers by the presence of escaping bubbles.

Furthermore, lid shear of the lidded QFN showed high strength with adhesive fracture as revealed by adhesive residues



Figure 7.



Figure 8a.



Figure 8b.

on both lid and package surfaces (Figure 9). Table 2 shows the lid shear results in excess of 10Kg for a 28 leaded OmPP QFN package.



Figure 9.

Sample	Force (Kgf)
1	14.831
2	11.588
3	13.370

Table 2. Lid shear results in excess of 10Kgfor a 28 leaded OmPP QFN package.

Summary and Conclusion

In this article, DAF is shown to be well established as a standard die attach material and can also work as a lid seal material for open cavity panels. Many types of DAF, including silver filled electrically conductive, diamond filled thermally conductive as well as nonconductive DAF for various complex microelectronic assemblies have been successfully implemented. \blacklozenge

References

[1] "Delamination from Process Induced Sources" A. Teng C., IEEE Electronic Component & Technology Conference, San Diego, June 1-4, 1999

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Wednesday, February 15, 2017 | 8:00am-9:00am Mary (Missy) Cummings, Naval Officer, Military Pilot & Professor, Duke University

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Five Industry-Leading Packaging Technologies

IC packages for implementing next-generation devices to support the connected world of the future

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OVER THE PAST FEW YEARS, THERE has been a significant shift from PCs and notebooks to smartphones and tablets as drivers of advanced packaging innovation. In an industry segment that has grown accustomed to a multitude of package options, consolidation could produce "The Big Five" advanced packaging platforms. These include low-cost flip chip, wafer-level chip-scale package (WLCSP), microelectromechanical systems (MEMS), laminate-based advanced system-in-package (SiP) and wafer-based advanced SiP designs. (See Determining the Big Five below.)

Low-Cost Flip Chip

Unlike the other four platforms, flip chip is not a package platform, but an interconnect method that uses bumps instead of wire bonds to connect the various circuits as well as attach the die to a package substrate. In the case of flip chip, connections are formed over the surface of the die area rather than at the package perimeter, as is the case with wire bonds. Flip-chip technology enables several ball grid array package families. Although WLCSP also uses interconnect bumps, the main distinction between a WLCSP and a flip-chip package is that the after the bump process, the WLCSP die is mounted directly on the printed circuit board and does not have a package substrate.

While WLCSP has been the go-to package of choice to meet mobile product requirements, WLCSP reaches a point where it is limited by its die size and the number of I/O it can support. According to Yole Développement, that magic number is roughly 500, typically in an 8 x 8 mm² package. Many industry analysts view fanout wafer-level packaging (FOWLP) as the solution to the increased I/O problem, since it enables higher density by expanding the footprint to slightly larger than the die size - and has lower cost than the flipchip alternative today. However, emerging low-cost flip-chip solutions will provide more viable alternatives and create the

next package platform to pick up where WLCSP leaves off.

Associating "low cost" with "flip chip" may seem like an oxymoron because the early adopters of flip-chip packages were high-performance devices like CPUs, graphical processing units (GPUs) and chipsets. However, as flip-chip processes have matured, the associated costs have been reduced, while still maintaining the performance benefits, making it the ideal platform for other IC technologies such as RF, FPGAs, ASICs, memory, CMOS image sensors, LEDs, and more. In fact, the newest low-cost flip-chip solutions are not only very cost competitive to FOWLP, but they are also competitive in thinness as newer methods are implemented.

Additionally, despite the recent hype regarding FOWLP, it is important to remember that low-cost flip-chip packages are currently dominating the advanced packaging market. Why? Because it's still a better choice than FOWLP for most applications. In fact, FOWLP is cur-

To zero in on "the Big Five" semiconductor packaging technologies, a team of packaging experts identified five key platforms that they believe will be leveraged across a multitude of applications and markets both now and in the future. The selected platforms are currently in different stages of adoption and production, and will hold up through generations of development to continue serving the industry needs. The figure shown at right lists the market seqments (mobility, Internet of Things (IoT), automotive, high-performance computing (HPC) and memory) and identifies which markets are served by one or more of these platforms.



The Big Five packages target different market segments.

DETERMINING THE BIG FIVE



Figure 1. As package to die ratio increases, there is more disparity between the FOWLP and fcCSP.

rently only suited to a small percentage of mobile, wireless, medical and military applications.

While many industry analysts proselytize FOWLPs as a lower-cost alternative to WLCSP than flip-chip CSPs (FCCSPs), FOWLP is lower cost only when the ratio of the package body size to the die size is nearly the same or only slightly larger. Figure 1 illustrates this relationship. The cost of the redistribution layer (RDL) is integral to the overall cost of the package. Standard WLCSP has the lowest-cost RDL impact, although as previously mentioned, its package size is limited to die size only. As the ratio of body size to die size increases, low-cost FCCSP structures become more favorable from a price point perspective. When the package body size is greater than 1 mm more than the die size, the cost for wafer-level redistribution becomes sufficiently high making FCCSP the best path for cost.

As flip chip continues to evolve, it remains more economical and more reliable than most fan-out packages. Investments in low-cost FCCSP technologies have created economies of scale and are driving down the unit cost. FCCSP's use is expanding beyond the computing, mobile and wireless markets, extending into automotive and medical, as well as the next big wave for low-cost applications: the wearable device market for the IoT.

WLCSP: The Workhorse of Advanced Packaging Technology

A WLCSP is a single-die package, limited by the die size, which includes wafer bumping (with or without pad layer redistribution), wafer-level final test, device singulation and packing in tape and reel to support a full turnkey solution.

Now in volume production, WLCSP is the workhorse of the Big Five advanced packaging technologies due to its cost/ performance ratio resulting from the elimination of the package substrate. Packaging considerations start with WLCSP, and only move to other formats when routing requirements exhaust the available real estate. Ultimately, customers will choose WLCSP over the other package options where technologically possible because it is the lowest-cost package.

Also known as fan-in wafer-level packaging (FIWLP) industry-wide, WLC-SPs are applicable to a wide range of markets and are generally related to analog and mixed-signal, wireless connectivity and automotive device categories. Typical applications include integrated passive devices, codec, power amplifiers, IC drivers, RF transceivers, wireless local area network chips, GPS and automotive radar. WLCSP offers the lowest total cost of ownership, enabling higher semiconductor content while leveraging the smallest form factor. It is one of the highestperforming, most reliable semiconductor package platforms on the market today. From a market perspective, WLCSP is ideally suited for, but not limited to, mobile phones, tablets, netbook PCs, disk drives, digital still and video cameras, navigation devices, game controllers, other portable/remote products and some automotive end applications.

Perpetual innovation is intrinsic to packaging success and focuses on driving existing technologies to lower cost points. With the anticipated growth in the WLCSP market, there are many reasons for improving and optimizing the WLCSP manufacturing process. A good example of optimization is the implementation of die sidewall protection. Although most WLCSPs are not molded, a method has developed to provide mold-like die surface protection. Using this approach, a molding compound is injected into the saw streets and then the wafer is diced again, creating five- and six-sided molded WLCSPs (see Figures 2a and 2b). This process is currently available, and customers are now designing it into their WLCSP requirements.

Die sidewall protection becomes even more critical as silicon nodes scale beyond 14 nm to 10 nm and 5 nm, where the risk of potential sidewall damage intensifies due to brittle dielectrics, smaller bump pitches and more.

TECHNOLOGY

MEMS Packaging

Many leading companies and industry experts predict that the growing trend for smart devices (smart cars, smart cities, smart factories and more) will result in the deployment of a trillion sensors, many of which will use MEMS technology. However, MEMS devices are not standard integrated circuits. Creative wafer fabrication techniques produce Si-based transducers and actuators that respond to or interact with, external or environmental stimulus.

At the onset of MEMS packaging, priority was given to solving the endmarket application over cost and package form factor. This created a broad diversity of package form factors, with a different approach for almost every application and end market. As the MEMS market grows and transitions into high-volume production, package and test standardization is needed to offer cost-competitive solutions without sacrificing performance. The requirement to control stress to the MEMS structure while allowing stimulus to go through remains the same. The combination of a standard cavity packaging platform and optimized material sets will ensure a near-stress-free environment that allows the MEMS device to function as it was designed to in the real world.

Amkor's focus is creating a standard cavity package platform that will provide the flexibility to support multiple MEMS applications. It will be customizable on the inside while remaining standard on the



Figure 2a. 5-sided molded WLP (CSPnl[™] technology).



Figure 2b. Top-down view of 5S molded WLP (CSPnl technology).

outside to maintain maximum compatibility during assembly, final test and surface board mount. The standard MEMS platforms will also allow the use of other packaging techniques like FlipStack[®] technology, through silicon via (TSV), Cu pillar and die stacking for MEMS sensor fusion and IoT applications. Figure 3 shows examples of these packaging approaches.

Sensor fusion, where software combines the data from different sensors to reduce application uncertainty, leverages all types advanced packaging expertise to integrate different MEMS and sensor functionalities with data processing ICs in multi-die packages. FlipStack CSP technology is an example of sensor fusion, where the bottom ASIC die is a flip chip, and the MEMS die is stacked on top and wire-bonded to reduce the overall package footprint.

Advanced MEMS packaging platforms will be essential to achieving the deployment of anything close to a trillion sensors.

Laminate-based Advanced SiP

Traditional laminate-based SiP solutions have existed for some time and have been manufactured by electronic manufacturing services (EMS) providers with printed circuit board (PCB) assembly design rules and relaxed form factors. Advanced laminate-based SiP solutions, on the other hand, are more complex systems that are miniaturized using tighter and smaller outsourced assembly and test (OSAT)-based assembly capabilities. Advanced laminatebased SIP solutions serve a higher end of the market. This is the case for 4G/LTE RF front end modules (FEMs) which require the complex integration of filters, mixers, demodulators, amplifiers and discretes in a highly dense form factor with ultra-low interconnect parasitics.

Advanced SiPs integrate disparate technologies, such as a small microprocessor with embedded memory, a sensing element such as a MEMS device or image

MEMS and Sensor Application	Accelerometer, Gyroscope, Magnetometer, IMUs	Visible Light, Proximity, Ambient Light, Depth Sensing, IR	Microphones, Pressure, Gas, Temperature, Humidity, Environmental, Gesture	Sensor Fusion and IoT
Package Type	Overmolded	Exposed Die Surface	Cavity Package	Hybrid Cavity Package
SOIC	Contart ELD SCIC 3-3-3-3-77777777	TITTT		
MLF [®] /QFN		-15	۱	-
ChipArray® LGA/FPBGA	Service Set			

Figure 3. MEMS and sensor standard package platforms.

sensor, RF die and power management ICs in a very small form factor. In these designs, it is not unusual to find various different interconnects such as wire bond, flip-chip and WLCSP BGA along with surface mounted components.

The laminate-based advanced SiP qualifies as one of the Big Five packaging technologies because it fits the bill for new market growth areas, providing a great deal of value in terms of form factor and increased functionality at a cost point that accelerates product penetration in new and existing markets. For example, laminatebased SiP solutions can enable miniaturized cost effective solutions in the consumer and industrial IoT space, since they integrate increased functionality and component counts in very small form factors.

Laminate-based SiP solutions that are currently in production achieve the lowest form factor at cost and performance points that address market needs in RF, storage, automotive, IoT and power segments. In addition, a core design kit enables customers to do module and substrate design and also supports system modeling, characterization and full turnkey services to achieve the smallest form factors and fastest time to market.

Wafer-based Advanced SiP

Similar to a laminate-based advanced SiP. a wafer-based advanced SiP allows for the integration of complex and disparate technologies, but meets the higher performance requirements for bandwidth, form factor and density requirements in high-performance computing (HPC), IoT, mobility and automotive segments. In addition to integrating basic microprocessors, sensing elements (MEMS or image sensors), RF dice and power management ICs, a wafer-based advanced SIP can integrate memory (high bandwidth memory (HBM), Hybrid Memory Cube (HMC), and others), ASIC devices and high-performance processors, such as GPUs and FPGAs. This final segment of the Big Five is the technology that serves the widest scope of applications.

The wafer-based advanced SiP is currently targeted for high-end devices and is still in the early introduction phases to the industry. It effectively addresses systemscaling needs and can help offset or delay the need for next-generation Si node based products. Its initial market entry points are



Figure 4. Wafer-based SiP offerings.

HPC, memory and high-end mobility. Over time, however, more devices will take advantage of wafer-based SiP technology to enable extreme form factor reductions and increased product performance at lower power.

While laminate-based SiP leverages the existing die scale infrastructure, waferbased processes differ significantly from laminate-based processes and require investment in wafer processing tooling. Wafer-based SiP replaces and/or complements the laminate substrate, providing RDL line/space (l/s) features down to $1 \,\mu m$ x 1 μ m. A wafer-based SiP RDL can scale to fab back end of line (BEoL)-like dimensions, whereas traditional laminate-based advanced SiPs are currently limited to 10 μ m x 10 μ m l/s. Therefore, wafer-based SiP systems provide the best-in-class (BiC) scaling capability and have the ability to scale to fab-like dimensions.

There are increased costs associated with wafer-based SiP due to the complexity of the products produced. One of the contributors to the increased costs compared to laminate-based advanced SiP is the capital expenditures (CapEx) required to build a platform for wafer-based processes in Class 1 or Class 10 cleanrooms. Fab-like infrastructure and additional toolsets including those used for traditional front-end processes such as physical and chemical vapor deposition (CVD) tools, chemical mechanical planarization (CMP) tools and temporary bond/debond systems, contribute to the increased upfront costs required to enable wafer-based SiP platforms. As the tools and factories depreciate, the manufacturing costs of wafer-based advanced SiPs will be reduced, enabling a wider set of applications to take advantage of the form factor reduction and significant product performance increases.

Package configurations in the wafer-

based advanced SiP family include highdensity fan-out wafer-level packages such as the SWIFT[™] and SLIM[™] product lines. These configurations use a "die last" approach that minimizes the yield loss risk prevalent in the complex die first WLFO packages. SWIFT is expected to ramp to production in the next few quarters and become a predominant driver of waferbased advanced SiP products. The SLIM and SWIFT small body sizes have passed chip-package interaction (CPI) qualifications, with large body sizes in development. Also on the wafer-based advanced SiP roadmap are 2.5D interposer and 3D IC stacks. The 2.5D TSV is available today, having been qualified since 2013. Working with ecosystem partners provides a seamless supply chain and qualified Si portfolio and also enables co-design by providing design kits for each of the waferbased SiP platforms. Figure 4 shows these packaging approaches.

Advanced Packages for Today and the Future

The mobility market is driving form factor reduction and high-density interconnects for multi-die integration. In the HPC, networking, deep learning and GPU applications, wafer-based advanced SiPs address the power, memory bandwidth and latency issues of new devices coming to the market in the next couple of years. The 2.5D, 3D, SLIM and SWIFT technologies can potentially help OEMs and fabless companies delay migration to the next node by enabling system-scaling approaches through wafer-based SiP technology.

Wafer-based advanced SiPs round out the Big Five portfolio, allowing continued innovative choices that will help achieve the best performance, form factor and value-to-cost ratio for any application. \blacklozenge

SMART MICROSYSTEMS

Gel Dispense for Encapsulation of MEMS Pressure Sensors

AS THE MEMS-BASED SENSING

industry grows, the environmental conditions in which these sensors must perform grow with it. Pressure sensing is one application of MEMS-based sensing where particularly harsh environments can be present. Examples of common challenging environmental conditions include automobile exhaust, fuels, refrigerants and atmosphere with moisture and ice. Unlike previous technology, which used large mechanical assemblies and welded or soldered interconnects in the fluid path, the MEMS-based technology offers the ability to place the microscopic sense element and wire bond interconnects directly in the fluid path. As a result of the harsh environment and exposed assemblies, it is often necessary to protect the sense element and interconnects with products such as encapsulation gels.

The first step in the process of protecting exposed MEMS-based assemblies is to select the proper gel for the design intent of the product and for the environment in which it will serve. Protective gels have come a long way in recent years with a virtually endless selection of silicone dielectric encapsulation gels. Typically encapsulation gels are selected based on desired final product properties, such as viscosity after cure and chemical properties best suited for the end-use environmental conditions. The manufacturing procedures for using gel are often overlooked in the initial design process, and must be reconciled by the process engineering team.

Once the design is complete, a process is developed by the engineering team to properly apply the correct amount of gel to best serve the end-use application without creating unintended consequences. These requirements compel the satisfaction of four critical factors during the application process:



Figure 1. X-ray of die and wire bonds after gel dispense.

1) complete gel coverage of critical components, 2) elimination of all air voids in the gel, 3) proper and complete cure, and 4) a controllable process with a measurable output.

Attaining and maintaining complete gel coverage over all critical components seems like a straightforward process. Verification of the gel dispense process ensures coverage of all critical components, but with shrinking product packages and complex layouts, an unobstructed view of critical areas is not often obtainable. At SMART Microsystems, analysis techniques, such as acoustic microscopy and 3D X-ray, are used to develop and validate gel dispense procedures during the initial design process (see Figure 1). These tools allow inspection inside of the part after dispense, confirmation that the product is properly protected, and verification that the gel dispense parameters have achieved the desired result.

The root cause for the prevailing gel dispense failure mode which plagues most MEMS-based sensor product designers is air voids trapped in the gel. For pressure sensors with gel in the fluid path, entrapped air in the gel will move under pressure and apply unintended and potentially damaging stress on the sense element and on the interconnects. This can cause premature output shift or product failure. Most silicone gels are hygroscopic in nature-they readily absorb moisture. In typical product designs the hygroscopic gel is placed in the fluid path. The hygroscopic nature of the gel and exposure to the fluid path will cause the gel to collect moisture in any air voids present. The moisture-filled voids immediately become a source of corrosion. For process engineers that have experience in gel dispense procedures, preventing air voids is the primary condition that must be accommodated during product and process design. This requires careful vacuum degas of the gel prior to dispense, with additional centrifuge use as needed due to the intrinsic properties of the gel. A post-dispense degas may also be required due to product design, such as if the product geometry entraps air.

Heat cure encapsulation gels are the preferred choice for many MEMS-based sensor products because they offer a complete cure. Heat cure encapsulation



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Creating robust and reliable interconnects for new technologies presents a series of new obstacles. Despite this, problems encountered as a result of custom packaging, unique geometry, and unusual material limitations can be overcome. Using a combination of well understood processes (such as wire bonding), emerging technologies (such as isotropic conductive adhesive) combined with creative engineering, SMART Microsystems can develop reliable interconnect processes for your new technology.

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Figure 2. Thermocouple embedded into the gel of a specially modified part.

gels are typically dispensed at a lower viscosity to promote flow and complete coverage. After the material has been degassed and dispensed, it must be properly cured to achieve the final viscosity to protect the product. In order to establish the proper cure profile for the gel, as recommended by the manufacturer, it is necessary to characterize the process. A calibrated thermocouple reader and a fine wire thermocouple are used in order to characterize the specific cure oven profile. The fine wire thermocouple is embedded into the gel of a specially modified part (see Figure 2). The thermal gradient of the gel will always lag the thermal gradient of the cure oven. Cure characterization ensures a proper and complete cure of every part every time.

Product specifications and requirements that cannot be measured or quantified serve little purpose. Therefore, a process must be designed which is controllable and which has a measurable output in order to meet product speci-



Figure 3. Shot weight test coupon.

fications. Gel dispense processes pose unique, but surmountable, challenges to quantification. At SMART Microsystems, highly accurate and precise measurement and dispense tools are used in the design, development, and production phases of gel encapsulation. The dispense process is designed using precise mass scales and with accurate programmable dispensing units to deliver a precise shot weight of gel material in every part (see Figure 3). This type of process design provides exceptional results with measurable outputs that can be controlled through statistical process control (SPC).

ENVIRONMENTAL LIFE TEST



SMART's precision automatic dispense equipment.

Not all MEMS sensor designs require dielectric encapsulation gel protection, but many on the front-line of harsh environmental sensing do. It is important to the end-use product viability that the process of protective gel encapsulation is designed and validated properly. Engineers at SMART Microsystems understand from experience that encapsulation gel is not simply a corrective action to a preexisting failure mode. Gel encapsulation is a process which is performed with equal diligence in design and development to wire bonding, die attach, assembly, and many other process crucial to the end-use sensor and the same diligence is observed throughout production.

For more information about SMART Microsystems services visit their website at www.smartmicrosystems.com. \blacklozenge

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MANUFACTURING SERVICES



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OPINION

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their capabilities in form of Assembly Design Kits (ADKs).

How Can IC Designers, EDA and IP Vendors, Foundries and Assembly Houses Work Together

The rest of this article will focus on the importance of ADKs and the roles of and data/product flow between these five EcoSystem partners. It also will outline how ADK and reference flow enable multi-die IC designers to walk the narrow road between costly over-designs and risky/unreliable under-designs. Together with die-level IP building blocks, ADK and reference flow offer a solid platform for multi-die IC design. This "three legged stool" will encourage many more IC designers to evaluate and choose multi-die solutions. Only then the IC manufacturers will be able to recoup their already significant investments in multi-die IC manufacturing equipment, flows and newly formed relationships with supply chain partners.

Figure 2 outlines the Multi-die IC EcoSystem and shows in green how the proven fabless/foundry cooperation dovetails into the emerging Assembly Design Flow and how 3rd party IP building blocks contribute to multi-die design and manufacturing.

This modular approach, combining one or more proprietary dies, manufactured in their most suitable process technology, with one or more 3rd party IP building blocks demonstrates how similar such a modular multi-die IC design project is to a system design approach and how much flexibility it offers, while significantly improving performance and reducing power, development cost and time to profit.

The green portion of Figure 2 also shows that multi-die IC technologies DO NOT REPLACE our proven SoC technology. To the contrary, they integrate proprietary SoC dies as differentiators into the multi-die EcoSystem and add to these SoCs more market value by combining such proprietary designs with off-the-shelf 3rd party IP. The high bandwidth memory cubes (HBMs) are such 3rd party die-level IP building blocks, already in use. SERDES dies, data converters, power management ICs (PMICs),



Green: IC Designer & Wafer Foundry, Yellow: Package Designer and Assembly House, Blue: EDA Vendors' contributions, Red: 3rd party IP Vendors' contributions

Figure 2. Multi-die IC EcoSystem.

all in die form, are other examples for how 3rd party IP complements and add value to one or more proprietary SoC die(s).

The yellow part shows that the role of EDA is to automate development of ADKs and to provide tools for planning, design and verification of multi-die ICs. Like foundries, assembly houses benefit significantly from highly automated flows for characterization of package materials and active as well as passive components. Streamlined model creation is also important. Data encryption protects proprietary know-how. Designers appreciate user-friendly tools, accurate and up-to-date information about multidie assembly flow as well as materials, components and equipment capabilities. These help designers significantly to minimize iterations and reduce time to profit and enable them to walk the narrow road between costly over-design and risky/unreliable under-design.

The red arrows show how 3rd party IP can flow into the design steps as models and into the manufacturing steps as die-level IP building blocks, to be combined with the customers' proprietary die-level IP building blocks. Because dielevel IP building blocks can be manufactured in their most suitable process technologies, they offer lower cost per function and best performance per Watt.

How Close is Such an EcoSystem to Becoming Reality?

Parts of this design/manufacturing EcoSystem have been in use for many years, to design and assemble SiP and PoP multi-die ICs.

Amkor and Cadence announced in Spring 2016 the start of a joint Package Assembly Design Kit (PADK) development, in support of advanced IC packaging technologies.

Please contact them or your EDA and assembly partner(s) to learn about their current capabilities and plans. \blacklozenge

HERB REITER founded eda2asic Consulting, Inc. in the spring of 2002 with the intention to focus on increasing the cooperation between EDA suppliers and semiconductor vendors. Herb earned an MBA at San Jose State University and Master Degrees in Business and Electrical Engineering at the University and the Technical College in Linz/Austria, respectively. Herb has also taken more than forty Continuing Education courses at Stanford University in recent years.

Henkel News



Everything-Proof: The Future of Mobile and Wearable Devices

Raj Peddi Henkel Adhesive Electronics

CONSUMERS' GROWING DEPENDENCE on mobile devices now extends well beyond the communications realm and into health, fitness, entertainment, transportation and more. With this reliance on smartphones, fitness bands and connected watches also comes huge expectations: expectations for reliability, expectations for enormous functionality, expectations for exceptional design and, yes, expectations for extreme durability.

In the early days of smartphones, users were generally happy if they could drop their phone with little consequence. The ability to cope with an occasional spill of a common beverage or sweat during those 6 a.m. workouts was also a nice-to-have. As reliability and environmental durability incrementally improved, so, too, did consumer demands. The quest for more features in shrinking dimensions continues to place huge pressure on thermal management, protection of exceptionally small and delicate components, EMI capability and reliable interconnects. Remarkably, many of these challenges have already been addressed. High-performance, re-workable underfills, capable thermal materials in pad, film and liquid formats, unique packagelevel EMI alternatives and game-changing solder pastes have, indeed, enabled the smallness, performance and reliability of today's mobile devices.

Now what? Top on the wish list has to be waterproof durability. Water resistance is something consumers have longed for and considered by some as a virtual smartphone utopia. As most smartphone owners have probably experienced the unfortunate result of a wet mobile phone, the idea that this could someday be avoidable is enticing. To be sure, leading smartphone manufacturers have already made moves in this direction, as evidenced by recent



promotions of the sort. However, reaching true waterproof status for the entire phone, watch or fitness band is a tall order but one where significant progress is being made. The product design and material selection considerations for ensuring water resistance are immense and extend from the PCB, where conformal coatings play an important role, to sealants for camera modules and, yes, even elimination of external jacks and connector ports.

As a leading provider of adhesive solutions for camera module assembly, Henkel has developed a full suite of materials that enable advanced camera module technology - from lens bonding to attachment of the lens holder to the substrate to voice coil motor bonding and everything in between. Now, in a new breakthrough, Henkel has developed a waterproof sealing adhesive for camera module lens bonding - yet another milestone on the path to fully waterproofed smartphones. LOCTITE ECCOBOND LS 3106P is an optically clear adhesive that effectively seals all of the lenses within a lens house bonding for both auto focus and fixed focus lenses, protecting the optical components against damage from water.

The new adhesive has a low thixotropic index, making it ideal for filling the small gaps present in a lens assembly. This material characteristic allows LOCTITE ECCO-BOND LS 3106P to flow easily without added pressure and provides excellent coverage for complete self-sealing. What's more, the thixotropic index of LOCTITE ECCOBOND LS 3106P shows very little change over time with similar performance at 30 days and 90 days. A long pot life allows manufacturers to minimize waste, as the adhesive can cope with continuous use for up to 60 days with no material degradation. In addition to these benefits, LOCTITE ECCOBOND LS 3106P has exceptionally low weight loss, indicating minimal outgassing for robust performance. The lens module's operation is dependent upon the optical lenses, so any outgassing during the cure process could fog the lens and affect the performance of the camera. Henkel's waterproof sealant remains stable during UV curing without any outgassing, ensuring predictable lens operation. LOC-TITE ECCOBOND LS 3106P also exhibits very low shrinkage, which is critical for fragile, thin lenses and alignment accuracy as shrinking of the material post-cure can result in shifting alignment or impaired lenses. With no change in linear shrinkage post-cure, LOCTITE ECCOBOND LS 3106P protects against lens misalignment and/or damage.

While all of these material properties are critically important, LOCTITE ECCO-BOND LS 3106P's primary function is waterproofing and here, too, the adhesive delivers. In waterproof simulation testing, LOCTITE ECCOBOND LS 3106P survived complete water submergence. The test vehicle was sealed with the adhesive and submerged in water for 24 hours at room temperature, following which it was exposed to an 85°C/ 80% relative humidity (RH) environment. The material showed no water leakage or swelling following the 24 hour submergence or the 85° C/85% RH exposure.

Henkel's LOCTITE ECCOBOND LS 3106P is one of many elements required for the waterproofed smartphones and wearables of the modern era. With success already proven with newer-generation devices, LOCTITE ECCOBOND LS 3106P is helping to facilitate the future of mobile durability.

To find out more, visit www.henkeladhesives.com/electronics. ◆



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Assembly Design Kit (ADK) for Multi-die ICs

Moving from Moore's Law to More-than-Moore is like the change from IDMs to the fabless model

Herb Reiter eda2asic Consulting, Inc.

IT TOOK SOME TIME TO TRANSITION our industry from the IDM model to the well-functioning cooperation between fabless IC vendors and foundry partners. In addition to establishing new business models, IC designers and wafer foundry experts as well as EDA vendors and IP providers needed to be trained in how to best work together. To make the technical cooperation between these four camps low risk, efficient and cost effective, they jointly built an EcoSystem with these major elements:

a) Process Design Kits (PDKs), to convey the foundry capabilities and constraints,

b) Low-level libraries, memory compilers, soft and hard IP blocks and

c) User friendly Reference Design Flows, to enable IC designers to fully utilize a) and b)

These are still the key elements for success of the rapidly expanding fabless / foundry cooperation.

As further shrinking of transistor feature sizes is getting much more costly and difficult, both in regards to IC development time, NRE and transistor cost, following Moore's Law is no longer economical for many medium to higher volume applications. Also as semiconductor experts notice, demand for heterogeneous function is increasing rapidly. Figure 1 shows that the revenues for heterogeneous functions already exceeded the worldwide revenues for digital functions in 2015.

Advanced packaging technologies (PoP and SiP) are offering proven ways to combine multiple known good dies (KGDs) in one package. However, footprint and height limitations for mobile,



Figure 1. Revenues for heterogeneous functions exceeded the worldwide revenues for digital functions in 2015.

wearable as well as other applications demand smaller packages. In addition, market needs for higher performance and lower power have encouraged the IC manufacturing community to develop a range of advanced IC packaging technologies, such as 2.5/3D-ICs and, more recently, multi-die Fan-out Wafer-level Packages (FO-WLP).

Recent **iPhone 7 teardown reports** confirm that Apple chose **TSMC's new InFO packaging technology** to vertically stack logic and a DRAM, to save footprint, increase bandwidth as well as reduce cost, latency and power of the A10 application processor. This highvolume design is **accelerating the development of similar advanced packaging technologies** at other foundries and at assembly & test houses (OSATs).

How to Broaden Market Acceptance for More-than-Moore Technologies

Apple and other early adopters (Hynix, Micron, Samsung, AMD, IBM, Marvell, Nvidia, Xilinx, ...) have demonstrated, that more of the value creation and product differentiation is shifting from the die to the IC package. These technology pioneers have, in close cooperation with their supply chain partners, contributed significantly to maturing the supply chain for multi-die IC design and manufacturing. Just like the quality of wafer suppliers' PDKs significantly influences customers' selection of foundry partners, now it is becoming important that assembly houses offer customers detailed and up-to-date information about

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