Heterogeneous Integration

Enabling the future of the Electronics Industry

Presented by W. R. Bottoms PhD

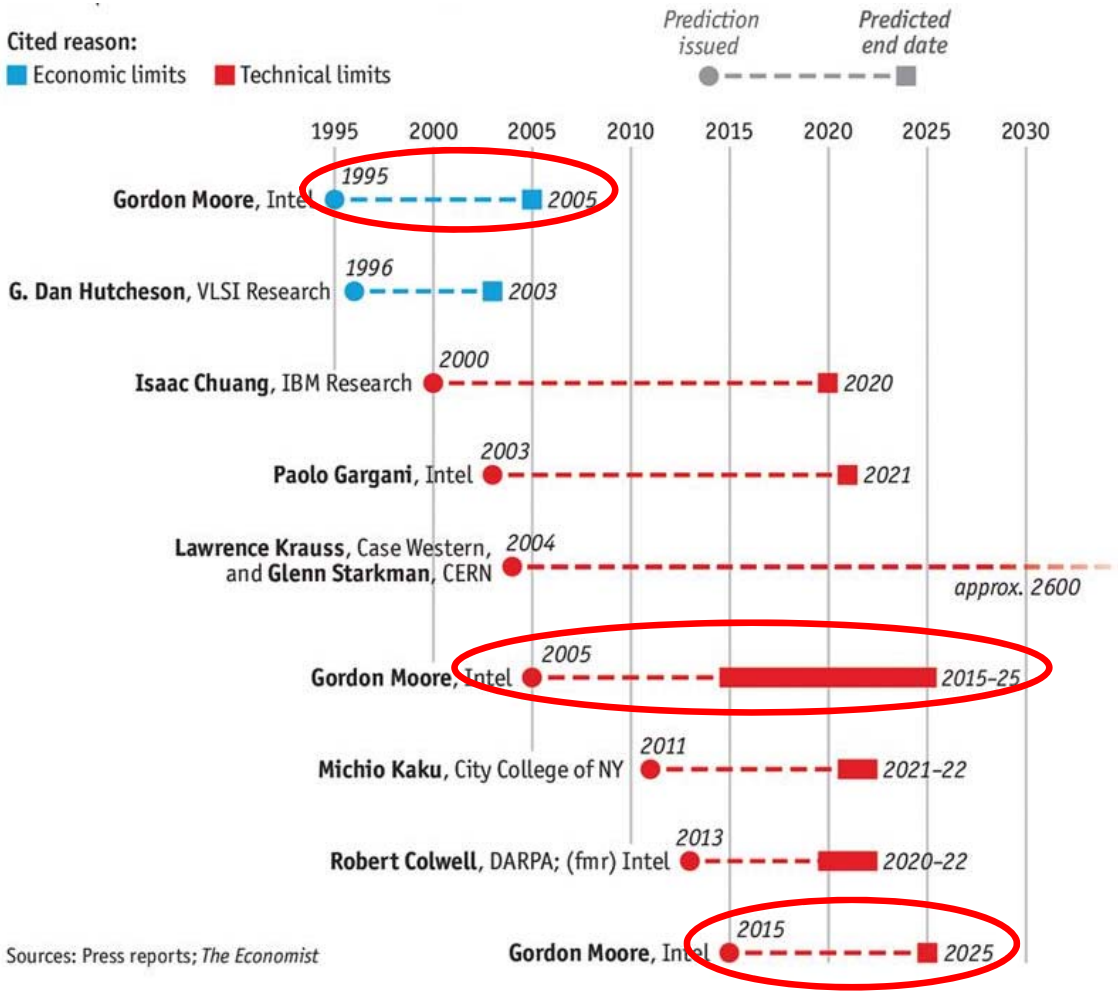
Four Issues Are Driving Change In Information Technology

- ✓ **The approaching end of Moore's Law scaling of CMOS**
- ✓ **Migration of Data, logic and applications to the Cloud**
- ✓ **The rise of the internet of things**
- ✓ **Consumerization of data and data access**

The End Is Coming

For Moore's Law

Many Predictions of The End



Further Scaling Is Possible But Is Becoming Irrelevant

Cost per transistor at the smallest node has not decreased since 2012

Moore's Law Was Over At 28ηm

✓*"From this point on we will still be able to double the amount of transistors in a single device but not at lower cost. And, for most applications, the cost will actually go up."*

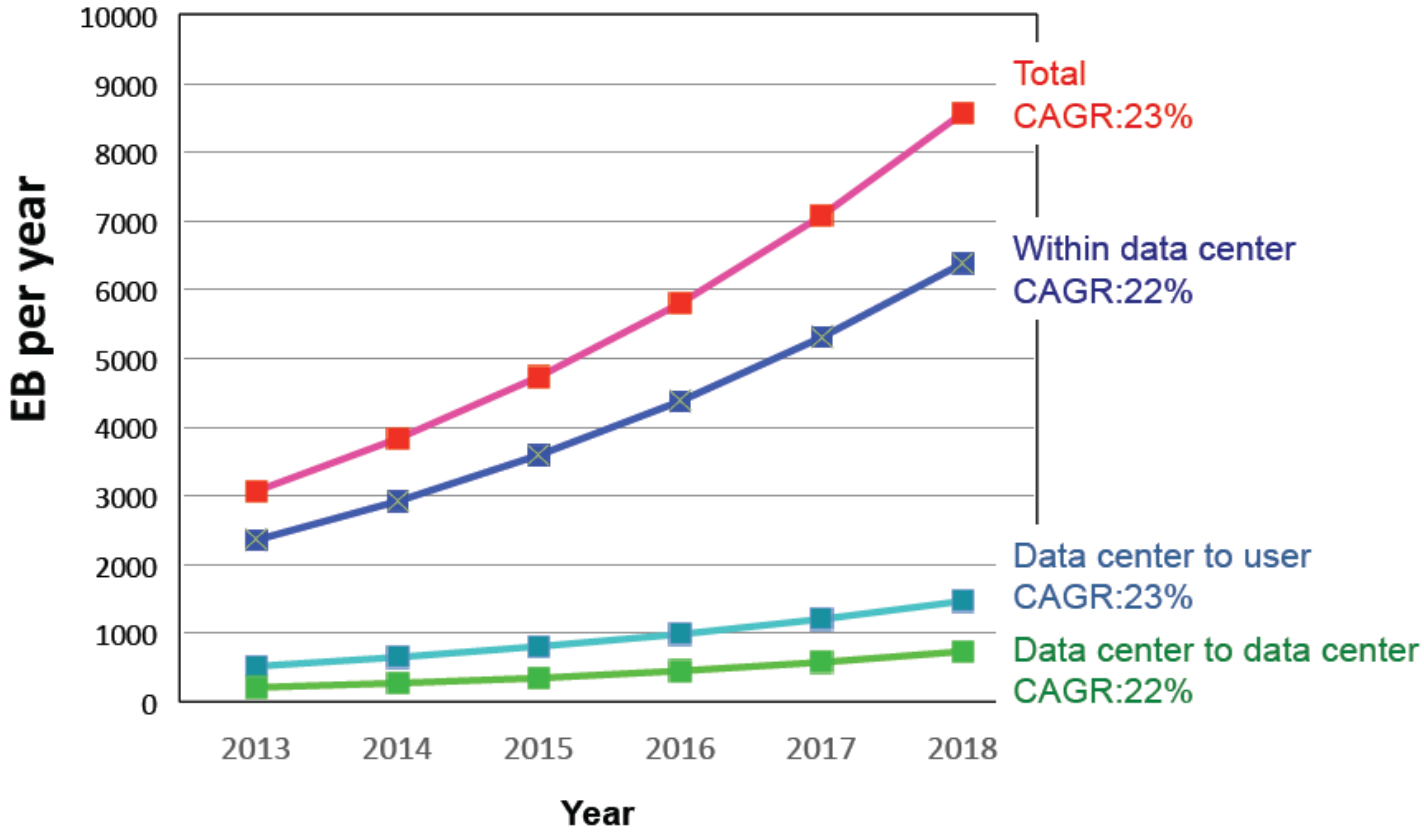
Zvi Or-Bach, President & CEO, MonolithIC 3D Inc. March 2014

IBIS data presented in Shanghai last month shows costs per gate costs continue to rise each generation after 28ηm

Technology	Cost per 100M gate ($)
90nm	4.01
65nm	2.82
45/40nm	1.94
28nm	1.30
20nm	1.42
16/14nm	1.43
10nm	1.45
7nm	1.52

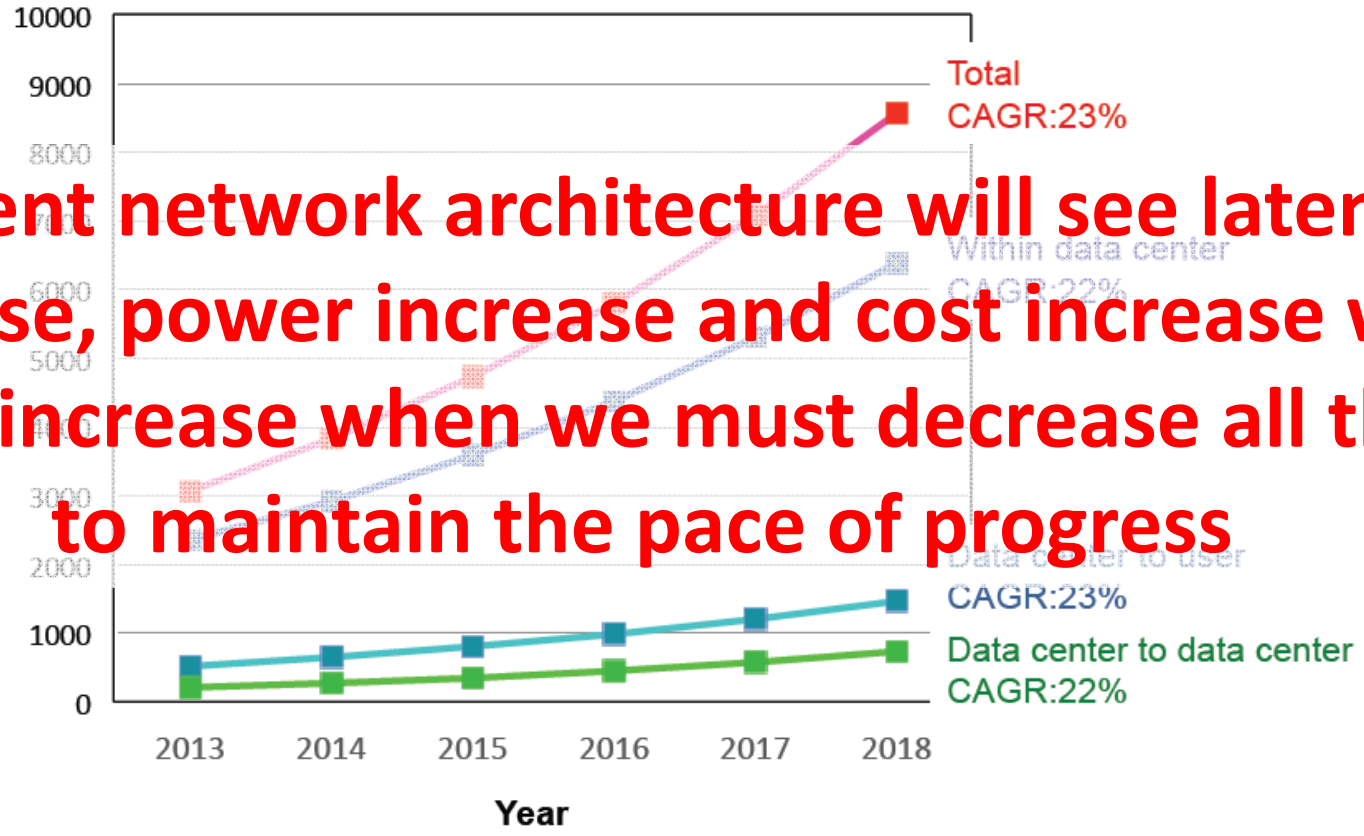
Migration of Data, Logic and Applications to the Cloud

Global Data Center Traffic



Source: Cisco Global Cloud Index

Global Data Center Traffic

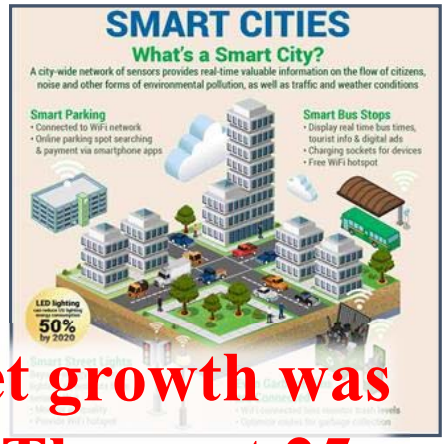


Current network architecture will see latency increase, power increase and cost increase with traffic increase when we must decrease all three to maintain the pace of progress

Source: Cisco Global Cloud Index

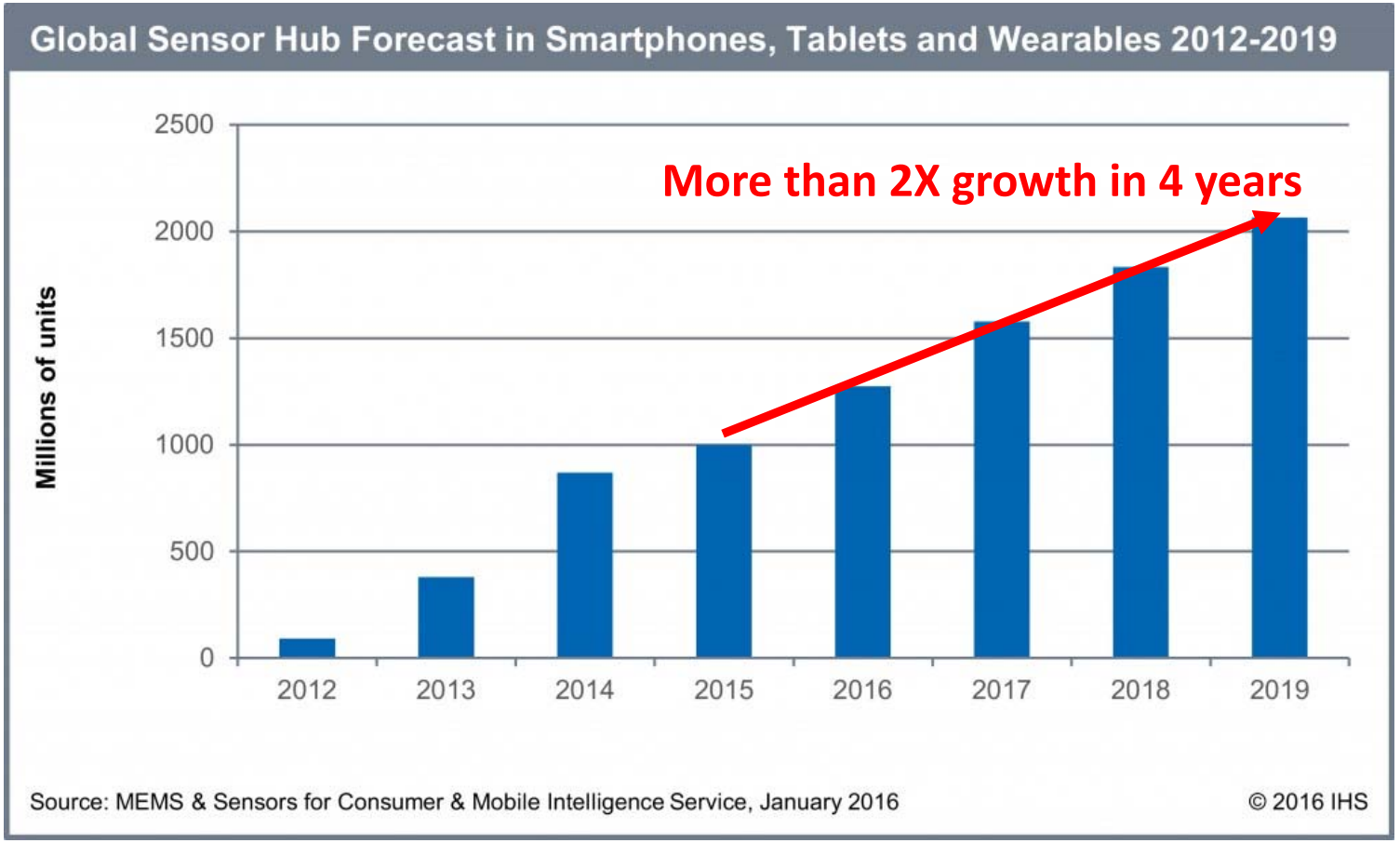
The Rise of the Internet of Things Brings New Data Sources With New Packaging And Network Connectivity Requirements

The Internet of Everything
Driven by Human Communication and Machines



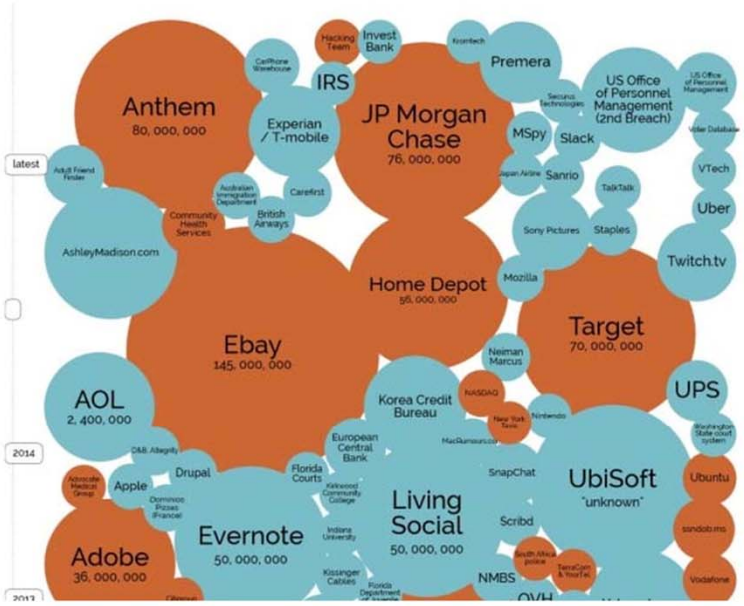
The first quarter century of internet growth was fueled by human communication. The next 25 years will be fueled by machines.

Personal Appliances will Be the Largest portion of the IoT Mobile Hub Market



Security Is A Critical Issue And Must Incorporate Hardware And Software In The Package For Latency

Sampling of recent security breaches and emerging concerns



Hackers cut Jeep's brakes, sending car into a ditch

Remote shutdown of home power through hacked meters

Sources: http://www.informationisbeautiful.net/visualizations/worlds-biggest-data-breaches-hacks/
http://www.wired.com/2015/07/hackers-remotely-kill-jeep-highway/
http://resources.infosecinstitute.com/how-hackers-violate-privacy-and-security-of-the-smart-home/

Every connection to the network including IoT must have embedded security

IoT components have Diverse Requirements
Low Cost/High Volume

IoT Hub May be stationary or mobile

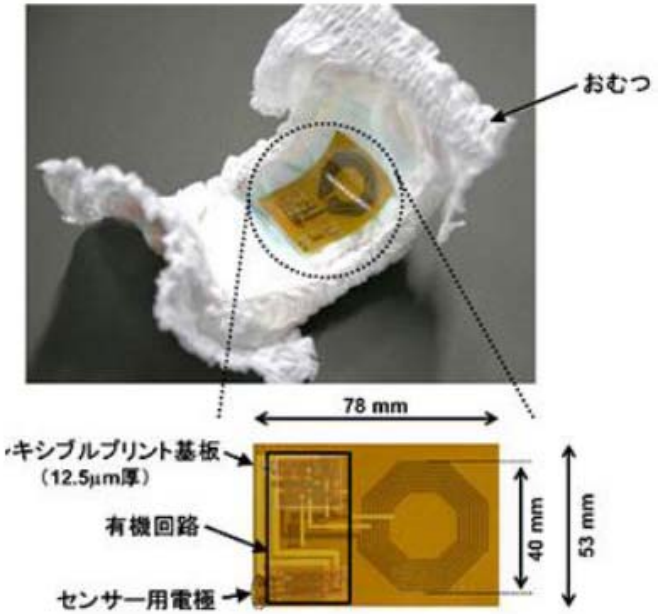
- ✓ Do nothing well (very low standby power)
- ✓ Reliability (years of operation with no service, maintenance or power connection)
- ✓ May include photonic sensors
- ✓ Standards (to maximize volume and reduce cost)
- ✓ RF communications (not likely to be connected to wires or fiber)
- ✓ Energy scavenging and power storage
- ✓ Security (will require both hardware and software components)
- ✓ Very low cost

Wireless personal appliances such as smart phones and tablets will be the largest initial IoT hub

New Connected Products Are Coming
High Volume Low Cost

Even diapers will be connected

- ✓ 40M/day in the US alone
  - 14.6B per year
  - A trillion sensors will not be difficult the product is adopted worldwide
- ✓ At this volume it only adds a few cents per diaper
- ✓ Communication will be an app on your smart phone



- Real-time diaper wetness sensor & notification
- Impedance measurement
- RF connection
- University of Tokyo work

Source: www.medgadget.com

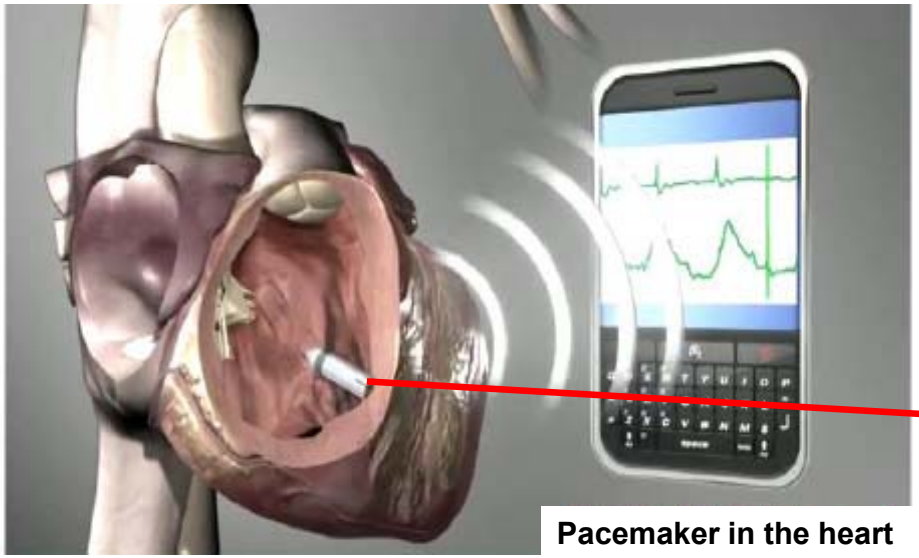
IoT components have Diverse Requirements
High Cost/Low Volume

IoT Hub May be stationary or mobile

- ✓ High bandwidth density
- ✓ Low latency
- ✓ Thermal management
- ✓ Reliability (years of operation with no service, maintenance or power connection)
- ✓ May include photonic sensors
- ✓ Custom form factors and functions
- ✓ High speed communications (may be photons, RF or electrical wires)
- ✓ Security (will require both hardware and software components)
- ✓ Figure of merit is cost per unit of performance

Medical devices are one example of high cost/low volume IoT components

New Connected Products Are Coming
Low Volume – High Cost



Pacemaker in the heart
With smart phone

Novel Energy Scavenging Devices

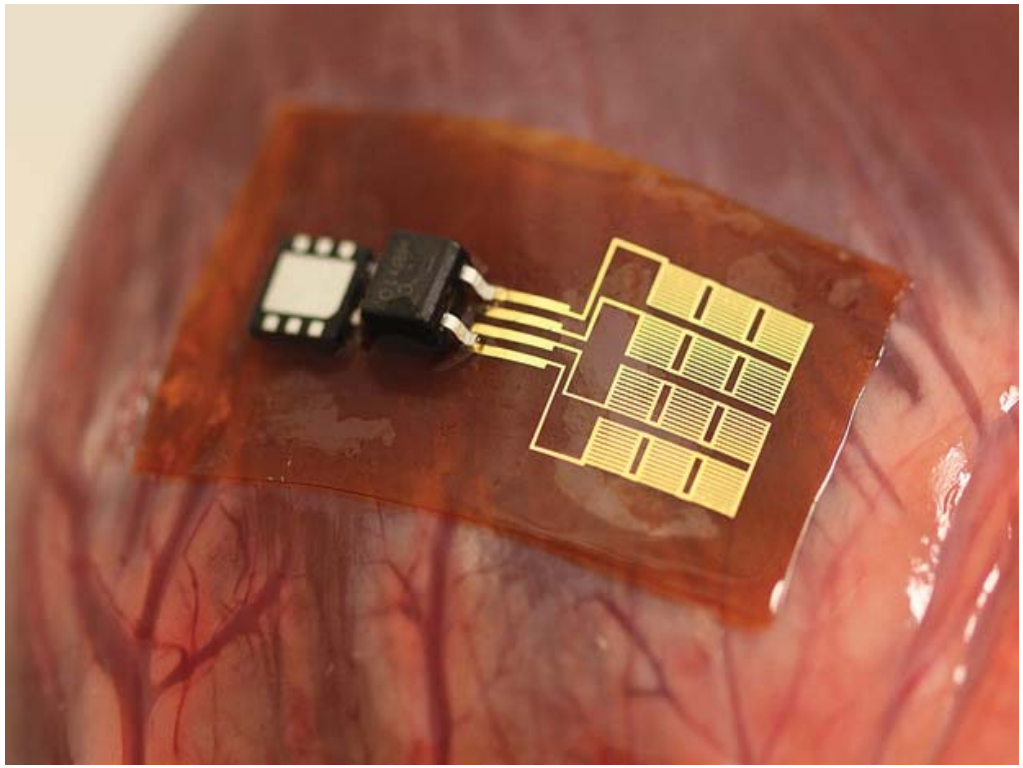
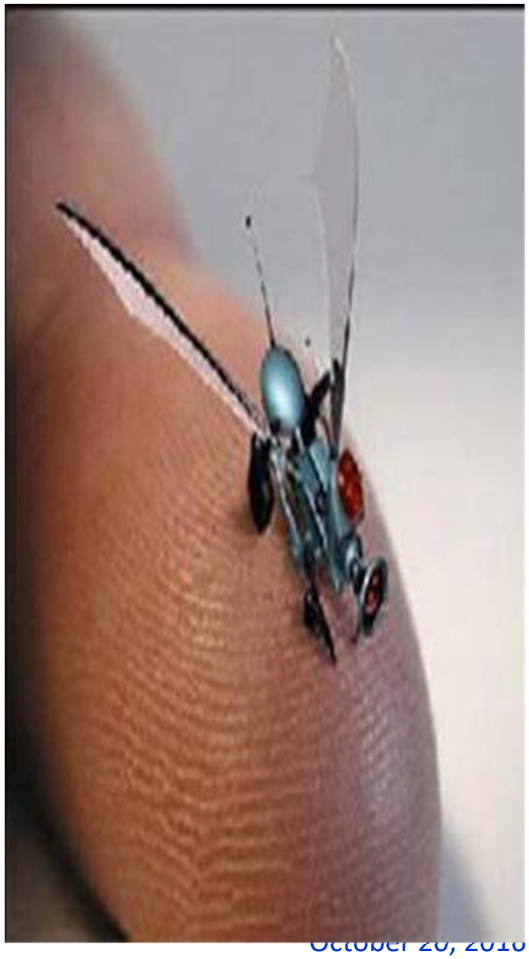


Photo: University of Illinois College of Engineering

A piezoelectric harvester is shown attached to the surface of a heart. The conformable design can harvest enough energy for a pacemaker.

The Military Is Supporting "Smart Dust"

- ✓ Smartdust is a system of many MEMS devices such as sensors, robots, or other devices, that can detect, light, temperature, vibration, magnetism, or chemicals.
- ✓ It can be embedded, dispersed and even ingested.



Smart dust is generation of computers the size of snowflakes predicted by Prabal Dutta of Univ of Michigan

Many IoT Medical Devices Are Here And More Are Coming

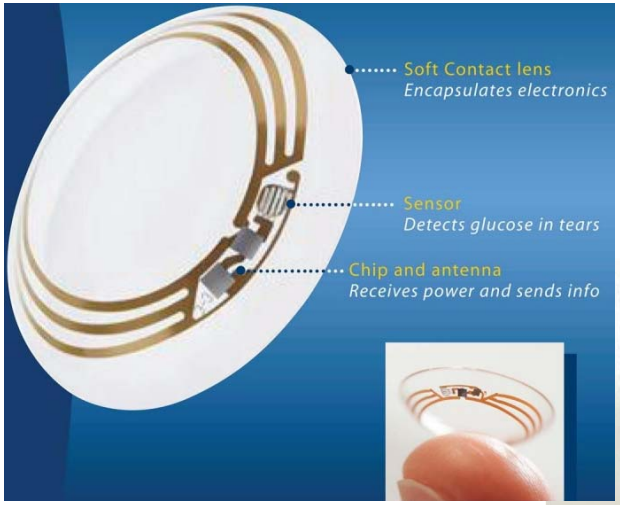
Patch for UV can be applied anywhere and be worn for 5 days

MC10's WiSP is a 300-micron-thin patch for monitoring electric-cardio activity.

Diverse Requirements For An Unlimited Number Of IoT Products Use HI

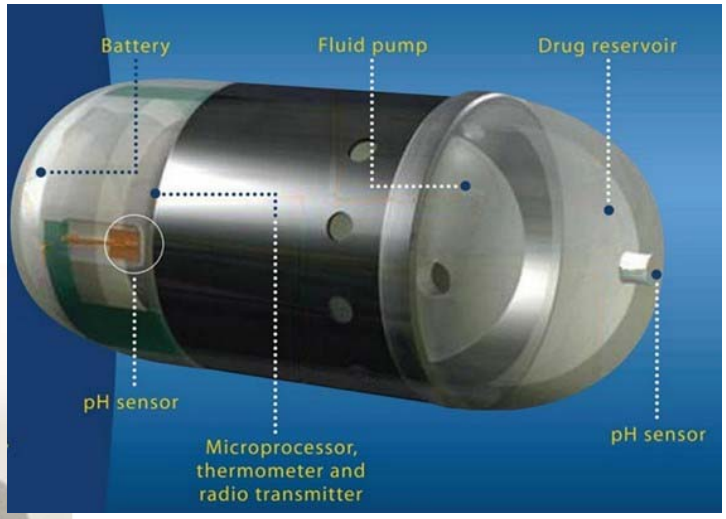
Wearable concussion sensor

- concussion history
- power management
- motion sensor
- Radio



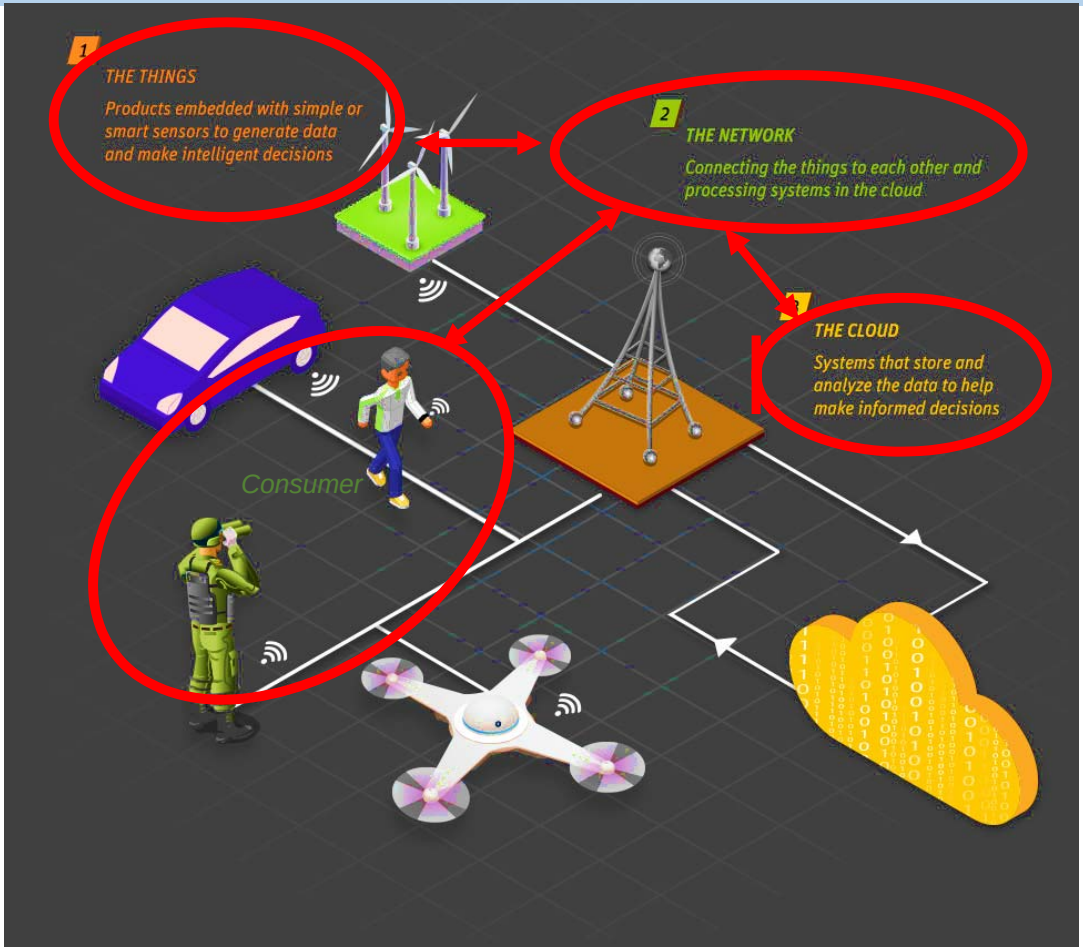
Wireless glucose sensor for diabetics

Frying pan controlled by smartphone app.



Robotic Drug delivery
Pill swallowed by Patient

Everything Must Change
Including Roadmaps



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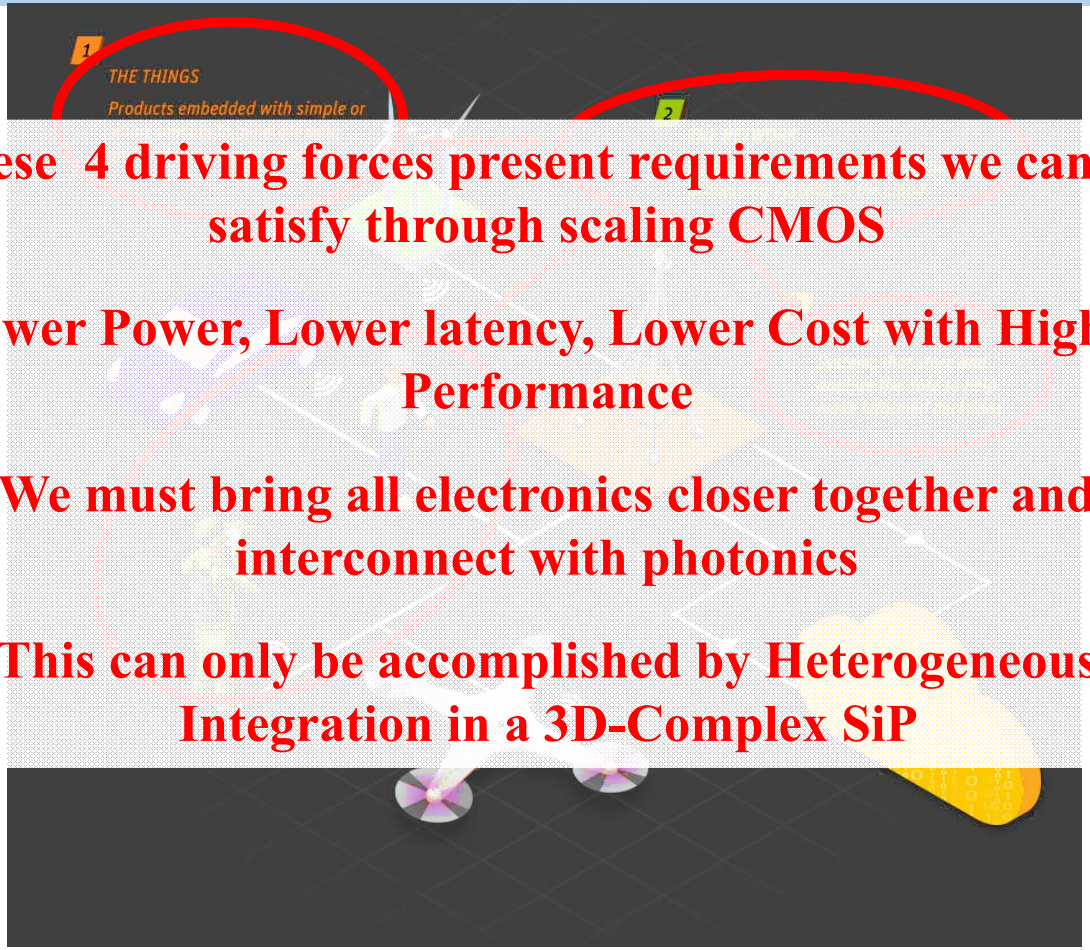
Including Roadmaps



These 4 driving forces present requirements we cannot satisfy through scaling CMOS

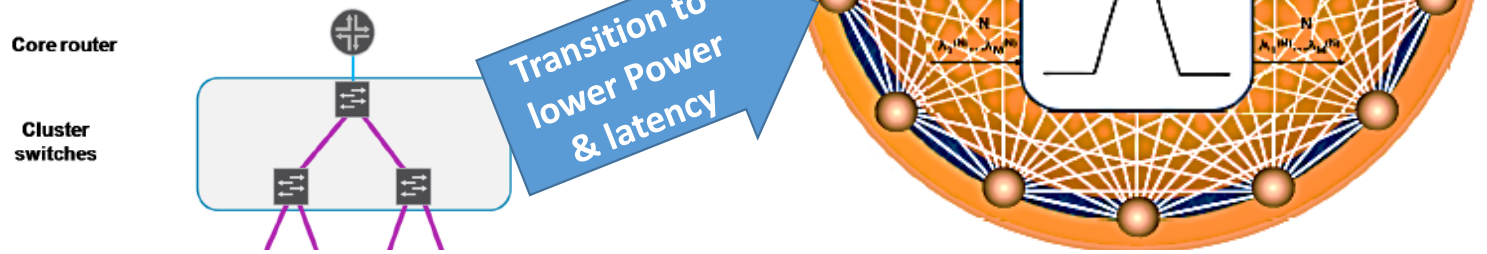
Lower Power, Lower latency, Lower Cost with Higher Performance

We must bring all electronics closer together and interconnect with photonics

This can only be accomplished by Heterogeneous Integration in a 3D-Complex SiP

The Network Architecture Must Change Globally and Locally

- ✓Higher connectivity Flat Architecture
- ✓Higher bandwidth per port
- ✓Lower end-to-end latency
- ✓Lower power
- ✓Lower cost



Photonics to the Board, package and even chip level may be required.

The Network Architecture Must Change Globally and Locally

All this is needed at *no increase in total cost and total Network power*.

Power and cost/function need *>10^4* improvement over the next 15 years.

Heterogeneous Integration Will Be Used Almost Everywhere

- ✓Computing
- ✓Communication
- ✓Transportation
- ✓Entertainment
- ✓Health care
- ✓Agriculture
- ✓Manufacturing
- ✓etc.

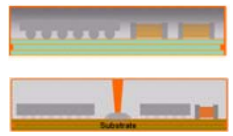
Heterogeneous Integration Will Be Used Almost Everywhere

- ✓Computing
- ✓Communication

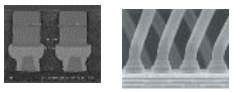
Each Application has its own difficult challenges

- ✓Agriculture
- ✓Manufacturing
- ✓etc.

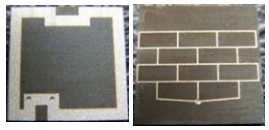
Electronic/Photonic SiP through Heterogeneous Integration



Shielding
-Board or package level
-Compartmental



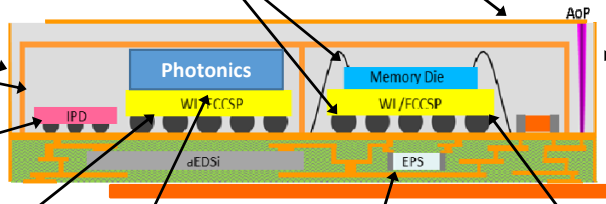
Interconnection
Flip Chip & Wire Bond



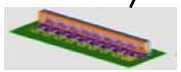
Antenna
-Package integration
for 2.4G/5G/60GHz

Molding
-MUF
-Exposed die

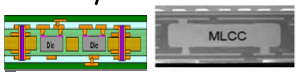
SMT
-Passives
-Components
-Connectors



Passives/IPD
-Integrated Passive
Devices



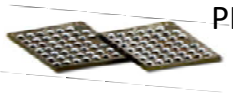
Photonics Layer
PIC Chip- optical bus



Embedded Technology
-Passive component
-Active device

Die/Pkg Stacking
-Die thinning
-Die interconnect

Mechanical Assy
-Laser welding
-Flex bending



Wafer Bumping/WLP
-Lead-free / Cu Pillar
-Bare die package

Source: ASE with additions

How Can We Maintain Progress

- ✓Continue Moore's Law scaling as long as it is practical
- ✓Replace the CMOS switch
- ✓New architectures using the 3rd dimension
- ✓New Materials
- ✓Heterogeneous Integration
  - Conventional CMOS Logic and memory
  - RF
  - Photonics
  - Analog
  - Power management
  - MEMS
  - Sensors
- ✓New manufacturing equipment and processes for packaging

How Can We Maintain Progress

- ✓ Continue Moore's Law scaling as long as it is practical
- ✓
- ✓
- ✓
- ✓

Moving data transport and as many switching functions as possible to photonics

and

bringing all the components as close together as possible is essential if we are to achieve the required improvement in power and cost over the next 15 years

- ✓ New manufacturing equipment and processes for packaging

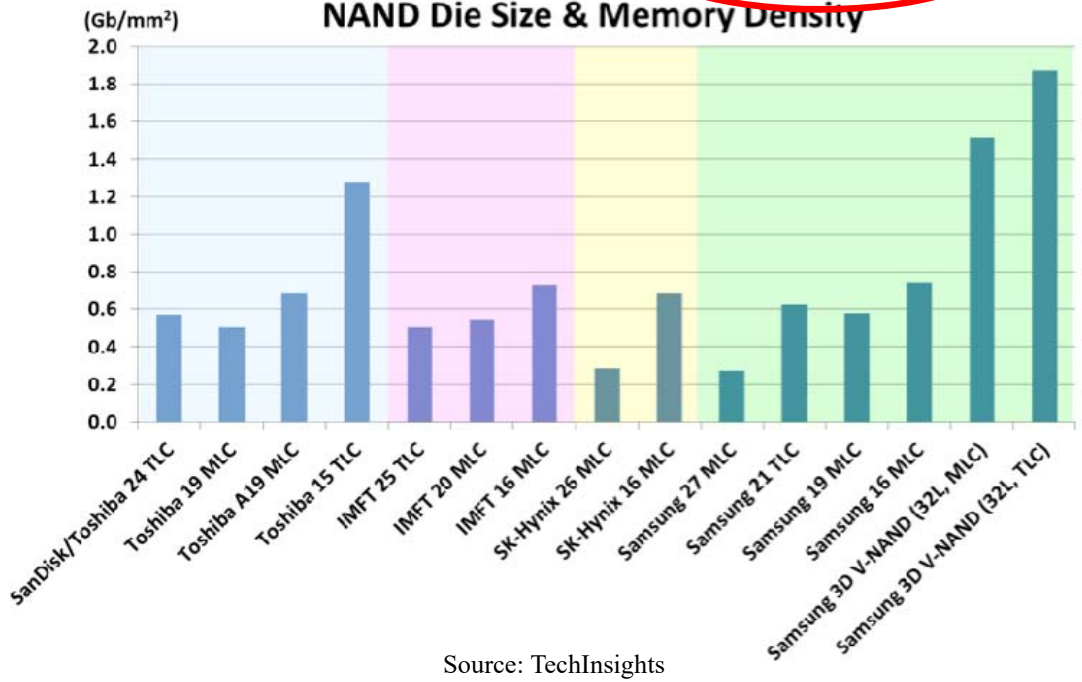
New Device and Packaging Architectures using the 3rd Dimension

SEMI Headquarters

October 20, 2016

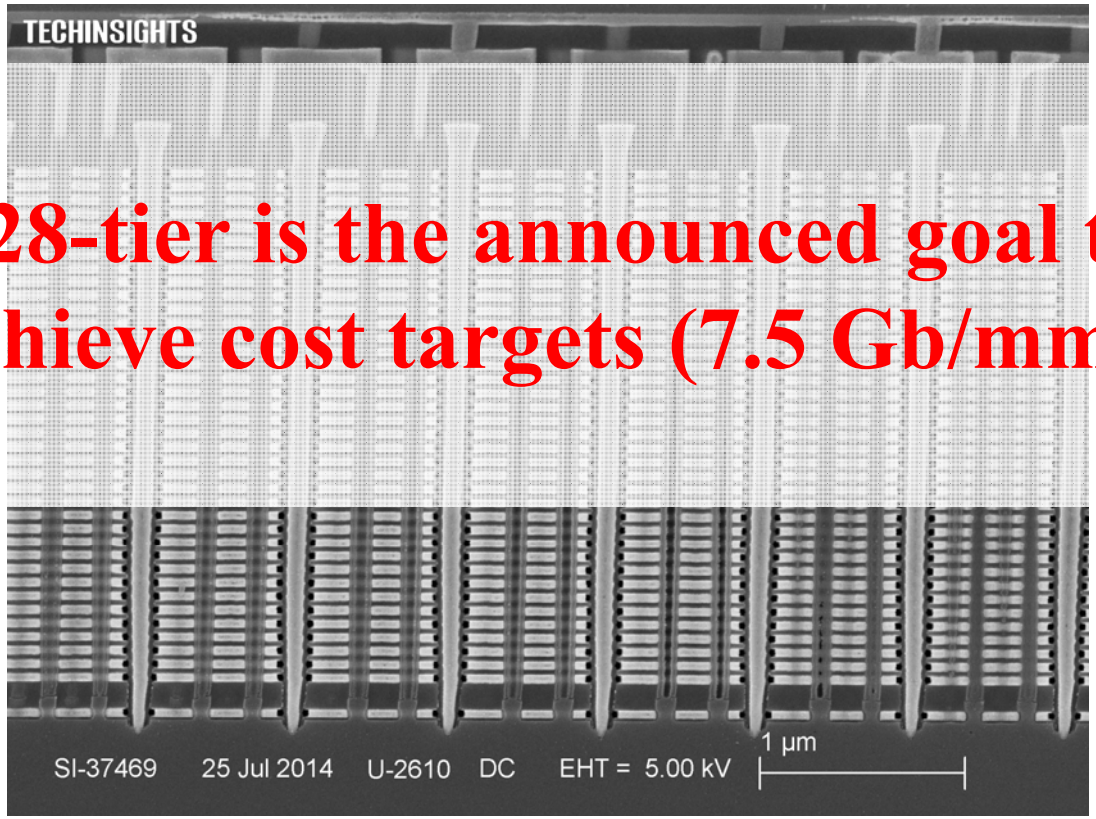
Fabricated 3D Memory

- ✓Toshiba, Hynix, Micron and Samsung have all announced 3D fabricated NAND Flash products
- ✓Samsung 32-tier fabricated 3D products have 1.87 Gb/mm^2



Source: TechInsights

Fabricated 3D Memory

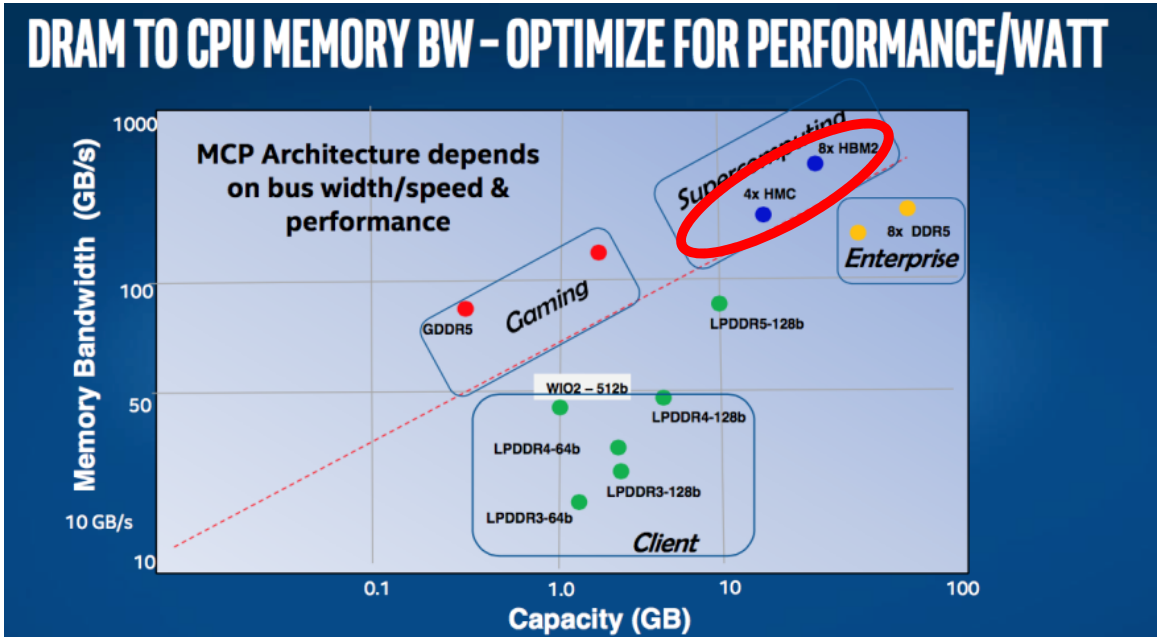


128-tier is the announced goal to achieve cost targets (7.5 Gb/mm^2)

Optimized Performance Per Watt Requires 3D Multi-chip Packaging

AMD, IBM and Intel have all announced 3D packaging

- ✓Shorter distance between components reduces resistance
- ✓Improves bandwidth, power and cost
- ✓Reduces time to market allows integration of parts from multiple process nodes



New Device And Packaging Materials Are Required

Carbon Conductors Look Better Than Cu

	Cu	CNT	GNR	
Max current density (A/cm^2)	**~10^6**	**> 1x10^8**	**> 1x10^8**	**x10^2**
Melting Point (K)	**1356**	**3800** (graphite)	**3800** (graphite)	
Tensile Strength (GPa)	**0.22**	**22.2**	**23.5**	**x10^2**
Thermal Conductivity ($\times 10^3$ W/m-K)	**0.385**	**1.75** *Hone, et al. Phys. Rev. B 1999*	**3 - 5** *Balandin, et al. Nano Let., 2008*	**x10**
Temp. Coefficient of Resistance (10^{-3} /K)	**4**	**< 1.1** *Kane, et al. Europhys. Lett.,1998*	**-1.47** *Shao et al. Appl Phys. Lett., 2008*	
Mean Free Path @ room-T (nm)	**40**	**> 1000** *McEuen, et al. Trans. Nano., 2002*	**~ 1000** *Bolotin, et al. Phys. Rev. Let. 2008*	**x25**

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Many questions still to be answered before graphene or CNT can be considered as practical interconnect materials. The results so far are very promising.

Conductors Are Changing

Composite Copper is in evaluation.

Current status:

Measurement	Conventional Copper	TeraCopper®
Resistivity (Ohm·cm)	**1.66×10^{-6}**	**1.26×10^{-6}**
Conductivity (S/m)	**6.02×10^{7}**	**7.94×10^{7}**
Increase in Conductivity	N/A	**32%**
Avg. Current Capacity(Amps/cm^2)	**3.88×10^{4}**	**5.57×10^{4}**
Increase in Current Capacity	N/A	**44%**

The first electrical performance improvement in copper since 1913 makes composite copper the most electrically conducting material known at room temperature.

Targets for improvement compared to conventional copper are:

- ✓ **100 % increase in electrical conductivity**
- ✓ **100% increase in thermal conductivity**
- ✓ **300% increase in tensile strength**

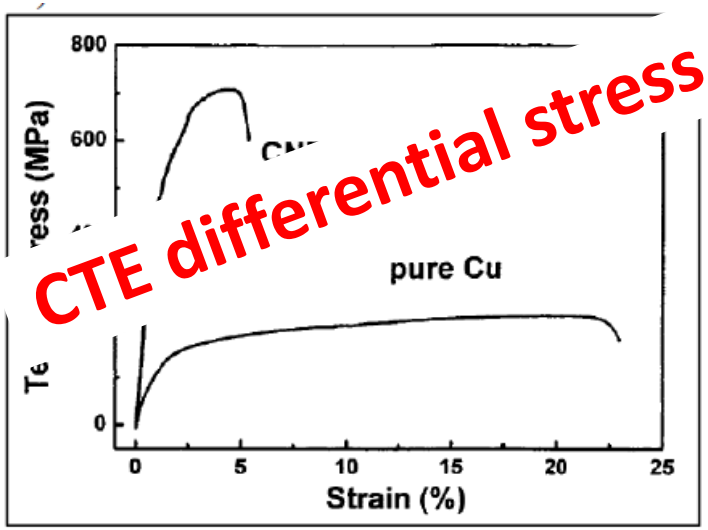
Source: NanoRidge

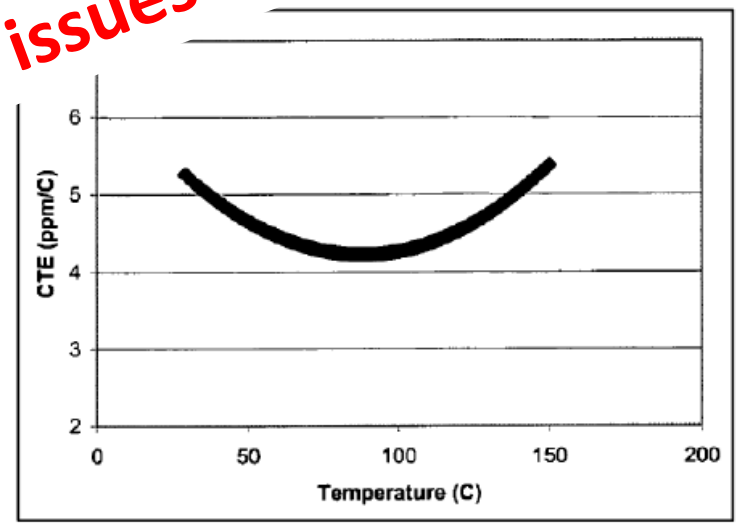
Composite Cu Properties

Measured Properties show:

- ✓The strength of the Cu-SWCNT composite is more than twice that of pure copper
- ✓Ductility is significantly lower.
- ✓Coefficient of thermal expansion ranges betw[illegible]x10-6/°C vs 17x10-6/°C for pure Cu.

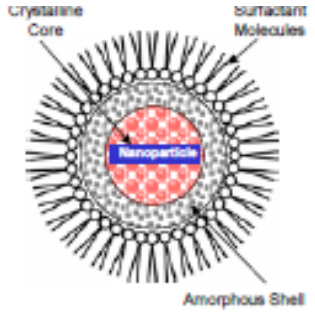
CTE differential stress issues should be solved!

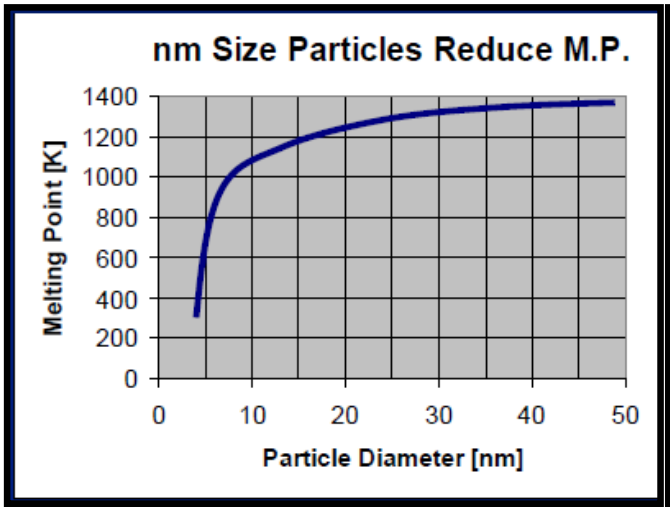


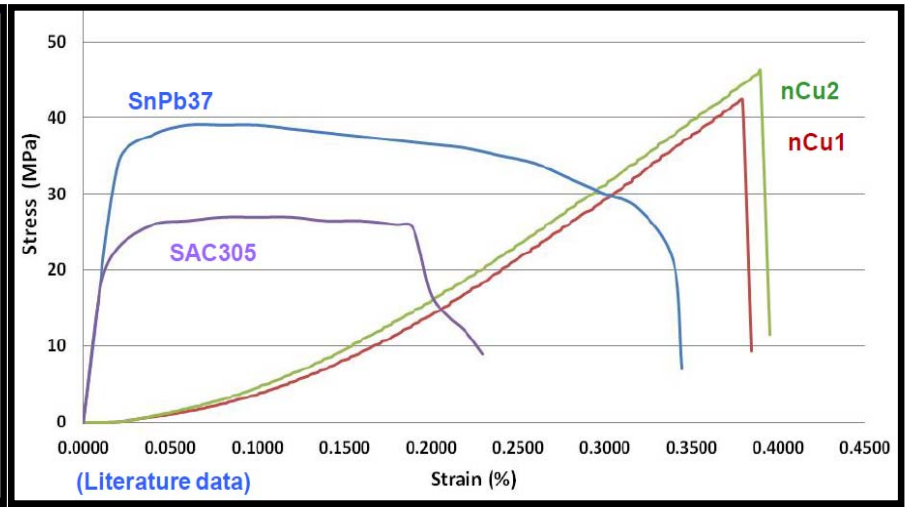


Low temp Cu Nano-solder

- ✓Package assembly at low temp (100C)
- ✓Reflow solder to PCB <200C
- ✓Consistent with Direct Interconnect Bonding
- ✓Thermal/electrical conductivity 10-15X that of SAC







All Processing At "Use Case" Temperature And Matched CTE

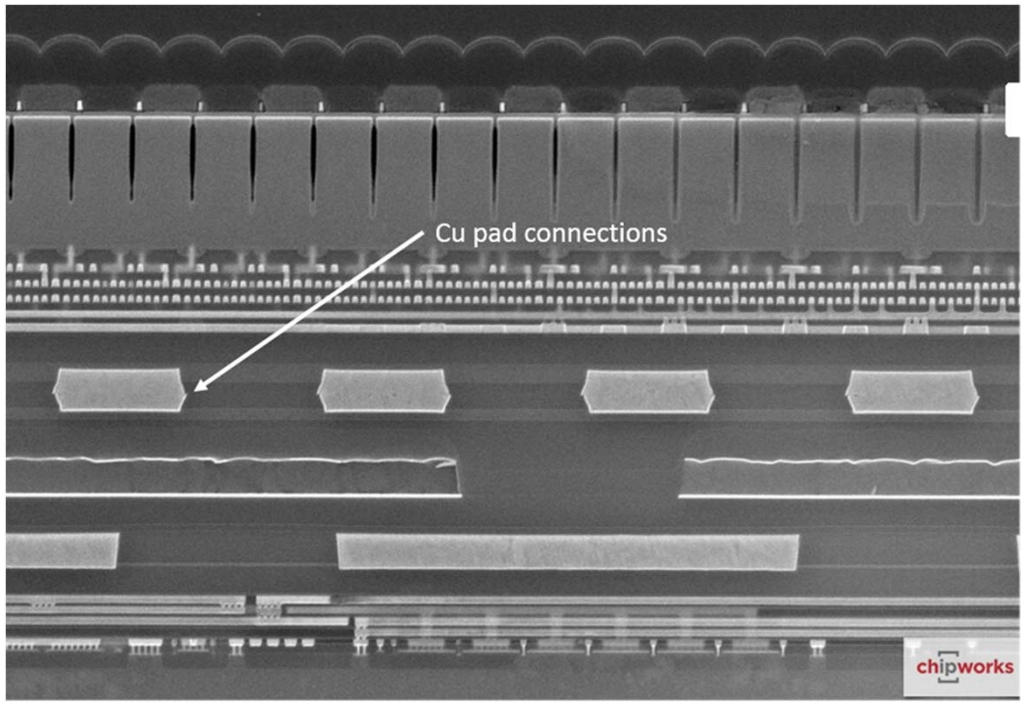
- ✓ Copper nano-solder can join connections at near use case temperature without pressure
- ✓ Limited stress induced due to differential CTE with composite copper
- ✓ No stress built in due to bonding/soldering at high temperature well above "use case" temperature
- ✓ W to W, D to W and D to D bonding using DBI technology

Direct Bond Interconnect Is Now In High Volume Production

Samsung's Galaxy S7 is the first high volume use of of the Ziptronix's DBI technology

- Bonding force is distributed over dielectric and conductor interfaces
- Near use case temperature processing
- No under fill required

Chipworks cross-section of CMOS image sensor shows DBI for Copper pad connections



All Processing At "Use Case" Temperature And Matched CTE

- ✓ Warpage problem is resolved
- ✓ No stress built in due to bonding/soldering at high temperature well above "use case"
- ✓ Limited stress induced due to differential CTE

The materials and processes needed have been demonstrated but not yet integrated

Heterogeneous Integration In 3D-Complex System in Package Enables Solutions To Maintain The Pace Of Progress

The Functions Of A Package

- ✓ **Protect the contents from damage**
  - Mechanical
  - Chemical
  - Electrical
  - Thermal

Packages may be in environments we don't contemplate in an IoT world.

- ✓ **Provide power for operation**
- ✓ **Provide data input/output connections**
- ✓ **Do no harm**
  - Latency
  - Power
  - Cost
  - Reliability

In many of these parameters packaging is the weak link

Heterogeneous Integration by Materials

Conductors

- ✓ Nanomaterials (CNT, graphene, nanowires)
- ✓ Metals (Cu, Al, W, Ag, etc.)
- ✓ Composites

Dielectrics

- ✓ Oxides
- ✓ Polymers
- ✓ Porous materials
- ✓ Composites

Semiconductors

- ✓ Elemental (Si, Ge)
- ✓ Compounds (IIIV, IIVI, tertiary)
- ✓ Polymers

Materials Parameters must be compatible with each other for processing and operation:

- ✓ Cost
- ✓ CTE differential
- ✓ Thermal conductivity
- ✓ Fracture toughness
- ✓ Modulus
- ✓ Processing temperature
- ✓ Interfacial adhesion
- ✓ Operating temperature
- ✓ Breakdown field strength

Heterogeneous Integration by Device

- ✓Memory (DRAM, MRAM, Flash, other)
- ✓Logic
- ✓Sensors
- ✓MEMS
- ✓Mixed Signal
  - Power IC
  - Control IC
- ✓Communications
  - RF
  - Electronic
  - Photonic
  - Plasmonic

During the next 15 years many new devices will be added, each with its own packaging needs:

- ✓ Replacements for the CMOS switch
- ✓ New, more complex sensors
- ✓ New, more complex MEMS
- ✓ Synaptic processors
- ✓ Haptic devices (maybe MEMS)
- ✓ Telepathic devices
- ✓ Telekinetic devices

and devices and functions we cannot yet imagine

Potential Solutions To Support This View Of The Future

- ✓ Higher bandwidth density

WDM single mode Photonics to the package

- ✓ Lower latency

Flat photonic network- replace tree architecture

- ✓ Increased data processing speed

Increased parallelism- more cores & software to match

- ✓ Expanded data storage

3D memory, new memory devices, hierarchical memory architecture

- ✓ Ensured reliability in a world where transistors wear out

Intelligent redundancy
Continuous test while running
Dynamic self repair
Graceful degradation

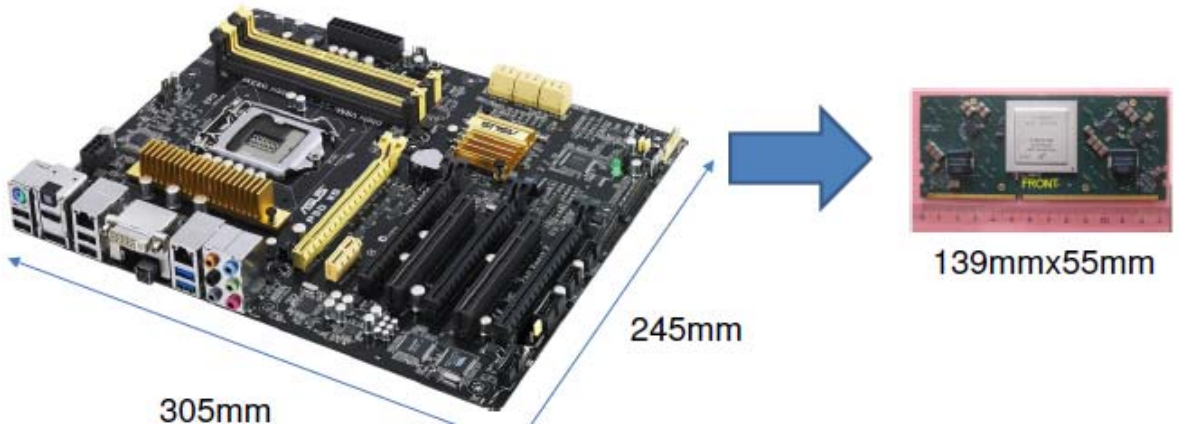
- ✓ Improved security while maintaining process speed and latency

Hardware and software combined-distributed over the global network

3D-SiP Package Architecture With Heterogeneous Integration Will Be Essential

Micro-server Packaging Can Enable Power, Cost and Performance Gains

- ✓The comparison with standard product is dramatic even with conventional PCB assembly and standard off-the-shelf components (Freescale T4240)
- ✓Small size allows photonics to remain at rack unit edge

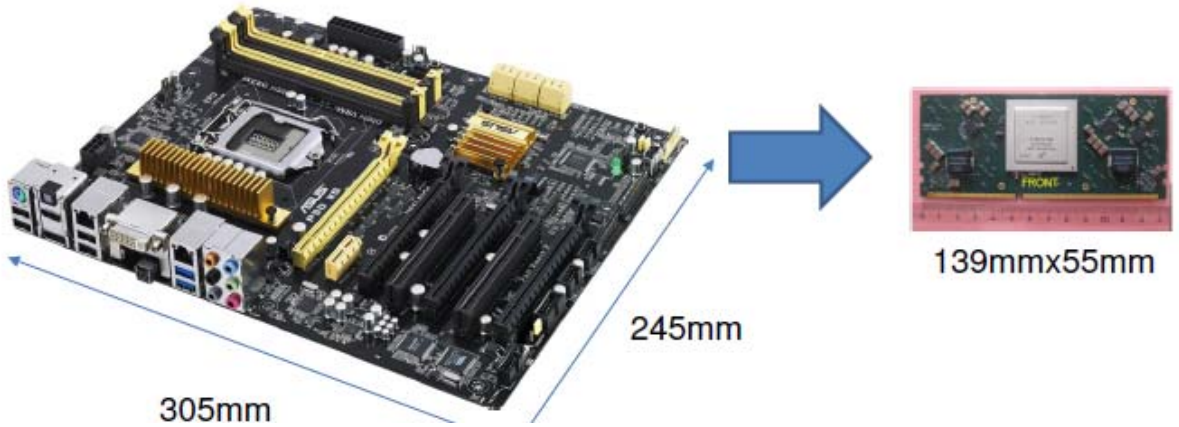


Source: Ronald P. Luijten MIT workshop 7/28/2015

Micro-server Packaging Can Enable Power, Cost and Performance Gains

- ✓The comparison with standard product is dramatic even with conventional PCB assembly and standard off-the-shelf components (Freescale T4240)
- ✓Small si

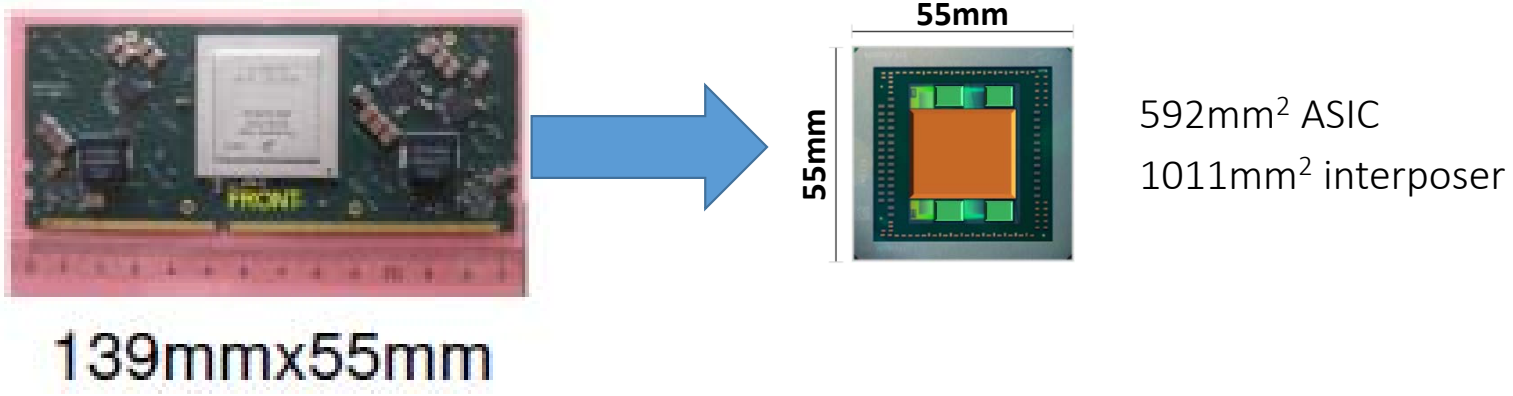
40% faster with 70% of Intel Xeon E3-1230l power yields 2X the operations per watt



Source: Ronald P. Luijten MIT workshop 7/28/2015

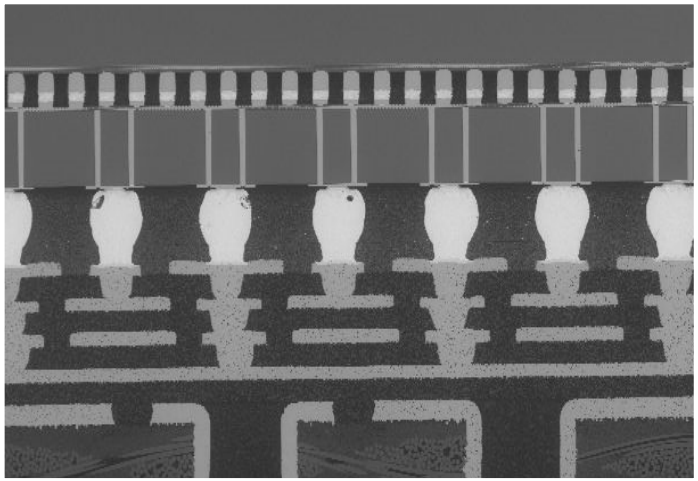
What Could We Do with 3D packaging?

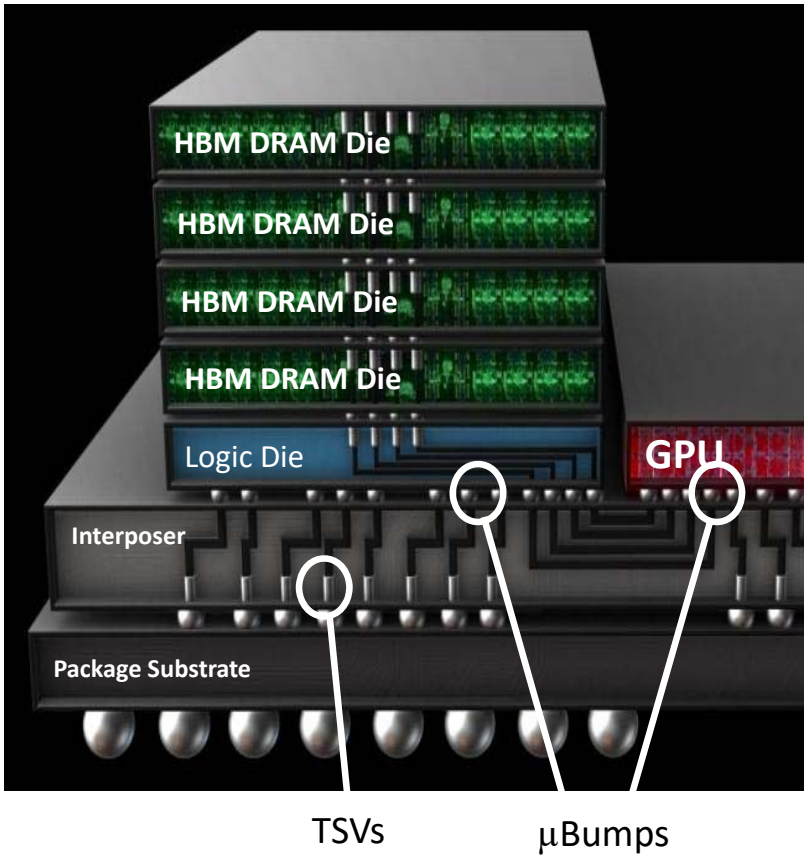
- ✓60% smaller with 16Gb high bandwidth memory
- ✓4096 bit memory interface
- ✓512GB/s memory bandwidth
- ✓Si interposer with TSV & µbump to package substrate
- ✓Lower power
- ✓22 discrete die plus passive components

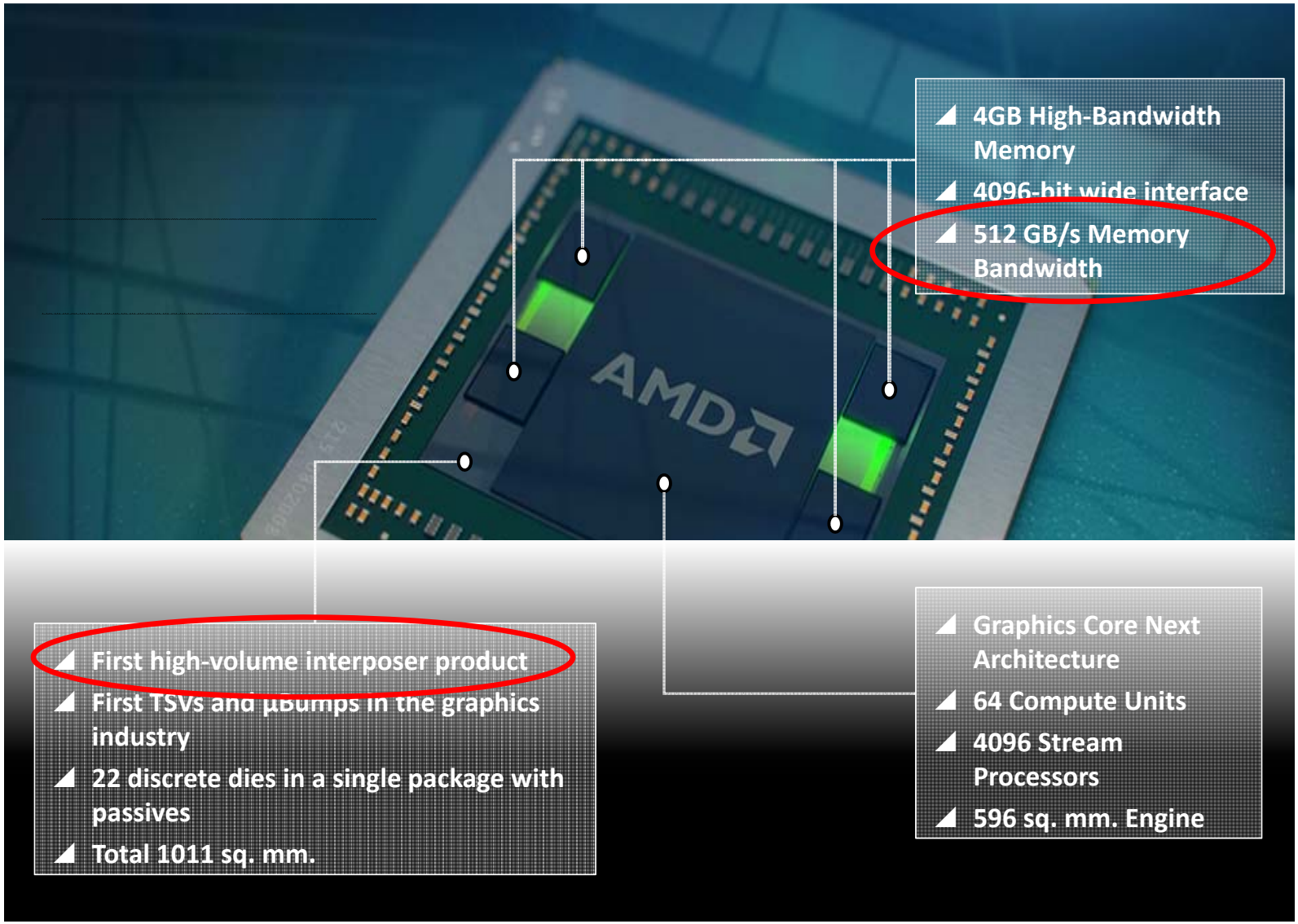


3D Die Stacking Technology (AMD FiJI)

- ✓ Die stacking facilitating the integration of discrete dies and passives
- ✓ 8.5 years of development by AMD and its technology partners






AMD
4GB High-Bandwidth Memory
4096-bit wide interface
512 GB/s Memory Bandwidth
First high-volume interposer product
First TSVs and µBumps in the graphics industry
22 discrete dies in a single package with passives
Total 1011 sq. mm.
Graphics Core Next Architecture
64 Compute Units
4096 Stream Processors
596 sq. mm. Engine

Adding Photonics To The SiP is Next

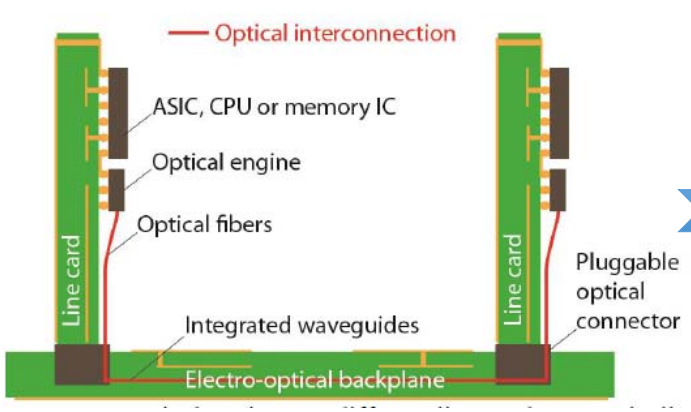
Adding a Silicon photonics chip to the stack would provide:

- ✓Further reductions in power
- ✓Further reductions in latency
- ✓Decrease in total system size

This additional step in heterogeneous integration has difficult challenges including cost reducing silicon photonics and thermal management with high thermal density

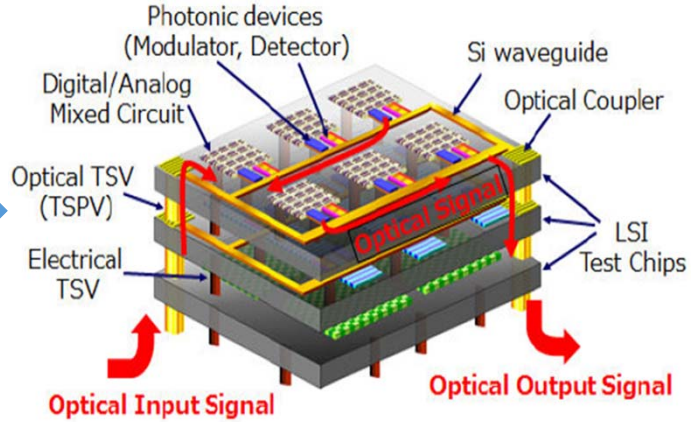
Fiber To The Board Cannot Meet The Challenge

Today



Optical engines on cards optically interconnected into an electro-optical backplane

Future



Optical engines on an electro-optical package substrate interconnected with system level components

What Are The Challenges?

- ✓ **Silicon photonics connections are too expensive for on-chip and perhaps for on-package applications**

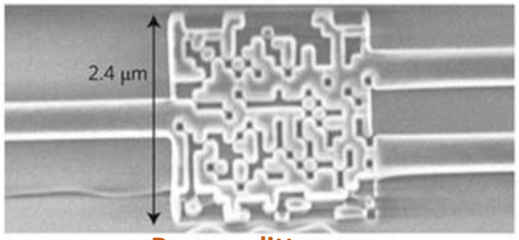
Directed research can change this

- ✓ **Roadblocks:**
  - Co-design tools are not available
  - Size of optical components
  - Lowest power requires heterogeneous integration with new mechanical and thermal challenges
  - Thermal stability of key components requires temp control
  - Hot spots in SiP assemblies and on-chip.

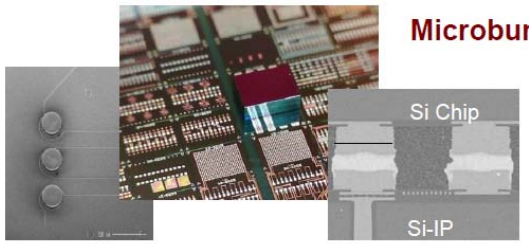
- ✓ **Solutions will require research and development**
  - New materials will be a key
  - TSVs filled with polymer for waveguide?
    - It can also carry electrical signals in TSV lining.

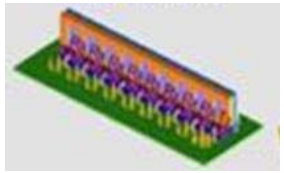
…….and things we have not yet thought of!

Building Blocks Exist For Integrating Photonics Into SiP

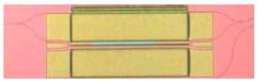


Beam splitters

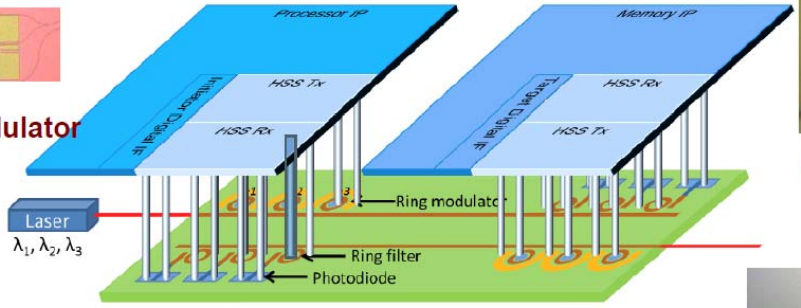


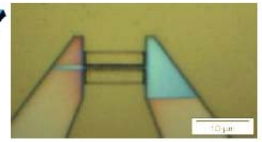


Optical bus

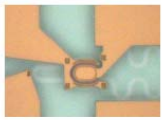


Optical modulator



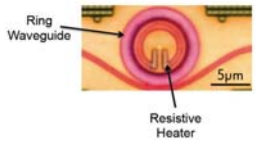


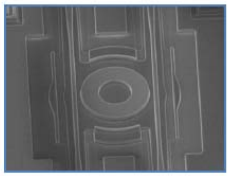
Photodetector



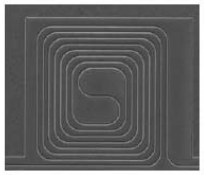
Laser source

Active Wavelength Locking

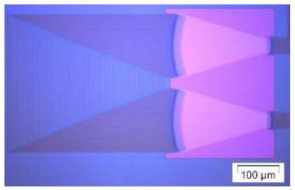




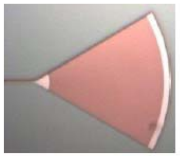
Ring modulator



Waveguides



WDM filters

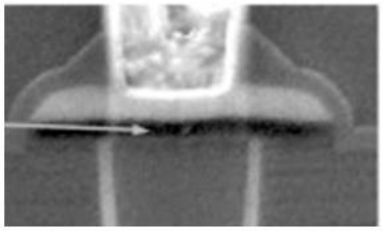


Fiber coupler

Source: ECTC2014 Si Photonics - Stephane BERNABE with additions

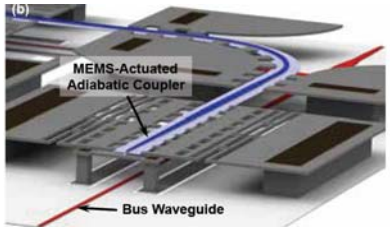
New Device Types Are Coming

These Devices And Their Packaging Will Use New Materials



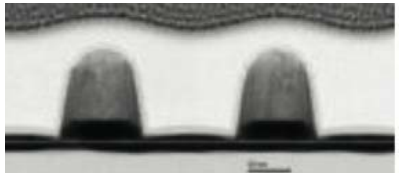
Carbon Nanotube Memory

Tolerant of temp and rad exposure



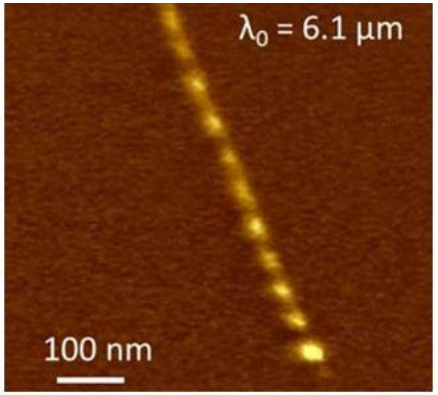
MEMS Photonic switch

Vertical coupler



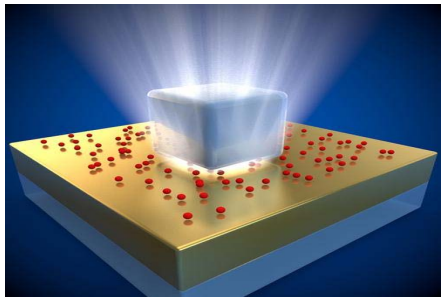
Spin torque devices

(2 magnetic junction pillars)



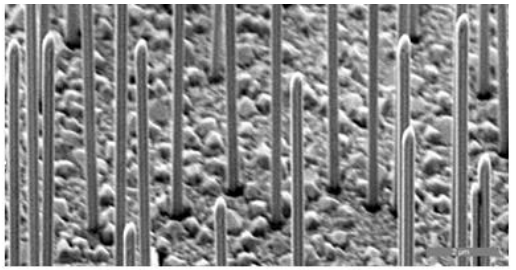
Plasmons in CNT Waveguide

1000 X smaller than photon



Plasmomic emission Source

(quantum dots and plasmons)



GaAs nanowire lasers

(grown on Si with waveguides embedded)

Co-Integration of Technologies

Use each technology where it is the best:

✓Electronics
- Active logic and memory (Processing and routing)
- Smallest size

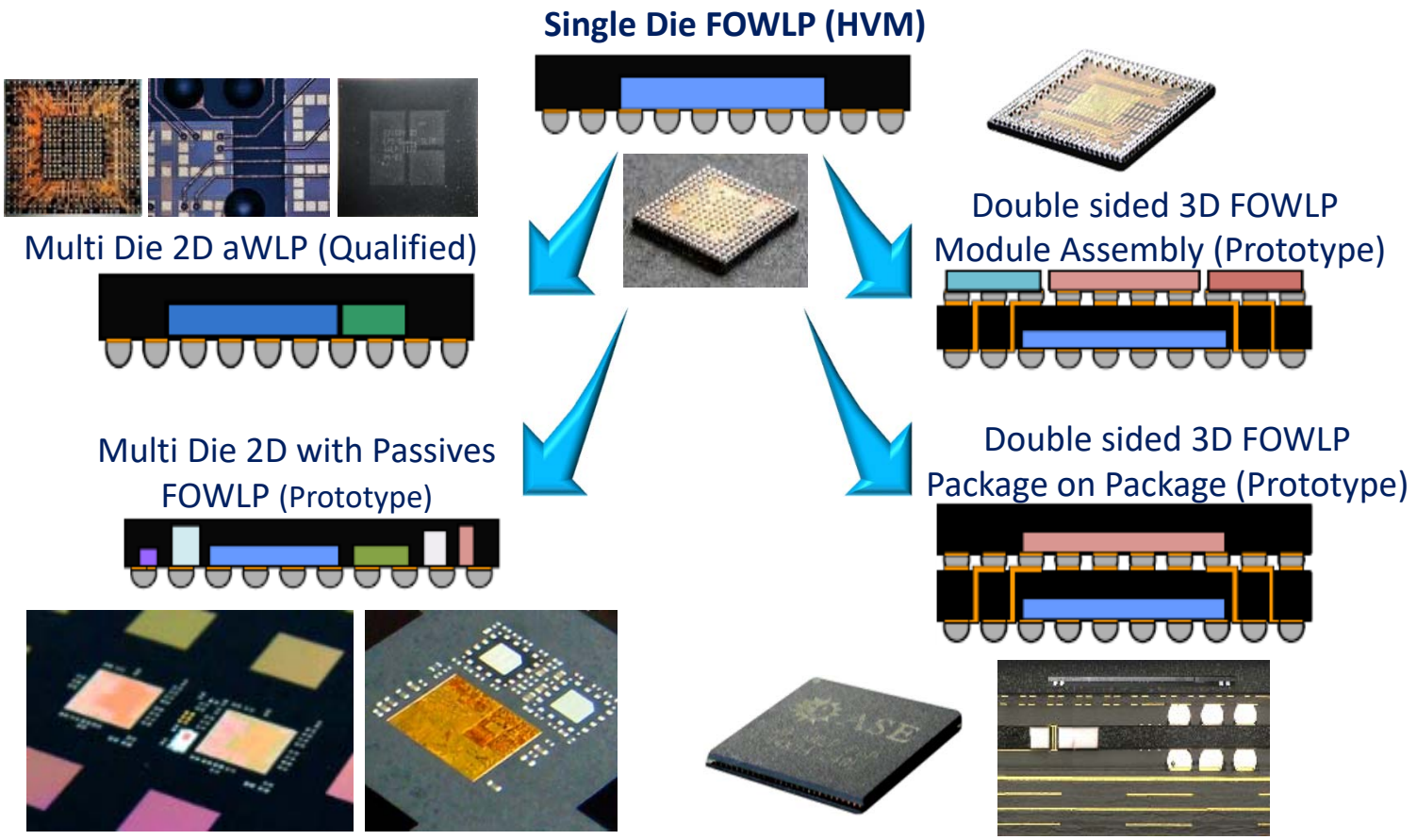
✓Photonics
- High bandwidth
- Energy efficient
- Long and intermediate distance

✓ Plasmonics
- Much smaller than photonic components
- Potentially seamless interface between Optics and Electronics
- Low power active functions

Cost Reduction in HI Manufacturing

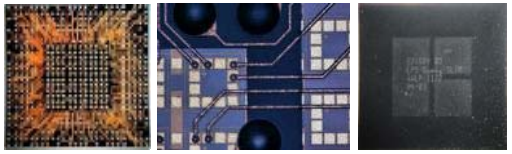
Packaging cost has not scaled with Moore's Law and is now often more expensive than package contents.

Wafer Level Fan Out: Miniaturization & Integration

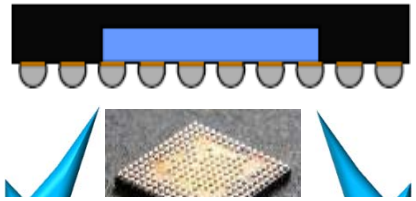


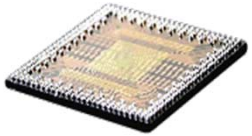
Source: ASE Group

Wafer Level Fan Out: Miniaturization & Integration



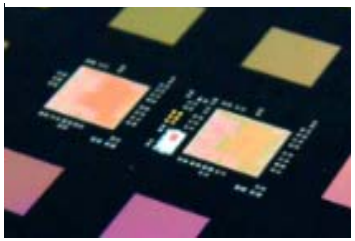
Single Die FOWLP (HVM)

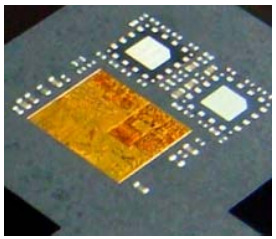


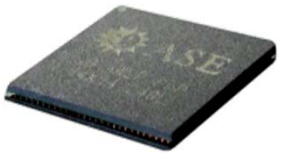


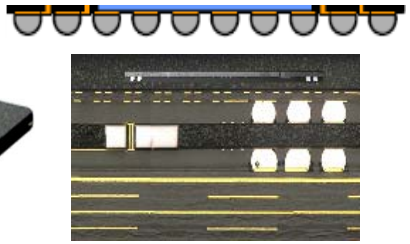
Double sided 3D FOWLP

Panel processing is the logical next step for increased parallelism in package manufacturing and OSATS have the process ready.





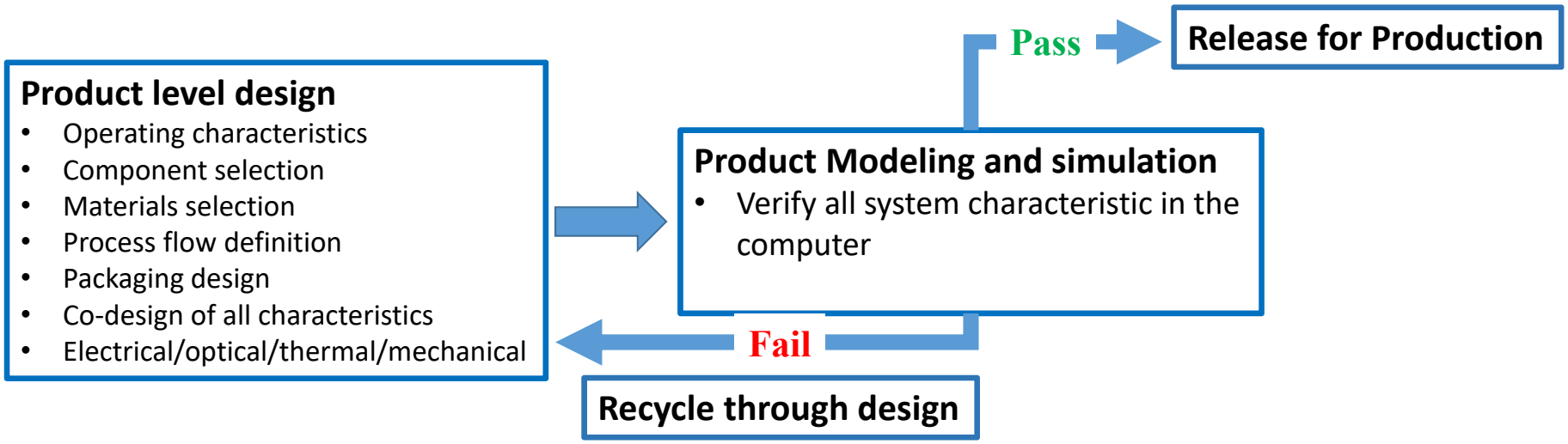




Source: ASE Group

Co-Design And Simulation

We are designing systems in a package and both time to market and non-recurring engineering cost will not allow “build-characterize-modify” cycles to develop consumer product. The future cycle must be:



Co-Design And Simulation

We are designing systems in a package and both time to market and non-recurring engineering cost will not allow “build-characterize-modify” cycles to develop consumer product. The future cycle must be:

Optimizing product characteristics in the computer saves time and money

We don’t know how today due to lack of software tools and unknown materials and interface properties for thin layers

Summary

New driving forces are increasing the demand for innovation in Heterogeneous Integration and Photonics Packaging

- ✓We have the components
- ✓Co-design and simulation tools are maturing although not yet ready
- ✓Progress will be paced by how aggressive we are in integrating these assets into high volume products with lower cost, reduced power, reduced latency, higher performance, and smaller size

Roadmaps enable pre-competitive collaboration to solve difficult challenges before they become Roadblocks while reducing cost and time to market.

Thank You for Your Attention