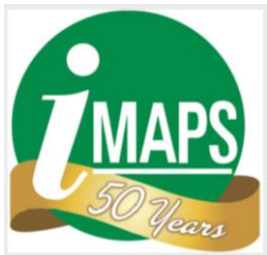**eda2asic**

Building an EcoSystem for User-friendly Design of Advanced System in Package (SiP) Solutions

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IMAPS, Oct 9 – 12 & MEPTEC, Nov 13, 2017

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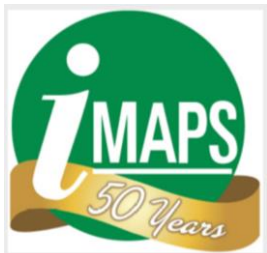
IMAPS' 50th International Symposium on Microelectronics

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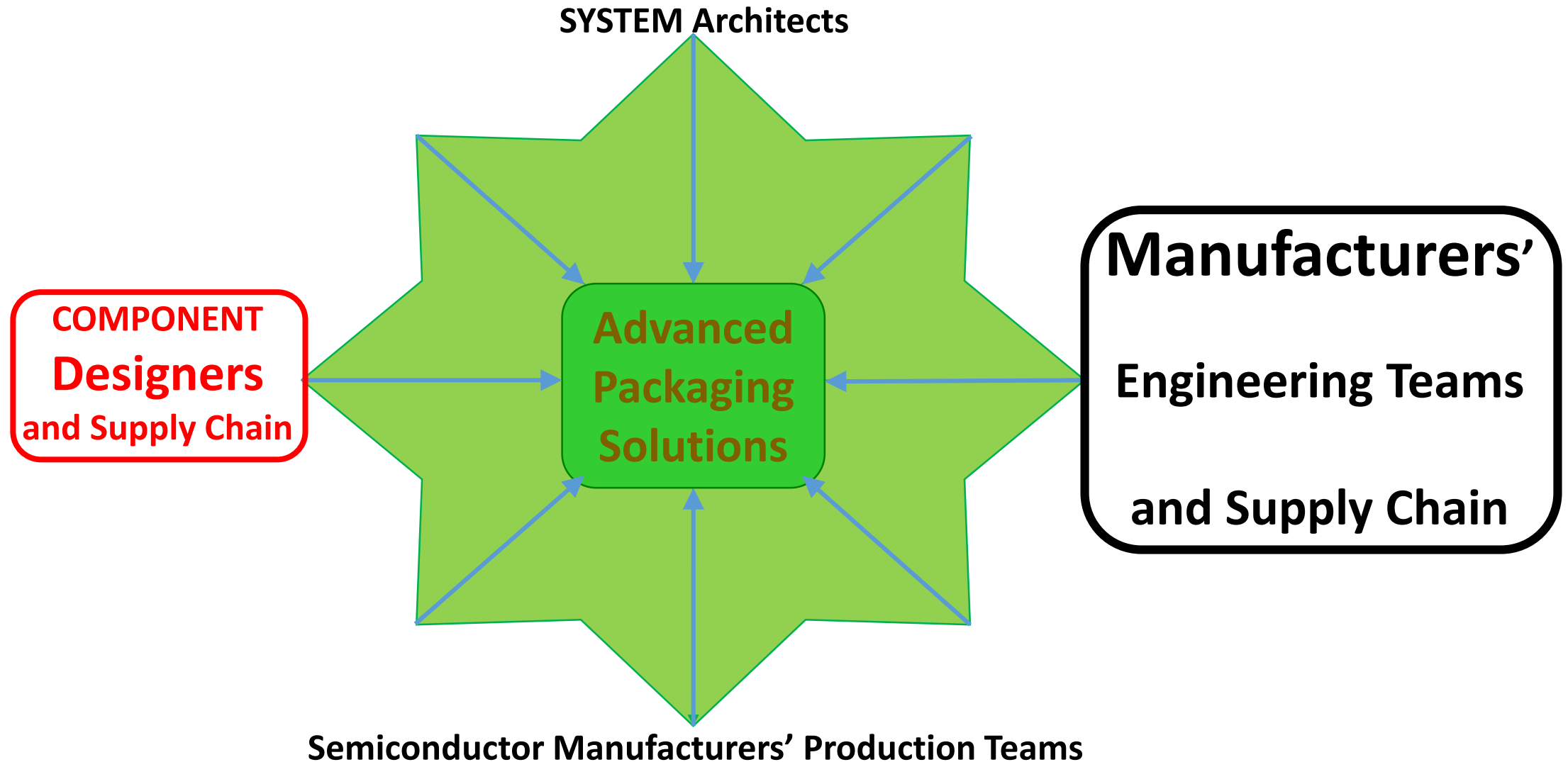
1)Introduction

2)EcoSystem Considerations

3)Summary

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- **Target Audience**

- **Major System in Package (SiP) Advantages**

- **Changes of Paradigm for IC Packaging**

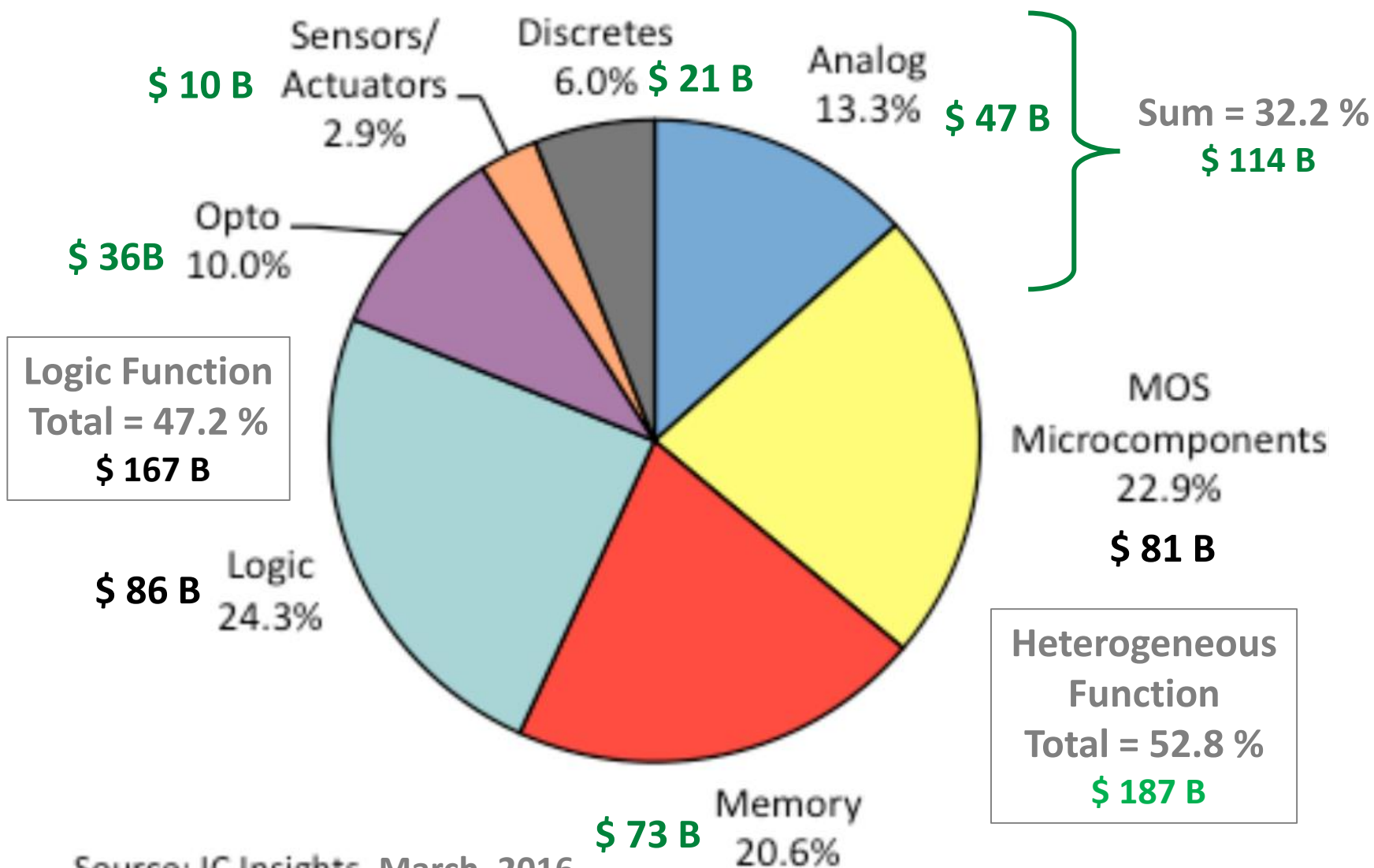- **New Technologies displace older ones**

SYSTEM Architects

COMPONENT Designers and Supply Chain

Advanced Packaging Solutions

Manufacturers' Engineering Teams and Supply Chain

Semiconductor Manufacturers' Production Teams

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- **RETURN ON INVESTMENT:** Lower NRE and system cost, less time to profit, smaller design teams

- **HETEROGENEOUS FUNCTIONS:** Integrates logic, Analog, RF, MEMS,... into one IC package

- **POWER DISSIPATION:** Reduces power consumed in I/Os and the connections between ICs

- **FORMFACTOR:** Reduces board-space as well as system weight and size

- **MODULARITY:** Simplifies and accelerates customization and incremental improvements

- **APPLICATIONS FOCUS:** Allows segment experts to focus on die-level IP building blocks ("dielets")

- **(De-facto) STANDARDS:** Will enable designers to draw from a "dielets" toolbox --- like LEGO !

Heterogeneous Integration is Key

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Sensors/Actuators 2.9% — **$ 10 B**

Discretes 6.0% **$ 21 B**

Analog 13.3% **$ 47 B**

Sum = 32.2 % **$ 114 B**

Opto 10.0% — **$ 36B**

Logic Function Total = 47.2 % **$ 167 B**

$ 86 B Logic 24.3%

MOS Microcomponents 22.9% **$ 81 B**

Heterogeneous Function Total = 52.8 % **$ 187 B**

$ 73 B Memory 20.6%

Source: IC Insights, March, 2016

Semiconductor Revenues in 2015: $ 353.7 B = 100%

Integration of the needed functions in the most appropriate process technologies reduces NRE & cost and lowers power dissipation!

http://www.icinsights.com/news/bulletins/Optoelectronics-SensorsActuators-And-Discretes-Will-Stabilize-After-Spotty-Growth-In-2015/

11/11/2017

6

Changes of Paradigm for IC Packaging

- ## Package as Commodity
  - Assembly & Test resides in low labor-cost countries
  - IC vendors dictate materials, manufacturing & test equipment, flows, Q&A,…

- ## Package as Differentiator
  - IC Vendors and Packaging Experts develop **custom solutions**
  - Both parties invest significant engineering resources into every program

- ## Package as Function and as System Integration Enabler
  - In addition to the traditional functions (protect die, supply power, conduct heat, …) SiPs enable:
    - Integrating sub-systems or entire systems, based on (heterogeneous) die-level building blocks
    - Serving many lower/medium volume applications, offering lower NREs & shorter times to market
    - Developing customizable platforms that reduce customers' and suppliers' engineering efforts
      - ➔ Assembly Design Kits and Reference Design Flows will be essential for this transition !

New Technologies Displace Older Ones

- **Examples for new technology roll-outs during Herb's career**
  - 7400 TTL ➔ **FPGAs / ASICs**
  - Bipolar Gate Arrays ➔ **CMOS ASICs: 3 / 2 / 1.5µ**

    ASIC: National Semiconductor ... 9 yrs

  - 1.0 ➔ 0.8 ➔ 0.6 ➔ 0.5 ➔ **0.35µ CMOS ASICs**
  - Proprietary CPUs ➔ **ARM cores**

    ASIC: VLSI Technology ... 9 yrs

  - Dynamic simulation ➔ **Static Timing Analysis**
  - IDM ➔ **Foundry: TSMC Ref. Flows & 1st PDKs**

    EDA: ViewLogic & Synopsys ... 5 yrs

  - 2D SoC ➔ **2.5/3D-ICs, FOWLP, SiP,…**
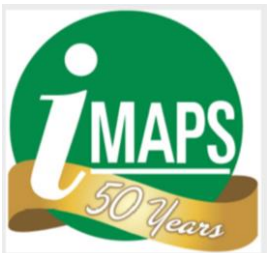
    eda**2**asic ... **16 yrs**

    GSA, SEMATECH, Si², EDAC

- **Key Success Criteria for every new technology**
  - Unit cost / Development cost & time / Flexibility / Functionality / **EcoSystem**

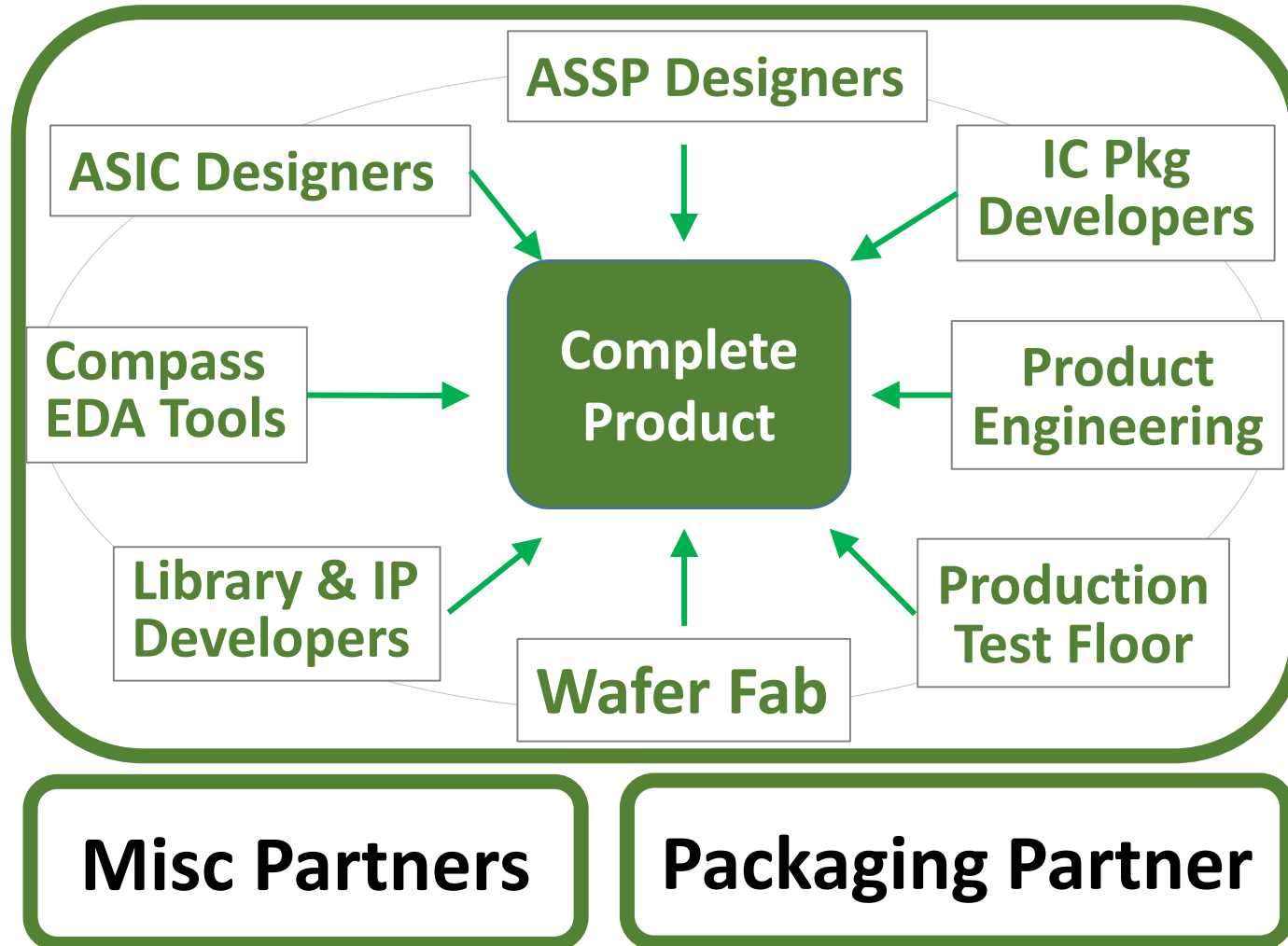# 2) EcoSystem Considerations

- **Technology roll out in the IDM business model**

- **Technology roll-out in today's EcoSystem**

- **Design** **EcoSystem partners' needs**

- **Assembly Design Kit**

- **Die(s) – Package – Board reference flow**

Technology Roll Out – IDM Business Model

VLSI Technology Program Management

- **Program Mgmt within an IDM:**
  - Same corporate ROI objectives
  - Developers know each other well
  - Regular coordination meetings
  - Development specifications and schedules tightly coordinated, even with captive EDA developers
  - Responsibilities clearly defined
  - Simple risks and rewards sharing
  - Technical expertise from partners
  - ONE decider settles conflicts
  - **Major customer as driver !!!**

Technology Roll-out in Today's EcoSystem

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Architects at Customers

DESIGN: Computer Science & Electrical Engineers

MANUFACTURING: Mechanical & Chemical Engineers

IC Silicon Designers

IC Package Developers

EDA Tools Suppliers

Advanced Packaging Solutions

Package Materials Suppliers

IP Building Blocks Suppliers

Suppliers of Manufacturing and Metrology Equipment

Manufacturing
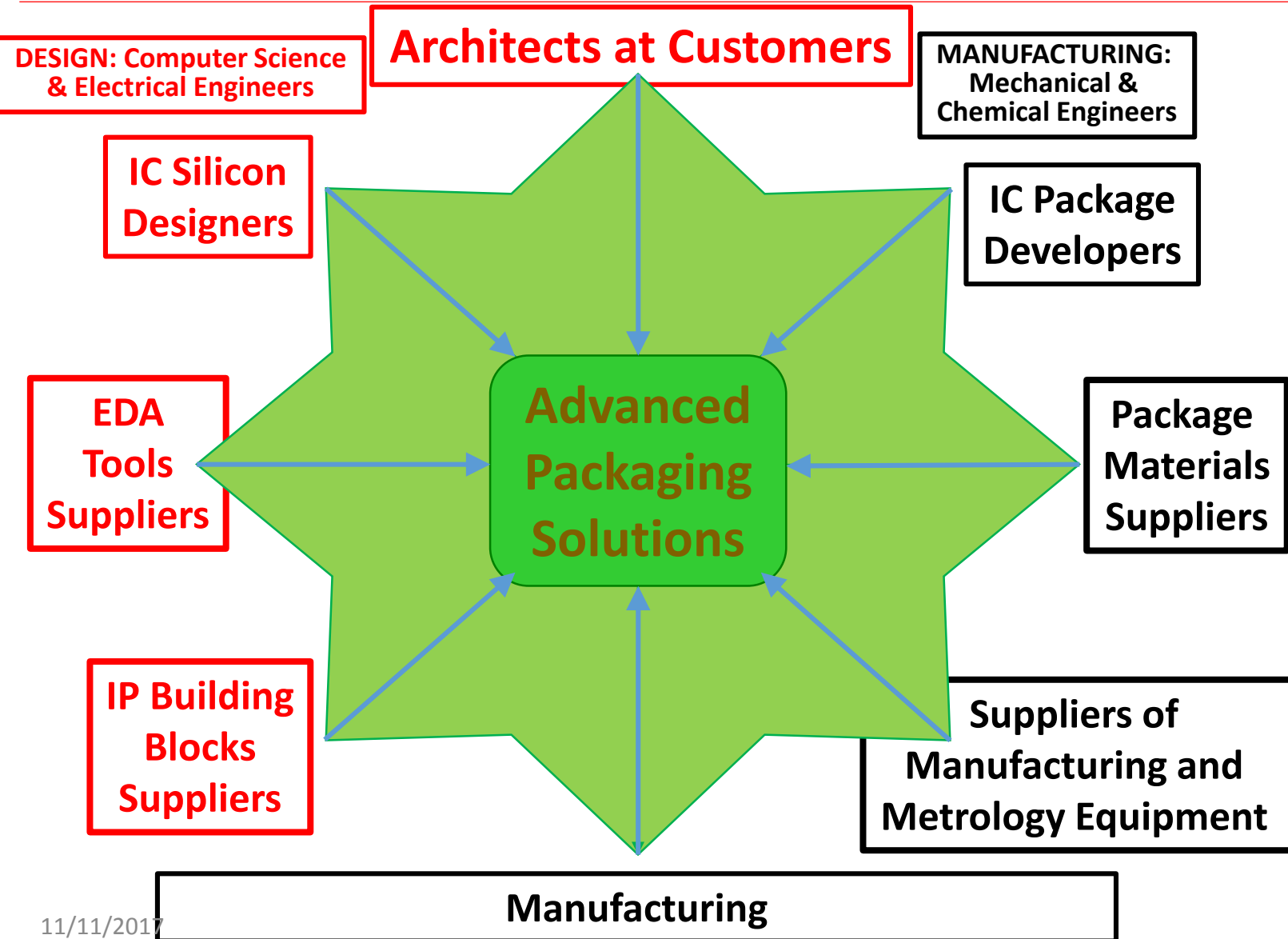
EcoSystem "Mgmt":

- Justify ROI to each company
- Introduce all new partners
- Attend industry conferences
- Agree on who does what and organize coordination mtgs
- Sync development schedules
- Find risks & rewards balance
- Define rules to arbitrate/resolve technical & biz conflicts
- **Key opportunities as drivers**

Design EcoSystem Partners' Needs

- ## Architects and IC Designers need, e.g.:
  - Management support and risk reductions to deploy a new technology
  - Education about die and package CO-design benefits
  - User-friendly multi-die and multi-physics design tools and flows
  - Accurate and up-to-date PDKs and **ADKs (Assembly Design Kits)**

- ## EDA Tools Suppliers need, e.g.:
  - Major potential customers to guarantee design tools ROI
  - Partner inputs to structure a complete die-pkg-board design flow
  - Funding and cooperation for joint development of encrypted ADK(s)
  - Industry standards for data exchange formats and hand-off criteria

- ## Die-level IP Building Blocks (Chiplets) Suppliers need, e.g.:
  - Major potential customers to ensure correct application focus and attractive ROI
  - Industry support to structure a profitable "bare die" business model
    - Cost effective design, manufacturing & test flow for KGD (smart wafer stacking,…)
    - Die-to-die interface standards and traceability system for all SiP components

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Packaging and EDA experts develop jointly – with customer(s) inputs:
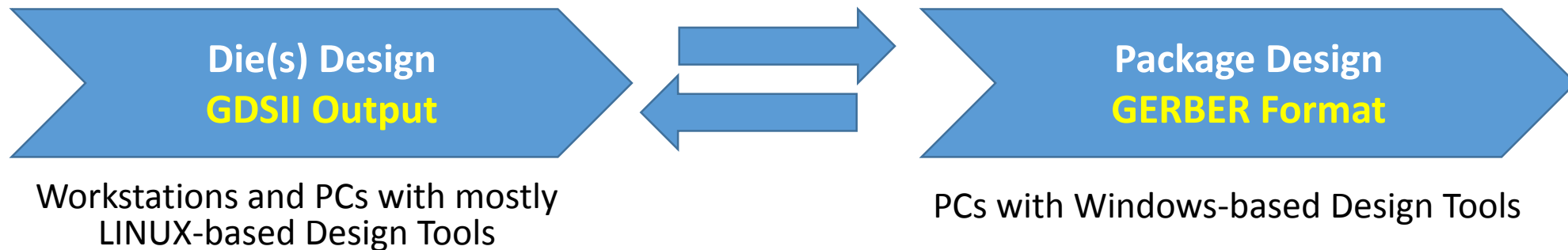
- **Assembly Design Kits (ADKs) to include:**
  - Available – off the shelf – packaging solutions (platforms) and rules for customization
  - Design Rules for TSV last, back-side RDL, Micro-balls, Cu-Studs,…
  - Material characteristics: CTE, Poisson ratio, Young's modulus, loss tangent, thermal conductivity for: Substrate, Over-Mold, Underfill, Interposer(s), UBM, Balls,…
  - Equipment capabilities: Accuracy, UPH, wafer / panel sizes, facility spec, temperature profiles,..
  - Above info – in encrypted format – to feed into the recommended tools – while protecting your IP
  - Description of feedback loop from customers and outline of logistics updating needed

- **ADKs serve three important design steps:**
  - Planning: Feasibility study, system level considerations, partitioning into dies,…
  - Implementing: Package selection, Interposer-design rules, die to die spacing,…
  - Verifying: Thermal profile, thermal-mechanical effects, power and signal paths,…

Multi-die Reference Design Flow

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Packaging and EDA experts develop jointly – with customer(s) inputs:

- ### Die – Package – Board Reference Design Flow:
  - Recommends tools for design planning, implementation and verification steps for multi-die ICs
  - Describes hand-of criteria from designers to manufacturing partner's assembly and test team
  - Outlines logistics and inputs needed for wafer-probe, interim and final test
  - Suggests how and who to cooperate with at the EDA as well as the assembly and test partner
  - Lists additional info sources: Web-pointers, industry standards, white papers, books, …
  - Describes best practices for data exchange between die(s) and package; encourages CO-design

Die(s) Design GDSII Output	⇒ ⇐	Package Design GERBER Format

Workstations and PCs with mostly
LINUX-based Design Tools

PCs with Windows-based Design Tools

- **Maturity of the manufacturing flow influences when to automate which design step(s) !**

EDA Tools Suppliers' Value Proposition

Rely on EDA tools instead of developing numerous prototypes!

EDA tools help designers to walk the fine line between a **costly** over-design and an **unreliable** under-design!

The outputs of EDA Tools are only as accurate and useful as their inputs:
- **Accurate and up-to-date PDK**
- **Accurate and up-to-date ADK**

COST

Reliability

EDA 3D

EDA

EDA 2.5D

EDA

Law

EDA

Moore's

EDA
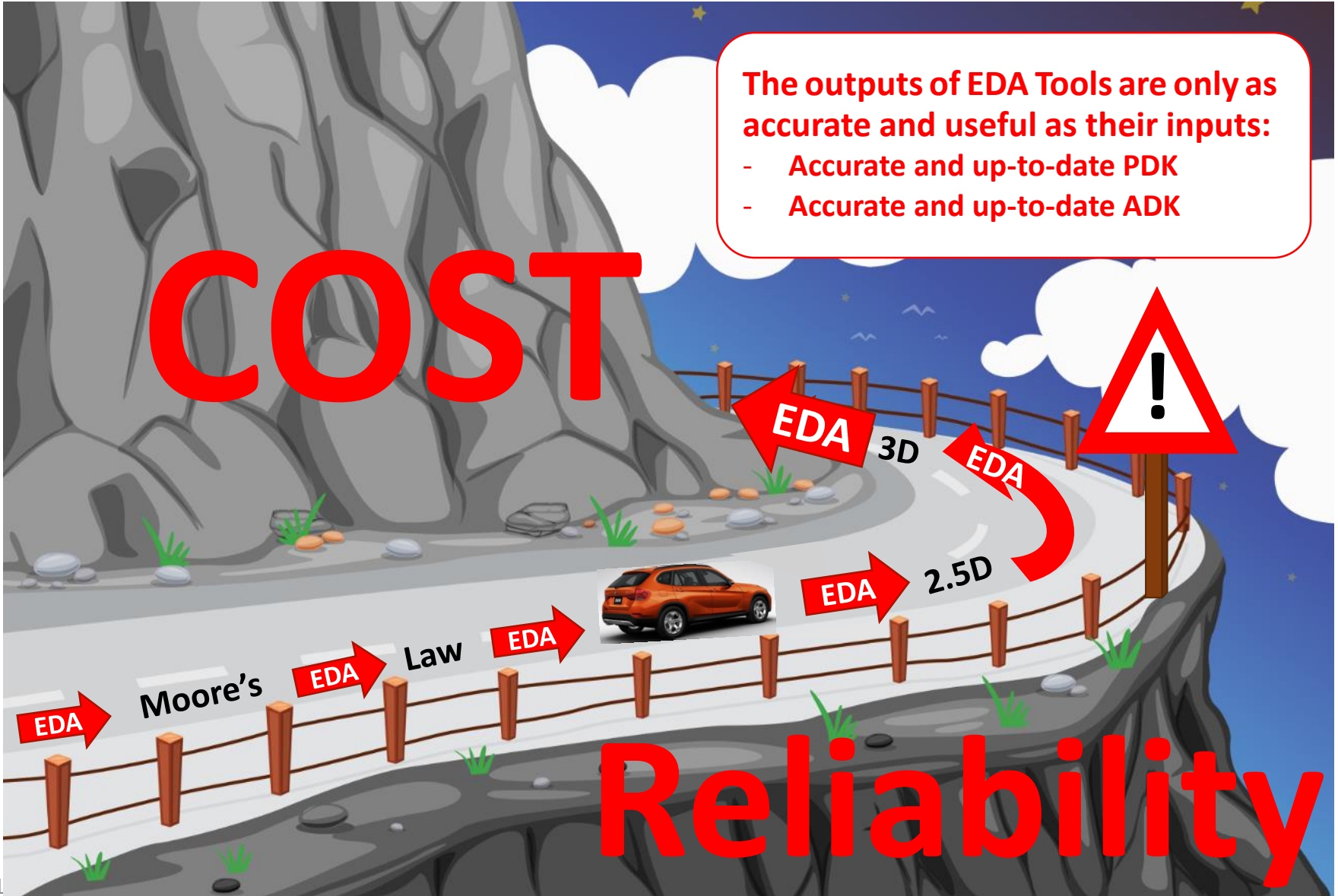
eda2asic EDA, IC Design & Manufacturing Cooperation

Chiplets & IC Designers

3 Tools for IC and Package CO-Planning, Design and Verification

4

ADK: Assembly Design Kit:
Electrical, Thermal, Mechanical, Chemical, Thermo-Mechanical Characteristics of all Package Materials.

Off-the-Shelf Packages, Test Strategies, Die-level IP Blocks,…

PDK: Process Design Kit:
Core & I/O Libraries, Memory Compilers.

Spice Decks, Rules for DRC & ESD & EM,..

EDA Vendors

Modeling and Encrypting Tools

Die(s) Manuf, Data:
GDSII Data Base(s), Wafer-probe Data

Package Manuf. Data:
Placement of Dies, Passives, Micro-balls or Cu-Studs or DBIs.

Specifications for Interposer, Underfill, Pkg Substrate, Caps.

Assembly Diagrams.

Electrical, Mechanical, Thermal and other SiP Test Conditions

1

Wafer-FABs

2

Assembly and Test Houses (OSATs)

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- **Automotive EcoSystem evolution**

- **No shortcuts, please**

- **Cooperation ! ! !**

Automotive EcoSystem Evolution

Model T

The Semiconductor EcoSystem is likely to develop
in a very similar way --- in the next few decades !
➜ **Leveraging SiP modularity, flexibility, cost, time to profit...**

Focus

~ 1900: Ford designed and manufactured
every Model T component in house

~ 2000: Ford's EcoSystem partners design and mass-
produce most of the Ford Focus components !

Ford designs and manufactures ONLY core components and assembles / markets / sells the final product.

NO Shortcuts, Please !

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Industry Trends:

- **Mergers & Acquisitions**

- **Partnerships & Alliances**

- **Industry Organizations**

- **Design & Manuf. Standards**

- **Machine Learning**

- **Continuous Education**

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Thank You !

IMAPS' 50th International Symposium on Microelectronics

Leadership Lessons of Steve Jobs

✓ Focus

✓ Simplify

✓ Take responsibility end to end

✓ When behind, leapfrog

✓ Put products before profits

✓ Don't be a slave to focus groups

✓ Bend reality

✓ Impute

✓ Push for perfection

✓ Tolerate only "A" players

✓ Engage face-to-face

✓ Know both the big picture and the details

✓ Combine the humanities with the sciences

✓ Stay hungry, stay foolish

http://hbr.org/2012/04/the-real-leadership-lessons-of-steve-jobs/ar/1

Steve Jobs by Walter Isaacson