Building an EcoSystem for User-friendly Design of Advanced System in Package (SiP) Solutions

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Agenda

1) Introduction

2) EcoSystem Considerations

3) Summary
1) Introduction

• Target Audience
• Major System in Package (SiP) Advantages
• Changes of Paradigm for IC Packaging
• New Technologies displace older ones
Target Audience

SYSTEM Architects

Advanced Packaging Solutions

Manufacturers’ Engineering Teams and Supply Chain

Semiconductor Manufacturers’ Production Teams

COMPONENT Designers and Supply Chain
Major SiP Advantages

• **RETURN ON INVESTMENT**: Lower NRE and system cost, less time to profit, smaller design teams

• **HETEROGENEOUS FUNCTIONS**: Integrates logic, Analog, RF, MEMS,... into one IC package

• **POWER DISSIPATION**: Reduces power consumed in I/Os and the connections between ICs

• **FORMFACTOR**: Reduces board-space as well as system weight and size

• **MODULARITY**: Simplifies and accelerates customization and incremental improvements

• **APPLICATIONS FOCUS**: Allows segment experts to focus on die-level IP building blocks (“dielets”)

• **(De-facto) STANDARDS**: Will enable designers to draw from a “dielets” toolbox --- like LEGO !
Heterogeneous Integration is Key

Semiconductor Revenues in 2015:
$ 353.7 B = 100%

Integration of the needed functions in the most appropriate process technologies reduces NRE & cost and lowers power dissipation!

Source: IC Insights, March, 2016

Changes of Paradigm for IC Packaging

• Package as Commodity
  • Assembly & Test resides in low labor-cost countries
  • IC vendors dictate materials, manufacturing & test equipment, flows, Q&A,…

• Package as Differentiator
  • IC Vendors and Packaging Experts develop custom solutions
  • Both parties invest significant engineering resources into every program

• Package as Function and as System Integration Enabler
  • In addition to the traditional functions (protect die, supply power, conduct heat, …) SiPs enable:
    • Integrating sub-systems or entire systems, based on (heterogeneous) die-level building blocks
    • Serving many lower/medium volume applications, offering lower NREs & shorter times to market
    • Developing customizable platforms that reduce customers’ and suppliers’ engineering efforts
      ➔ Assembly Design Kits and Reference Design Flows will be essential for this transition!
New Technologies Displace Older Ones

- Examples for new technology roll-outs during Herb’s career
  - 7400 TTL → FPGAs / ASICs
  - Bipolar Gate Arrays → CMOS ASICs: 3 / 2 / 1.5μ
  - 1.0 → 0.8 → 0.6 → 0.5 → 0.35μ CMOS ASICs
  - Proprietary CPUs → ARM cores
  - Dynamic simulation → Static Timing Analysis
  - IDM → Foundry: TSMC Ref. Flows & 1st PDKs
  - 2D SoC → 2.5/3D-ICs, FOWLP, SiP,…

- Key Success Criteria for every new technology
  - Unit cost / Development cost & time / Flexibility / Functionality / EcoSystem
2) EcoSystem Considerations

• Technology roll out in the IDM business model

• Technology roll-out in today’s EcoSystem

• Design EcoSystem partners’ needs

• Assembly Design Kit

• Die(s) – Package – Board reference flow
Program Mgmt within an IDM:
- Same corporate ROI objectives
- Developers know each other well
- Regular coordination meetings
- Development specifications and schedules tightly coordinated, even with captive EDA developers
- Responsibilities clearly defined
- Simple risks and rewards sharing
- Technical expertise from partners
- ONE decider settles conflicts
- Major customer as driver !!!
Technology Roll-out in Today’s EcoSystem

EcoSystem “Mgmt”:

- Justify ROI to each company
- Introduce all new partners
- Attend industry conferences
- Agree on who does what and organize coordination mtgs
- Sync development schedules
- Find risks & rewards balance
- Define rules to arbitrate/resolve technical & biz conflicts
- Key opportunities as drivers
Design EcoSystem Partners’ Needs

• Architects and IC Designers need, e.g.:
  • Management support and risk reductions to deploy a new technology
  • Education about die and package CO-design benefits
  • User-friendly multi-die and multi-physics design tools and flows
  • Accurate and up-to-date PDKs and ADKs (Assembly Design Kits)

• EDA Tools Suppliers need, e.g.:
  • Major potential customers to guarantee design tools ROI
  • Partner inputs to structure a complete die-pkg-board design flow
  • Funding and cooperation for joint development of encrypted ADK(s)
  • Industry standards for data exchange formats and hand-off criteria

• Die-level IP Building Blocks (Chiplets) Suppliers need, e.g.:
  • Major potential customers to ensure correct application focus and attractive ROI
  • Industry support to structure a profitable “bare die” business model
    • Cost effective design, manufacturing & test flow for KGD (smart wafer stacking,…)
    • Die-to-die interface standards and traceability system for all SiP components
Packaging and EDA experts develop jointly – with customer(s) inputs:

- **Assembly Design Kits (ADKs) to include:**
  - Available – off the shelf – packaging solutions (platforms) and rules for customization
  - Design Rules for TSV last, back-side RDL, Micro-balls, Cu-Studs,…
  - Material characteristics: CTE, Poisson ratio, Young’s modulus, loss tangent, thermal conductivity for: Substrate, Over-Mold, Underfill, Interposer(s), UBM, Balls,…
  - Equipment capabilities: Accuracy, UPH, wafer / panel sizes, facility spec, temperature profiles,…
  - Above info – in encrypted format – to feed into the recommended tools – while protecting your IP
  - Description of feedback loop from customers and outline of logistics updating needed

- **ADKs serve three important design steps:**
  - Planning: Feasibility study, system level considerations, partitioning into dies,…
  - Implementing: Package selection, Interposer-design rules, die to die spacing,…
  - Verifying: Thermal profile, thermal-mechanical effects, power and signal paths,…
Packaging and EDA experts develop jointly – with customer(s) inputs:

- **Die – Package – Board Reference Design Flow:**
  - Recommends tools for design planning, implementation and verification steps for multi-die ICs
  - Describes hand-of criteria from designers to manufacturing partner’s assembly and test team
  - Outlines logistics and inputs needed for wafer-probe, interim and final test
  - Suggests how and who to cooperate with at the EDA as well as the assembly and test partner
  - Lists additional info sources: Web-pointers, industry standards, white papers, books, ...
  - Describes best practices for data exchange between die(s) and package; encourages CO-design

- **Maturity of the manufacturing flow influences when to automate which design step(s) !**
EDA Tools Suppliers’ Value Proposition

Rely on EDA tools instead of developing numerous prototypes!

EDA tools help designers to walk the fine line between a costly over-design and an unreliable under-design!

The outputs of EDA Tools are only as accurate and useful as their inputs:
- Accurate and up-to-date PDK
- Accurate and up-to-date ADK
EDA, IC Design & Manufacturing Cooperation

1. Wafer-FABs
   - Die(s) Manuf. Data: GDSII Data Base(s), Wafer-probe Data
   - Package Manuf. Data: Placement of Dies, Passives, Micro-balls or Cu-Studs or DBIs.
   - Specifications for Interposer, Underfill, Pkg Substrate, Caps.
   - Assembly Diagrams.
   - Electrical, Mechanical, Thermal and other SiP Test Conditions

2. Assembly and Test Houses (OSATs)
   - Tools for IC and Package CO-Planning, Design and Verification

3. Chiplets & IC Designers
   - Modeling and Encrypting Tools
   - ADK: Assembly Design Kit:
     - Electrical, Thermal, Mechanical, Chemical, Thermo-Mechanical Characteristics of all Package Materials.
     - Off-the-Shelf Packages, Test Strategies, Die-level IP Blocks,…
   - PDK: Process Design Kit:
     - Core & I/O Libraries, Memory Compilers.
     - Spice Decks, Rules for DRC & ESD & EM,…

4. EDA Vendors
   - Spcie Decks, Rules for DRC & ESD & EM,…
   - PDK: Process Design Kit:
     - Core & I/O Libraries, Memory Compilers.
     - Spice Decks, Rules for DRC & ESD & EM,…
   - ADK: Assembly Design Kit:
     - Electrical, Thermal, Mechanical, Chemical, Thermo-Mechanical Characteristics of all Package Materials.
     - Off-the-Shelf Packages, Test Strategies, Die-level IP Blocks,…
3) Summary

• Automotive EcoSystem evolution

• No shortcuts, please

• Cooperation ! ! !
Automotive EcoSystem Evolution

~ 1900: Ford designed and manufactured every Model T component in house

~ 2000: Ford’s EcoSystem partners design and mass-produce most of the Ford Focus components!

The Semiconductor EcoSystem is likely to develop in a very similar way --- in the next few decades!

→ Leveraging SiP modularity, flexibility, cost, time to profit...

Ford designs and manufactures ONLY core components and assembles / markets / sells the final product.
NO Shortcuts, Please!

https://static.spiceworks.com/shared/post/0014/0498/74994_1270917636268671_3573180879514682641_n.jpg
Cooperation

Industry Trends:
- Mergers & Acquisitions
- Partnerships & Alliances
- Industry Organizations
- Design & Manuf. Standards
- Machine Learning
- Continuous Education
Thank You !
Leadership Lessons of Steve Jobs

✓ Focus
✓ Simplify
✓ Take responsibility end to end
✓ When behind, leapfrog
✓ Put products before profits
✓ Don’t be a slave to focus groups
✓ Bend reality
✓ Impute
✓ Push for perfection
✓ Tolerate only “A” players
✓ Engage face-to-face
✓ Know both the big picture and the details
✓ Combine the humanities with the sciences
✓ Stay hungry, stay foolish

http://hbr.org/2012/04/the-real-leadership-lessons-of-steve-jobs/ar/1