Progress and Prospects of Heterogeneous Integration at DARPA

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Arlington, VA

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Heterogeneous Integration: DARPA's initial view of opportunity space

High Performance III-V

Diverse
Accessible
Heterogeneous
Integration

Si CMOS

GaN HEMT

InP HBT

COSMOS

InP HEMT

ABCS HBT

GaAs MESFET

SiGe HBT

ABCS HEMT

Si MOSFET

Johnson Figure of Merit (GHz*Volt)

10^1 10^2 10^3 10^4

10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}

Number of transistors

Terminology:
InP = indium phosphide, GaN = gallium nitride, SiGe = silicon germanium, ABCS = antimonide-based compound semiconductor
HBT = heterojunction bipolar transistor, HEMT = high electron mobility transistor, CMOS = complementary metal oxide semiconductor
COSMOS = Compound Semiconductor Materials on Silicon

Motivates a portfolio of investment

			← device materials →					integration
Parameter	Why?	Unit	Si	GaAs	InP[1]	GaN[2]		COSMOS / DAHI
Electron Mobility	Carrier velocity	10^3 cm²/V·s	1.4	8.5	12	<1		InP
V_{peak}	Transit time	10^7 cm/s	1	2	2.5	2.5		InP / GaN
E_{BK}	Voltage swing	10^5 V/cm	5.7	6.4	4	40		GaN
E_g	Charge density	eV	1.12	1.42	0.74	3.4		GaN
κ	Heat removal	W/cm·K	1.3	0.5	0.05	2.9		GaN / Si
Maturity	Circuit complexity		Excellent	Good	OK	Limited		Si + GaN + InP (heterogeneous)
DARPA Investment			~$100M	~$600M	~$200M	~$300M		~$180M
Programs			Portions of GRATE, ADRT, LPE, and TEAM	MIMIC	SWIFT, TFAST, THz Electronics, SMART	GaN Title III, WBGS-RF, NEXT, MPC, NJTT		COSMOS, DAHI

Materials and device parameters favor a diversity of semiconductors

1. InGaAs channel
2. SiC substrate

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Progress of Heterogeneous Integration at DARPA

Transistor-scale Integration Technology | *Yield Enhancement & Circuit Integration* | *Advanced Circuits*

Differential amplifier ✓

- *~10 heterogeneous interconnects (HICs)*
- *≤ 5μm HIC length and pitch*
- *~5 HBTs, 4 CMOS*

D/A converter ✓

- *~500 HICs*
- *~400 HBTs, 3200 CMOS.*

A/D converter ✓

- *~1800 HICS.*
- *~1000HBTs, 18000 CMOS*

integration	Phase I	Phase II/III
monolithic	✓	X (yield)
epi printing	✓	X (yield)
chiplet	✓	✓

Y-axis: # of Heterogeneous Interconnects (10, 100, 1000)

X-axis: FY07, FY08, FY09, FY10, FY11, FY12, FY13

✓ COSMOS Phase I completed → ✓ COSMOS Phase II completed → ✓ COSMOS Phase III completed

COSMOS[1]:

1. **Developed technology for intimate integration of III-Vs and Si.**
2. **Demonstrated world-record capabilities with heterogeneous circuits:**
   a. **Differential amplifier gain-bandwidth**
   b. **DAC SFDR**
3. **Clarified benefits of integration processes that:**
   a. **are scalable,**
   b. **use finished devices, and**
   c. **leverage industry efforts.**

[1]Compound Semiconductor Materials on Silicon

COSMOS: Demonstrated benefits of integration of completed devices.

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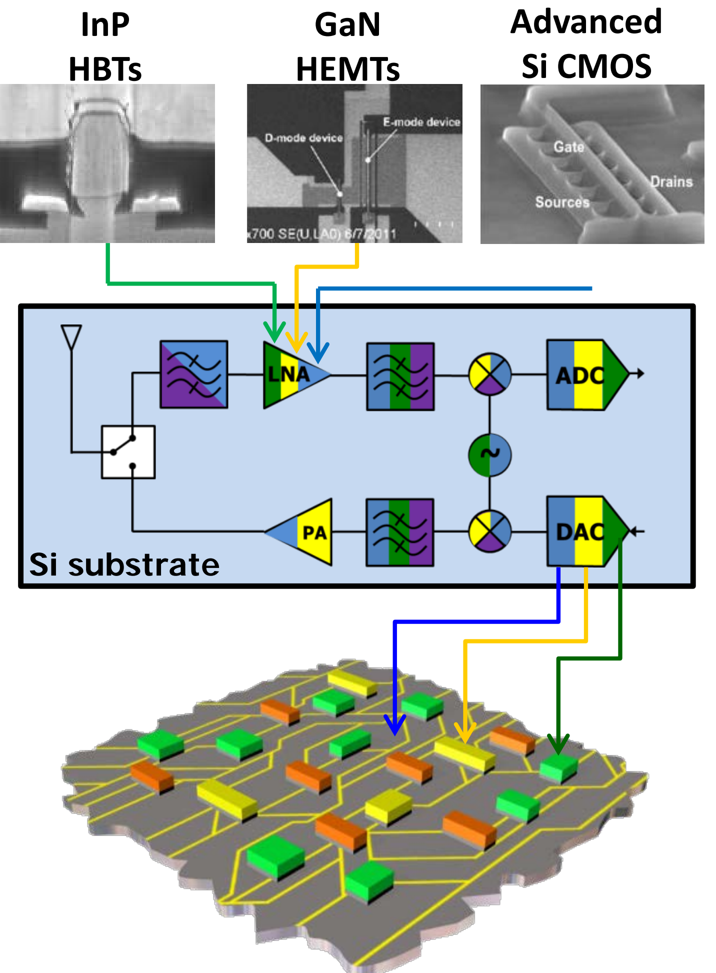
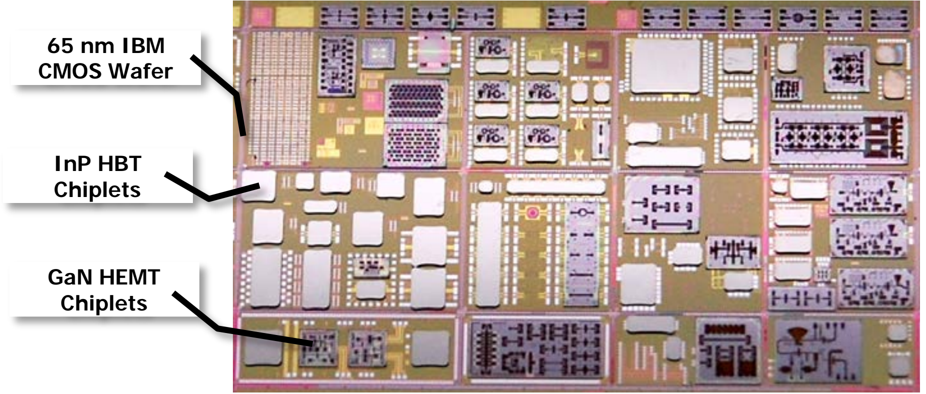
Diverse Accessible Heterogeneous Integration (DAHI) Foundry for Heterogeneous Integration



Heterogeneous Integration of a diverse array of devices on a common Si CMOS platform

Heterogeneous technology integration in accessible foundry



(first three-technology integration demonstrated in Jan 2015)

Goal: To establish a versatile platform of heterogeneous integration that enables pervasive impact on DoD systems.

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DAHI MPW0 CMOS + InP HBT + GaN HEMT Demonstration

65 nm IBM CMOS Wafer

InP HBT Chiplets

GaN HEMT Chiplets

Team 1

Yield TV

Team 4

Team 7

Team 1

Team 5

Team 8

Calibration

Team 2

Team 3

Team 6

Team 9

(3 technology integration demonstrated in Jan 2015)

Successful integration of high performance III-V technologies with CMOS.

DAHI MPW1: Excellent Yield, Successful Initial Tests

GLOBALFOUNDRIES

NORTHROP GRUMMAN

300mm diameter Si CMOS wafer (45nm node)

DAHI integration (Dec 2015): Si (45nm), InP (TF5 HBT), GaN (GaN20 HEMT)

NORTHROP GRUMMAN

99.94% HIC yield
98% HBT post-integration

High foundry integration yields; test vehicles fully functional

f_{OUT} 2.9 GHz

Output Spectrum

(noise floor ~ -75 dBm)

BAE SYSTEMS
INSPIRED WORK

DAC with very low digital noise (-70dBc)

TELEDYNE SCIENTIFIC & IMAGING
Everywhereyoulook

V0-1
V1-1
V3-1
V1-2
V2
V0-2
V3-2

Successful testing identified optimal S/H circuit for ADC (>65dB SFDR @ 2GHz)

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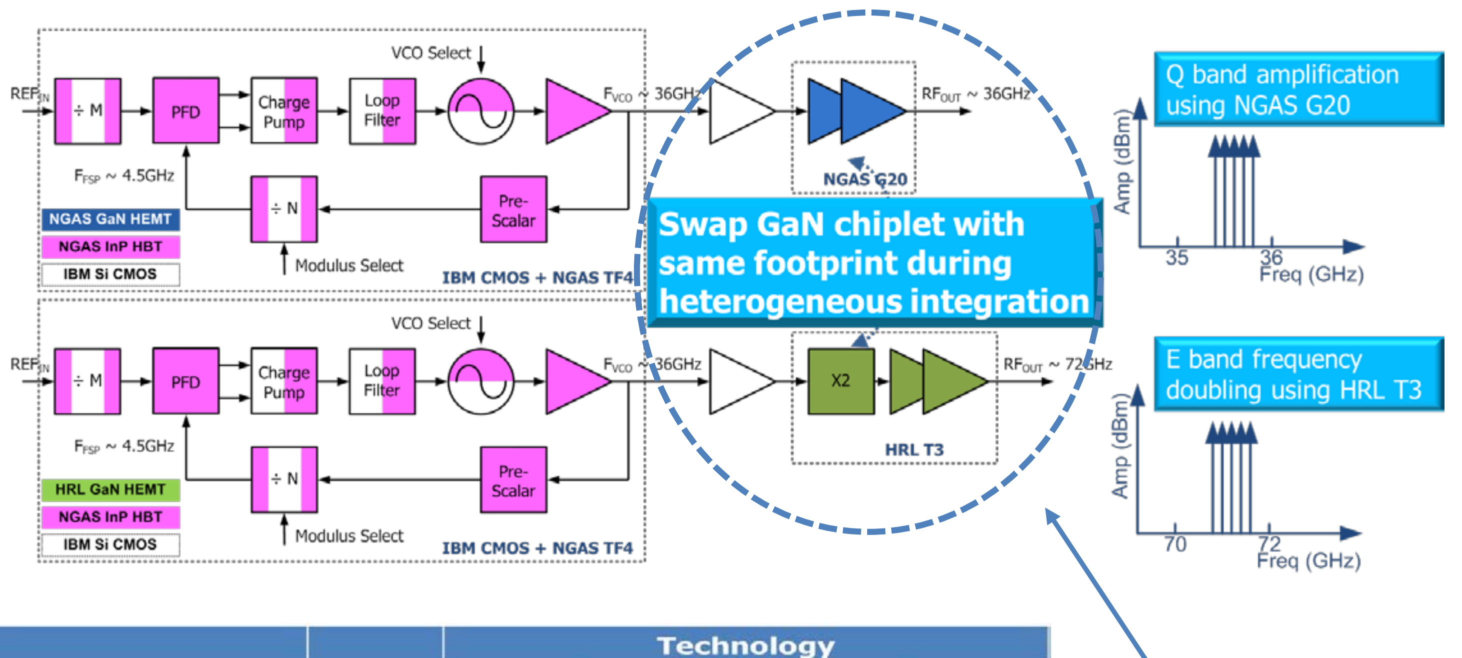
DAHI MPW1: Dual-Band Frequency Synthesizer Demonstrates Modularity

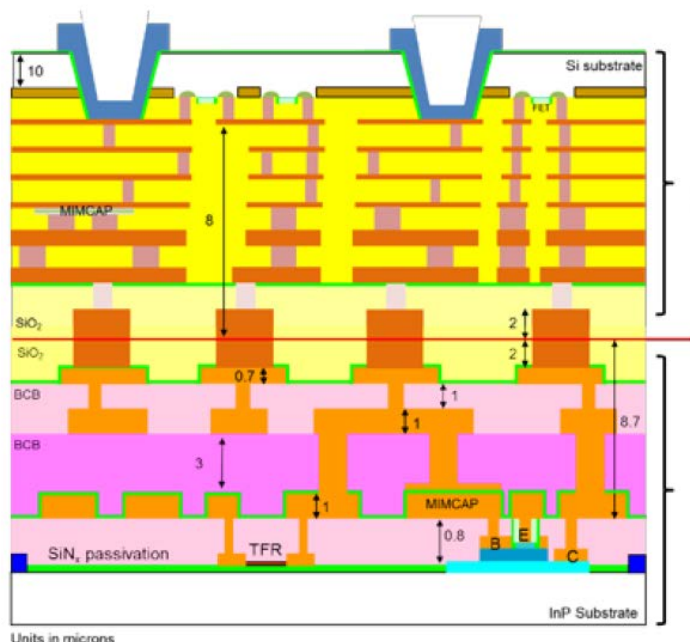
MPW1 Q/E Dual Band Frequency Synthesizer (36 and 72 GHz)



	Function	Freq (GHz)	CMOS 12SOI	InP TF4	GaN G20	GaN T3
			Technology			
A	Amplifier	36			✓	
	Frequency Doubler	72				✓
B	Buffer	36	✓			
C	Buffer + Amp	36	✓		✓	
	Buffer + FD	72				✓
D	VCO + Buffer + Amp	36	✓	✓	✓	
	VCO + Buffer + FD	72	✓	✓		✓
E	Frequency Synthesizer	36	✓	✓	✓	
	Frequency Synthesizer	72	✓	✓		✓

Integration of diverse device technologies enables modular functionality.

DAHI Alternate Flow: Wafer Bonding of InP and Si CMOS (Teledyne/Tezzaron)



130 nm Si CMOS wafer

Cu/SiO_2 wafer bond interface

250 nm InP HBT wafer

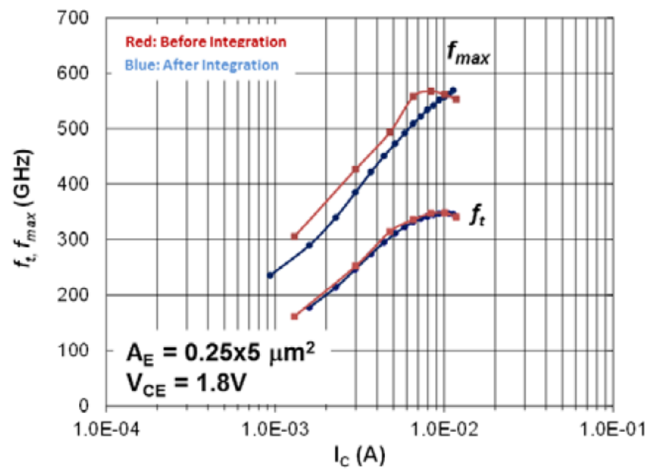
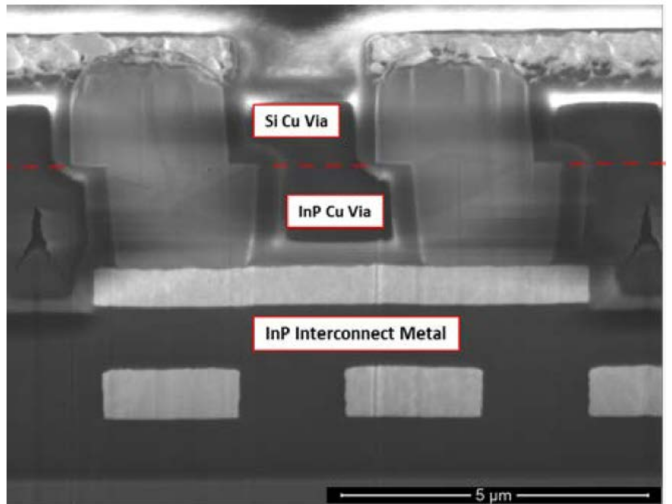
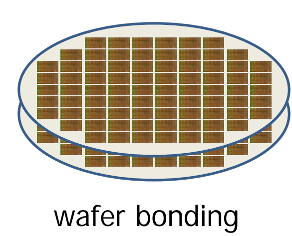


Fig. 5. Extrapolated f_t and f_{max} of 0.25x4μm^2 HBT before and after integration ($V_{CE} = 1.8V$)





wafer bonding

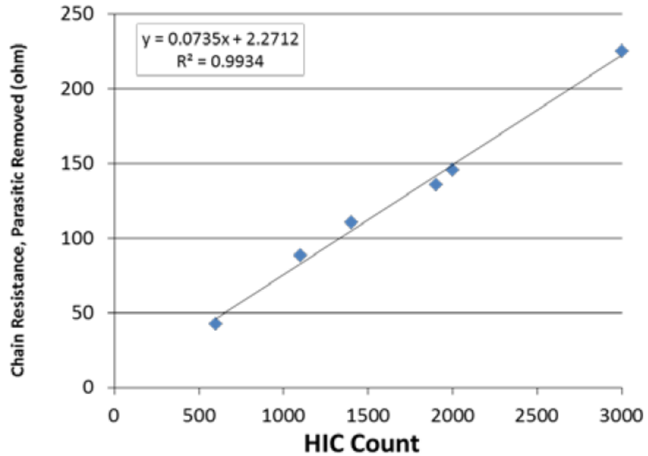


Fig. 6. Heterogeneous interconnection via chain resistance versus chain length.

Exploring Emerging Integration Technologies

GaN Transistor

Nb_2N

SiC Substrate

Carrier Substrate

Bonding Layer

1. Fabricate GaN devices on Nb_2N template on SiC substrate using standard processes.
2. Attach carrier substrate to GaN devices using bonding layer.
3. Etch Nb_2N layer with XeF_2 gas to separate GaN devices from SiC substrate.

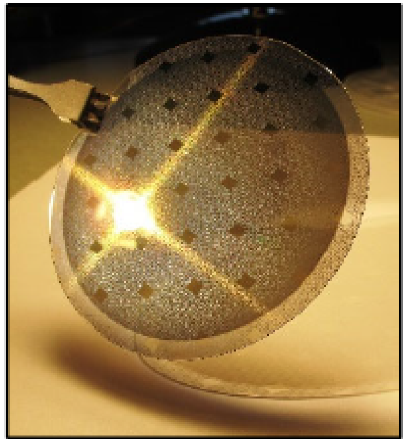
GaN Transistor

Alternative Substrate (copper, diamond, etc.)

Alternative Substrate (copper, diamond, etc.)

5. Remove carrier substrate and bonding layer from GaN devices.
4. Attach GaN devices to desired alternative substrate.

Figure 1. Epitaxial liftoff and transfer of GaN transistor from Nb_2N/SiC.



Source: Naval Research Laboratory, CS ManTech 2016

Heterogeneous Integration Platform Options

	Integration during device fabrication		Integration after device fabrication	
Integration Scheme:	**Monolithic Fabrication**	**Epitaxial Printing**	**Chiplet Assembly**	**Wafer Bonding**
COSMOS / DAHI performer	Raytheon	HRL	Northrop Grumman	Teledyne / Tezzaron
Structure				
Performance: Density	+ +	+ +	+	+ +
Performance: Speed	+ +	+ +	+	+ +
Performance: Thermal	-	-	-	-
Performance: Low cost	-	-	+	-
Performance: Maturity	-	-	+	-
Performance: Roadmap*	-	-	+ +	+

Yield Limited

*"Roadmap" metric indicates ease of integrating new technologies in the future.

DAHI integration (post-device fabrication) provides a platform combining density, performance, heterogeneity, and ease of integrating new technologies

End of Moore's Law?

Moore's Law

Relative Manufacturing Cost/Component

10^5, 10^4, 10^3, 10^2, 10, 1

1962
1965
1970

1, 10, 10^2, 10^3, 10^4, 10^5

Number of Components Per Integrated Circuit

The Economist

Faith no Moore

Selected predictions for the end of Moore's Law

Cited reason: Economic limits / Technical limits

Prediction issued — *Predicted end date*

1995 2000 2005 2010 2015 2020 2025 2030

Gordon Moore, Intel — *1995* — *2005*
G. Dan Hutcheson, VLSI Research — *1996* — *2003*
Isaac Chuang, IBM Research — *2000* — *2020*
Paolo Gargani, Intel — *2003* — *2021*
Lawrence Krauss, Case Western, and **Glenn Starkman**, CERN — *2004* — *approx. 2600*
Gordon Moore, Intel — *2005* — *2015–25*
Michio Kaku, City College of NY — *2011* — *2021–22*
Robert Colwell, DARPA; (fmr) Intel — *2013* — *2020–22*
Gordon Moore, Intel — *2015* — *2025*

Sources: Press reports; *The Economist*

Economist.com

End of Moore's Law means everyone is becoming low volume

Data source: Electronics Magazine, Economist.com

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Moore's Law INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Electronics, Volume 38, Number 8, April 19, 1965

G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

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More Than Moore? ⇨ More Of Moore

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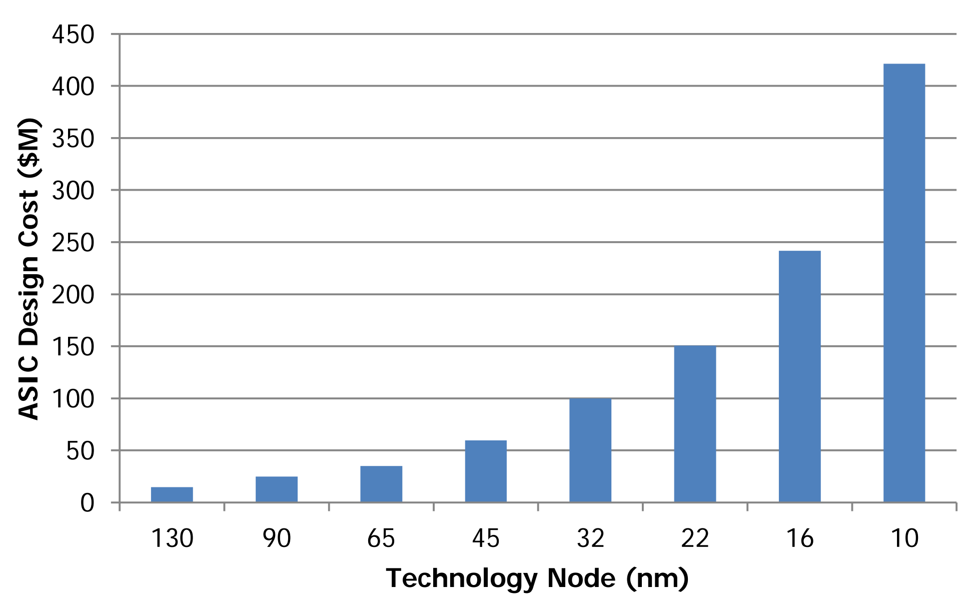
The Problem: Advanced Si is Expensive…

Expensive to design at advanced nodes …



… which some commercial products can support …

© apple.com

Fab cost for commercial electronics amortized over **one day's** worth of iPhones

… but DoD cannot.

Fab cost for a DoD IC amortized over **entire 29-year** acquisition of JSF

Source: "Cashing in with Chips" AlixPartners Semiconductor R&D outlook report, 2014.

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…and IP Reuse is Common for Multicore SoCs…

2016 average:
- 175 IP blocks
- 80% reuse

18 blocks

55 blocks

110 blocks

52 blocks

Average % of reused IP Blocks

Average # of IP Blocks

100% 90% 80% 70% 60% 50% 40% 30% 20% 10% 0%

250 200 150 100 50 0

1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014* 2015* 2016* 2017* 2018*

Percent of Reuse — Avg. Number of IP Blocks

SEMICO Research Corporation, 2014

IP Reuse is increasingly important and shows no signs of slowing

…but Challenging for the DoD

Limited access to global pool of knowledge **and** talent

Semiconductor fabrication market

Huahong Grace, 1%
Fujitsu Semiconductor, 1%
Vanguard Int'l, 2%
Others, 9%
TowerJazz, 2%
Powerchip, 2%
SMIC, 4%
Samsung, 5%
TSMC, 54%
Globalfoundries, 9%
UMC, 10%

Trusted 1%

Classic
Classic ARM
Embedded
Cortex Embedded
Application
Cortex Application
Next Gen
ARMv8

Features and Performance

iPhone 4S
iPhone 3GS
iPhone 6S
ARMv8-A
Cortex-A9
Cortex-A8
Cortex-A5
ARMv8-M
ARM11
Cortex-R4
ARM9
Cortex-M3
ARM7
Cortex-M0
TAPO
IoT
Images: Apple

Efficiency

1995 2005 2009 2012 2015

TAPO	TSMC
17 processes	>55 processes
>50 IP blocks	>8500 IP blocks

CHIPS is designed to expand the pool of IP and design resources

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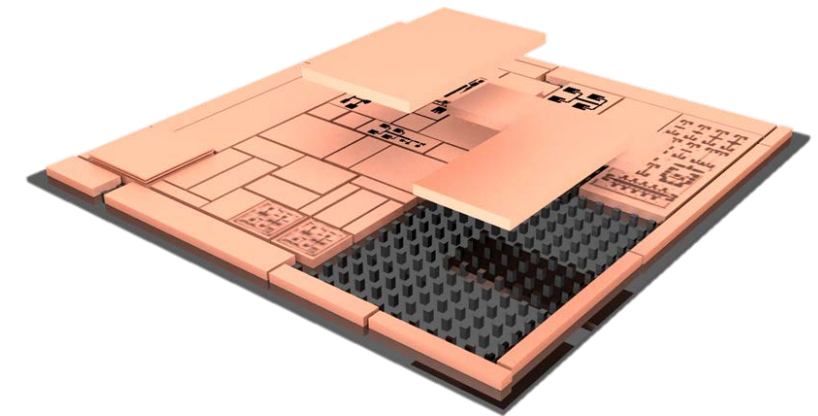
What is CHIPS?

Common Heterogeneous integration and IP reuse Strategies program

CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic

Tomorrow – Modular



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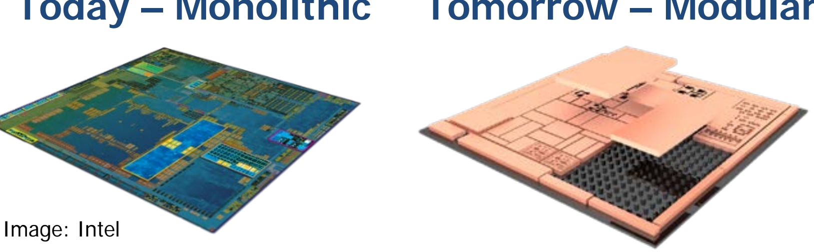

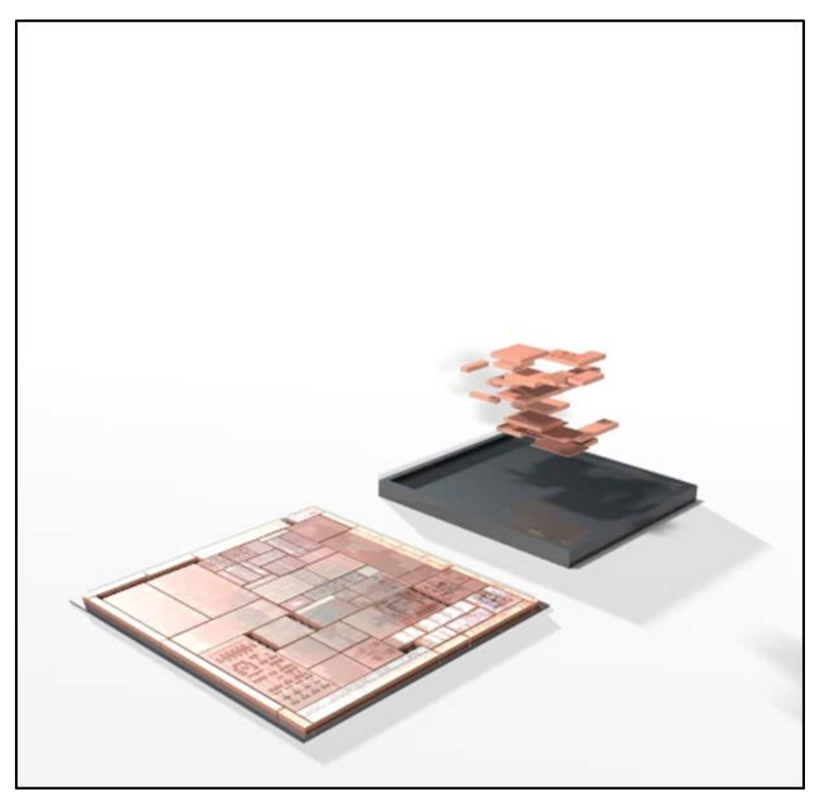

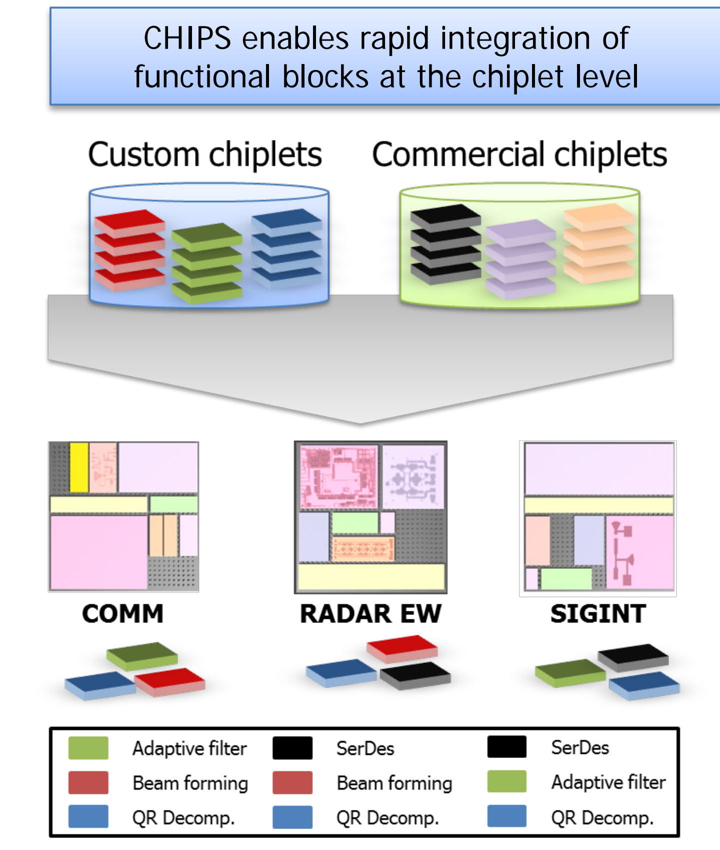

Interface Standards: Too Many? Not Enough? How to Compare?

$$\frac{Gbps/mm}{Energy/bit}$$

CHIPS challenge: make a usable interface standard

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Interface Standards: Too Many? Not Enough? How to Compare?

Convergence to a minimal set of standards is necessary

CHIPS

$$\frac{Gbps/mm}{Energy/bit}$$

BWD/EPB

WideIO

HBM

32nm_SerDes

Proprietary

28nm_SerDes

Si Photonic

65nm_SerDes

28nm_SerDes

LVDS

PCIe

1.00E-05 1.00E-04 1.00E-03 1.00E-02 1.00E-01 1.00E+00

Interconnect Length (m)

MonoLithic

PCB

CHIPS challenge: make a usable interface standard

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Implications: CHIPS end state vs. conventional supply chain

	IP Blocks	CAD tools	Architecture	Design	Verification	Fabrication	Pkg / Test	Systems
Commercial	ARM TSMC Cadence Imagination	Cadence Mentor Graphics Synopsys	Google Apple Microsoft Samsung	Qualcomm Broadcom Apple TI Marvell	Qualcomm Broadcom Apple TI Marvell	TSMC SMIC GlobalFoun. Intel Samsung	TSMC ASE Group Amkor	Google Apple Microsoft Samsung
DoD	ARM Global Foundries	Cadence Mentor Graphics Synopsys	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE	Northrop TowerJazz HRL Global Foundries	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE

CHIPS

- IP Blocks: ARM, TSMC, Cadence, Imagination / Raytheon, Northrop, Lockheed, Boeing, BAE
- CAD tools: Cadence, Mentor Graphics, Synopsys
- Architecture: Raytheon, Northrop, Lockheed, Boeing, BAE
- CHIPS → Pkg / Test: Northrop, Novati, US OSAT
- Systems: Raytheon, Northrop, Lockheed, Boeing, BAE

Design specs → Chiplets:

Commercial	Defense	Emerging	Distributor
TSMC Intel Global Foundries	Northrop Raytheon HRL	Jariet Intrinsix Flexlogix ?	Mouser Digi-Key ?

(Note: Companies listed are examples only.)

Trusted sources for critical components

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What CHIPS Means for the DOD and industry

Reusable function blocks
- QR decomposition
- Waveforms
- FFT

Access to Commercial IP
- Memory
- SerDes
- Processors

Big Data Movement
- Image processing
- Machine Learning
- High-speed chiplet networks

CHIPS modularity targets the enabling of a wide range of custom solutions

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Working with DARPA

Common Heterogeneous Integration and IP Reuse Strategies Broad Agency Announcement:

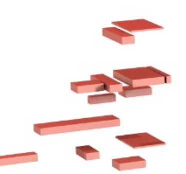
https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-BAA-16-62/listing.html

Commercial Performer Program Announcement, DARPA-PA-17-01

https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-PA-17-01/listing.html

- **What:** DARPA is looking to fund and de-risk non-incremental ideas that are beyond the standard corporate R&D roadmap.
- **Who:** Companies that have received less than $50M in defense contracts in the past year
- **How:**
  1. Start a conversation with a Program Manager
  2. E-mail your idea to MTOProgramAnnouncement@darpa.mil
- **When:** Rolling call, open all year

CHIPS future of heterogeneous integration



Requires a lot of pieces coming together!

www.darpa.mil

GIGAOM.com

Vision for Representative Transceiver: 4+ Device Technologies

Pre-select filter
High-Q MEMS

Low noise InP or GaN with Si-enabled control

LNA

Tunable filter
InP HBTs for high gain-bandwidth

High-speed InP T/H + Si-based interleaved ADCs

ADC

Local oscillator

PA

DAC

GaN for high $V_{br;}$
CMOS for digital assistance and reconfigurability

High-speed, high V_{br} InP HBTs;
Si CMOS for static and dynamic error correction

Legend:
- Si CMOS/SiGe BiCMOS
- InP HBTs/HEMTs
- GaN HEMTs
- RF MEMS/High-Q passives

DAHI Chiplet Assembly Evolving

CMOS	Standard CMOS fabrication ✓IBM 8WL (130nm) ✓IBM 10LPe (65nm) ✓IBM 8HP (130nm) **IBM 12SOI (45nm)**	→ HIC Interface deposition		→ CMOS wafer with HICs ready for integration
NGAS	Standard GaN20 fabrication →	Thinning / backside via etching →	Backside metal deposition →	Integration
HRL	Standard T-3 fabrication →	Thinning / backside via etching →	Backside metal deposition →	Integration
				CMOS wafer with integrated GaN chiplets
NGAS	Standard TF4/TF5 InP HBT fabrication →	Thinning →	Singulation and integration	
				CMOS wafer with integrated InP and GaN chiplets
Nuvotronics	High-Q Passives standard process →	Mechanical Integration		

- ✓ COSMOS: *130nm CMOS with InP HBTs*
- ✓ DAHI MPW0: *65nm CMOS, Add two GaN HEMT options*
- **DAHI MPW1: *45nm CMOS, Add high-Q passives and InP HBT variant – fab complete (right), testing underway***

45nm Si CMOS Wafer

GaN HEMT Chiplets

InP HBT Chiplets

(Second three-technology integration demonstrated in Dec 2015)

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CHIPS Program – Program Summary

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	Module Demo with IP Blocks	Rapid Module Upgrade
Integration platform Interface demo	Full system IP reuse demo	Reconfigured demo
TA1 Modular Digital Systems		
• Modularize existing digital design via interface standard. • Critical design review for standards at 8-month mark. • Demonstrate functional IP blocks.	• Demonstrate functional digital design. • Cost + design cycle analysis. • Present design for Phase3.	• Demonstrate rapid upgradability. • Cost + design cycle analysis comparing CHIPS module versus a monolithic implementation.
TA2 Modular Analog Systems		
• Modularize existing analog design via interface standard. • Review design and interface at the 8-month mark. • Demonstrate interconnect performance.	• Integrate blocks into PLIC. • Analyze against SoA for performance, unit cost, NRE, and turnaround time. • Develop business model for modular analog ecosystem.	• Demonstrate rapid assembly of new PLICs. • Analyze against SoA for performance, unit cost, NRE, and turnaround time. • Cost / development time analysis of CHIPS PLIC vs MMIC.
TA3 Supporting Technologies		
• Design Tools, Assembly Methods, IP in support of TA1 and/or TA2 tasks and metrics		

What do we plan to spend? and When?

- **Anticipated Funding Available for Award:** DARPA anticipates a funding level of approximately $70M for the CHIPS program.
- **Anticipated individual awards** – Multiple awards in each Technical Area are anticipated.
- **Anticipated funding type** - 6.2 and/or 6.3
- **Types of instruments that may be awarded** – Procurement contract, grant, cooperative agreement or other transaction.

Important Dates	
Proposers Day	21-Sep-2016
BAA Release (est.)	26-Sep-2016
Abstracts Due*	26-Oct-2016
FAQ Deadline*	23-Nov-2016
Proposals Due*	7-Dec-2016
Program Kick-Off*	Mar-2017

*Dates are a function of actual BAA release date.

www.darpa.mil

Conventional Assembly Has Attractive Features for HI … But Isn't Keeping Up on Pitch and Performance

10000
1000
IBM C4
100
10
1
0.1
0.01
0.001

microns

PCB

Flip Chip

Wire Bond

Global wiring (min)

Local wiring (M1)

Process node

1971 1973 1975 1977 1979 1981 1983 1985 1987 1989 1991 1993 1995 1997 1999 2001 2003 2005 2007 2009 2011 2013 2015 2017 2019 2021 2023 2025

Packaging

Image: EETimes

- Flexible heterogeneous integration
- Quick design / manufacturing turn
- Coarse pitch
- Lower performance

Silicon

- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance

Image: IBM

Need to combine speed and flexibility of packaging with
pitch and performance of advanced heterogeneous device technology.

Source: 2003-13 ITRS, Wikipedia

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Conventional Assembly Has Attractive Features for HI … But Isn't Keeping Up on Pitch and Performance

10000
1000
100
10
1
0.1
0.01
0.001

microns

IBM C4

PCB

Flip Chip

Wire Bond

Global wiring (min)

Local wiring (M1)

Process node

1971 1973 1975 1977 1979 1981 1983 1985 1987 1989 1991 1993 1995 1997 1999 2001 2003 2005 2007 2009 2011 2013 2015 2017 2019 2021 2023 2025

Packaging

Image: EETimes

- Flexible heterogeneous integration
- Quick design / manufacturing turn
- Coarse pitch
- Lower performance

How to get both?

- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance

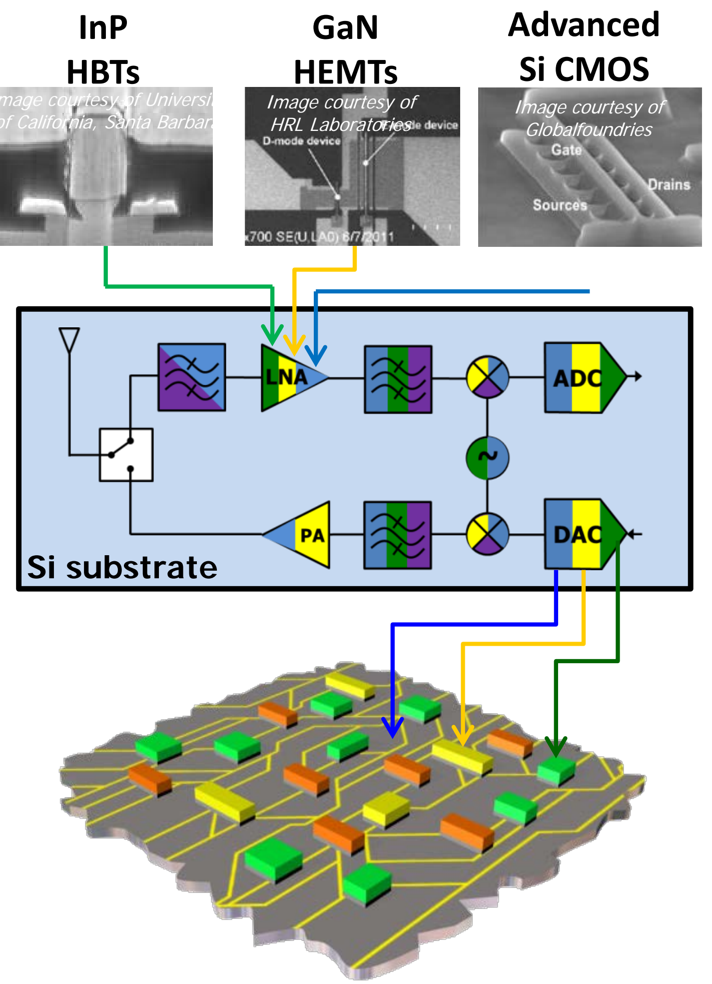
Silicon

Image: IBM

Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

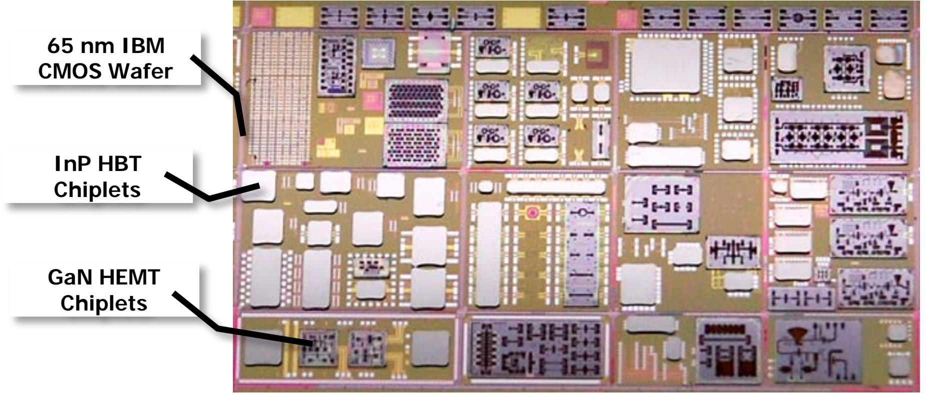
Source: 2003-13 ITRS, Wikipedia

Diverse Accessible Heterogeneous Integration (DAHI) Foundry for Heterogeneous Integration



Heterogeneous Integration of a diverse array of devices on a common Si CMOS platform

Heterogeneous technology integration in accessible foundry



(first three-technology integration demonstrated in Jan 2015)

Image: Northrop Grumman

Goal: To establish a versatile platform of heterogeneous integration that enables pervasive impact on DoD systems.

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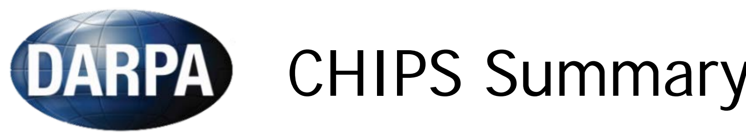
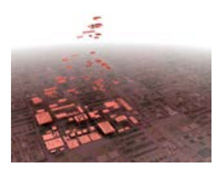
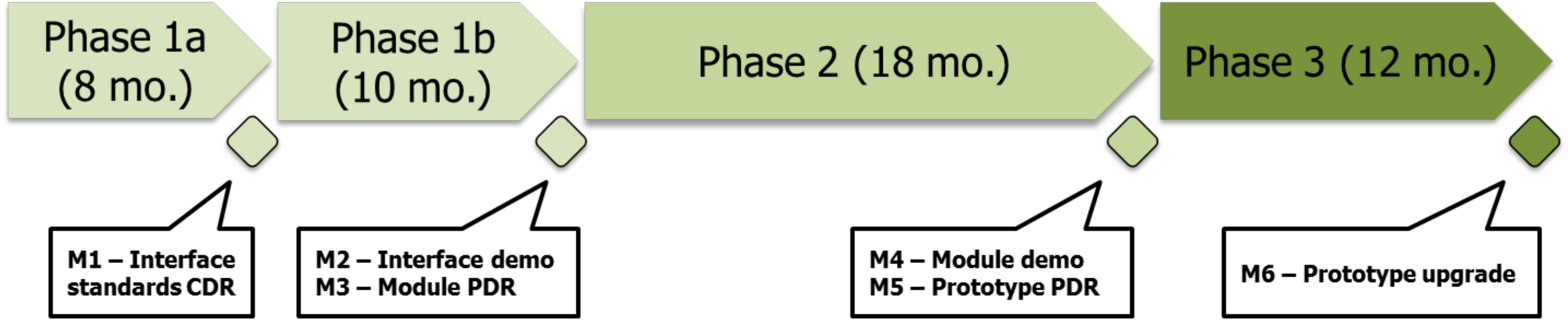


CHIPS Summary





Important Dates	
Proposers Day	21-Sep-2016
BAA Release (est.)	26-Sep-2016
Abstracts Due*	26-Oct-2016
FAQ Deadline*	23-Nov-2016
Proposals Due*	7-Dec-2016
Program Kick-Off*	Mar-2017

*Dates are a function of actual BAA release date.

TA1	Modular Digital Systems
TA2	Modular Analog Systems
TA3	Supporting Technologies

Questions: DARPA-BAA-16-62@darpa.mil

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CHIPS Program – Structure and Timing

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	Module Demo with IP Blocks	Rapid Module Upgrade
Integration platform → Interface demo	Full system IP reuse demo	Reconfigured demo

Phase 1a (8 mo.) → Phase 1b (10 mo.) → Phase 2 (18 mo.) → Phase 3 (12 mo.)

- M1 – Interface standards CDR
- M1 – Interface demo; M3 – Module PDR
- M4 – Module demo; M5 – Prototype PDR
- M6 – Prototype upgrade

TA1	Modular Digital Systems
TA3	Supporting Technologies
TA2	Modular Analog Systems

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CHIPS Program - Metrics

CHIPS Program Metrics			
Metric	Phase 1	Phase 2	Phase 3
Design level			
IP reuse (1)	> 50% public IP blocks	> 50% public IP blocks	> 50% public IP blocks
Modular design (2)	—		> 80% reused, > 50% prefabricated IP
Access to IP (3)	> 2 sources of IP	> 2 sources of IP	> 3 sources of IP
Heterogeneous integration (4)	> 2 technologies	> 2 technologies	> 3 technologies
NRE reduction (5)	—	> 50%	>70%
Turnaround time reduction (5)	—	> 50%	>70%
Performance Benchmarks (performer defined)	—	>95% benchmark	>100% benchmark
Digital Interfaces			
Data rate (scalable) (6)	10 Gbps	10 Gbps	10 Gbps
Energy efficiency (7)	< 1 pJ/bit	< 1 pJ/bit	< 1 pJ/bit
Latency (7)	≤ 5 nsec	≤ 5 nsec	≤ 5 nsec
Bandwidth density	> 1000 Gbps/mm	> 1000 Gbps/mm	> 1000 Gbps/mm
Analog interfaces			
Insertion loss (across full bandwidth)	< 1 dB	< 1 dB	< 1 dB
Bandwidth	≥ 50 GHz	≥ 50 GHz	≥ 50 GHz
Power Handling	≥ 20 dBm	≥ 20 dBm	≥ 20 dBm

Notes:

1. Public IP is defined as IP blocks available through commercial vendors or shared among performers.
2. Reuse is defined as existing or previously designed IP that is re-implemented into the current system. Prefabricated IP is defined as IP blocks already physically instantiated.
3. Valid sources of IP must be those that are outside of the performer team.
4. Various Silicon process nodes, RF passives, or compound semiconductor devices.
5. The non-recurring engineering (NRE) cost and turnaround time will be compared against a benchmark design.
6. Minimum bus/lane data rate and should be capable of scaling to higher data rates.
7. Performance relating to transferring data between chiplets compared against a benchmark design.

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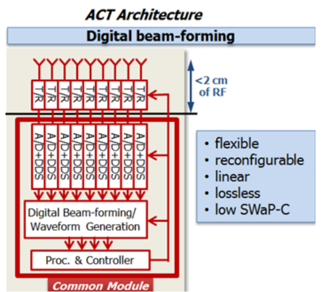
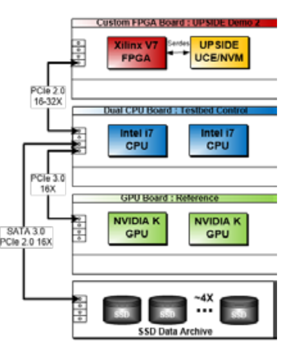
TA1: Modular Digital Systems

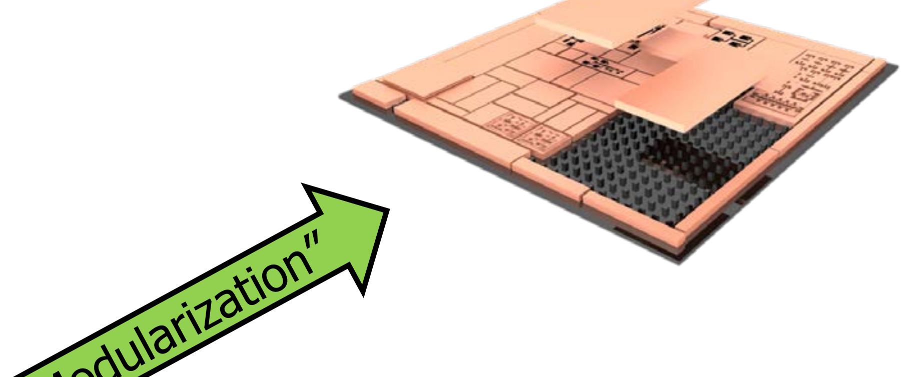


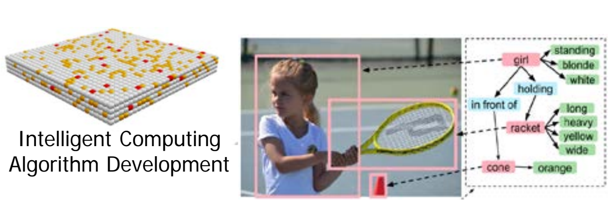
Arrays at Commercial Timescales (ACT)



Unconventional Processing of Signals for Intelligent Data Exploitation (UPSIDE)

"Modularization"





Cortical Processor

Semiconductor Technology Advanced Research Network (STARnet)

Targets modular circuits that leverage digital interfaces.

Looking for designs that:
- Leverage modular interface
- Reuse existing IP
- Are DoD relevant

Includes:
- Analog/Mixed signal circuits with digital interface
- non-DARPA designs

Others: CLASS, Mobile Hotspots, MFRF, ViSAR, ELASTx, …

Don't need to start from scratch!

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TA2: Modular Analog Systems

RF Unit Cell

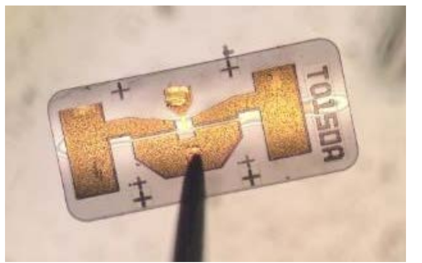
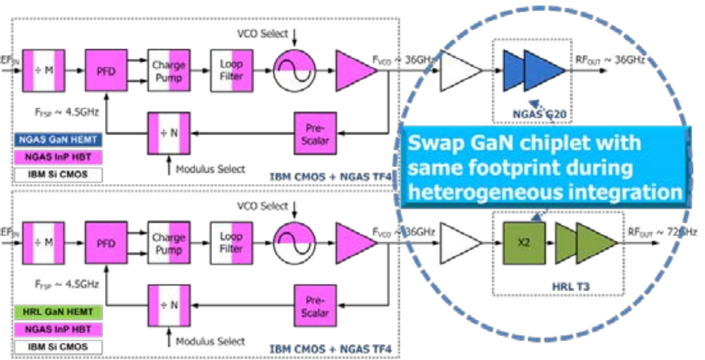
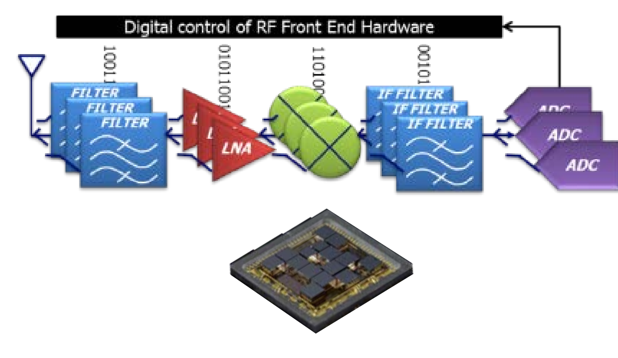


Image: NRL

Modular Devices



Modular Signal Blocks



Range of analog building block granularity

Seeks to realize modular pseudolithic microwave integrated circuits:

- Leverage modular building blocks
- Demonstrate performance into mm-Wave regime
- Develop sustainable attractive business models

Balance granularity with accessibility, reusability and cycle time

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TA3: CHIPS Supporting Technologies

- Design tools
  - Heterogeneous integration
  - Modular design flows
- Assembly methods
  - Fine pitch
  - Small device handling / testing
  - Multi-device technology processing
- IP blocks

Sample Digital IP

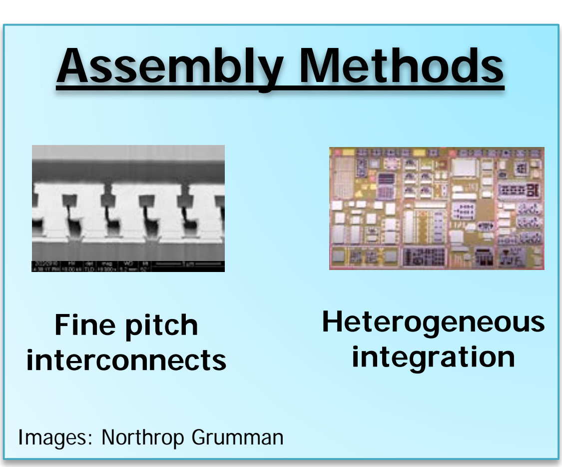
Processor	Interface	Memory
Image signal	SerDes	Controller
Audio signal	USB	DRAM
Digital signal	PCIe	SRAM
Compression		Flash
GPU		
CPU		
Machine Learning		

Design Tools

Design

Simulation

Layout



Sample Analog IP

Amplifiers	Passives
LNA	Filters
DAC / ADC	PMIC
Envelope Tracker	Transistor Unit Cell
Mixer	PLL

Key challenge will be alignment to TA1 and TA2

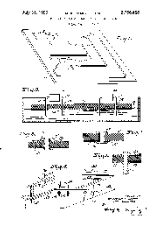
Non-CHIPS Developments

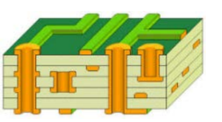
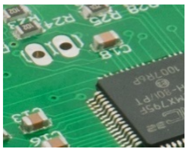
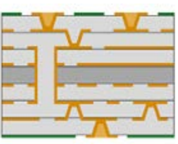
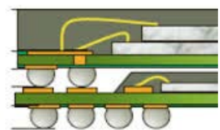
Technology NOT germane to CHIPS:

- New device technologies
- Wholly new circuits
- Security specific processes (e.g. obscuration, split fabrication)

Focus is on making modularity work!

Propelled by Standards and Modularity: Electronics Industry Built via Integration on PCBs



- 1936: "Printed circuit board" invented by Paul Eisler.
- 1941: Early PCB demo in a radio.
- 1943: First HVM PCBs enable proximity fuze during WWII.
- 1956: Patent to US Army for PCB assembly.
- 1957: IPC (Institute for Printed Circuits) founded; standards follow.
- 1960: Multi-layer PCB invented.
- 1980s: Surface Mount Technology on PCBs revolutionizes manufacturing.
- 1995: HDI / Microvia technology enables further integration.
- 2006: First package-on-package standard from JEDEC

DoD jump-start

PCB industry sees steady expansion with DoD origins, standardization, and technology development.

Global PCB Revenue ($M)

$70,000 · $60,000 · $50,000 · $40,000 · $30,000 · $20,000 · $10,000 · $-

1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016

Computers, smartphones, and tablet sales: 1975-2011

Unit sales (thousands)

500,000 · 450,000 · 400,000 · 350,000 · 300,000 · 250,000 · 200,000 · 150,000 · 100,000 · 50,000 · 0

1975 1980 1985 1990 1995 2000 2005 2010

Smartphones · Computers · Tablets

Sources: Prismark, Arstechnica, USPTO, Wikipedia, IPC, SMTA

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Heterogeneous Integration: Bridging the Gap

65 nm IBM CMOS Wafer

InP HBT Chiplets

GaN HEMT Chiplets

DAHI MPW0

DAHI MPW1

Technologies Integrated

4

3

2

1+ (>1 Si)

1

0.1µm 1µm 10µm 100µm

Interconnect Pitch

Package-based: Mature and flexible, but not scalable

Antenna feed line

Antenna GND

Antenna cavity

Patch

Low freq. line

RFIC GND

BGA

GND via

GND via

Advanced PCB

MEMS + ASIC

PoP memory

Stacked die (WB)

Processor + memory PoP

DRAM Layers

Logic Layer

Substrate

Monolithic 3D NAND

Processor + memory TSV

Tier 2

Tier 1

F2F wafer-bond

TSV / Wafer-scale: Immature or not well-suited for Heterogeneous Integration

NAND/DRAM TSV

Image sensor TSV

Interposer-based: Scalable and flexible

Die 1

Die 2

Die 3

Micro-bump

TSV

Silicon interposer

C4 bump

Package bump

Package substrate

2.5D Si interposer

DAHI creates integration capabilities beyond current advanced interconnect technologies.

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Looking Ahead: Enabling **Rapid** Heterogeneous Technology Uptake

InP HBTs

GaN HEMTs

Si CMOS

LNA

ADC

PA

DAC

Si substrate

Design Advances

- Modular design concepts
- Interconnect standards
- Advancing CMOS nodes
- Integration-enabled design techniques

Emerging Technologies

Polystrata High-Q passives

PCM switches

Graphene mixers

Revolutionary RF/mixed signal systems

Platform gives ability to rapidly add technologies as they are developed

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