MEPTEC Report

SPRING 2013

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 17, Number 1

Eleventh Annual

MEMS TECHNOLOGY SYMPOSIUM

MEMS-Enabled eHealth Revolution

MEMS and NEMS Based Applications for Emerging Healthcare Off-body, On-body, and In-body

page 19

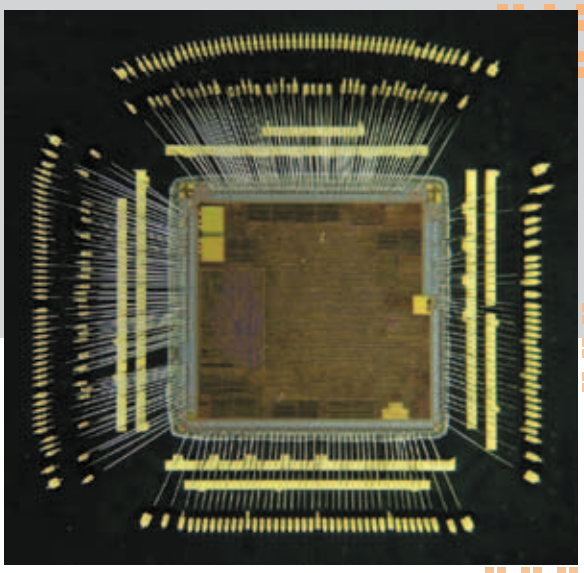
LSI Corporation's unique products help IT architects and managers deploy the architectures that store, share and accelerate data around the world.

page 20

INSIDE THIS ISSUE

ASE GROUP

Copper Wire



- Cu wire bond as good as gold
- Low cost opportunity
- Wire diameters as low as 0.7 mils
- Leader in high volume production
- Quality and yield equivalent to gold
- High reliability, typically 2x JEDEC

www.aseglobal.com

MEPTEC's Long Role of Cooperative Association

Phil Marcoux
PPM Associates
MEPTEC Advisory Board Member

THE PRIMARY ROLE OF ASSOCIATIONS, such as IPC, SEMI, GSA, IEEE, and MEPTEC is to serve the interests of its membership. The associations need to be as responsive as possible to those needs as they change or else the associations cease to be relevant. As the lines between associations and their self-defined interests in the industry blur, it's incumbent on these associations to welcome change.

From its very early roots as MEPPE, the association we now know as MEPTEC has had a history of helping influence industry growth through change and cooperation. The name change to MEPTEC years ago is a reflection of how the original group, one focused exclusively on packaging, altered its mission to embrace and associate with the needs of the test part of the electronics business. This was only the first of many cooperative gestures.

Today the electronics industry is investigating another set of new technologies in order to meet what many consider to be our guiding "laws". Within the IC side of the industry the guiding law most cited is Moore's Law (the number of transistors per square inch on integrated circuits will double every year). Surrounding the IC and extending to the final product, the "law" most cited is the rule of make it "smaller, faster, and cheaper". The only other "law" I've had quoted to me more is the law of KISS (Keep it Simple, Stupid), which I'm reminded of as I write this article!

Most recently MEPTEC has extended its association to include many of the other associations who are providing insight and guidance to their members to help with some of the newer technologies, such as 3D, TSVs, and nanotechnology. It has partnered with other groups, such as SMTA to produce symposiums on topics including Medical Electronics, MEMS, and Known Good Die. Our newest partnership is the Semi-Therm Conference.

For the 3D movement, MEPTEC has been a co-sponsor or a media sponsor of events with the IEEE/CPMT, IMAPS, GSA, and SEMI. MEPTEC is an advisor to the new 3D Business Council as well as the producer of its own Roadmap and other symposium series.

MEPTEC recently agreed to be a media and association sponsor of the newly announced IP Electronic System Technologies Conference and Expo or ESTC (www.estc.ipc.org). The IPC is one of the larger groups, with over 3000 member companies (1100 of who are OEMs) with a perceived focus on the printed circuit board fabrication, pcb assembly and solder interconnection segments.

The 3D and 2.5D technologies, with their dependence on interposers (aka pcbs) and solder interconnections can benefit greatly from the knowledge and infrastructure of the IPC.

The drivers for MEPTEC's leadership and flexibility have always been the broadly based Advisory Board. We have tried to have an AB that as closely as possible reflects the membership base. Each year the AB meets to map out MEPTECs direction and to review our mission and the wishes of the members.

We are about to hold our next planning meeting and I encourage your input and ongoing support of MEPTEC and our cooperative ventures. ◆

PHIL MARCOUX is a long term member of MEPTEC's Advisory Board and served as it's Executive Director from 2003 to 2006. He is the past CEO of AWI, ChipScale, and IQT. For the past ten years he's been a business and technical consultant to several companies in the areas of advanced packaging, sub-system architecture, and intellectual property commercialization. He is a named inventor and co-owner of over 40 packaging related patents. In 2007 the IPC named Phil as "The Father of SMT (in the US) during its 50th anniversary. He holds a BSEE from University of Florida and an MSEM (MSEE/MBA equivalent) from Santa Clara University where he also served as an Associate Professor in the Graduate School of Engineering.

UPCOMING MEPTEC EVENTS

WEDNESDAY, APRIL 10
MEPTEC Luncheon
Biltmore Hotel & Suites
Santa Clara, CA

WEDNESDAY, MAY 22
Eleventh Annual MEPTEC
MEMS Technology Symposium
Holiday Inn - San Jose Airport
San Jose, CA

WEDNESDAY, JUNE 12
MEPTEC Luncheon
Biltmore Hotel & Suites
Santa Clara, CA

WEDNESDAY, SEPT 11
MEPTEC Gartner Luncheon
Biltmore Hotel & Suites
Santa Clara, CA

WEDNESDAY, SEPT 17 & THURSDAY, SEPT 18
Eighth Annual MEPTEC
Medical Electronics Symposium
Arizona State University
Tempe Campus, Tempe, AZ

TUESDAY, SEPT 24
MEPTEC Roadmaps Symposium
Biltmore Hotel & Suites
Santa Clara, CA

WEDNESDAY, OCT 9
MEPTEC Luncheon
Biltmore Hotel & Suites
Santa Clara, CA

WEDNESDAY, DEC 18
MEPTEC Holiday Luncheon
Biltmore Hotel & Suites
Santa Clara, CA

MEPTEC Report

SPRING 2013

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council — Volume 17, Number 1

ON THE COVER

19 MEPTEC presents its Eleventh Annual MEMS Technology Symposium titled "MEMS-Enabled eHealth Revolution: MEMS and NEMS Based Applications for Emerging Healthcare Off-body, On-body and In-body" on Wednesday, May 22, 2013 at the Holiday Inn - San Jose Airport in San Jose, California. Invited speakers will focus on sensors, actuators, and architectures that enable the eHealth revolution.

16 ANALYSIS – Consolidation must clearly occur in order to maximize efficiencies of scale in the SATS market. Additional mergers and acquisitions will also likely occur as the leading SATS providers strengthen their position at the expense of smaller competitors.

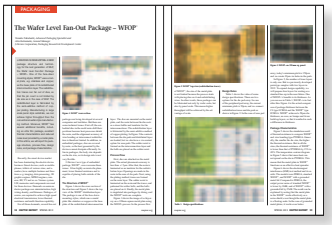
BY JIM WALKER
GARTNER

20 PROFILE – LSI answers the call for faster information access with semiconductors and software that accelerate data across enterprise and mobile networks, datacenters and client devices including solid-state and hard disk drives. At the heart of the LSI high-speed designs is intelligent silicon.

LSI CORPORATION
MEMBER COMPANY PROFILE

25 TECHNOLOGY – 3D has moved into the mainstream, but, as still a relatively new technology, it is not surprising that there are technical and non-technical barriers that exist. Potential solutions can be many, but Xilinx is already delivering and extending the value and usage of 3D ICs.

BY KIRK SABIN
XILINX INC.



28 PACKAGING – J-Devices introduces WFOP™, a new embedded wafer level package structure and fabrication technology. This structure is a promising solution for a thinner package with more traces, lower thermal resistance and better electrical characteristics.

BY TOMOKO TAKAHASHI AND AKIO KATSUMATA
J-DEVICES CORPORATION

DEPARTMENTS

MEPTEC

THE NEXT GENERATION

The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

P. O. Box 222, Medicine Park, OK 73557
Tel: (650) 714-1570 Email: info@meptec.org

Publisher MEPCOM LLC
Editor Bette Cooper
Art Director/Designer Gary Brown
Sales Manager Gina Edwards

Contributors

Joel J. Camarda
Amonix Inc.

Richard Chen
Dow Electronic Materials

Ira Feldman
Feldman Engineering Corp.

Shashi Gupta
Henkel Electronic Materials, LLC

Ron Jones
N-Able Group International

Akio Katsumata
J-Devices Corporation

Phil Marcoux
PPM Associates

Kirk Sabin
Xilinx Inc.

Tomoko Takahashi
J-Devices Corporation

Jim Walker
Gartner

Howard Yun
Henkel Electronic Materials, LLC

Cactus CSI021; Programmable Current Sink/Source

New ASSP to Reduce Risk and Development Time for Medical Device Makers

CACTUS SEMICONDUCTOR, INC. IS pleased to announce the introduction of their first ASSP (Application Specific Standard Product); developed for medical device designers and manufacturers to reduce risk and development time for implantable neurostimulation, neuromodulation and other Implantable Pulse Generator (IPG) applications. The CSI021 will be most beneficial to medical device manufacturers involved in peripheral nerve stimulation by providing a building block suitable for proof-of-concept, trials and even production; depending on the specific application.

Cactus Semiconductor's CSI021 offers 4 stimulation channels with unlimited expansion capability; high voltage and high current outputs with integrated charge balancing. The device has an SPI Interface for programming, low overhead power and ultra-low standby power performance; all in an industry-leading 4mm x 4mm QFN package.

"Neurostimulation is a growing segment of the medical device market" says James McDonald, president of Cactus Semiconductor. "We felt this market segment was not being effectively served by other standard products on the market. The products available today do not adequately address the unique low power and performance requirements for this application space. The CSI021 will reduce risk and time to market challenges, especially for the many small and mid-size medical device companies who are developing new devices and therapies. Our decades of combined experience in designing and producing mixed-signal ICs for the medical market positions Cactus Semiconductor perfectly to help these customers build success and improve people's lives."

The CSI021 will be available for engineering evaluation in June of 2013.

For more information contact Scott Montgomery, 480.497.4511, sales@cactussemi.com or visit www.cactussemiconductor.com. ◆

Nitto Denko to Open New Manufacturing Plant in Brazil

AS PART OF ITS ONGOING international expansion plans, Japan's leading diversified materials manufacturer, Nitto Denko Corporation, has announced that it has decided to invest 1400 million Yen (approximately US$17.9 million) in the construction of a new manufacturing plant in Sao Paulo Brazil. With its large population and rapidly developing economy Brazil represents an important market for Nitto Denko in the future.

The Sao Paulo metropolitan area is the second most populous in the Americas and the city itself is Brazil's largest, with an estimated 20 million people. It is Brazil's industrial and financial center and has experienced rapid growth and development over the last decade. This along with encouraging growth in the automotive parts business has lead Nitto Denko to consider it a suitable place for production and development.

Nitto Denko has recently established or expanded operations in India, China, Turkey and is determined to continue to be proactive in establishing a presence in new markets to better serve the needs of local customers. The company's move into Brazil is part of its long term Area Niche Top Strategy, in which top market share is sought in particular niche markets where Nitto Denko can most effectively leverage its unique technologies and regional resources.

Nitto Denko America Latina (LTDA) will be the first plant built by Nitto Denko in South America.

Construction of the new plant will start in February 2013 and is expected to be completed in December 2013. Initially the plant will manufacture products for the auto related sector such as NVH (Noise, Vibration and Harshness) products.

For more information about Nitto Denko visit their website at www.nito.com. ◆

AMKOR NAMES ROBERT MORSE TO BOARD

Amkor Technology has announced that Robert Morse has been appointed as a new member of the Company's Board of Directors. With this appointment, Amkor's Board has been expanded to eight members.

Mr. Morse is currently serving as Chairman of Bridge Investment Group Partners and its affiliates, a real estate fund manager, and as Chairman and CEO of PMC Partners, a private equity firm. Prior to that, Mr. Morse served in various positions with Citi and Salomon Smith Barney since the 1980s, including CEO of Citi's Asia Institutional Client Group and Global Head of Investment Banking. Mr. Morse is a graduate of Yale University, the Harvard Graduate School of Business and the Harvard Law School.

www.amkor.com

DOW ESTABLISHES INNOVATION CENTER AT UNIVERSITY OF ILLINOIS

Dow Chemical Co. has established an information technology development center at the University of Illinois Research Park in Urbana-Champaign, Ill., where 16 accomplished students in computer science and related fields will work part-time to help develop data management solutions to drive value and accelerate discovery in the Research and Development (R&D) organizations throughout Dow. The Innovation center will start its operations in the spring

2013 semester.

In conjunction with the opening of the new office, Dow has entered into an industry partnership with the National Center for Supercomputing Applications (NCSA), also located at the University of Illinois at Urbana-Champaign. As part of the partnership agreement, NCSA will provide powerful computers and expert support to help Dow's scientists and student researchers accelerate discovery.

Dow and the University of Illinois at Urbana-Champaign have been in close collaboration since 2011 when the university became one of 11 leading academic institutions to enter into a Strategic University Partnership with Dow. Through the partnerships, Dow is committing $250 million over 10 years to expand research capabilities with the top chemistry, materials science and chemical engineering departments in the country.
www.dow.com/Innovation

MICROSS COMPONENTS ACQUIRES DITRONIX, INC.

Micross Components is pleased to announce the acquisition of Ditronix, Inc., a semiconductor die and passive components distributor based in Woburn, Massachusetts. Ditronix is valued by its customers for personalized customer service, broad inventory, and quick turn capability. Ditronix will operate as a separate division of Micross Components, maintaining all of the traditional service to which its customers are

Dow Unveils First CMP Polishing Pads from its IKONIC™ Platform

Brings New, Advanced Materials to the Semiconductor Market

FOLLOWING THE INTRODUCTION of its IKONIC™ chemical mechanical planarization (CMP) polishing pad platform in late 2012, Dow Electronic Materials has launched the first pads from its new IKONIC™ 2000 and IKONIC™ 3000 polishing pad series. All pads in the IKONIC CMP polishing pad platform are designed for use at the 28nm manufacturing node and below, with IKONIC 2000 polishing pads targeting copper barrier, HKMG and buffing applications, and IKONIC 3000 polishing pads developed initially for use in bulk copper polishing.

The first of the new pads, IKONIC 2020H, achieves defectivity levels significantly lower than traditional pads while maintaining removal rate. Additionally, every pad in the IKONIC 2000 series is formulated to be easily conditioned for optimal texture and longer pad life time. This improves polishing consistency and lowers overall cost of ownership.

IKONIC 3040M is the first polishing pad in the IKONIC 3000 series. This pad delivers a significant reduction in scratch defects compared to other bulk copper pads. Additionally, IKONIC 3040M demonstrates improved topography performance and lower cost of ownership. This pad is available in a range of configurations and options for multiple applications.

Samples are currently available and in beta testing with multiple customers.

Dow Electronic Materials brings innovative leadership to the semiconductor, interconnect, finishing, photovoltaic, display, LED and optics markets.

More information about Dow Electronic Materials can be found at www.dowelectronicmaterials.com. ◆

InvenSense® Sets a New Industry Standard with the World's Smallest, Lowest Power Integrated 9-Axis MotionTracking Device

INVENSENSE, INC., THE LEADING provider of MotionTracking™ devices, introduces a second generation, category defining, 9-axis MotionTracking device. The MPU-9250, in a 3x3x1mm QFN package, is 33% smaller than the nearest competitor. With only 9.2mW, it is the lowest power 9-axis motion sensing device on the market, and offers the best available gyroscope noise and compass full scale range. This fully-integrated 9-axis device includes a gyroscope, accelerometer and electronic compass, with an onboard Digital Motion Processor™, and comes factory tested and calibrated. The MPU-9250 is ideal for mobile devices, wearable sensors, fitness watches and remote health monitoring applications that require small form factor, low-power consumption and performance accuracy.

"InvenSense is an industry leader with best-in-class, world's first MotionTracking solutions," said Behrooz Abdi, President and CEO of InvenSense. "With the MPU-9250, we are moving the industry forward by delivering breakthroughs in 9-axis package size, power and performance. Moreover, InvenSense is continuing to raise the bar for Motion Interface innovations."

Ali Foughi, Vice President of Marketing and Business Development at InvenSense noted, "InvenSense is enabling rapid adoption of leading MotionTracking solutions for mainstream consumer applications as well as emerging markets. Our MPU-9250 is the smallest and most cost-effective 9-axis device serving the highly-elastic combo sensor market, which is estimated by Yole Developpment to grow to $1.5 billion USD by 2017. Customers are showing increasing interest in our 9-axis solutions which are targeted for smartphones, tablets, wearable sensors for sport and activity monitoring, remote health monitoring and a whole host of new and exciting applications."

The MPU-9250 has other compelling advantages beyond size, power and noise performance breakthroughs. The accelerometer consumes as little as 6.4μA of current in low-power mode. The compass has a resolution of 16-bits, and full scale measurement range of ±4800μT. The MPU-9250 is supported by the production-proven MotionApps™ software platform from InvenSense. The MPU-9250 software drivers are fully compliant with Google's latest Android 4.2.1 Jelly Bean, Microsoft Windows 8 and Windows RT releases, and support new low-power DMP capabilities that offload the host processor to reduce power consumption and simplify application development. For additional information visit www.invensense.com or contact InvenSense Sales at sales@invensense.com. ◆

February 2013 Book-to-Bill Ratio of 1.10

North America-based manufacturers of semiconductor equipment posted $1.07 billion in orders worldwide in February 2013 (three-month average basis) and a book-to-bill ratio of 1.10, according to the February Book-to-Bill Report published today by SEMI. A book-to-bill of 1.10 means that $110 worth of orders were received for every $100 of product billed for the month. The three-month average of worldwide bookings in February 2013 was $1.07 billion. The three-month average of worldwide billings in February 2013 was $975.3 million. The billings figure is 0.8 percent higher than the final January 2013 level of $968.0 million, and is 26.3 percent lower than the February 2012 billings level of $1.32 billion. Visit www.semi.org. ◆

accustomed and now augmented by the full force of the Micross Components portfolio of suppliers and technical expertise.

Bob Sarkisian, Ditronix founder and owner, will continue to run the operation with the same staff, supported now by the full breadth of resources as Micross Components Die Products Division.
www.micross.com

TESSERA AND STATS CHIPPAC ENTER INTO FIVE-YEAR PATENT LICENSING AGREEMENT

Tessera Technologies, Inc. has announced that its Tessera, Inc. subsidiary entered into a new five-year patent license agreement with STATS ChipPAC Ltd.

"We are delighted that STATS ChipPAC joined us in moving beyond litigation," said Bernard "Barney" Cassidy, president, Tessera Intellectual Property Corp. "STATS ChipPAC is a leading semiconductor assembly and test company and they now have freedom of operation under more than 800 Tessera, Inc. patents and patent applications."

The companies did not disclose the specific financial terms of the agreements. Tessera, Inc. and STATS ChipPAC also agreed to dismiss claims and counterclaims between the two parties relating to Tessera, Inc.'s patent infringement claims pending in the United States District Court, Northern District of California. The Company is not providing

additional financial guidance in connection with this license.
www.tessera.com

RAMBUS AND FUJITSU SIGN PATENT LICENSE AGREEMENT

Rambus Inc., one of the world's premier technology licensing companies, has signed a patent license agreement with Fujitsu Semiconductor Limited. The six-year agreement covers the use of Rambus patented innovations implemented in a broad range of integrated circuit (IC) products offered by Fujitsu Semiconductor.

Rambus is one of the world's premier technology licensing companies. As a company of inventors, Rambus focuses on the development of technologies that enrich the end-user experience of electronic systems. Rambus licenses both its world-class patent portfolio, as well as its family of leadership and industry-standard solutions.
www.rambus.com

MICROSS LOOKS TO THE FUTURE

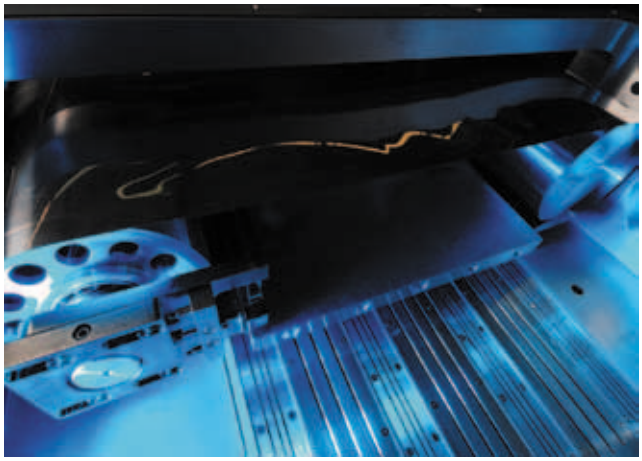
Micross Components is pleased to announce that in accordance with the company's long term strategic plan, Insight Equity recently acquired the company from Vance Street Capital, which holds companies with revenues up to $200M. Micross grew to maturity in the Vance Street portfolio in the timeframe envisioned by the companies when they began their partnership.

In 2010, Micross

Aventa Technologies Receives Strategic Investment from Applied Ventures to Support High Temperature Superconductor Technology

AVENTA TECHNOLOGIES, Inc., a provider of manufacturing equipment for emerging alternative energy markets such as high-temperature superconductors (HTS), has announced that Applied Ventures, LLC, the venture capital arm of Applied Materials, Inc., has made a strategic investment in its series A financing. The investment will be used to support its operation to commercialize the equipment the HTS industry needs to meet growing global demand.

HTS technology promises to significantly improve power distribution by enabling the lossless transmission of electrical power over long distances. Several applications of HTS wires are expected to move from demonstration to large-scale projects in the near future. As old grid infrastructures get upgraded with more advanced technologies to increase efficiency, substantial adoption of superconducting fault current limiters and HTS cables is expected. For example, China plans to spend $530B in this decade to build a strong and smart grid, according to the China Greentech Initiative. Aventa Technologies offers a comprehensive set of systems for manufacturing advanced HTS wires. The company's advanced vacuum deposition tools can accelerate the adoption of HTS solutions by increasing the productivity of HTS wire manufacturing.



Aventa Technologies system for manufacturing HTS wires.

Aventa Technologies is a manufacturer of thin film deposition equipment for alternative energy markets, specializing in highly customized advanced vacuum deposition tools. For more information, visit www.aventatech.com.

Applied Ventures, LLC, a subsidiary of Applied Materials, Inc., invests in early stage technology companies with high growth potential that provide a window on technologies that advance or complement Applied Materials' core expertise. Learn more at www.appliedventures.com. ◆

InvenSense® Announces Contextual Awareness SDK for Embedded Developers and Mobile Devices

Poised to drive new era of health and fitness monitoring products

INVENSENSE, INC. HAS LAUNCHED A Contextual Awareness System Development Kit (CA-SDK) to further drive the proliferation of wearable sensor innovations. The CA-SDK is comprised of nine sensors and software on a 1.71in. x 1.46in. PCB configured into a wearable watchband. By leveraging the CA-SDK, developers can create advanced applications and end products with orientation tracking and activity recognition capabilities such as running, swimming, biking, playing tennis, walking up or down hill, and determining calorie burn rate. The CA-SDK can also be used for the development of sleep monitoring, posture detection, and applications that detect if the wearer is indoors, outdoors, or driving a car.

The CA-SDK features InvenSense's MPU-9250, 9-axis MotionTracking device that was also announced recently. The CA-SDK leverages InvenSense' algorithms for MotionFusion™, and incorporates temperature, humidity, ultraviolet light, proximity, pressure, and light sensors. The CA-SDK comes with an embedded motion processing library for hardware developers, a USB port, on-board memory, and a Bluetooth module that supports Bluetooth low energy for interfacing with Android and iOS smartphones, tablets, and PCs.

More information can be found at www.invensense.com. ◆

Micross Components Debuts New Website

MICROSS COMPONENTS, a global provider of specialty electronic components, has unveiled their newly redesigned website and logo. Both speak to the company's overall efforts to provide a comprehensive destination for electronic system engineers and purchasers to acquire information, products, and services for all their specialty electronic needs. The new Micross.com streamlines navigation and coordinates the many capabilities that now comprise the Micross Components portfolio of first-rate suppliers and extensive resources to serve the marketplace.

The Micross logo has received a tagline and color treatment to convey the company's commitment to strength as a trusted partner and their active progress in extending their product-service selection in anticipation of market desires.

"The new Micross.com brings valuable information to our customers through a richer and more intuitive browsing experience," said Alan Taylor, CEO. "This complements our growing portfolio and reflects our role as the definitive source for specialty electronic components."

During the last few years, Micross has expanded its offerings and increased its value and relevance to the customer. By bringing together more products and capabilities, Micross has helped its critical-application customer base achieve success in their own product developments. Micross now offers more sales channels throughout the world as well as effective solutions to several additional industries.

For more information, visit www.micross.com. ◆

Intersil's New 24-bit ADCs Feature Industry's Highest Measurement Accuracy

INTERSIL CORPORATION has introduced new integrated, ultra low noise 24-bit ADCs with programmable gain amplifiers that provide optimal measurement accuracy over a wide range of conversion rates with a minimum of external components.

The ISL26102 and ISL26104 are 24-bit ADCs that offer an on-chip ultra-low noise programmable gain amplifier. The ADCs' wide PGA gain range facilitates direct connection to load cells, thermocouples and other popular sensors with a wide variety of sensitivities. The devices feature best-in-class noise performance through their entire output word rate range from 2.5 to 4,000SPS, delivering system flexibility unmatched by competitive devices. The ISL26102 and ISL26104 provide two-channel and four-channel input multiplexers, respectively, and are designed for instrumentation such as weighing systems and temperature monitoring and control. They provide designers of these precision instruments the ability to digitize, with unmatched accuracy, small signals from low cost sensors, without the added cost and complexity of external amplifiers and signal conditioning circuits.

Both the ISL26102 and ISL26104 complement Intersil's industry-leading portfolio of low-noise, precision signal path products. At the Renesas DevCon 2012, Intersil demonstrated a precision temperature and strain gauge AFE paired with a RL78/G13 Renesas microcontroller. In addition to the ISL26102, this reference design combined the ISL28617 40V Instrumentation Amplifier, ISL21090, low noise precision voltage reference, ISL28134, 5V Low Noise Zero-Drift Op Amp, and ISL22317 DCP to create turnkey solutions for both temperature and strain applications.

For more information visit www.intersil.com/products/ISL26102 and www.intersil.com/products/ISL26104. ◆

promised its customers, suppliers, employees and investors, to expand its offerings, to bring new products and services, and to improve service to all stakeholders. In the past two years, the company added four new franchises; earned three new Defense Logistics Agency manufacturing certifications; achieved AS9100 registration in the US and UK; successfully transferred memory product manufacturing to Orlando; expanded production clean room area for assembly and test, among several other notable improvements. *www.micross.com*

APPLIED MATERIALS ANNOUNCES DEPARTURE OF CFO GEORGE DAVIS

Applied Materials, Inc. has announced that George S. Davis, executive vice president and chief financial officer (CFO), will be departing the company effective March 8, 2013. The company expects to name a successor in the weeks following after a review of both internal and external candidates. Davis will be taking up the position of CFO for Qualcomm Incorporated.

Davis joined Applied Materials in 1999 as corporate treasurer. He was named CFO in 2006 after serving as head of the Corporate Business Development group, where he was responsible for merger and acquisition activities, strategic planning, and management of the Company's venture investments. *www.appliedmaterials.com*

PLEXUS NOMINATES RAINER JUECKSTOCK TO JOIN BOARD

Plexus Corporation announced that its Board of Directors nominated Rainer Jueckstock for election to the board at the 2013 Annual Meeting of Shareholders on February 13, 2013. Upon election, Mr. Jueckstock fills the board seat now held by Mr. John Nussbaum, who retires as Chairman on the same date. Mr. Jueckstock serves as Co-Chief Executive Officer, as a member of the Board of Directors of Federal-Mogul Corporation, and as Chief Executive Officer of Federal-Mogul's Powertrain segment.

Rainer Jueckstock holds a degree in Engineering from the Military College at Zittau, Germany.

www.plexus.com

INTEL RECOGNIZES FINETECH WITH APPRECIATION AWARD

Intel Corporation has recognized Finetech with an Appreciation Award presented by Intel's Equipment Vendor Enabling program. The Equipment Vendor Enabling Program maintains communication between Intel and equipment vendors to proactively align equipment capacities with the requirements of technology developments. Finetech has provided Intel manufacturing sites around the world with FINEPLACER® hot gas rework and advanced packaging and bonding solutions for 9 years, offering additional application support, training and service.

www.intel.com ◆

Spreadtrum Adopts STATS ChipPAC's Innovative Packaging for China's Smartphone Market

STATS CHIPPAC LTD. HAS ANNOUNCED implementation of breakthrough performance and packaging innovation in multiple advanced chipsets for the rapidly developing smartphone market in China. Spreadtrum Communications, a leading fabless semiconductor provider in China, has adopted STATS ChipPAC's packaging innovations for a number of its mobile chipsets. The combination of Spreadtrum's advanced silicon design capabilities with STATS ChipPAC's next generation embedded Wafer Level Ball Grid Array (eWLB) packaging technology offers increased performance and compact form factor at a competitive cost for the fast-growing China smartphone market.

Spreadtrum offers mobile chipsets for a range of smartphones, feature phones and other consumer electronics products that support 2G, 3G and 4G wireless communications standards. Spreadtrum's TD-SCDMA (time division synchronous code division multiple access) chipsets have set a new standard for increased performance and size reduction in the highly competitive smartphone market in China. TD-SCDMA is a 3G mobile telecommunications standard that is currently utilized in China to enable data, voice, video and media in mobile phones and internet-enabled devices.

"China is now the single largest smartphone market in the world and is rapidly growing," said Brian Chen, Vice President of Operations at Spreadtrum. "By combining our unique chip architecture and leading TD-SCDMA modem technology with STATS ChipPAC's technology and manufacturing leadership, we have been able to deliver high performance TD-SCDMA chipsets in a package format that continues to provide Spreadtrum and our customers with a clear competitive advantage in the China market."

eWLB is a powerful fan-out wafer level packaging (FOWLP) technology and integration platform that provides significant advantages including a more space-efficient package design enabling a smaller footprint, higher density input/output (IO) and a lower package height than is possible with laminate or flip chip semiconductor packages. Spreadtrum and STATS ChipPAC are jointly working to utilize innovative packaging technology across a full spectrum of complex product designs such as dual and quad core mobile processors.

Visit www.statschippac.com for more. ◆

Plexus Expanding Design and Manufacturing Operations in the UK

PLEXUS CORPORATION, the Product Realization Company, has announced its intention to expand its Livingston Design Centre to larger premises at the Pyramids Business Park, in Bathgate. Having worked closely with Scottish Enterprise on funding support, Plexus will expand its UK manufacturing footprint by opening a new manufacturing facility at the same location.

"Plexus' ability to provide full product realization solutions within the UK market has attracted several new customers. This increasing demand is the fuel for the expansion of our UK operations," commented Steve Frisch, Plexus Regional President in EMEA. "This demand sends a very positive signal that companies need a UK-based solution for the design and manufacturing of their low-to-mid volume, higher complexity products. These investments answer that need and demonstrate Plexus' continued commitment to investing in its UK engineering and manufacturing operations."

Welcoming the news, First Minister Alex Salmond said: "Plexus' decision to invest £9 million in expanding their Scottish operations will provide a welcome boost to the local economy, creating 130 new jobs and a new design, prototyping and manufacturing facility in Bathgate. The Scottish Government and our enterprise agencies are focused on securing new jobs, and investment and Plexus expansion plans will receive up to £1m of support through Scottish Enterprise. News that this international design and manufacturing firm is stepping up its Scottish operations is testament to the quality and skills of the West Lothian workforce and reinforces Scotland's reputation for excellence in innovation and manufacturing."

The new manufacturing facility will be approximately 47,000 sq ft and will include prototyping, manufacturing and warehousing areas. The site will complement Plexus' existing manufacturing facility in Kelso as well as becoming a European centre of excellence for prototyping. The co-location of design, prototyping, and manufacturing in one facility, enhances the value proposition for Plexus customers and reinforces Plexus as the Product Realization Company in the UK.

It is anticipated that Plexus will start the fit out of the new site later this year and that both the design centre and manufacturing site will be operational in February 2013. ◆

INDUSTRY INSIGHTS

By Ron Jones

PDIP – The Trend Setter

WE SELDOM THINK ABOUT the lowly PDIP these days, unless it is to ponder when it will finally disappear. We certainly wouldn't consider it to be a technology trend setter. But if we look back to the 3 year period from 1972 to 1975, numerous equipment and process advances were made that are still in use today. Many of these were enabled by small computer boards and computer aided vision. I would make the case that more innovation happened during these years than at any other time in the history of plastic packaging.

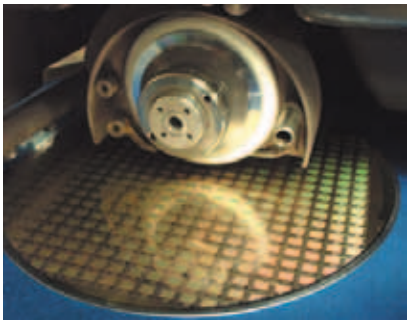
Early packages were typically fired ceramic/metal packages with lots of gold content. This included a variety of flat packs and side/bottom braze DIP versions. They were hermetic and very good, but also very expensive. The CDIP/CerDIP was introduced as a cost reduction to brazed packages.

As will all things semiconductor, there is a constant drive for lower cost and packaging was no different ... thus enter the PDIP. The labor content of PDIP and CERDIP was similar, but PDIP had a significantly lower bill-of-materials cost.

Let's start by looking at the PDIP package, circa 1972. Units were processed on a 10 unit leadframe strips with the bodies aligned along the long axis of the frame. Die were attached manually with gold preforms, bonding was done by operators with manual wire bonders, mold compound was injected at one end of the 10 unit strip and flowed past all units. An ink stamp was used to put information on the back after molding as all units looked alike and lot mixing was a problem. The units were processed through several mechanical operations to form the leads, remove shorting bars and separate units from each other. A top side mark was applied, sometimes after testing due to product binning. These processes were the same whether manufacturing was being carried out in Asia or the US. Though assembly in Asia reduced the cost, there was a pressing need for better quality and lower cost.

We'll now look, by major operation, at the changes that occurred between 1972 and 1975. As noted earlier, many of these technologies are still in use today, 40 years later, across a broad spectrum of plastic packages.

Die Separation



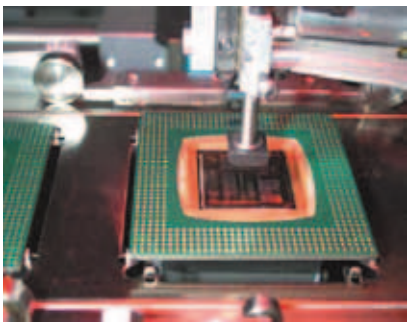
Dicing saw with diamond tipped blade.

The early dicing process used a diamond tipped scribe to "scratch" the surface of the wafer along the "streets" between the die. This is like using a diamond scribe to score a piece of glass before breaking. The wafer was attached to a piece of organic film before scribing. After scribing, the film was stretched over an anvil and a roller was used to break the wafer along the scribe lines. There were anvils of various radii to optimize the breaking process for die of different dimensions. There were often incomplete breaks which were difficult to rework.

Along came a high tech solution, the laser scriber. In theory it looked great, but had two significant drawbacks: 1) each machine cost $250,000 but wasn't a lot faster than diamond scribe, and 2) because of slag (tiny particles of Si that were thrown off during the lasing process) the wafers had to be spin coated with an organic polymer that trapped the slag and did not allow the particles to attach to the die surfaces. After the dicing operation, the polymer coating had to be removed from the wafer which had issues of residual contamination.

At about the same time, the winner appeared on the scene. It was a circular saw blade with tiny diamond particles bonded to the cutting edge of the blade. The wafer was mounted on an organic tape and the saw blade sawed through the wafer and slightly into the tape below. Water flooded the wafer during sawing for heat dissipation and surface clean involved merely spraying the sawn wafer with clean water. Though lower tech than the laser approach, the machines were relatively inexpensive and the consumable saw blades were reasonably priced and could be reworked. After 40 years, the dicing saw accounts for most dicing capacity in the world.

Die Attach



Epoxy die attach work station.

For years, most PDIP die attach was done with Au preforms on a heated stage. The operator would use needle nose tweezers to pick up a gold preform and place it on the leadframe. Next a die would be picked up with tweezers and scrubbed into the gold preform. The operator had to ensure that the die was in the correct x, y position and rotation. This process was slow, requiring an operator to do two manual pick and place operations. It was also prone to yield loss from die that were dropped between pick up and placement.

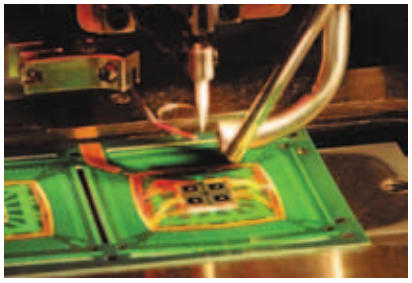
The first major improvement was automatic die attach. The gold preform material was in the form of a ribbon and was wound on a spool. There were various widths of ribbon (for different size die) and the spools could be changed out quickly. The other preform dimension was set by a micrometer dial. The correct amount of preform ribbon was fed out and a cutter separated the preform from the reel. The machine was designed such that the preform station and the die pickup station were in line and on opposite sides of the heated die attach station. While a preform was being placed on the leadframe, a die was being picked up by the die collet. The arm moved and while the die was being scrubbed in, a new preform was being picked up. The machine had high throughput and quick die size and leadframe changeover.

The next improvement came with the introduction of epoxy die attach. While the gold die attach machine provided good throughput and yield, the cost of the gold

continued on next page

preform was a significant item in the bill of material. The logic and memory chips of the day did not generate much heat and gold was not required for heat conduction from the chip to the leadframe. Pure epoxy compounds had been tried, but had little heat conduction and provided no electrical connection between the back of the chip and the leadframe. The solution was a silver filled epoxy with tiny flecks of silver mixed in to provide both thermal and electrical conduction. Modifications to the auto die attachers were relatively straight forward with an epoxy pot and rubber stamp pick up station replacing the preform cut and pick up station. Throughput was roughly the same, but the cost dropped significantly with the elimination of the gold preform.

Wire Bonding



Gold thermosonic wire bond work station.

In the early 70's, wire bonding involved manual wire bond machines. The operator used a leveraged joy stick to move the capillary threaded with gold wire into position over a bond pad on the chip. The capillary would be lowered and pressure applied to cause the wire to form a metallurgical ball bond with the bond pad. The capillary was raised and moved to a location over the leadframe bonding finger. The capillary was lowered and pressure applied to make the stitch bond between the wire and the lead finger. The capillary was raised, and a gas torch was used to melt the gold wire at the end of the capillary, thus forming a ball for the next ball bond. This process was repeated for the remaining wires. In many cases, lifting the capillary would not break the wire at the stitch and an operator would have to go in with tweezers and pull the pigtails. Some bonders were equipped with a light spot that illuminated where the capillary would land, which improved both speed and accuracy. The production standard for operators on 16 pin devices was approximately 60 units per hour. This equates to 1 unit per minute or 1 wire every 4 seconds.

The next improvement was the automatic gold wire bonder. The bond head was driven to the correct location by x and Y axis drive screws with digital encoders. Cameras with pattern recognition software scanned the die and the leadframe to determine the real location of each bond pad and lead finger. High speed algorithms were then used to map the stored theoretical die pad and lead finger locations to the actual locations. This allowed for adjustments when the die was not in the correct x, y location, when the die was rotated, or when lead fingers on the frame were out of position. The first release of the auto bonders achieved 350 parts her hour, a 6x improvement over manual bonding. The next release, a year later, increased the throughput to 700 pph. This equates to 3 wires per second. A circuit was also developed to sense when a wire didn't stick, which triggered an automatic re-bond procedure. These bonders had quick payback even with Asian labor rates and were quickly fanned out worldwide. The consistency of the automated processes also improved quality and reliability and material usage.

Inspection cameras were fitted to the output side of the bonder so that a remote process control operator could monitor the bonders output. Sixteen bonders were multiplexed together and monitored by a single PC operator.

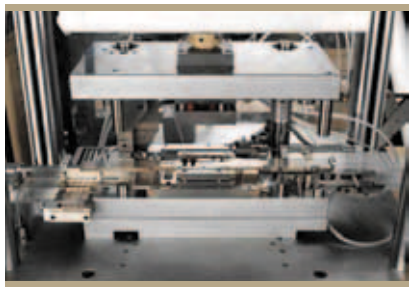
Molding

Modern auto mold system.

In 1972, PDIPs were process on 10 unit leadframe strips with the units oriented end to end. A significant problem with this orientation was that the mold compound for all ten units flowed past and through the wires on the nearest unit. Ninety percent passed the second unit and so on until only a small amount of compound passed the wires for the 10th unit. As compound flowed, it began to increase in viscosity as time passed. Due to variations in mold compound formulation, pelletizing , shipping and storage history, pellet preheater control and mold press parameters, there was significant variations in the viscosity of the compound upon injection. When the compound was too viscous, it would sweep the wires, either causing wires to break or short together.

The solution to this problem was the introduction of Single CAVity (or SCAV) mold designs. The leadframes were redesigned to rotate the units 90° so that the units were perpendicular to the flow of the compound and each unit was parallel with its neighbors. Mold compound would run the length of the 10 unit strip in a runner channel until the channel was full. As more compound was injected into the channel, the pressure would build forcing compound to enter through a small opening (gate) in each of the 10 individual cavities simultaneously. This allowed for only a small amount of compound to flow past the wires, and also all units were injected simultaneously, provided better uniformity. New mold dies had to be built, but the payback was quick from increased yield, improved reliability and reduced material usage.

Trim/ Form/Singulation



Trim-form-singulate die set.

With strip molding, the T/F/S steps were carried out serially in several semi-automatic tools. The first tool used punches to remove the tie bar between leads and also the flash between the tie bar and the package body. The next tool formed the leads from flat into their final form factor and the last tool remove the rail that was connecting the lead tips. The 10 unit strip was then fed through a saw that separated each of the units from its neighbor.

With single cavity design, the various stations could be incorporated into one machine with better uniformity and higher throughput. The steps were typically tie bar punch, lead tip separate, lead form and rail shear. The operations could be done serially in a single machine, or all at once in a single machine with a more complex trim/form die set.

Package Marking

Package marking was typically done with rubber stamps in the early days. An enhancement was introduced with gravure marking where the marking material was transferred to a plate and the plate transferred the ink to the package. This significantly improved the throughput and legibility of the mark operation. Laser marking came much later.

PDIP Design

In the early days, the pin one identifier was stamped on with ink. To eliminate

PDIP package showing pin 1 notch and half-leads.

this step, the mold die was modified to include some feature that would identify pin one during the molding operation, eliminating a step and guarding against improper orientation.

Standardization of 14/16 Pin Package Length

PDIPs always have a lead to lead tip spacing of 100 mils. The greater the number of package leads, the longer the package. The length is usually a few dozen mils more than 100 mils times half the number of leads (remember it's a DIP). In a move to get more leverage between tooling in the very high volume 14 and 16 lead packages, the design of the 16 lead package was modified. The four corner leads retained the dimension of the portion of the lead that would go through the PCB, but the shoulder of the corner leads was shaved off to make them narrower. The outcome of this was that both 14 and 16 lead PDIP's had the same package length. Not only did this improve tool utilization, but it also reduced the amount of mold compound required. This same design tweak was subsequently incorporated into all PDIP's from 18 lead to 64 lead.

Summary

The short period of time between 1972 and 1975 was a truly innovative time in the history of plastic packaging and the semiconductor industry. ◆

COUPLING & CROSSTALK

By Ira Feldman

ELECTRONIC COUPLING IS THE transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions like this one may deliver a message closer to home.

Measuring Up

TAP TO TURN ON. WAIT FOR it to zero. Step on. I haven't lost any weight, still 205 pounds even with all this exercise and careful eating? Step off, step back on. 212 pounds. Damn, wrong answer. Step off, step back on. 206 pounds. Okay maybe the first reading was right. Optimistically record 205 pounds. Does this nightly dance sound familiar? **Not only are bathroom scales the bearer of bad news, their erratic behavior may make them one of the most despised home appliances.**

I cannot say that the conversion of bathroom scales from purely mechanical systems to digital electronics has increased their accuracy. The precision of the data has increased moving from coarse analog dials to digital displays but scales do not appear to have improved accuracy or repeatability. Even though my scale displays weight to the nearest 0.1 pound (precision), the specified accuracy is only +/- 0.2 pounds. Many people, engineers included, often confuse the precision for the accuracy. (See my blog or this Wikipedia http://j.mp/WWwWbT entry for a refresher on the difference between accuracy and precision.)

I haven't done an analysis of variance (ANOVA) gauge repeatability and reproducibility (often shortened to "ANOVA gauge R&R" or simply "gauge R&R") study of my bathroom scales and measurement techniques, but I just *know* the R&R is awful. Perhaps this may be a good elementary school science project for my children? *In any case, it certainly is not user error…* As a statistical process control (SPC) chart "junkie", I plot each of my measurements by hand in real-time. I'm all for deep statistical analysis of data, preferably in as close to real time as possible. There is often a significant delay between when the measurement is made and when the statistics are run. By manually charting key parameters at the time of measurement, the user gains a "feel" for the data and insight into the stability of the process and measurement challenges. Beyond general optimism, I can pick the most likely "accurate" value for my weight.

The typical digital bathroom scale is based upon load cell technology where the resistance of a strain gauge changes due to the applied load. Four load cells are often connected in a Wheatstone bridge configuration whose resistance is then measured. From that resistance the strain can be calculated knowing the geometry of the strain gauge. This is certainly **not terribly complex technology when compared to modern microelectromechanical systems (MEMS) based sensors.** However, there are plenty of challenges in designing and producing a digital bathroom scale especially when considering the low average selling price (ASP).

Most MEMS based sensors measure fundamental forces – acceleration, rotation, and pressure – using miniature structures that move slightly. This movement results in a minute change to either capacitance or resistance that can be measured with high sensitivity electronics and used to calculate the movement. These sensors in turn provide measurements to calculate meaningful information about objects such as: How fast is an automobile moving or turning? Are the tires inflated properly? Sensor fusion adds a layer of computational intelligence to combine the data from multiple sensors in order to increase accuracy, eliminate spurious measurements, and provide greater insights into what has just happened. With my bathroom scale, I provide the "intelligence" to eliminate bad data.

For inanimate objects, MEMS sensing is fairly straightforward and accurate. But like measuring a person's weight, **measuring and providing meaningful information about people is significantly more complex.** Did the wristband sensor actually measure several steps or was the user waving their arms? These measurement challenges may be why some technologists differentiate types of sensors as off-body, on-body (wearable), and in-body (implantable or digestible).

Most successful MEMS sensors to-date are off-body applications typified by automotive and smartphone applications. Even though a user may wear a smartphone, the data collected is more about the motion of the smartphone than the wearer. Not only is obtaining meaningful data easier in off-body applications, the devices may not need biocompatibility testing or medical regulatory approval.

With few exceptions, many of the mass marketed MEMS based systems today have coarse accuracy sufficient only for sensing large changes. **Coarse accuracy is sufficient for idiot lights (such as low tire pressure), toys, and gadgets.** I've noticed that my global position system (GPS) watch and sports measurement application on my smartphone (using sensor fusion of GPS and MEMS sensors combined with map data) are always slightly "off" in terms of distance for my bicycle rides. And neither measures exactly the same as my wheel based odometer.

The distance difference on these devices is minor compared to the ~2x difference in vertical climbing and ~3x difference between calculated calories. I could probably design a gauge R&R study and calibration method between the devices for distances, possibly for vertical climbing, but what about the calorie difference? As much as I am interested in improving my physical performance, **perhaps I am better off enjoying my bike ride and the half-gallon of ice cream that the high calorie expenditure data permits.** As the demand for self-awareness and quantification devices such as activity monitors and calorie counters grows, a greater number of enthusiasts are likely to push for increased accuracy. As MEMS sensor technology improves, market-leading product companies will find it easier to supply high accuracy and repeatable devices at reasonable costs. I look forward to the day when all of my devices have a much higher degree of correlation to each other.

As applications move to on-body or in-body their sophistication, accuracy, repeatability, and reliability need to increase significantly. This will permit many of the devices that are currently closer to toys and gadgets to become better diagnostic tools. The desire for self-administered medical diagnostics, often envisioned using a smartphone as the computing and connectivity engine, comes with significant system performance challenges. These devices may start out as "idiot lights" for our body – i.e. time to see the doctor for "check engine" – but greater specificity to provide "medical grade" measurements will be demanded over time. System accuracy and repeatability will be essential to detect acute symptoms and prevent false positives.

Once medical or mission critical reliability is proven for more than a handful of devices, MEMS will quickly move from on-body to in-body applications. At the same time MEMS has the opportunity to move from measurement to interaction. The unique size of MEMS may enable multiple measurement points and/or new therapeutic methods. **High volume MEMS fabrication processes and packaging technologies that lower costs will increase the adoption rate of home or individual centric point-of-care.** This greater access to advanced automated healthcare in non-clinical settings should reduce out-of-control medical spending.

Properly measuring, analyzing, and adjusting human activity and medical state are clearly challenging tasks. As a MEPTEC committee member, I'm looking forward to the upcoming conference ***"MEMS-enabled eHealth Revolution"*** focusing on sensors, actuators, and architectures that enable advanced healthcare applications. One particular interesting area is how biological sensors and actuators may differ greatly from "traditional" MEMS due to unique requirements of these "wetware" devices.

If your curiosity includes how to make these devices work better than your bathroom scale, I look forward to seeing you at the conference! As always I encourage your comments on my blog http://hightechbizdev.com. ◆

IRA FELDMAN (ira@feldmanengineering.com) is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to commercialization. He follows many "small technologies" from semiconductors to MEMS to nanotechnology engaging on a wide range of projects including product generation, marketing, and business development.

The Coming Consolidation in the SATS Market

Jim Walker, Research Vice President and Mark Stromberg, Principal Analyst
Gartner

THE SEMICONDUCTOR ASSEMBLY and Test Services (SATS) industry is made up of specialized contract manufacturers that perform packaging and/or test services for the various segments (fabless, integrated device manufacturers [IDMs] and system OEMs) of the semiconductor industry. In the majority of cases, the SATS customer designs and fabricates the semiconductor or integrated circuit die. The SATS industry player receives the fabricated wafers of isolated die and then proceeds with final assembly and test processes.

Packaging was the first of the three main electronics manufacturing segments to move offshore (in other words, to Asia/Pacific), beginning with the construction of the Fairchild Semiconductor plant in Hong Kong in 1962. In the years that followed, most IDMs built their packaging plants in many countries of Asia/Pacific, driven by low-cost labor, tax holidays and government subsidies. This trend was so prevalent that by the late 1980s, almost all the top 25 semiconductor companies had moved to or built the majority of their packaging plants in the region.

With this migration to Asia/Pacific, local companies had access to technology and began offering packaging services as well. Initially, the IDM and OEM companies would provide engineering assistance and/or equipment to these "subcontractors." With the proliferation of package development came the risk management assessment of internal versus external manufacturing. The key factor was to determine if IDMs and OEMs own their own factory or share the manufacturing burden with others (even competitors) through outsourcing. By the early 1990s, the outsourced packaging model was in full bloom and accelerated even more with the emerging fabless/foundry business model.

Fluctuating market conditions, especially in the past 10 years, has dictated the careful management of manufacturing assets. Outsourcing growth has accelerated more as package proliferation has grown, especially due to the development of customized or application-specific packaging. During this time, many of the privately held, closely owned SATS companies succumbed to the initial public offering hysteria, such that by the end of 2001, the top 10 were now publicly traded companies. Today, the SATS market has grown from $5 billion in 1997 to almost $25 billion 15 years later.

Of the more than 130 companies that participate in the SATS market, nearly all of them are located in the greater Asia/Pacific region (including Japan). The extent of participation depends greatly on the market being served, because barriers to entry increase depending on the complexity of the packaging technology. Manufacturing of simple discrete transistors does not require the extensive capital outlay of new, emerging packaging technology, such as those used in wafer-level packaging (WLP) or through-silicon via (TSV) processes.

Technological leadership, along with packaging and test proficiency are key differentiators in this market. Those that develop the technology first, while providing solutions at very competitive prices, experience the greatest rewards. But this achievement comes only with a large commitment of capital resources. Thus, the top players are those that develop the new technologies, while the others follow in due time.

This trend toward more customized, application-specific packaging is causing convergence and, at the same time, competition among wafer fabrication, packaging and board-level (or system-level) assembly companies. The emerging WLP, flip chip and TSV technologies require more extensive wafer fabrication and packaging manufacturing equipment, processes and expertise. Correspondingly, 3D package stacking, embedded components and system-in-package (SiP) processes require both packaging and printed circuit board assembly (PCBA) technologies. Even-newer technologies on the horizon, such as system-on-package (SoP), will further blur the distinction. This overlap of processes and technologies will result in increased competition for value-added services among the foundry, SATS and EMS/ODM providers in the future.

2011 Rank	2010 Rank	Company	Region	2010 Revenue	2011 Revenue	2010 Market Share (%)	2011 Market Share (%)	% Change 2010-2011
1	1	**ASE**	Taiwan	3,903	4,252	16.5%	17.7%	9.0%
2	2	**Amkor Technology**	United States	2,939	2,776	12.5%	11.6%	-5.5%
3	3	**SPIL**	Taiwan	2,104	2,024	8.9%	8.4%	-3.8%
4	4	**STATS ChipPAC**	Singapore	1,678	1,707	7.1%	7.1%	1.7%
5	5	**Powertech Technology**	Taiwan	1,173	1,252	5.0%	5.2%	6.7%
6	6	**UTAC**	Singapore	925	981	3.9%	4.1%	6.0%
7	8	**ChipMOS Technologies**	Taiwan	591	620	2.5%	2.6%	4.9%
8	9	**Jiangsu Changjiang Electronics Technology**	China	531	611	2.3%	2.5%	15.0%
9	7	**J-Devices**	Japan	600	565	2.5%	2.4%	-5.8%
10	12	**Chipbond Technology**	Taiwan	431	441	1.8%	1.8%	2.3%
Top 10 Total				**14,874**	**15,228**	**63.0%**	**63.4%**	**2.4%**
Other Companies				8,718	8,796	37.0%	36.6%	0.9%
TOTAL MARKET				**23,593**	**24,024**	**100.0%**	**100.0%**	**1.8%**

Table 1. Top 10 SATS Companies' Sales as a Percentage of Total Market, 2011 (Millions of Dollars).

The SATS Market

The worldwide SATS market reached $24 billion in 2011, up 1.8% from 2010 (while full market share analysis has not been completed for 2012 as of this writing, the total SATS market revenues are expected to grow 1.4% in 2012). The top 10 SATS companies' combined packaging and test revenue increased 2.4% in 2011 (see Table 1). As a group, their combined revenue performed better than the overall SATS market. Among the top 10, five companies each had more than $1 billion in revenue and all but one had more than $500 million.

Notably, the top five companies combined represent only 50% of the market. The next 15 make up 27% of the market; therefore, the top 20 comprise a little more than three-fourths of the total market. Even at that, there are still more than 100 other companies that make up the remaining 23% of the market, with nearly all of them having factories in Asia/Pacific or Japan.

As mentioned before, since 1997, total revenue for the SATS market has more than quadrupled, driven by the proliferation of more customized, application-specific packages to meet device size, density and performance requirements. During this time, the outsourced share of the total semiconductor packaging market has more than doubled, growing from 22% in 1998 to 50% in 2011.

Since the SATS industry hit the halfway saturation mark for penetration of the total available market (TAM) in 2011, the rate of growth for the SATS market has and will likely continue to slow. For this year SATS revenues are expected to grow 6.8%. Gartner estimates that the market will reach $33.4 billion in 2016, with a five-year CAGR of 6.8%.

Industry Consolidation

Consolidation must clearly occur in order to maximize efficiencies of scale in the SATS market. Additional mergers and acquisitions will also likely occur as the leading SATS providers strengthen their position at the expense of smaller competitors. More than 130 SATS companies are in this market, with no single company having more than 18% of the market. Additional consolidation may come from the IDMs' and OEMs' own internal facilities, as the customization of packages required makes the capital intensity versus manufacturing utilization becomes inefficient.

Additionally, 3D packaging and TSV represent major opportunities for continued growth. The biggest competitive threat may come from front-end wafer fabs that start doing much of the wafer-level processing. TSMC's announcement to move into the WLP arena should serve as a wake-up call for SATS companies. This entry into packaging by the foundries could perhaps accelerate the SATS companies teaming up or merging with them, while relying on the 3D expertise of the leading SATS companies.

Gartner has identified more than 130 companies in the SATS business. Among them, they represent more than 400 of the nearly 675 of the worldwide total packaging and assembly factories. Since the top 20 companies represented 77% of the SATS market revenue, or $18.49 billion in 2011, the remaining 110 companies generated the other 23%, or $5.53 billion. This averages out to revenue of $50 million per year for each of these 110 companies. As advanced packages of flip chip and WLP become mainstream (with TSV to follow), it will be very difficult for them to generate and spend the capital required (ranging from $10 million to $50 million initially), to install production capacity for these new, advanced technologies. Thus, consolidation via mergers and/or acquisitions (or bankruptcy/exiting the business) must occur as a method of developing or creating the necessary capital base to remain competitive. ◆

SYMPOSIUM

MEPTEC PRESENTS

MicroElectronics Packaging and Test Engineering Council

Association Sponsor

MEMS INDUSTRY GROUP®

Eleventh Annual

MEMS TECHNOLOGY SYMPOSIUM

MEMS-Enabled eHealth Revolution

MEMS and NEMS Based Applications for Emerging Healthcare Off-body, On-body, and In-body

Topics will include:

- MEMS and Sensors for eHealth - Market Overview
- eHealth Revolution Enabled by Wearable MEMS Motion Trackers
- Wireless Health: Remaking of Medicine by Pervasive Technologies
- Mouth Guards, Sweatbands, and Bandages: On-Body Chemical Sensors
- Miniaturized Electronic Packaging for Wearable Health Monitors
- Revolutionizing Consumer Fitness & Digital Health: Ultrathin Conformal Electronics
- Printed and MEMS Gas Sensing Systems: The Next Generation of Situational Awareness in the Trillion Sensor Universe
- eHealth: Path to Healthcare for All
- Advanced Manufacturing of Integrated Labs-on-a-Chip for Ubiquitous Diagnostics

Diamond Sponsor

ASE GROUP

REGISTER ONLINE TODAY AT WWW.MEPTEC.ORG

Media Sponsors

3DInCites.com · Chip Scale Review · Circuits Assembly · Global SMT & Packaging · MEMS and Nanotechnology Exchange · MEMS Journal · Micronews · semiconductor packaging news · Test, Assembly & Packaging TIMES

Eleventh Annual MEPTEC MEMS Technology Symposium

Wednesday, May 22, 2013
Holiday Inn, San Jose, California

FOR INANIMATE OBJECTS, microelectromechanical systems (MEMS) sensing is sufficiently accurate. Measuring and providing meaningful information about people, however, is significantly more complex. This challenge may be why some technologists differentiate types of sensors based on their location: off-body, on-body (wearable), and in-body (implantable or digestible), as their packaging and functionality significantly vary.

Most successful MEMS sensors to-date for animate objects are off-body and on-body, typified by smart phone and fitness applications. Not only is obtaining meaningful data easier for these applications, they most often do not need biocompatibility testing or medical regulatory approval.

As more applications move to on-body, and in-body sensors emerge, sensor sophistication and packaging technologies need to significantly improve. Self-administered medical diagnostics are envisioned using one's smartphone as the computing and communication engine. These systems require accuracy and repeatability to adequately detect acute symptoms while preventing false positives. eHealth solutions will demand unique and flexible packaging from sensors to system creating additional technical challenges and providing new market opportunities. While raw data is of great value, increasing software sophistication is expected with the ultimate goal of local interpretation and understanding of sensor data ("doctor on a chip"). Adequacy in the clinical medical setting is being systematically proven for more and more devices, enabling new diagnostic and therapeutic methods.

The Holiday Inn - San Jose Airport is conveniently located at 1350 North First Street in San Jose, CA just minutes from the Airport.

MEMS and nanoelectromechanical systems (NEMS) based products with embedded actuators are starting to emerge, creating smart drug delivery systems. In combination with sensors, these technologies promise a dramatic restructuring of the medical industry. Patients may easily obtain (at low cost) diagnostic and therapeutic equipment in the first phase of this evolution, receive diagnosis from sophisticated embedded software (doctor on chip) in the second phase, and play a significant role in dramatically reducing the root causes of medical problems through personalized medications and gene therapy in the third phase.

As a byproduct of the eHealth revolution, the skyrocketing costs of medical care are expected to come under control, and a much higher standard of healthcare brought to every person on Earth, creating healthcare Abundance[1] in the next 20 years.

Invited speakers will focus on sensors, actuators, and architectures that enable the eHealth revolution. Technologies that increase the accuracy or reliability of devices, lower manufacturing costs, and/or enable unique diagnostics or treatment will be highlighted. ◆

[1] Concept of Abundance was introduced by Peter Diamandis of XPrize Foundation in his book "Abundance". Abundance is defined as equality between supply and demand for goods and services on Earth. Visit www.abundancethebook.com for more.

On the day following this event, **MEPTEC** and **MEMS Journal** are co-presenting the second annual **MEMS Business Forum**. Discounted attendance and exhibiting opportunities are available to those who wish to attend both events. Contact bcooper@meptec.org or go to www.memsforum2013.com for pricing details.

Special Showcase Session:

Digital Health for All of Us

Exponential growth of sensors in mobile applications over the last five years brought dramatic reduction of sensors footprint, cost and power consumption. These advances started to enable the next market Tornado, the digital health. Initial products focused on wearable "wellness" devices driven by simple sensors, such as accelerometers, pulse, sweat and temperature sensors. In parallel, more advanced devices started to reach the market, such as ECG monitors, ultrasound imagers and body fluid analyzers.

One of the notable developments in this market is emergence of "doctor-on-a-chip": cellphone software performing medical diagnostics.

At the post-conference reception a special showcase called ***Digital Health for All of Us*** will be held to introduce selected healthcare and wellbeing products driven by sensors and sensor software. During the reception, attendees will have an opportunity to have hands on demo with such products.

Digital Health for All of Us will be open to symposium attendees, outside industry groups, editors and the public. ◆

LSI®

Accelerating the World's Applications with Smart Silicon.

LSI's new corporate headquarters in San Jose, a 10-acre campus with 220,000 square feet of office and engineering space and a state-of-the-art datacenter.

In today's data-centric world, the ability to rapidly manage massive increases in data generated by consumers and businesses is being challenged at all levels. LSI's unique products help IT architects and managers deploy the architectures that store, share and accelerate data around the world. The need for data speed is acute among consumers – tablet, mobile phone and PC users – the organizations that need to quickly monetize data, and the storage and network infrastructures that transport and analyze digital information.

LSI answers the call for faster information access with semiconductors and software that accelerate data across enterprise and mobile networks, datacenters and client devices including solid-state and hard disk drives. At the heart of the LSI high-speed designs is intelligent silicon.

For datacenters, information speed is a matter of competitive business advantage. Now more than ever, companies rely on fast data access for deeper business knowledge, productivity gains and greater operating efficiencies. IT managers are pressed to increase computing efficiency while reducing power, cooling and other costs. For their part, end users expect uninterrupted access to content, anywhere and on any device.

Today, no consumer or business escapes network slowdowns, and the consequences can range from merely frustrating to costly. Sluggish data networks causing download lags of only seconds on websites can decrease page views, overall traffic and, for online retailers, revenue as shoppers flee to competitors for a faster purchase. For financial institutions that use electronic trading platforms, a millisecond disadvantage in trading applications can cost millions of dollars. A choppy movie download degrades the user experience. The challenge is to accelerate the applications.

LSI Smart Silicon Takes On Latency

The chief cause of lags in data flow is the perennial problem of latency – the time it takes for information to flow between two points in a server or network. Over the past 30 years, network bandwidth has improved about 3,000-fold, and processor throughput, disk capacity and memory capacity have also seen large gains. Over the same period, latency has seen a comparatively modest 30-fold improvement.

LSI helps IT architects and managers harness the data deluge by making data infrastructures smarter – and faster. The company's technology is the intelligence critical to reducing latency and enhancing application performance. LSI's broad range of storage and networking solutions help IT organizations store, share and protect digital information not only with greater speed, but more efficiently and at lower cost, touching data at virtually every point from source to consumption.

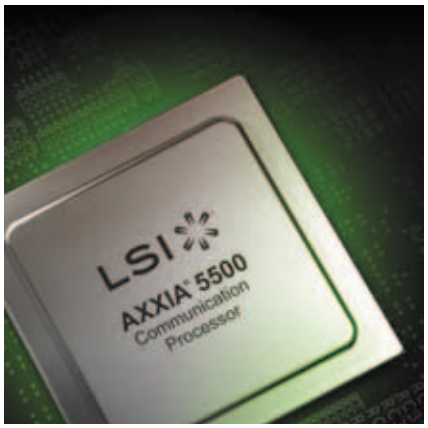
To help deliver digital content faster to organizations and end users, LSI focuses on the following areas:

Advancing Storage Technologies to Accelerate Applications

To enable the build-out of higher-performance datacenters, LSI offers the broadest portfolio of storage silicon in the industry, including hard disk drive System on Chips (SoCs), intelligent solid state storage solutions, flash storage processors, Serial Attached SCSI (SAS) host bus adapters (HBAs), RAID-on-Chip (ROC) solutions, RAID controller cards, and SAS switches and expanders. Only LSI offers both standard and custom flash storage processors for manufacturers of solid-state drives (SSDs) and PCIe®-attached SSDs. Nearly 70 percent of servers shipped use LSI technology.

Server-side flash technologies such as the LSI® Nytro™ application acceleration family can provide the lower latency and higher bandwidth required to speed information access. When combined with intelligent flash caching software, these solutions hold the key to breaking through I/O bottlenecks to accelerate database transactions, reduce total cost of ownership and help businesses extract the full value from data.

- The LSI Nytro MegaRAID® application acceleration card for direct-attached storage (DAS) is designed to accelerate applications economically by combining leading RAID performance and intelligent caching with onboard flash storage. Nytro MegaRAID cards can reduce DAS response times 30-fold over traditional



hard disk drives and enable hard disk drive rebuilds to complete up to 10 times faster.

- LSI Nytro XD solutions, designed for storage area network (SAN) environments, combine flash with seamless caching and acceleration software that detects hot spots and stores this frequently accessed data in a Nytro WarpDrive® card to accelerate application response.
- While flash technology is fast and energy-efficient, flash reliability is sometimes a concern for the heavy transactional loads common in the datacenter. LSI SandForce® flash storage processors give enterprises the flash reliability they need to increase performance and power efficiency. LSI SandForce DuraClass™ technology delivers industry-leading data protection and reliability – increasing the endurance of SSDs up to 8-fold over competitive solutions.
- LSI Nytro WarpDrive cards accelerate database transactions and application I/O performance – delivering up to 100 times the speed of a traditional hard disk drive.
- LSI hard disk drive, flash and server storage customers include ASUS, Cisco, Dell, EMC, Hitachi, HP, IBM, Intel, Lenovo, Micron, NetApp, Oracle, Samsung, SanDisk, Seagate, Supermicro, Toshiba and Western Digital.

continued on page 23

Left to right: The Nytro MegaRAID card combines on-board flash technology with LSI RAID-on-Chip technology to help accelerate key business applications. The Axxia communication processor family is designed to meet the increased performance and low-power demands of next-generation mobile and enterprise networks. LSI SandForce flash storage processors enable standard flash memory to operate in enterprise, cloud and client storage environments.

LSI – A Rich Tradition of Innovation

Formed in 1981, LSI sprang from the storied technology wellspring of Silicon Valley. LSI – then LSI Logic – pioneered the modern-day gate array, standard-cell application-specific integrated circuit (ASIC), system-on-a-chip, platform ASIC and other technologies that gave rise to a rich tradition of innovation that continues today.

Little did the founder and his contemporaries know that digital communications and data would become the new currency, uniting people from all over the world in ways unimaginable even 10 years ago. The rise and explosive growth of social platforms, the mobile Internet, video and cloud computing are all among the drivers of a massive data deluge. And as the value of data increases, a new standard for speed has emerged: users want their data in an instant, sometimes in microseconds.

LSI products move data faster, more efficiently and at lower cost, touching information at virtually every point from source to consumption – from datacenters and enterprise and mobile networks to consumer devices including laptops, tablets and smartphones.

LSI®

Massive Data Growth Continues.

In the enterprise, demand for greater business knowledge, productivity gains and operating efficiencies – all in the service of competitive business advantage – is driving explosive data growth. According to industry analyst firm IDC, demand for storage capacity is growing at an annual rate of 30 to 50 percent, spurred by the rapid expansion of traditional enterprise applications and databases and cloud applications ranging from social media to virtualization and big data analytics.

Wireless infrastructure buildouts continue apace to support the swift adoption of smartphones, tablets, ultrabooks and other portable devices, and thriving demand for richer and higher-speed multimedia applications such as gaming, navigation and video. Globally, mobile data traffic is expected to grow 18-fold between 2011 and 2016, reaching 10.8 exabytes per month by 2016. Today, video traffic alone accounts for 40 percent of the wireless network load. The number of mobile devices connected to wireless networks will reach 25 billion, 3.5 for every person on the planet, by 2015. That number is expected to double, to 50 billion, by 2020. In 2012, 700 million smartphones shipped, supported by 1.5 million mobile applications representing 85 billion downloads.

LSI – Accelerating Storage and Networking

LSI offers a wide range of storage and networking products that accelerate data and applications across enterprise and mobile networks, datacenters and client devices.

Storage Products

For organizations that demand the highest level of storage performance, LSI delivers the industry's broadest portfolio of storage technology solutions, including flash storage processors for client and enterprise SSDs. The product family, from silicon and boards to advanced software solutions, enables the entire storage ecosystem. All major server and storage original equipment manufacturers use LSI storage technology. LSI is a market leader in SAS, RAID and application acceleration PCIe-attached SSD products. The company's storage products increase performance and reduce total cost of ownership for mega and enterprise datacenters, and public and private clouds. LSI MegaRAID is one of the most trusted brands in storage.

Building on a history of technology leadership that includes more than 10,000 patents and patent applications, LSI's recent innovations include solid state storage and 12Gb/s SAS products for storage server connectivity. LSI serves all segments of the storage market including mobile, desktop and enterprise disk drive electronics; custom silicon solutions for storage and SAN infrastructure devices; and standard components and storage adapters for servers.

The LSI family of SAS products includes ROC integrated circuits, HBAs, RAID controller cards and advanced software. Server and external storage vendors use these products to build industry-leading storage systems. The company's SoC solutions for hard disk and solid-state drives enable

LSI Product Snapshot	
Storage	
Flash Adapters	PCI Express (PCIe) flash adapters and related software
Flash Components	Flash storage processors for solid state drives (SSDs) and PCIe flash adapters, firmware and software, and development kits
RAID Storage	RAID-on-chip and Serial Attached SCSI (SAS) input/output controllers, RAID controller cards, host bus adapters, and software
Storage Peripherals	Hard disk drives SoCs (System on Chips) and preamps
Networking	
Custom Solutions	Custom SoCs for networking and storage
Networking Components	Standard and custom SoCs for mobile and enterprise networks

higher storage capacities for ever-growing amounts of data.

Networking Products

The explosion of digitized, shared and stored information around the globe is driving demand for powerful solutions for mobile and datacenter networks. LSI is meeting this challenge with a wide range of solutions that enables consumers and businesses to stay connected.

LSI's end-to-end portfolio of networking solutions for datacenters and mobile networks includes advanced, asymmetric multicore communication processors and a growing Axxia family of powerful network accelerators. The company's technology partners use its products to accelerate the deployment of next-generation mobile and enterprise networking solutions. LSI networking products allow intelligence, control and security to be distributed throughout networks.

LSI's multicore communication processors and accelerators deliver high performance and reliability for applications such as wireless base stations for mobile networks, gateways and datacenter management.

The LSI media processing family of products powers media gateways and accelerates transmission speeds of rich media for applications such as enterprise video conferencing. With the company's multiservice processors, legacy networks can be migrated to lower-cost Ethernet and IP-based networks. ◆

continued from page 21

Adding Intelligence to Accelerate the Mobile Network

Mobile network traffic is growing approximately 33 percent annually as users continue to create, share and consume massive amounts of digital content. The industry leader in traffic management and security processing for mobile infrastructures, LSI is helping network providers accelerate network traffic.

- The LSI Axxia® multicore platform accelerates wireless networks by combining the design flexibility of general-purpose CPUs with the speed and efficiency of specialized networking accelerators, enabling service providers to deliver higher, more predictable performance with higher security. LSI Axxia communication processors and accelerators deliver high performance for both base station management and subscriber data and voice in cellular base stations.
- Peaks in network traffic can distort video. LSI intelligent silicon helps mobile network providers improve quality of service by detecting and prioritizing traffic to bring predictable performance that allows the right data to get to the right users at the right time.
- Base station manufacturers take different approaches to designing their base stations, requiring a breadth of signal, data and control processing. LSI delivers a full spectrum of products, from standard to custom silicon, that allows mobile network manufacturers to build solutions ranging from macrocell to microcell base stations.
- Content delivery networks need a low-power solution for caching content to reduce latency and improve performance. The combination of the LSI Axxia network accelerators and Nytro solid-state acceleration cards speeds storage and networking for content delivery in mobile networks and datacenters.
- LSI customers in enterprise and mobile networking include Cisco, Ericsson and Nokia Siemens.

Reinventing the Datacenter to Deliver a Better Cloud

Enterprises and service providers are increasingly deploying cloud architectures to pool storage, processing and networking to increase computing resource efficiency and utilization, improve resiliency and scalability, increase agility and reduce costs. LSI smart silicon enables providers to optimize their cloud networks and reduce latency, a key measure of cloud performance.

- The LSI Nytro architecture uses PCIe-attached SSD technology and intelligent caching software to accelerate cloud deployments, optimizing customer response times across any workload cost-effectively with minimal datacenter footprint.
- Massive data growth increases the challenge of managing costs, power consumption, downtime and data reliability in datacenters. The LSI Syncro™ MX-B rack boot appliance allows multiple servers to share and scale storage, reducing costs, power demands and failure rates while improving storage utilization and application uptime.
- LSI SandForce flash storage processors give lower-cost flash the higher performance, lower latency and better endurance required for cloud applications.
- LSI Syncro MX-B is a smart, easy-to-use shared boot drive solution that significantly increases server reliability in mega datacenters and the cloud.
- LSI SAS components enable datacenter architects to support large topologies for public clouds and on-premise data environments. LSI SAS input/output controllers support up to 16,000 devices and LSI SAS expanders up to 2,000 devices.
- LSI SAS RAID products deliver the industry's highest levels of server-storage performance and data protection for cloud and enterprise IT environments.
- LSI Axxia communication processors increase the performance and scalability of cloud infrastructures by offloading control plane traffic associated with managing virtual machines.
- LSI cloud networking customers include Alcatel-Lucent, Cisco, Emulex, Fujitsu, Intel, Nokia Siemens and Oracle.

The proliferation of digital information has transformed the way people live, and LSI continues to innovate to store, share and protect data – faster and more efficiently.

To learn more about LSI, please visit www.lsi.com. ◆

SEMICONDUCTORS • SOLAR/PV
LEDS • MEMS • FPD
PLASTIC ELECTRONICS
EMERGING MARKETS

The Power of [x]

The Power of [Packaging]

Wire Bond
WFCSP
Flip Chip
3D IC
BGA
FO-WLP

Advances in microelectronics design bring new requirements and challenges for electronic packaging. As front-end and final manufacturing processes become more integrated, packaging is increasingly integral to the design, manufacture, and function of microelectronic devices.

SEMICON® West 2013 connects contemporary and advanced packaging innovations from the world's leading technology companies with the engineers, designers, scientists, and key decision-makers needing answers and solutions that improve performance and productivity and help move products to market.

Packaging at SEMICON West

- The latest packaging trends and developments for mobile applications including system-in-package (SiP), stacked packages, fan-in QFNs, fan-out WLPs, interconnection styles of 3D and 2.5D through-silicon vias (TSVs), and flip chip
- Integration and Implementation 2.5D and 3D stacked ICs, including chip on chip on substrate (CoCoS) and chip on wafer on substrate (CoWoS) flows and overcoming key barriers in thermal, test and manufacturability
- Packaging the Internet-of-Things (MEMS/Sensors)
- CPMT/SEMI Packaging Workshop
- 150 exhibitors with equipment and technology solutions for advanced microelectronics packaging

SEMICON® West 2013

July 9–11
Moscone Center
San Francisco, California
www.semiconwest.org

SEMICON West is brought to you by:

ADVANTEST · APPLIED MATERIALS® · KLA-Tencor Accelerating Yield · semi™

Yes, 3D ICs are Worth the Effort

Kirk Sabin, Senior Product Line Manager - Virtex-7T/XTFPGAs
Xilinx Inc.

3D ICS: THE WHAT & WHY?

In 2008, Xilinx set in motion a plan to expand "programmability" beyond traditional programmable logic and deliver at the 28nm node a new line of devices that enable new levels of system integration, improved performance and productivity while reducing BoM costs and lowering system power – delivering greater value to customers. One of the keys to making this happen was the bold decision to offer commercially – not just in the lab – the first 3D IC to the industry. Needless to say developing the technology and the infrastructure to assemble and test it, is very complex. But today 3D ICs are being proven to be well worth it.

By moving to a 3D architecture called Stacked Silicon Interconnect (SSI) technology at 28nm, customers today are taking delivery of two homogenous All Programmable 3D ICs the Virtex-7 2000T and the Virtex-7 X1140T. These devices include four FPGA dice (called Super Logic Regions) side by side on a passive silicon interposer. The SSI architecture enables a single device to offer twice as many logic gates than one would have typically expected on a monolithic 28nm FPGA – exceeding Moore's Law and shattering transistor and logic count records, as well as moving ahead of the competition. Demonstrating the benefits of modularity, Xilinx is also leveraging SSI technology to provide two heterogeneous 3D IC devices that include multiple FPGA logic dice connected to a 28-Gb/s transceiver-laden ASIC die – all interconnected via the passive silicon interposer. These new devices, the Virtex-7 H580T and H870T, enables communication companies to double the bandwidth of existing optical network equipment rather than replacing it with entirely new equipment – in turn, offering greater value to their customers.

With all this pioneering work accomplished, Xilinx has proven that 3D ICs are not only a technology that is commercially viable but one that has provided

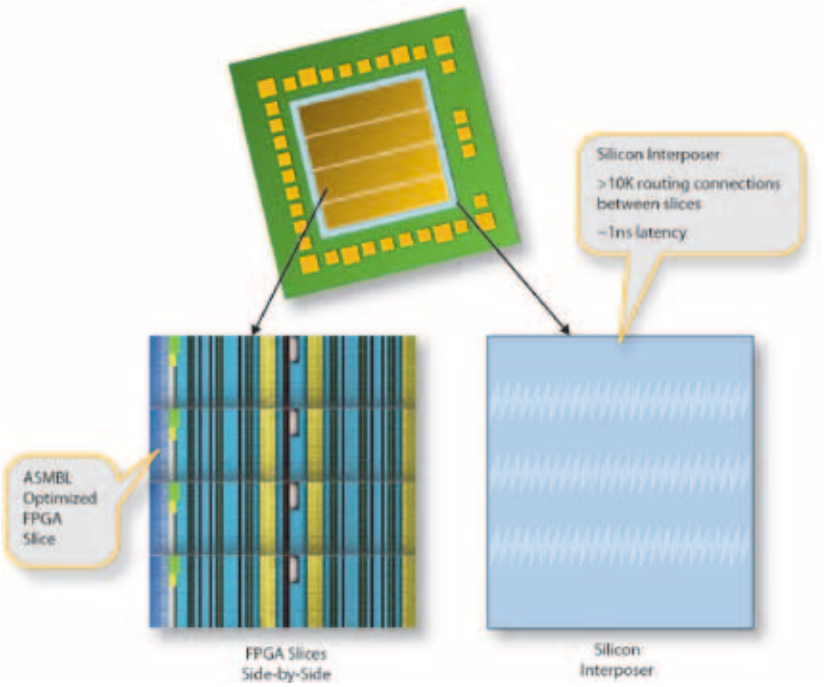


Figure 1. The stacked silicon architecture places several dice or slices side-by-side on a silicon interposer.

the company with a technology that leads competitors delivering only monolithic ICs. Indeed, aided by TSMC's 3D IC technology, many other companies are drawing up and will likely deliver at the next process node their own 1st generation of 3D ICs. And in the coming years we will likely see 3D ICs become an exciting new market within the semiconductor sector. 3D IC technology will certainly evolve but to accelerate its growth and become a booming mainstream market will require innovation and refinement at an industry level.

There are several trends that are aiding, as well as those that are hindering the adoption of 3D ICs. 3D ICs enable smaller, lighter, and faster multi-chip devices. Adopting this technology throughout the industry is beginning to have a significant impact on the entire semiconductor supply chain – from chip concept and design into the manufacturing fab and then through final assembly and test.

The migration towards 3D ICs is primarily happening based on the accelerated demand for higher bandwidths, reduced power consumption, and higher density. 3D IC technology has begun to realize commercial success recently. This is mainly attributed to the high efficiency of the solution and the guaranteed return on investment (ROI).

As a specific example, the telecommunications market needs FPGAs that incorporate dozens of serial transceivers with increased interconnect logic and block RAM for advanced data processing and traffic management, while enabling use within current form factors and power footprints. To reap first-mover advantage, the equipment makers want to ramp up manufacturing of their new products as rapidly as possible. This is where 3D ICs play well.

All Programmable 3D IC SSI Technology

At a time when the complexity, cost and thus risk of designing on the latest process geometries are becoming prohibitive for a greater number of companies, devising a unique and innovative way to more than double the capacity in next-generation devices is today a reality in the FPGA world. Today SSI technology

is being leveraged as a way to mix and match complementary types of dice on a single IC footprint to offer vast leaps forward in system performance, bill-of-materials (BoM) savings and power efficiency. Let's take a deeper look at Xilinx's SSI approach.

As die size gets larger, the yield goes down exponentially, so building large dice is quite difficult and very costly. With the SSI architecture a number of smaller dice can be built and then by using a silicon interposer to connect those smaller dice lying side-by-side on top of the interposer so they appear to be, and function as, one integrated die (see Figure 1).

Each of the dice is interconnected via layers in the silicon interposer in much the same way that discrete components are interconnected on the many layers of a printed-circuit board (see Figure 2). The die and silicon interposer layers connect by means of multiple microbumps.

With the SSI architecture, the various die on the device are connected through the passive silicon interposer and use through silicon vias (TSVs) and microbumps to further facilitate communications between regions of each die on the device as well as communication between the 3D IC and ultimately resources off-chip (see Figure 3).

All the packages that are chosen to be put into a device, still sit on the plane of the interposer. Data flows between the adjacent FPGA die across more than 10,000 routing connections. But instead of copper traces running across the motherboard from package to package, these configuration copper connections run through TSVs and past the interposer layer, where the vertical wiring is connected in a series of horizontal patterned layers. By moving all the connections outside the plane, device makers can place chips right next to one another, saving space and power. Using a passive silicon interposer rather than going with a system-in-package or multichip module configuration has huge advantages. In the SSI process regular silicon interconnect or metallization to connect up the dice on the device is used. Many more connections within the silicon can be used than with a system-in-package.

Within the passive silicon interposer over 10,000 user-programmable routing connections can be implemented between

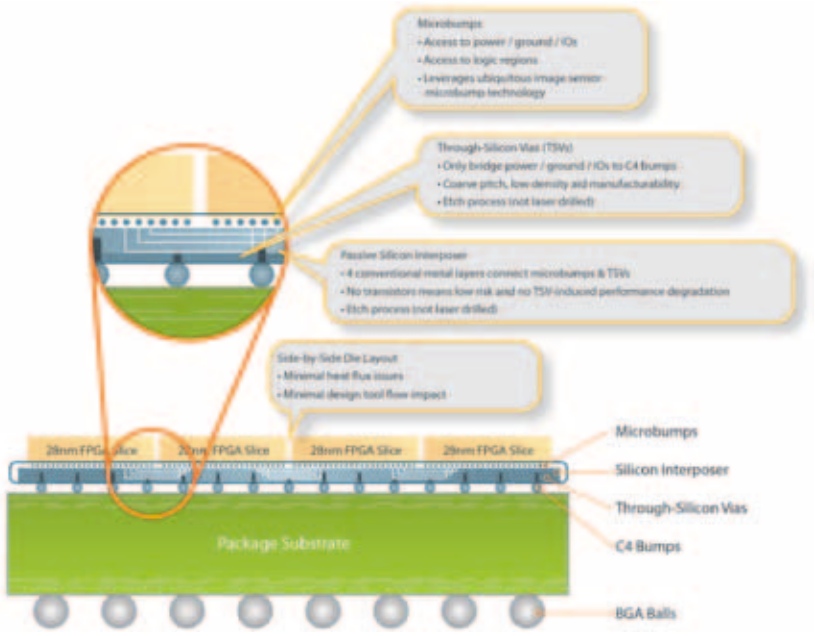


Figure 2. Stacked Silicon Interconnect Technology uses passive silicon-based interposers, microbumps and TSVs.

die to allow designers to configure the device for optimal use. Silicon is a better conductor than plastic PCB materials and facilitates a density of interconnect that simply can't be achieved with system-in-package or multi-chip modules.

The biggest advantage of the SSI technology approach however is power savings. Using chip interconnects to connect the dice is much more power efficient than connecting dice through big traces, through packages or through circuit boards. SSI technology provides more than 100 times the die-to-die connectivity bandwidth per watt, at one-fifth the latency, without consuming any high-speed serial or parallel I/O resources.

What's more, while the SSI technology offers some radical leaps forward in terms of capacity, Xilinx made sure the technology did not force a radical change in customer design methodologies. These FPGAs use a columnar architecture in which large logic regions on a given FPGA are divided into columns by long-wire connections. In creating the SSI

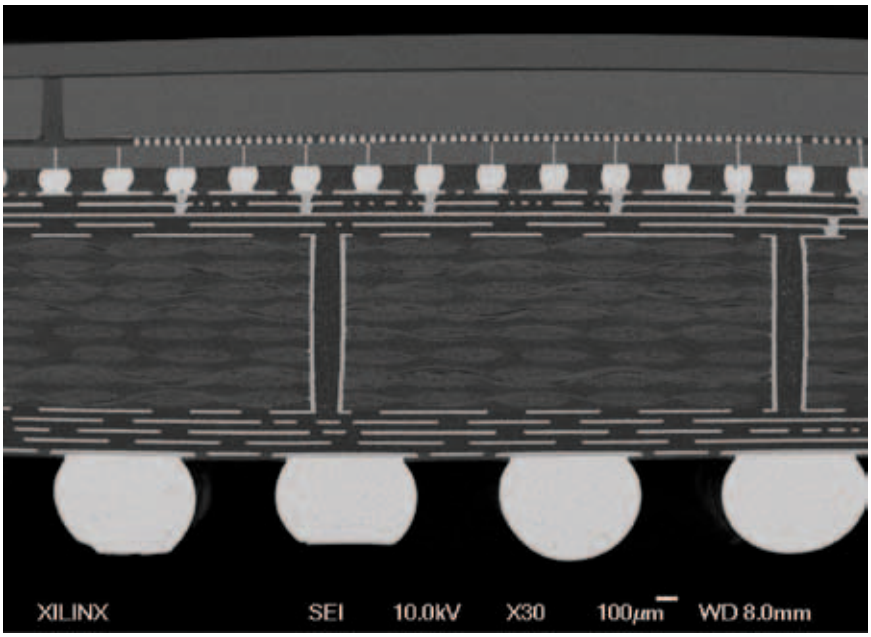


Figure 3. An actual cross-section of the 28-nm Virtex-7 FPGA. TSVs can be seen connecting the microbumps (dotted line, top) through the silicon interposer.

architecture, the edges of each SSI slice along these natural borders in the logic regions were defined where long-long wire connections would normally reside. Because the slices fall along these natural borders, design tools did not need to be radically modified. In fact, programming an All Programmable 3D IC is almost exactly like programming a very large monolithic device. Because 3D ICs are so large, floorplanning is requirement rather than a recommended step.

FPGA Design with SSI Technology

One of the many advantages afforded by SSI technology is the ability to treat it like a monolithic device. This is most important as partitioning a large design across multiple FPGAs presents a number of complicated design challenges that monolithic implementations avoid. The typical steps in a monolithic FPGA design flow include:

- Create a high-level description
- Synthesize into an RTL description that matches the hardware resources
- Perform physical place and route
- Estimate timing and adjust design for timing closure
- Generate a bitstream to program FPGA

When working with multiple FPGAs, the designer/team must take the additional step to partition the netlist across multiple FPGAs. Working with multiple netlists means opening and managing multiple projects, each with its own design file, IP libraries, constraint files, packaging information, etc.

Timing closure for multiple FPGA designs can also be very challenging. Calculating and accommodating propagation delays through the board to the other FPGAs poses new and complex problems. Likewise, debugging a design through multiple partial netlists in multiple FPGAs can be extremely complicated and difficult.

In contrast, when using FPGAs with SSI technology, the designer creates and manages a single design project; SSI technology routing is transparent to the user. The user performs a single design bring-up and debug with a standard timing closure flow.

The Challenges of Interconnecting Multiple FPGAs

Among its many advantages is the fact that 3D IC SSI technology solves the challenges that had previously obstructed attempts to combine the interconnect logic of two or more FPGAs to create a larger, "virtual FPGA" for implementing a complex design:

- The amount of available I/O is insufficient for connecting the complex networks of signals that must pass between FPGAs in a partitioned design and as well as connecting the FPGAs to the rest of the system
- The latency of signals passing between FPGAs limits performance
- Using standard device I/O to create logical connections between multiple FPGAs increases power consumption

Applications

FPGAs with SSI technology break through the limitations of monolithic FPGAs, extending their value in a wide variety of the most demanding applications. With the need for bandwidth exploding, the communications sector is frantically racing to establish new networks. The wireless industry is scrambling to produce equipment supporting 40-Gb/s data transfer today, while wired networking is deploying 100 Gb/s systems and architecting 400 Gb/s systems. By leveraging this SSI technology to combine an FPGA and a high-speed transceiver dice on a single IC, customers in the communications sector are creating a growing number of applications requiring high speed I/O.

SSI technology is being leveraged to offer Virtex-7 devices with a 28G capability, by offering the transceivers on a separate ASIC die. This allows optimization of 28-Gb/s transceiver performance and electrically isolates functions to offer an even higher degree of reliability for applications requiring cutting-edge transceiver performance and reliability.

Noise isolation becomes a very important parameter at 28-Gb/s signaling speeds because the FPGA fabric and transceivers are on separate dice, the sensitive 28-Gb/s analog circuitry is isolated from the digital FPGA circuits, providing superior isolation compared to monolithic implementations (see Figure 4).

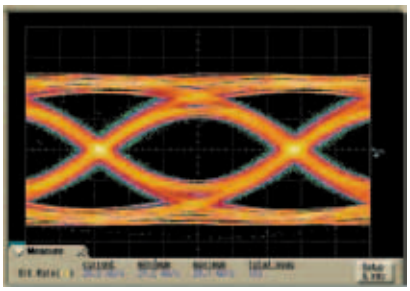


Figure 4. Xilinx 28-Gbps transceiver displays an excellent eye opening and jitter performance (using PRBS31 data pattern).

SSI Technology - Concept to Reality

As current scaling trends require enormous investments only affordable to a select few, Moore's Law is at its limit and 3D IC technology has become reality. 3D ICs are the natural evolution of the industry; it is the convergence of performance, power and portability. The economic and technical improvements in performance, power, form factor, time-to-market and cost drive the use of 3D system ICs. Six years of extensive research and development came to fruition with the announcement of the SSI technology in October 2010, and with the Virtex-7 2000T device, the world's highest capacity FPGA, which began shipping in October 2011, enabled by SSI technology. Xilinx is also now shipping the 7VX1140T and 7VH580T devices, also enabled by SSI technology.

The idea of 3D is not new. The known technologies have delivered the same benefits via scaling, which has delayed the need to transition to a new technology. However, with scaling beginning to slow and increasing demand for better performance at a lower power and cost, a change is needed now. Yet many companies do not see 3D becoming a mainstream technology for several more years. So what are the barriers to adoption and solutions that can help accelerate this process?

3D has moved into the mainstream, but, as still a relatively new technology, it is not surprising that there are technical and non-technical barriers that exist. Technical barriers include a lack of commercial EDA tool support, modeling, thermal dissipation, testing and standards. Non-technical barriers consist of cost, markets, a mature business model and supply chain, yield ownership and risk. Potential solutions can be many, but Xilinx is already delivering and extending the value and usage of 3D ICs. ◆

The Wafer Level Fan-Out Package – WFOP™

Tomoko Takahashi, Advanced Packaging Specialist and
Akio Katsumata, General Manager
J-Devices Corporation, Packaging Research & Development Center

J-DEVICES IS DEVELOPING A NEW package structure and technology for the next generation of WLP, the Wafer level Fan-Out Package – WFOP™. One of the face-down mounting styles, WFOP™ uses a metal plate, e.g. stainless and copper, as the base plate of its redistributed interconnection layer. The redistribution traces can fan out of dies, so that the pin count is not limited by die size as in the case of WLP. The redistributed layer is fabricated by the semi-additive method of copper plating. Manufacturing in large scale panel style substrate, a higher throughput than the conventional wafer style manufacturing method can be achieved. Moreover, WFOP™ has several additional benefits, including an ultra thin package, excellent thermal characteristics and reduced noise level provided by a metal plate. This article will report its package structure, process flow, design rules, and package characteristics.

Recently, the smart device market has been dominating the electric device business. Smart devices, such as mobile phones, tablets of various sizes, and e-readers, have multiple features and functions, e.g. imaging, data processing, 3D graphic engines, MPEG engines, cameras, RF, TV and so on. Various system LSI, memories and components are used for those devices. Demands on semiconductor packages are miniaturization, high wiring density, and thinness. Packages, of course, are required to achieve high speed electrical transmission, lower thermal resistance and multi-function capability.

For all those demands, several fan-out packages are being developed at several companies and institutes. But there are some technical issues. First off, the embedded dies in the mold resin shift their positions because heat processes shrink the resin, and the alignment accuracy of wire bonding or interconnect redistribution is therefore limited. In addition, in embedded packages, dies are covered by resin, so the heat generated by the devices cannot dissipate efficiently. In fan-in packages, the body size depends on the die size, so its design rule is not very flexible.

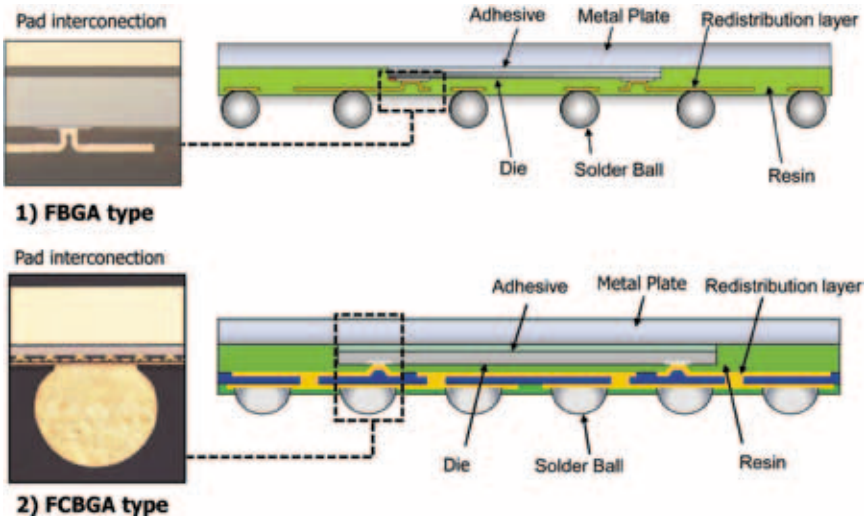


Figure 1. WFOP™ cross section.

J-Devices' new type of embedded package, WFOP™, can overcome these issues. It has highly accurate die placement, lower thermal resistance and is capable of placing balls outside of the die.

The Structure of WFOP™

Figure 1 shows the cross section of the structure and Figure 2 shows the top view of the WFOP™ distribution layer. The package is one of the face-down mounting styles, which uses a metal plate like stainless or copper as the base plate of the redistributed interconnection layer. The dies are mounted on the metal plate, and the resin between the dies acts as a stress buffer and insulator for the interconnections. The redistribution layer is fabricated by the semi-additive method of copper plating. In Figure 2 the contacts between the die pads and distributed layer are leaded, but there is also a via contact option for area pads. The solder resist is formed on the interconnection layer and the balls are placed on the solder resist.

Process Flow

First, dies are attached on the metal plate. The actual placement accuracy is less than +/-5μm. After that, the resin is laminated as an insulator for the redistribution layer. Openings are made in the resin in the area of die pads. Next, using the plating method, traces are formed on the resin layer. The solder resist is laminated on the resin and the traces, and patterned for solder balls, and the balls are placed on it. Finally, the metal plate is singulated into packages by dicing, and the WFOP™ units are complete.

Figure 3 shows the image of a chip array on a 320mm square metal plate using the WFOP™ process. In the process flow

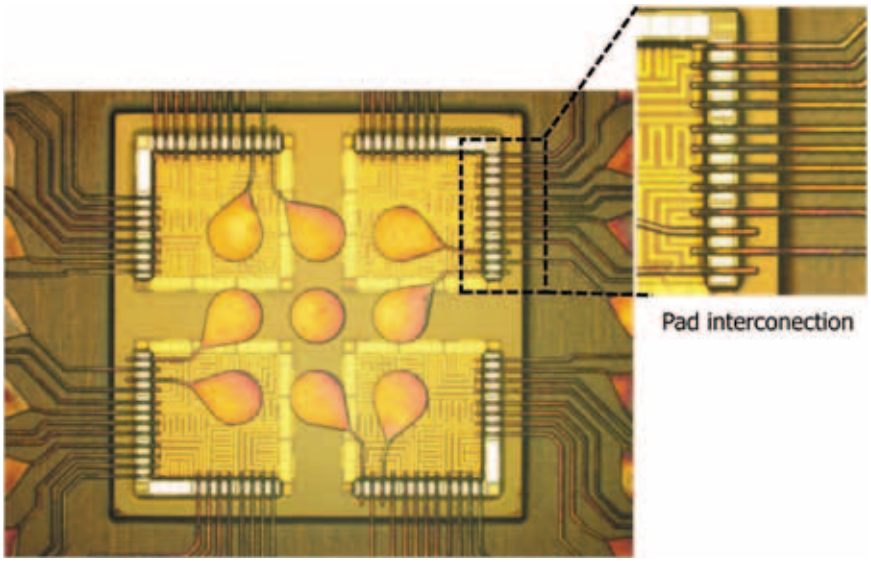


Figure 2. WFOP™ top view (redistribution traces).

of WFOP™, the size of the metal plate is not limited because the process starts with placing dies on it and redistributing wires. In other words, those packages can be fabricated not only by wafer scale, but also by panel scale. This means higher throughput will be achieved by the advantage of scale.

Design Rules

Table 1 shows the value of some design specifications. There are two options for the die pad array. In the case of the peripheral pad array, the current minimum pitch is 50μm, and we connect redistribution traces and die pads as shown in Figure 2. In the case of area pad array, today's minimum pitch is 150μm and we create 30μm via holes in the pads.

In Figure 2 there is only one trace layer, but in 2012 prototype samples with two layers were developed. To expand design capability, J-Devices will prepare four layers for routing as a standard line-up in the near future. One of WFOP™'s benefits is its thickness. As you can see in Table 1, WFOP™ is in fact ultra thin. Figure 4 is the actual comparison of package thickness between the C4 type FCBGA and the WFOP™ type FCBGA. WFOP™ achieved a 50μm die thickness, no core, no bumps and fewer build-up layers, so that it resulted in such a difference in thickness.

Item	Design specifications	
	Peripheral Pad	Area Pad
Line width	20µm	
Line space	20µm	
Pad pitch	50µm	150µm
Via land diameter on pad	-	86µm
Via diameter on pad	-	30µm
Via land diameter on RDL	86µm	
Via diameter on RDL	30µm	
Via land -line space	20µm	
Ball land - line space	20µm	
Ball land – via land space (Same NET)	0µm	
Ball land – via land space (Different NET)	20µm	
Package outline – resist space	50µm	
Resist – Copper pattern space	50µm	

Ball pitch	Ball land diameter	Resist opening diameter	Package height	Stand off
No Ball	-	-	445µm TYP	-
0.80mm	530µm	380µm	845µm TYP	400µm
0.65mm	480µm	350µm	775µm TYP	330µm
0.50mm	350µm	230µm	695µm TYP	250µm
0.40mm	290µm	220µm	645µm TYP	200µm

Table 1. Design specifications.

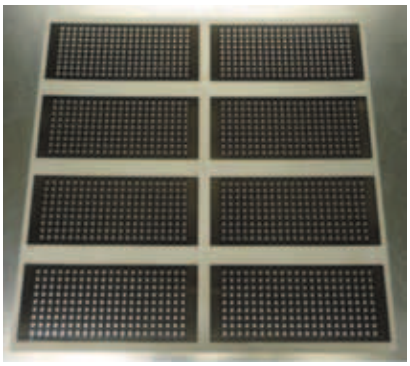


Figure 3. WFOP™ on 320mm sq. panel.

Package Characteristics

Figure 5 shows the simulation result of thermal resistance to compare WFOP™ and wire bonding type PTFBGA. Generally, the smaller the die size, the higher the thermal resistance. But in all die sizes, the thermal resistance of WFOP™ is lower than that of PTFBGA by 15% to 40%. The temperature contour diagram in Figure 5 shows that more heat cannot spread on the die in PTFBGA. This means that the metal plate in WFOP™ functions as an effective heat spreader.

Figure 6 shows the electromagnet interference (EMI) test method and its results. The models were PFBGA, standard WFOP™, and WFOP™ with a grounded metal lid. Compared to PFBGA, the output power noise of standard WFOP™ is lower by 10dB, and of WFOP™ with a grounded lid by 25dB. The result can be explained by noting that the metal plate in the WFOP™ works effectively as a noise shield, even though the metal plate is a floating node. In the case of grounded metal plates, it works even better.

Conclusions

In this article the WFOP™, a new embedded wafer level package structure and fabrication technology was introduced. This structure is a promising solution for a thinner package with more traces, lower thermal resistance and better electrical characteristics. J-Devices is planning to have two types of WFOP™ package lines. One is the FBGA. Its package size will be around 3-10 square millimeters with a peripheral pads array of 40-50μm pad pitch. WFOP™'s lower thermal resistance will please users. Possible applications are CPU and MPU peripherals in smart devices. The other type of WFOP™ is FCBGA such as CPU and MPU. The package size will be around 20-40 square millimeters with an area pads array of 120-150 pad pitch. The thickness and cost will be great benefits in this area.

J-Devices is planning to expand this technology to future packages. The plan includes 3D packages, such as multiple dies, stack dies and POP. Also considering less EMI of WFOP™, it will be a promising solution for RF.

It is expected that WFOP™ will become one of the leading packaging technologies for the next generation. ◆

Acknowledgments: The authors deeply appreciate support by the staff in cooperating companies on development of WFOP™.

AKIO KATSUMATA is the General Manager of the Packaging Research & Development Center at J-Devices Corporation. He previously spent 23 years at Toshiba Corporation as a development researcher on semiconductor package design and new package development after graduating from Chiba University in Japan. He holds 13 US Patents granted and 4 US Patents pending. He joined J-Devices in 2009.

TOMOKO TAKAHASHI is an Advanced Packaging Specialist for the Packaging Research & Development Center at J-Devices Corporation. She got her master's degree in physics and graduated from Osaka University in 1995. After that, she spent 14 years at Toshiba Corporation as a process coordinator and development researcher on semiconductor packages. She holds 1 US patent granted and 4 US patents filed. She joined J-Devices in 2009.

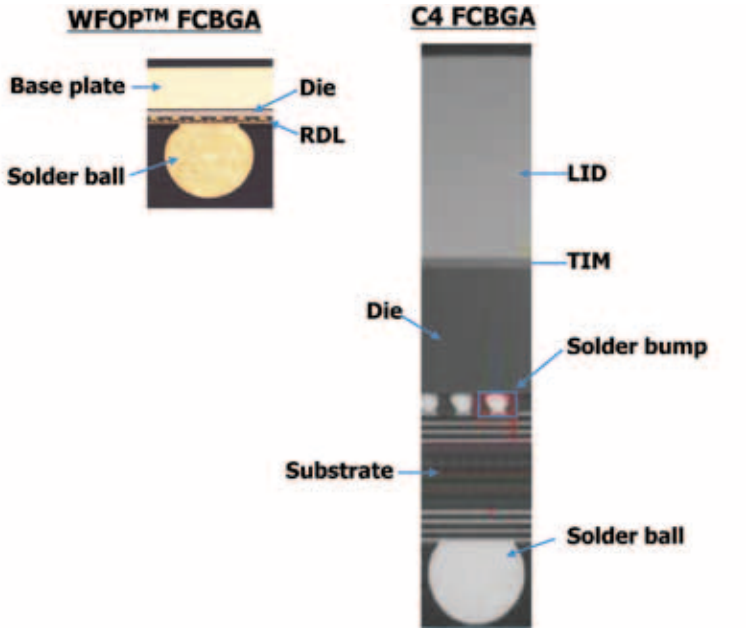


Figure 4. Comparison of package thickness – WFOP™ vs. C4 FCBGA.

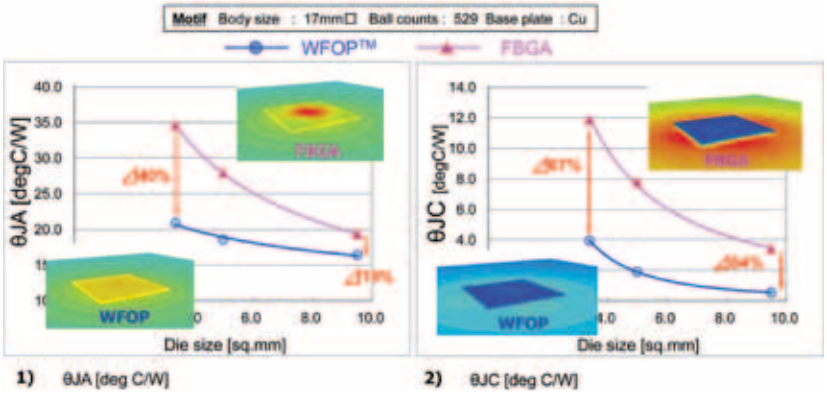


Figure 5. Comparison of thermal resistance – WFOP™ vs. FBGA.

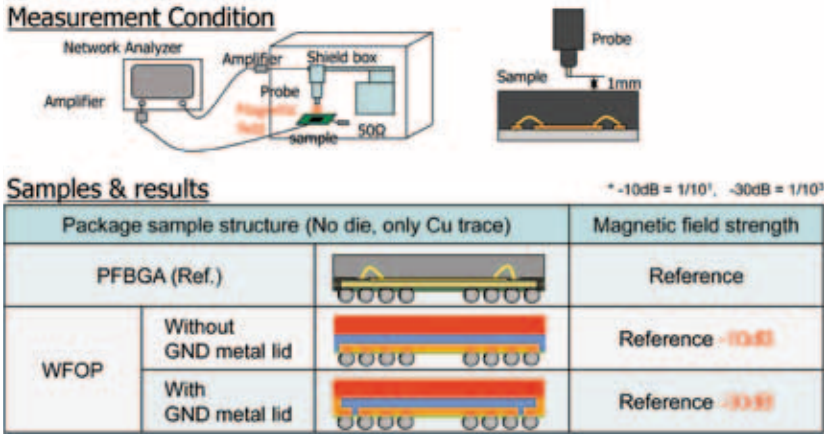


Figure 6. Comparison of EMI – WFOP™ vs. FBGA.

IPC®

May 20–23, 2013
The New Tropicana
Las Vegas, Nevada
www.ipc.org/ESTC

ESTC

Electronic System Technologies Conference & Exhibition

IPC ESTC will offer 13 tracks covering:

- Product Design and Development
- Assembly and SMT
- PCB Fabrication, Materials and Design
- Quality and Reliability
- Fab and Silicon
- Test
- Equipment, Tools and Modules
- Packaging and Substrates
- Mechanics
- Thermals
- Electrical
- Materials
- Industry Analysis and Issues

Bringing the entire electronics industry together

• foundry • components • board assemblies • complete systems

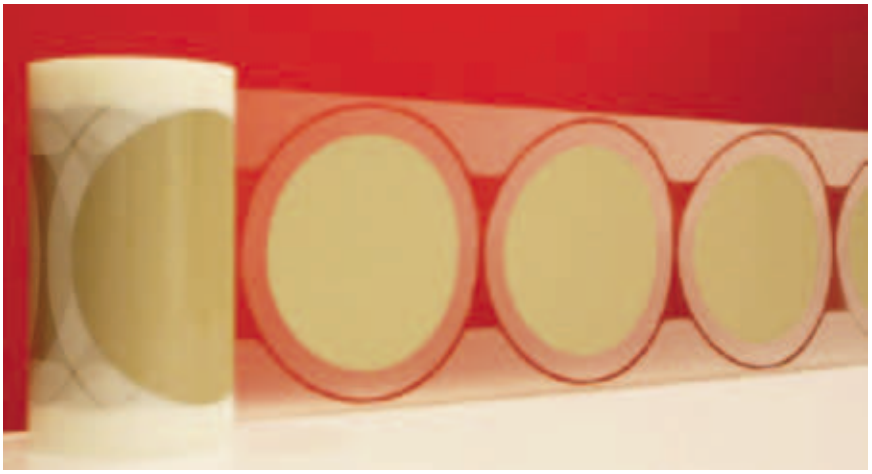
www.ipc.org/ESTC

Groundbreaking Conductive Die Attach Film Takes Thin Die Processing to a New Level

Shashi Gupta and Howard Yun
Henkel Electronic Materials, LLC

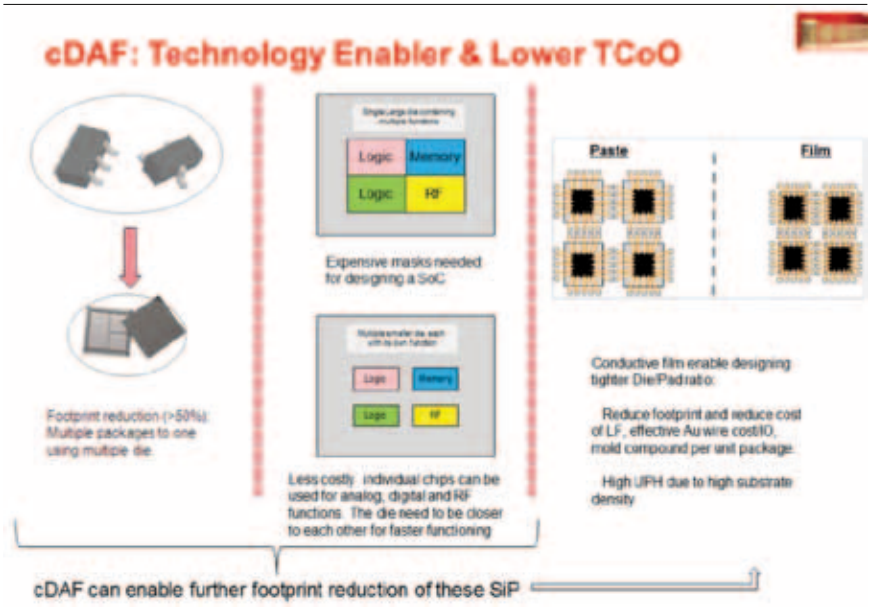
SEMICONDUCTOR PACKAGES continue to add even more functionality to ever-thinner devices and meeting these demands requires solutions that allow for robust processing of thinner, smaller, higher density packages. Central to progressing device miniaturization are the materials used to build today's ultra-small semiconductor devices. This goes not only for laminate-based (non-conductive) devices, but for leadframe (conductive) applications as well – the miniaturization trend extends to multiple package types. Manufacturers of laminate-based packages have long relied on die attach film technology to enable incorporation of much thinner die and to ensure consistent, uniform bondlines with no die tilt. But, this same technology has been unavailable for conductive applications until recently.

When Henkel introduced the first-ever conductive die attach film materials two years ago it was, indeed, welcome news for the semiconductor packaging market. LOCTITE ABLESTIK C100 debuted to widespread validation, with major semiconductor device manufacturers publicly stating the advantages of the material's ability to enable package scalability. With a viable alternative to traditional paste-based die attach materials, leadframe device specialists could now capitalize on the inherent benefits of film-based mediums – namely, the ability to incorporate thinner wafers, realize uniform bondlines and integrate more die per package due to the tighter die to pad clearance afforded by film. Originally available in roll format, where both the die attach film and dicing tape are laminated onto the wafer in two separate lamination processes, Henkel has now extended the portfolio to also include a pre-cut version of the breakthrough conductive film technology that is ideal for use with ultra-thin wafers.



LOCTITE ABLESTIK CDF 200P is the latest innovation from Henkel's expert materials development team. A two-in-one, pre-cut conductive die attach film, LOCTITE ABLESTIK CDF 200P combines dicing tape and die attach material into single, pre-cut 6" or 8" wafer-sized film formats for easy application. Compatible with lamination equipment commonly used in the field, LOCTITE ABLESTIK CDF 200P requires no capital equipment investment, as it has been specifically designed for equipment adaptability. With a lami-

continued on page 36



World's First!

LOCTITE ABLESTIK CDF 200P

LOCTITE ABLESTIK CDF 200P is the world's first conductive dicing die attach film (2-in-1, precut format) designed for semiconductor packaging.

LOCTITE ABLESTIK CDF 200P is an innovative material developed to be both electrically and thermally conductive, and it can be used for a wide range of die sizes from 0.2 mm x 0.2 mm to 5.0 mm x 5.0 mm. It can be applied to various wafer metallizations (such as bare Si, TiNiAg and Au) and also on various leadframe finishes (NiPdAu, Ag Spot or Cu). LOCTITE ABLESTIK CDF 200P enables the miniaturization of packages while providing a clean and robust process, leading to a more reliable package.

New Aqueous-developable Dielectric Offers Multi-stack Capability with Reliability

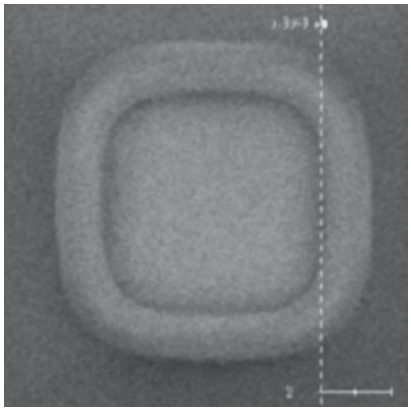
Richard Chen
Dow Electronic Materials

THE DEMAND FOR SMALLER, thinner and more powerful mobile devices with increased and more integrated functionality is a central driver for advanced semiconductor packaging designs. Consumers are demanding a wide variety of functions in a single device and the traditional lines between mobility and computing power have been blurred. Devices such as smartphones, tablets and ultrabooks offer much of the same functionality delivered in different form.

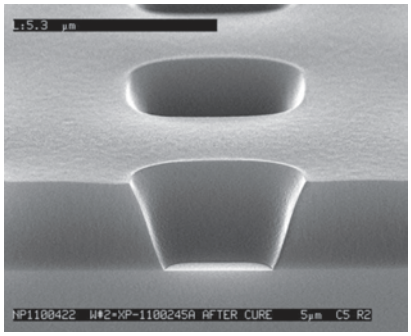
Whatever the form it comes in, the need for more power, speed and function in a smaller footprint poses a fundamental challenge – meeting these consumer demands while delivering reliable devices at affordable prices. The complexities of advanced packaging schemes have increased dramatically and materials play an important role in the success or failure of a device. And, clearly, a material's performance is measured not only on its individual merits but also on how well it or its processing impacts adjacent materials.

Inherent in the latest packaging schemes is a high density of structures and the need for higher speed interconnectivity, which require the use of redistribution layers to re-route I/Os for wafer level chip scale packaging (WLCSP), system-in-package, 3D packaging, and others. The need for permanent dielectrics to electrically isolate these copper redistribution layers comes with its challenges. Dielectric materials must process without impacting surrounding layers and they must maintain their integrity during subsequent processing.

To meet the need for an aqueous-base developable version of its benzocyclobutene (BCB) chemistry, Dow Electronic Materials is offering CYCLOTENE™ 6500 Photodielectric. This positive-tone material for i-line and broadband exposure is capable of imaging features as small as 3 μm vias with either a mask aligner or i-line stepper. Because the material is not cross-linked when exposed, CYCLOTENE 6500 Photodielectric is capable of high-resolution images with repeatability, and it delivers superior aerial image quality. Additionally, the chemistry is advantageous for manipulating the sidewalls of the features through the bake process, providing users the ability to control the profile to obtain desired slope or straightness. Using standard lithographic processing, desired features can be achieved without the need for a plasma step or other related steps.



1:2 pitch 5 µm Via at 5 µm film thickness, post cure (top view).



1:2 pitch 5 µm Vias at 5 µm film thickness, post cure.

Processing with an aqueous-base developable photodielectric has its advantages from a cost perspective. Because CYCLOTENE 6500 Photodielectric can use common drain lines and equipment used for photoresist processing, the material has a lower cost of ownership versus competitive materials. It also eliminates the need for solvent develop processing and maintaining separate systems.

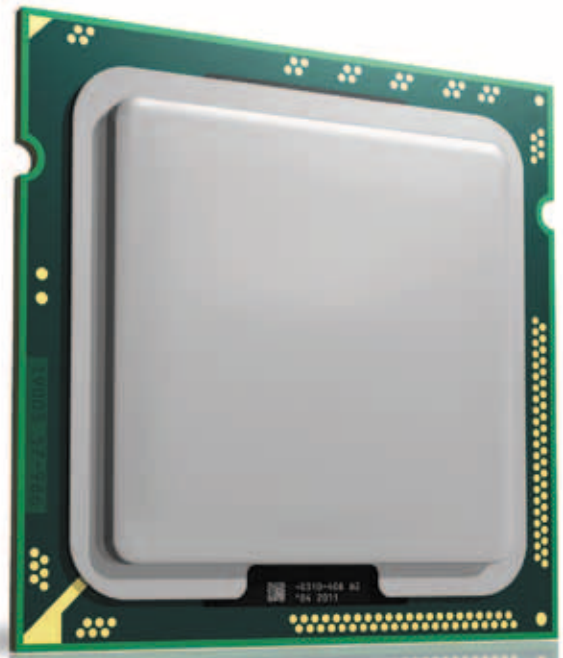
CYCLOTENE 6500 Photodielectric is also an ideal material to be used in redistribution layers because it has minimal impact on other materials. Most notably, the material has a low-temperature cure with a range between 180-210°C, and it exhibits a smooth surface with no residues post cure while meeting customers' requirement for low-thermal budget materials. In addition, CYCLOTENE 6500 Photodielectric does not outgas during processing, which could potentially cause reliability issues or failure. Consequences of dielectric outgassing include impact or damage to adjacent materials and delamination during the bonding step or early failure.

Despite its minimal impact of adjacent materials, CYCLOTENE 6500 Photodielectric provides excellent adhesion on many widely used substrates, including Si, SiO_2, Si_3N_4, Cu, BCB and organic polymers, and this adhesion is maintained during subsequent processing. The material is resistant to chemical attack by common solvents and removers used for packaging applications. Additionally, CYCLOTENE 6500 Photodielectric has good thermal stability up to 350°C if needed. This stability is particularly beneficial if the material is subjected to subsequent processing that is heat intensive, such as CVD deposition of barrier layers, solder reflow and copper-copper bonding. These characteristics are critical to eliminating delamination failure, which can potentially lead to failure of the package. Finally, copper migration into CYCLOTENE 6500 Photodielectric is very low, which is exceptionally critical given the need for the material to maintain its insulating integrity within the copper redistribution layer structures. The material has industry-leading copper drift values for polymers used in dielectric applications.

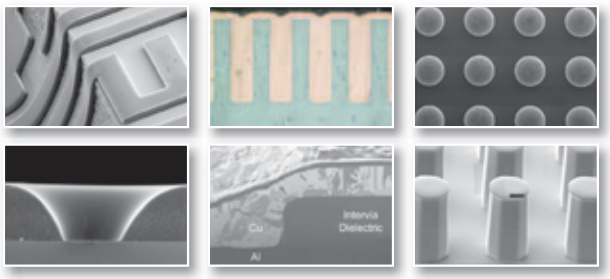
CYCLOTENE 6500 Photodielectric's properties also make the material ideal for multi-stack builds. Not only does the material bond well to other layers of CYCLOTENE 6500 Photodielectric, but also it is capable of bonding other substrates, such as Si to Si and Si to glass. From a reliability standpoint, the material's lower cure temperature capability results in reduced film stress – approximately 28 MPa.

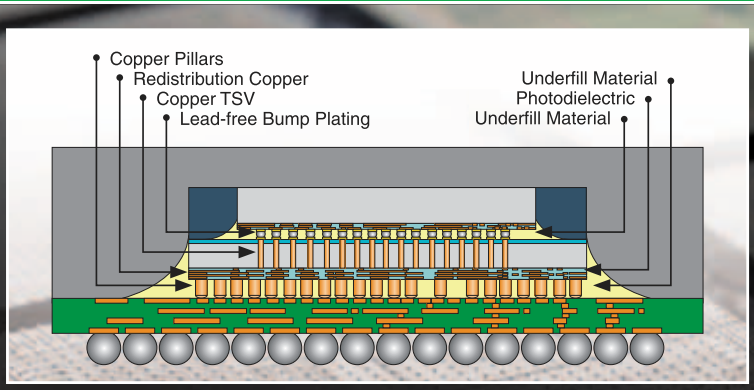
For packaging fabs looking for a cost-effective photodielectric for redistribution layers that performs reliably and has excellent resolution with smooth, residue-free features, CYCLOTENE 6500 Photodielectric may be the ideal choice. For information regarding this material or any of Dow's advanced packaging materials, visit www.dow.com or call 508-481-7950. ◆

With Innovation Comes Revolution



Leading-edge packaging schemes are spurring a revolution in electronics. Dow Electronic Materials is there with a wide range of innovative metallization, dielectric, lithography and assembly materials – all delivered with global support from technical labs positioned close to customers. These are the innovations that drive the revolution.





DOW® Electronic Materials

www.dow.com

Henkel News

continued from page 32

nation temperature requirement of 65°C, Henkel's conductive film complies with most existing equipment and processes for both lamination and backgrinding. (For manufacturers that may need to invest in lamination equipment for pre-cut films, there are multiple pre-cut lamination platforms from which to select.) Because of its unique two-in-one format, LOCTITE ABLESTIK CDF 200P streamlines manufacturing by facilitating an in-line process (backgrinding and lamination) for thin and ultra-thin wafers and also allows for a single lamination process in one, combined step.

Flexibility and extreme capability is at the heart of Henkel's latest conductive die attach film. Proven effective on a wide range of die sizes (from 0.2mm x 0.2mm to 5.0mm x 5.0mm currently and a 9.0mm x 9.0mm capable formula in development), a variety of wafer metallizations including bare silicon, TiNiAg and Au, and multiple leadframe metallizations such as Cu, Ag or Au, LOCTITE ABLESTIK CDF 200P offers superior process adaptability. Not only can the material manage such a wide die range, but its effectiveness has now been proven on die as thin as 50μm! Internal testing confirms LOCTITE ABLESTIK CDF 200P's ability to achieve lamination, dicing, pick-up and die bond processing on 50μm thick wafers with die sizes ranging from 0.2mm x 0.2mm to 2.0mm x 2.0mm. And,

Henkel's not stopping there: the company is currently testing the new material's capability on 50μm thin 9.0mm x 9.0mm die, as well as its laser dicing performance. Results of these evaluations are expected by year-end.

Not only are these new materials process-friendly, they also offer all of the advantages of film technology. Henkel's portfolio of conductive die attach films provide greater design leverage by allowing tighter clearance between the die and the die pad due to the elimination of the fillet. This means that packaging designers can incorporate more die and/or more functionality into a single package. With no fillet and higher density chip designs, packaging specialist can also lower costs because the amount of gold wire, substrate and mold compound required per unit package is significantly reduced. As compared to alternative materials, LOCTITE ABLESTIK CDF 200P's total cost of ownership (TCoO) is measurably lower.

Henkel's portfolio of conductive die attach films – both LOCTITE ABLESTIK C100 in roll format and LOCTITE ABLESTIK CDF 200P in pre-cut, two-in-one format – are set to accelerate effective implementation of highly miniaturized, multi-die device designs which are simply unachievable with paste- or liquid-based mediums.

To find out more about Henkel's line of conductive die attach film materials, log onto www.henkel.com/electronics, send an e-mail to electronics@henkel.com or call 1-888-943-6535 in the Americas, +44 1442 278 000 in Europe and +86 21 3898 4800 in Asia. ◆

continued from page 38

ness Times, China invested $47 billion in renewable energy projects in 2010. The majority is solar. According to *Forbes*, that number increased to $52 billion in 2011. That does not necessarily make those businesses successful. Per *Forbes*, China's four largest solar manufacturers lost a combined $1.7 billion in 2011. The Chinese government will most likely continue to keep the larger companies afloat to maintain the employment and avoid the social unrest that could result from shut-downs and layoffs. I guess they can continue doing that via the very beneficial trade balance of payment resulting from building all our "i-stuff". Maybe not.

Solyndra, of Fremont, California, has become the political poster-child for U.S. solar power and U.S. government investment. The $500 million DOE loan to Solyndra is quite modest. According to *Forbes* and Mercon Capital Group, state owned Chinese banks agreed to loan $41 billion to Chinese solar companies since last year. My personal opinion is that if the government wants to be in the venture capital business, it should expect to win some and lose some, as does any VC company. I also believe the U.S. government should be in the VC business for strategic programs and technologies. May I mention programs such as Gemini, Apollo, Mars' Rovers? Isn't this VC at its best? Do we doubt the benefits that endure decades later? I am not comparing NASA to a terrestrial solar project, although the latter is probably indebted to the former. Maybe the U.S. DOE could have done better due diligence as to how Solyndra spent the $500 million. Constructing a new, custom $200 million building, a mile away from an empty, 5 million square foot NUMMI plant, may not have been the best investment. Commercial VC companies usually exercise better due diligence over how their investments are spent, but not always. Tesla Motors got the right idea, occupying a portion of NUMMI for a minimal cost.

Aside from the choice of building, the Solyndra case is a good lesson in design for manufacturing (DFM) or not designing for manufacturing. The Solyndra product is a brilliant design, maximizing power conversion efficiency for a fixed panel installation. I shall not explain the technology. BUT, it was totally unique. It required a number of custom, multi-million dollar manufacturing machines. There was virtually no supporting industry infrastructure. There were no second source opportunities. That equates to higher costs. The IP may have lost to volume, but in this case, I don't believe the odds were ever very good.

Amonix has received no government funding for its commercial operations, such as Alamosa. There are tax incentives in the renewable energy business. Oil companies receive tax incentives for capital investment and research.

In the utility scale power business, logistics of final system (tracker) assembly is also a cost factor. For example, each Amonix system is 105 feet x 45 feet, and ships in seven 15 foot x 45 foot sections. A central contract manufacturing operation final-assembled systems for installations in the U.S. Southwest. For new commercial projects outside of the U.S., the company is researching those sites and local tracker manufacturing options. Package manufacturing has been moved from a U.S. (EMS) contract manufacturing partner to a prominent (OSAT) semiconductor assembly company in Malaysia. This is a more synergistic match of process expertise as well as a cost improvement.

For those of us from the semiconductor industry, cost competition is not foreign ground. In energy and renewable energy, there is global competition, technology competition (solar flavors, wind, hydro, geothermal), and let's not forget good old fossil fuels. Thanks to hydraulic fracturing (fracking) extraction, the U.S. now has 100 years worth of (low cost) natural gas. With the new supplies of U.S. shale natural gas and Canadian shale oil, North America can potentially become energy independent by 2025 or thereabouts. Of course, the renewables provide a better solution to reduce carbon footprints and global warming. Our coastlines are threatened to recede a few miles in the worst case. In the best case, there will still be more coastal flooding during *the 25-year* and *50-year storms*. We may be coining terms with fewer years. Statistically, nuclear energy can be competitive but suffers from the meltdown scenario, and the possibility that global warming may flood the seaside reactors (where most reside).

In the U.S., the PV installation business is thriving. This is a time and materials business, and the materials are low cost, i.e., below cost, Chinese PV panels. Solar City, of San Mateo, California had a successful IPO in 2012. A new tariff may sober this business segment somewhat.

Renewable power is not always available 24x7. The sun is not always shining and the wind is not always blowing. Energy grids must adjust and balance the load vs. supply between renewable and conventional power sources.

I believe the PV and CPV industry, like the MEMS industry in past years, suffers from too many suppliers competing for too small a market, making ambitious assumptions on rate of market growth. For CPV, in particular, lacking an industry infrastructure to lean on, many suppliers build totally integrated manufacturing operations, believing the forecasted higher volumes will eventually underwrite all the capital investment. Semiconductor start-ups don't currently think this way, but there are huge resources of contract fab and assembly-test infrastructure. The PV market is further along in establishing that infrastructure. The global installed PV base is about 66 gigawatts, per Navigant Consulting, vs. less than 200 megawatts for CPV. How can CPV move to a shared infrastructure model? Will CPV compete on volume, as PV currently does (albeit in a distorted way), or can CPV providers compete on intellectual property and power efficiency? Can standardization reduce costs, without sacrificing differentiation? Ultimately, we still have to deliver more watts for the dollar, more power output per acre. The technology IP will be driven by the cell, the optics, the tracking algorithm, and alignment mechanics. Can a company be successful owning one, two, or three out of the four, and using industry infrastructure?

In CPV, there are a number of supporting hardware infrastructure industries starting to develop. I see this as a positive direction for the entire industry and affording more options to success. ◆

Comments? Email bcooper@meptec.org.

Personal Observations in the (CPV) Solar Business

Joel J. Camarda
Sr. Director, CPV Receiver Manufacturing & Process Technology
Amonix Inc.

LET ME PREFACE THIS ARTICLE with some qualifying statements. I am not a spokesman for Amonix. The views expressed herein are my personal observations and opinions. Hence, we call this an *opinion*. I do not claim to be a solar expert. As most MEPTEC members know, I am a *semiconductor guy*. My expertise is semiconductor manufacturing, operations, process technologies, and package design. At Amonix, my responsibilities lie within the semiconductor section of that business, wafer fab through packaging and package test. We call the packaged photocell a *receiver*.

That said, Amonix is the #1 global CPV (concentrated photovoltaics) system supplier, based on installed megawatts. The solar power business, as we know, has become somewhat controversial, and somewhat political, at least in the U.S.

Within the solar power business, there are competing technologies as illustrated in Figure 1. The market is currently dominated by monocrystaline and polycrystalline silicon, categorized as PV. HCPV (high concentration PV) or CPV, uses a series of lenses, reflectors, or mirrors to concentrate the incoming sunlight, typically 300X to 1000X, onto the photocell. This requires direct, focused light onto the cell, facilitated by dual-axis tracking systems, to follow the sun during the course of the day. Somewhat more complicated than fixed panels. The net objective for CPV is to be the lowest LCOE* (levelized cost of energy) among the solar alternatives, i.e. more energy per acre. According to IMS Research, as reported in *PC Tech*, CPV could be 30% cheaper than PV by 2016. The CPV

Figure 1. Comparison of efficiencies across the solar landscape. Source: Amonix Inc.

Note: Amonix has demonstrated efficiency improvements beyond these figures above.

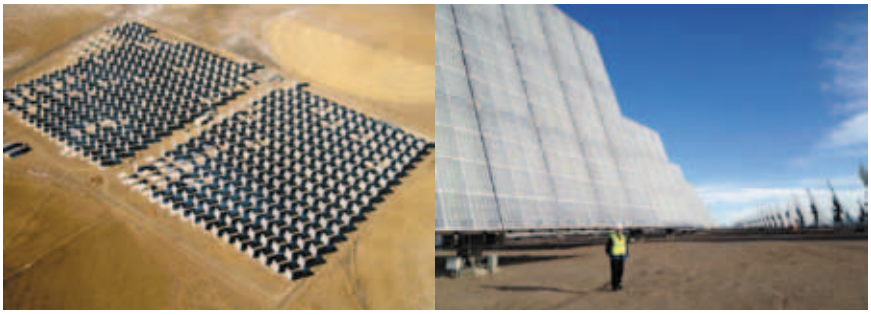
advantage works best in industrial scale, i.e. utility power plants. Currently, CPV is still only a very small share of the total solar market, less than one percent, but growing.

The advantage of CPV is best in hot, dry climates. A high DNI (direct normal irradiance) factor is required. Globally that translates to the U.S. Southwest, Mexico, Middle East North Africa (MENA), Southern Europe, South Africa, parts of India, China, and Australia. There are CPV initiatives in all of these zones. The governments of China and Saudi Arabia are committed to new gigawatt level solar programs, which may include mixed technology solutions.

The world's largest CPV power plant is currently the Amonix installation in Alamosa, Colorado completed in 2012. The plant produces 30 megawatts and can power 6,500 homes. The operation is visually impressive – 504 systems on 200 acres.

We all know China has grown to a dominant position in PV. The reason is not superior technology or low cost labor. Low cost labor does help. The predominant reason is extraordinary government investment and loans by government owned banks. *ZEENEWS.com* has quoted Jonathan Silver, U.S. DOE Executive Director, addressing U.S. Congress, stating that the Chinese solar energy budget is 20X greater than the U.S. According to the *International Busi-*

continued on page 37



Alamosa, Colorado

The industry journal, *Solar Server* magazine, named Alamosa the *Solar Energy System of the Month*, November, 2012. *ENR (Engineering News Record)* named Alamosa as a *Best Project of 2012*. The editors of *Power Engineering* magazine, *RenewableEnergyWorld.com* and PennWell (publishing) Corp. have included Alamosa among the 15 overall finalists for the annual *Projects of the Year Awards* program, and among the 2 finalists for the Best Solar Project.

* NREL (National Renewable Energy Laboratory) has developed a LCOE calculator for utility scale and distributed renewable energy. The model compares capital costs, operations and maintenance, performance, and fuel costs.

Copper Pillar µBumps

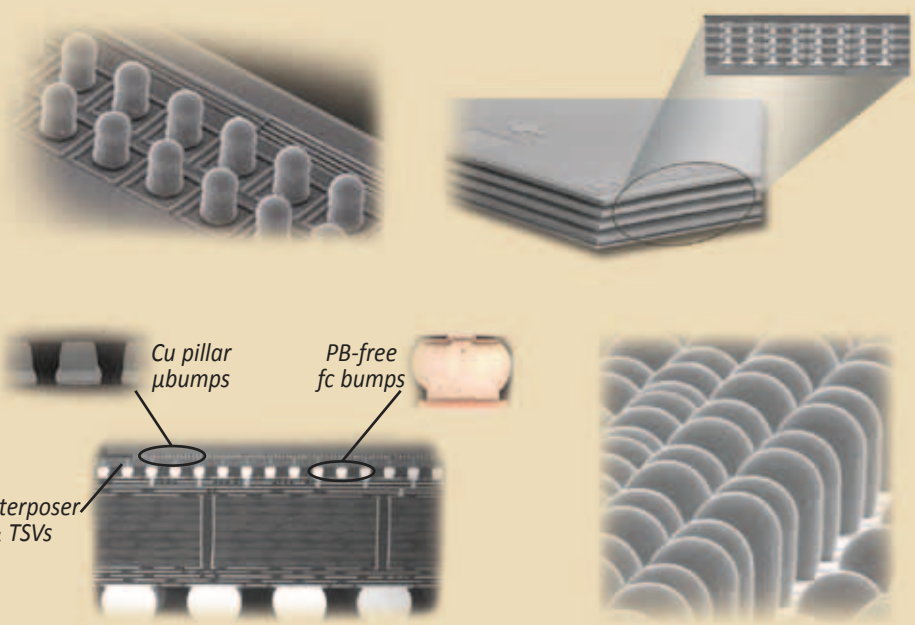
Platform Provides:

- Lower cost system packaging
- Ultra-fine pitch, ultra-thin die
- 28nm node
- Controlled stress for ULK
- 2.5/3D Through Silicon Via (TSV) enablement
- Enhanced electromigration resistance
- Superior thermal performance
- Pb-free / Low alpha solution
- High manufacturing throughput

With proven reliability in volume manufacturing!
Bump • Assembly • Test

Amkor Technology®

Copper Pillar µBumps

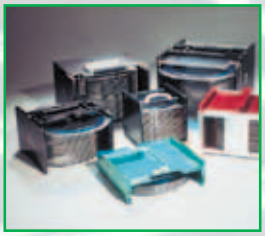


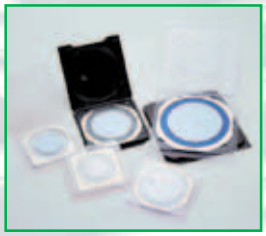
VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

www.amkor.com

Magazines and Carriers for Process Handling Solutions


Film Frames

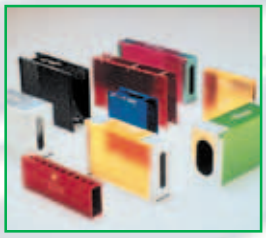

Film Frame Magazines


Film Frame Shippers


Grip Rings

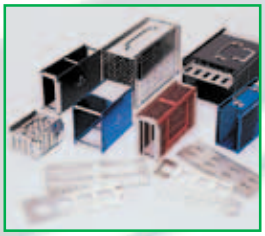

Grip Ring Magazines

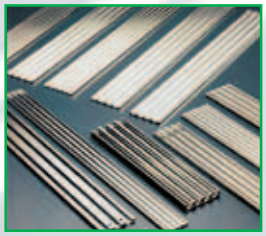

Grip Ring Shippers

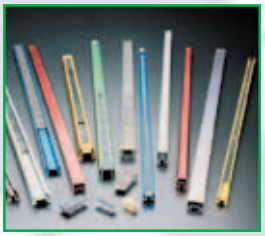

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.

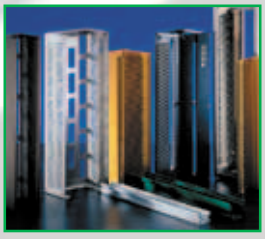

Process Carriers (Boats)

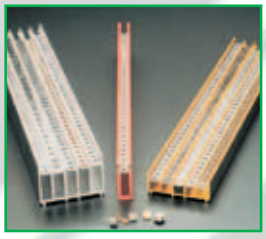

Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails


Miscellaneous Magazines


Substrate Carrier Magazines


TO Tapes & Magazines


Wafer Carriers

Accept Nothing Less.

Perfection

Perfection Products Inc.
1320 S. Indianapolis Ave. • Lebanon, IN 46052
Phone: (765) 482-7786 • Fax: (765) 482-7792
Check out our Website: www.perfection-products.com
Email: sales@perfection-products.com